18 GHz to 44 GHz, GaAs, pHEMT, MMIC Power Amplifier

Data Sheet

ADPA7006

FEATURES

Output P1dB: up to 29 dBm typical
P_{SAT}: up to 29 dBm typical
Gain: up to 23 dB typical
Output IP3: up to 39 dBm typical
Integrated power detector
Supply voltage: 5 V at I_{DQ} = 800 mA
16-terminal, 6 mm × 6 mm LCC_HS

APPLICATIONS

Military
Test instrumentation
Communications

FUNCTIONAL BLOCK DIAGRAM

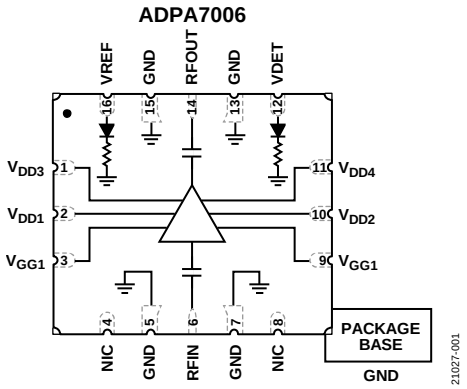

Figure 1.

GENERAL DESCRIPTION

The ADPA7006 is a gallium arsenide (GaAs), pseudomorphic high electron mobility transfer (pHEMT), monolithic microwave integrated circuit (MMIC), with up to 29 dBm of output P1dB. The ADPA7006 has an integrated temperature compensated on-chip power detector that operates between 18 GHz and 44 GHz. The ADPA7006 provides 23 dB of small signal gain and approximately 30 dBm of saturated output power at 30 GHz from a 5 V supply (see Figure 26). With an output IP3 of 37.5 dBm, the ADPA7006 is ideal for linear applications such as electronic countermeasure and instrumentation applications requiring >27 dBm of efficient saturated output power. The RF inputs and outputs are internally matched and dc blocked for ease of integration into higher level assemblies. The ADPA7006 is housed in a 6 mm × 6 mm, 16-terminal ceramic leadless chip carrier with heat sink (LCC_HS) that exhibits low thermal resistance and is compatible with surface-mount manufacturing techniques.

Rev. 0 Document Feedback

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REVISION HISTORY

4/2020—Revision 0: Initial Version

SPECIFICATIONS

18 GHz TO 24 GHz FREQUENCY RANGE

T_A = 25°C, drain bias voltage (V_{DD}) = 5 V, and quiescent drain current (I_{DQ}) = 800 mA for nominal operation, unless otherwise noted.

Table 1.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
FREQUENCY RANGE		18		20	GHz	
GAIN			21		dB	
Gain Flatness			±1		dB	
Gain Variation over Temperature			0.026		dB/°C	
NOISE FIGURE			11		dB	
RETURN LOSS						
Input			12.5		dB	
Output			15		dB	
OUTPUT						
Output Power for 1 dB Compression	P1dB		24		dBm	
Saturated Output Power	P_{SAT}		26.5		dBm	
Output Third-Order Intercept	IP3		34		dBm	Measurement taken at output power (P_{OUT}) per tone = 16 dBm
POWER ADDED EFFICIENCY	PAE		9.5		%	Measured at P_{SAT}
SUPPLY						
Quiescent Drain Current	I_{DQ}		800		mA	Adjust V_{GG1} between −1.5 V and 0 V to achieve I_{DQ} = 800 mA, V_{GG1} = −0.68 V typical to achieve I_{DQ} = 800 mA
Drain Bias Voltage	V_{DD}	4	5		V	

20 GHz TO 24 GHz FREQUENCY RANGE

T_A = 25°C, V_{DD} = 5 V, and I_{DQ} = 800 mA for nominal operation, unless otherwise noted.

Table 2.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
FREQUENCY RANGE		20		24	GHz	
GAIN		20.5	23		dB	
Gain Flatness			±1		dB	
Gain Variation over Temperature			0.026		dB/°C	
NOISE FIGURE			7		dB	
RETURN LOSS						
Input			12		dB	
Output			15		dB	
OUTPUT						
Output Power for 1 dB Compression	P1dB	24	26.5		dBm	
Saturated Output Power	P_{SAT}		28		dBm	
Output Third-Order Intercept	IP3		35		dBm	Measurement taken at P_{OUT} per tone = 16 dBm
POWER ADDED EFFICIENCY	PAE		12		%	Measured at P_{SAT}
SUPPLY						
Quiescent Drain Current	I_{DQ}		800		mA	Adjust V_{GG1} between −1.5 V and 0 V to achieve I_{DQ} = 800 mA, V_{GG1} = −0.68 V typical to achieve I_{DQ} = 800 mA
Drain Bias Voltage	V_{DD}	4	5		V	

24 GHz TO 34 GHz FREQUENCY RANGE

T_A = 25°C, V_{DD} = 5 V, and I_{DQ} = 800 mA for nominal operation, unless otherwise noted.

Table 3.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
FREQUENCY RANGE		24		34	GHz	
GAIN		20.5	23		dB	
Gain Flatness			±1		dB	
Gain Variation over Temperature			0.026		dB/°C	
NOISE FIGURE			7		dB	
RETURN LOSS						
Input			12		dB	
Output			15		dB	
OUTPUT						
Output Power for 1 dB Compression	P1dB	26	29		dBm	
Saturated Output Power	P_{SAT}		29		dBm	
Output Third-Order Intercept	IP3		37.5		dBm	Measurement taken at P_{OUT} per tone = 16 dBm
POWER ADDED EFFICIENCY	PAE		14		%	Measured at P_{SAT}
SUPPLY						
Quiescent Drain Current	I_{DQ}		800		mA	Adjust V_{GG1} between −1.5 V and 0 V to achieve I_{DQ} = 800 mA, V_{GG1} = −0.68 V typical to achieve I_{DQ} = 800 mA
Drain Bias Voltage	V_{DD}	4	5		V	

34 GHz TO 44 GHz FREQUENCY RANGE

T_A = 25°C, V_{DD} = 5 V, and I_{DQ} = 800 mA for nominal operation, unless otherwise noted.

Table 4.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
FREQUENCY RANGE		34		44	GHz	
GAIN		20	22.5		dB	
Gain Flatness			±1		dB	
Gain Variation over Temperature			0.034		dB/°C	
NOISE FIGURE			4.5		dB	
RETURN LOSS						
Input			18		dB	
Output			15		dB	
OUTPUT						
Output Power for 1 dB Compression	P1dB	23	26		dBm	
Saturated Output Power	P_{SAT}		28		dBm	
Output Third-Order Intercept	IP3		39		dBm	Measurement taken at P_{OUT} per tone = 16 dBm
POWER ADDED EFFICIENCY	PAE		8		%	Measured at P_{SAT}
SUPPLY						
Quiescent Drain Current	I_{DQ}		800		mA	Adjust V_{GG1} between −1.5 V and 0 V to achieve I_{DQ} = 800 mA, V_{GG1} = −0.68 V typical to achieve I_{DQ} = 800 mA
Drain Bias Voltage	V_{DD}	4	5		V	

ABSOLUTE MAXIMUM RATINGS

Table 5.

Parameter	Rating
Drain Bias Voltage (V_{DDx})	6.0 V
Gate Bias Voltage (V_{GG1})	−1.6 V to 0 V
Radio Frequency Input Power (RFIN)	20 dBm
Continuous Power Dissipation (P_{DISS}), T = 85°C (Derate 88.5 mW/°C above 85°C)	7.96 W
Temperature	
Storage Range	−55°C to +150°C
Operating Range	−40°C to +85°C
Nominal Junction (T = 85°C, V_{DD} = 5 V, I_{DQ} = 800 mA)	130.2°C
Junction to Maintain 1,000,0000 Hour Mean Time to Failure (MTTF)	175°C
Peak Reflow (Moisture Sensitivity Level 3 (MSL3))[1]	260°C
Moisture Sensitivity Level	MSL3
Electrostatic Discharge (ESD) Sensitivity	
Human Body Model (HBM)	Class 1B (passed 750 V)

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

θ_{JC} is the channel to case thermal resistance, channel to bottom of the die using die attach epoxy.

Table 6. Thermal Resistance

Package Type	θ_{JC}	Unit
EH-16-1[1]	11.3	°C/W

[1] θ_{JC} is determined by simulation under the following conditions: the heat transfer is due solely to thermal conduction from the channel through the ground pin to the PCB. The ground pin is held constant at the operating temperature of 85°C.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

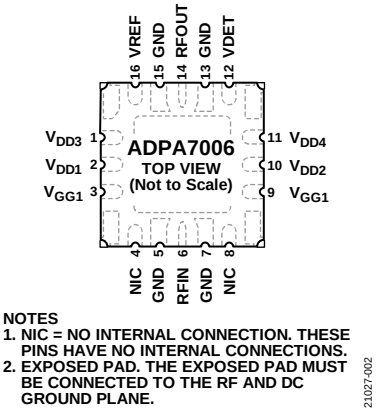

Figure 2. Pin Configuration

Table 7. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 11	V_{DD3}, V_{DD4}	Drain Bias for the Output Stage. External bypass capacitors are required.
2, 10	V_{DD1}, V_{DD2}	Drain Bias for the Driver Stage. External bypass capacitors are required.
3, 9	V_{GG1}	Gate Bias Controls. External bypass capacitors are required.
4, 8	NIC	No Internal Connection. These pins have no internal connections.
5, 7, 13, 15	GND	Ground. These pins must be connected to RF and dc ground.
6	RFIN	Radio Frequency Signal Input. This pin is ac-coupled and matched to 50 Ω.
12	VDET	Detector Diode to Measure RF Output Power. Output power detection via this pin requires the application of a dc bias voltage through an external series resistor. Used in combination with the VREF pin, the difference voltage (VREF − VDET) is a temperature compensated dc voltage that is proportional to the RF output power.
14	RFOUT	RF Signal Output. This pin is ac-coupled and matched to 50 Ω.
16	VREF	Reference Diode Used for Temperature Compensation of VDET RF Output Power Measurements. Used in combination with VDET, this voltage provides temperature compensation to the VDET RF output power measurements.
	EPAD	Exposed Pad. The exposed pad must be connected to the RF and dc ground plane.

INTERFACE SCHEMATICS

Figure 3. GND Interface Schematic

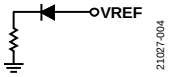

Figure 4. VREF Interface Schematic

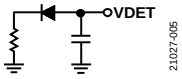

Figure 5. VDET Interface Schematic

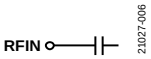

Figure 6. RFIN Interface Schematic

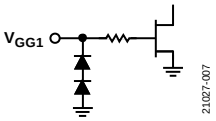

Figure 7. V_{GG1} Schematic

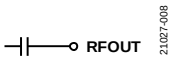

Figure 8. RFOUT Interface Schematic

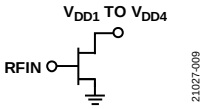

Figure 9. V_{DD1} to V_{DD4} Interface Schematic

TYPICAL PERFORMANCE CHARACTERISTICS

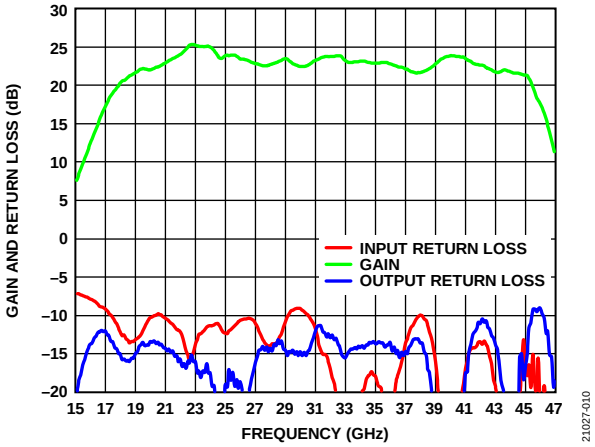

Figure 10. Gain and Return Loss vs. Frequency, V_{DD} = 5 V, I_{DQ} = 800 mA

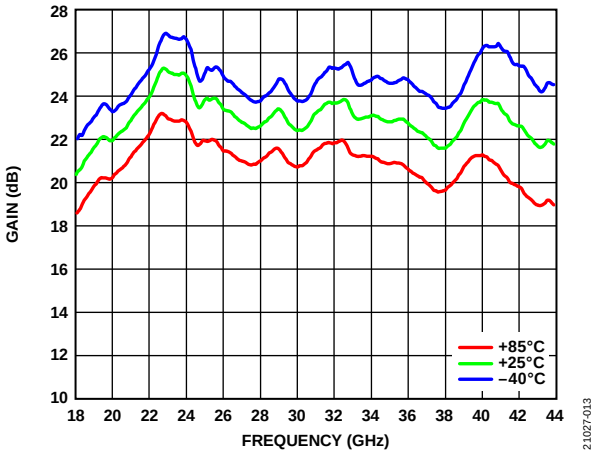

Figure 13. Gain vs. Frequency for Various Temperatures, V_{DD} = 5 V, I_{DQ} = 800 mA

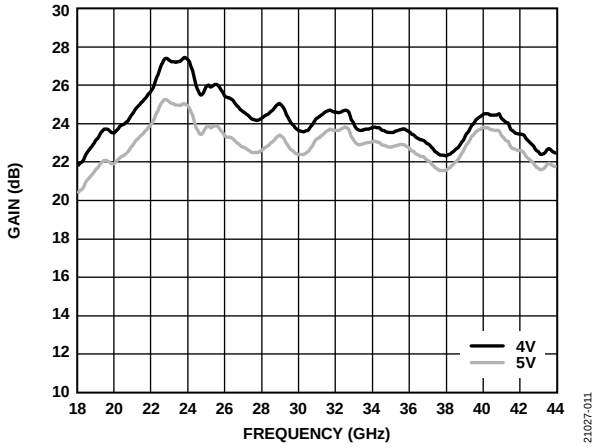

Figure 11. Gain vs. Frequency for Various V_{DD}, I_{DQ} = 800 mA

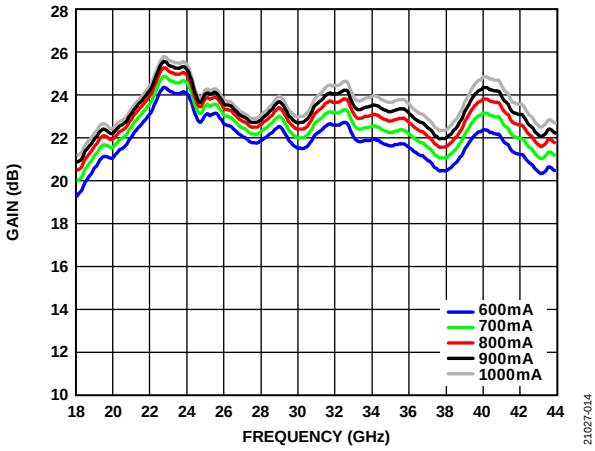

Figure 14. Gain vs. Frequency for Various I_{DQ}, V_{DD} = 5 V

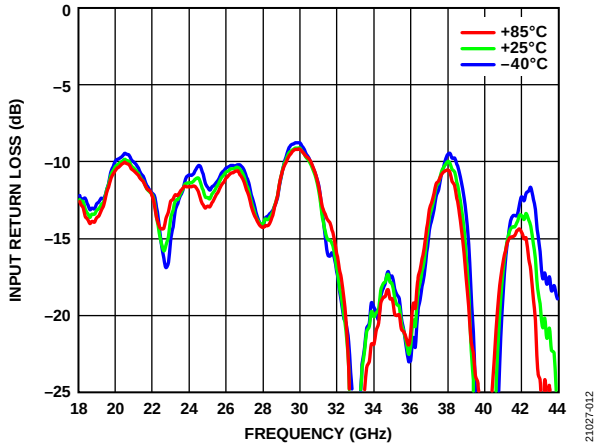

Figure 12. Input Return Loss vs. Frequency for Various Temperatures, V_{DD} = 5 V, I_{DQ} = 800 mA

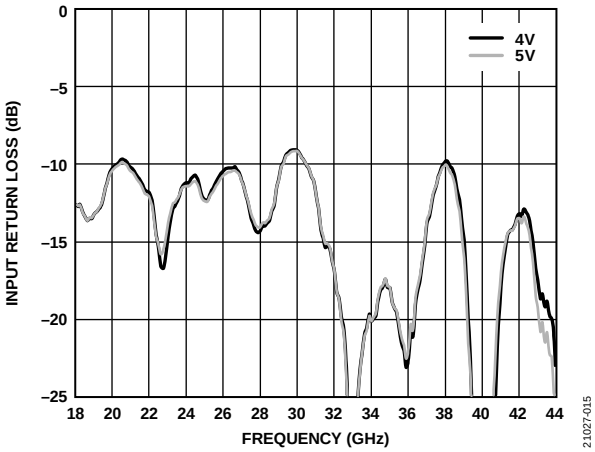

Figure 15. Input Return Loss vs. Frequency for Various V_{DD}, I_{DQ} = 800 mA

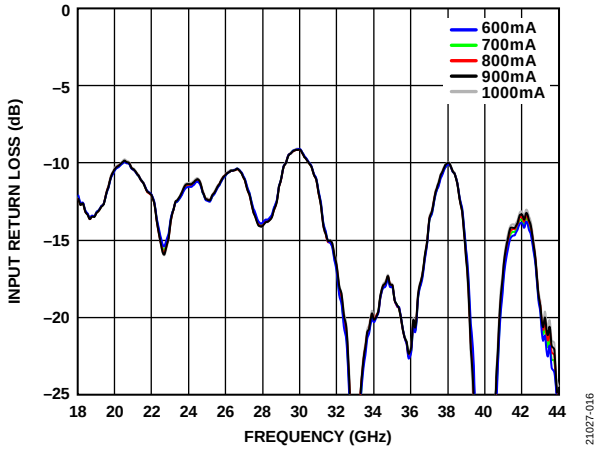

Figure 16. Input Return Loss vs. Frequency for Various I_{DQ}, V_{DD} = 5 V

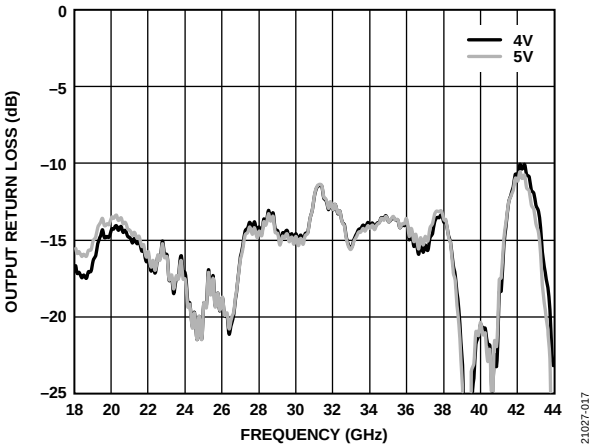

Figure 17. Output Return Loss vs. Frequency for Various V_{DD}, I_{DQ} = 800 mA

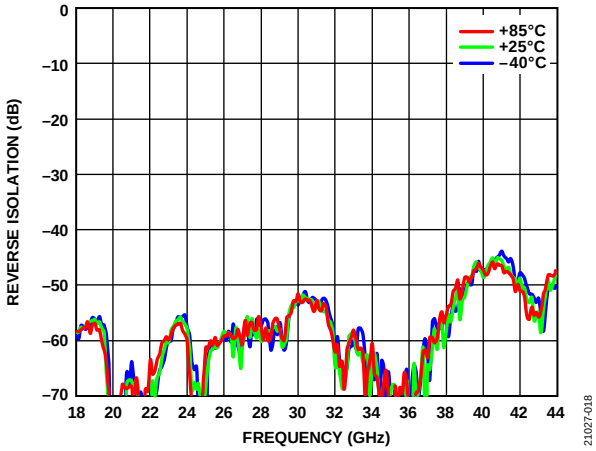

Figure 18. Reverse Isolation vs. Frequency for Various Temperatures, V_{DD} = 5 V, I_{DQ} = 800 mA

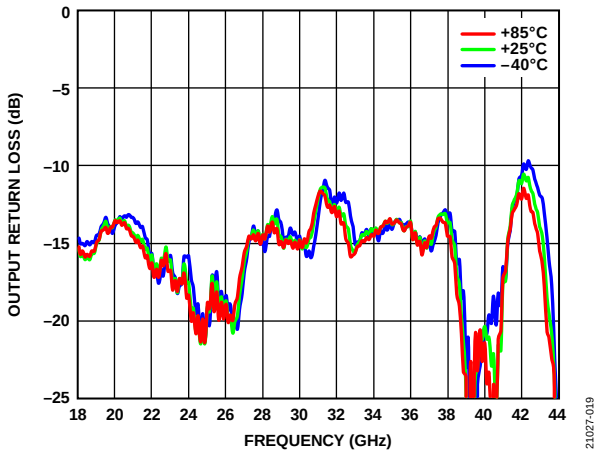

Figure 19. Output Return Loss vs. Frequency for Various Temperatures, V_{DD} = 5 V, I_{DQ} = 800 mA

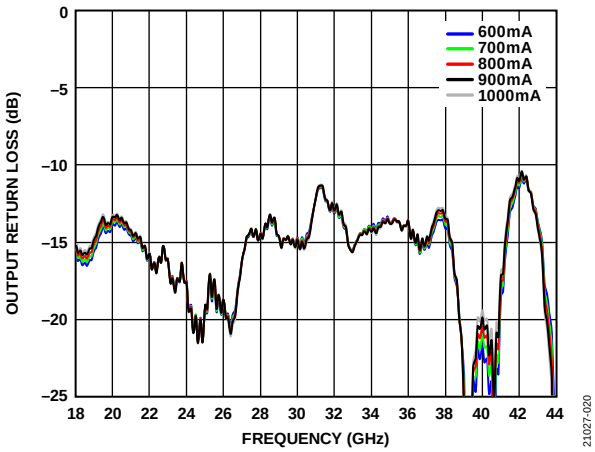

Figure 20. Output Return Loss vs. Frequency for Various I_{DQ}, V_{DD} = 5 V

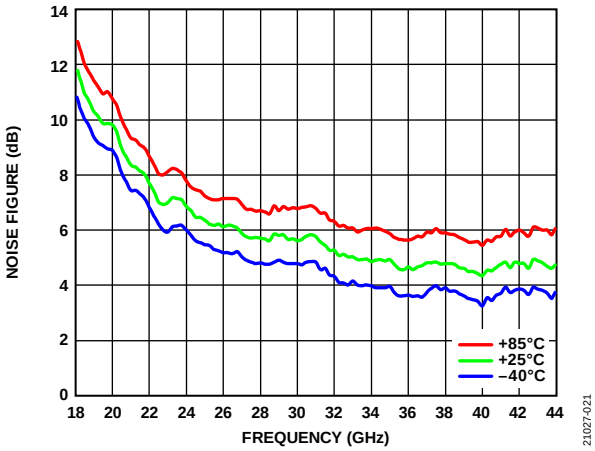

Figure 21. Noise Figure vs. Frequency for Various Temperatures, V_{DD} = 5 V, I_{DQ} = 800 mA

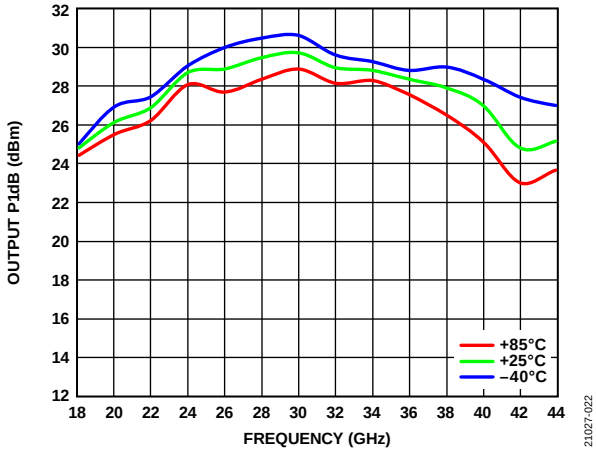

Figure 22. Output P1dB vs. Frequency for Various Temperatures, V_{DD} = 5 V, I_{DQ} = 800 mA

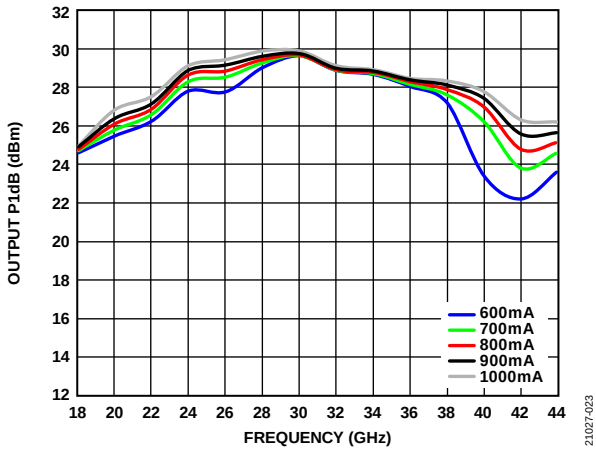

Figure 23. Output P1dB vs. Frequency for Various I_{DQ}, V_{DD} = 5 V

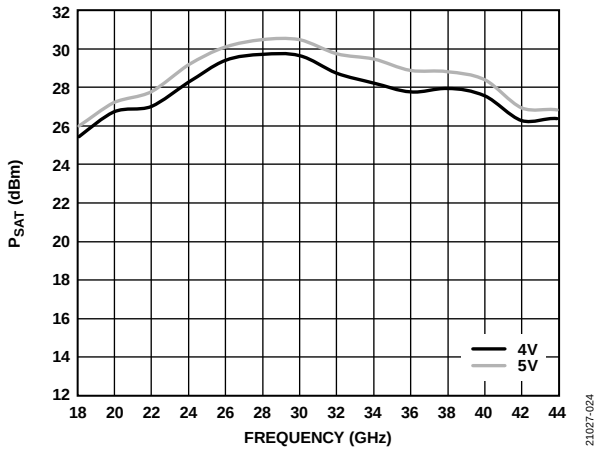

Figure 24. P_{SAT} vs. Frequency for Various V_{DD}, I_{DQ} = 800 mA

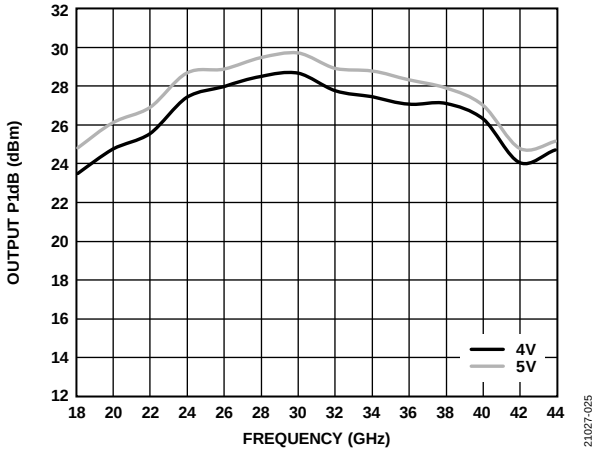

Figure 25. Output P1dB vs. Frequency for Various V_{DD}, I_{DQ} = 800 mA

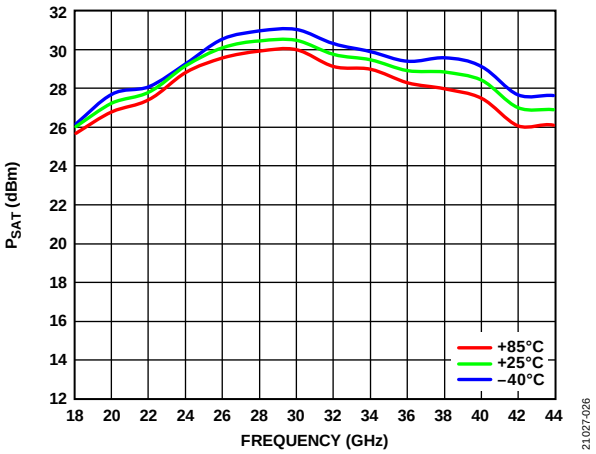

Figure 26. P_{SAT} vs. Frequency for Various Temperatures, V_{DD} = 5 V, I_{DQ} = 800 mA

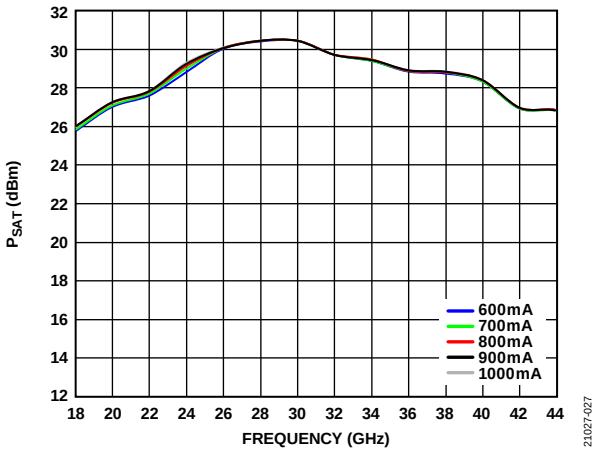

Figure 27. P_{SAT} vs. Frequency for Various I_{DQ}, V_{DD} = 5 V

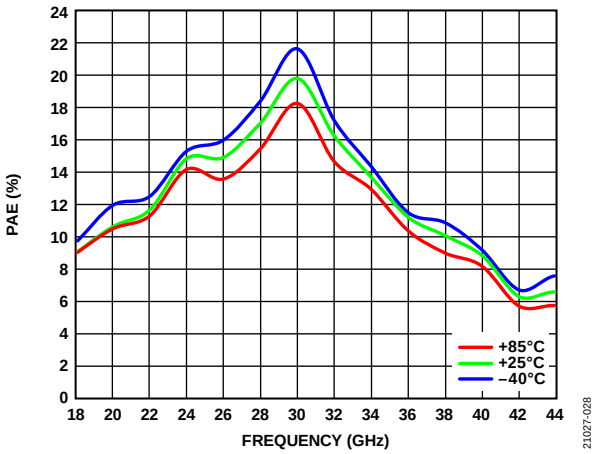

Figure 28. Power Added Efficiency (PAE) vs. Frequency for Various Temperatures, V_{DD} = 5 V, I_{DQ} = 800 mA, PAE Measured at P_{SAT}

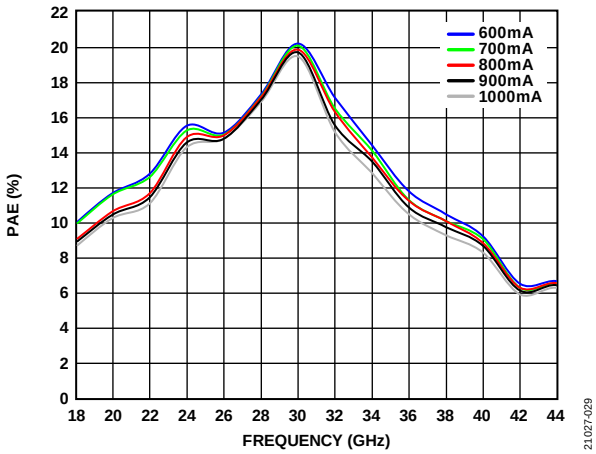

Figure 29. PAE vs. Frequency for Various I_{DQ}, V_{DD} = 5 V, PAE Measured at P_{SAT}

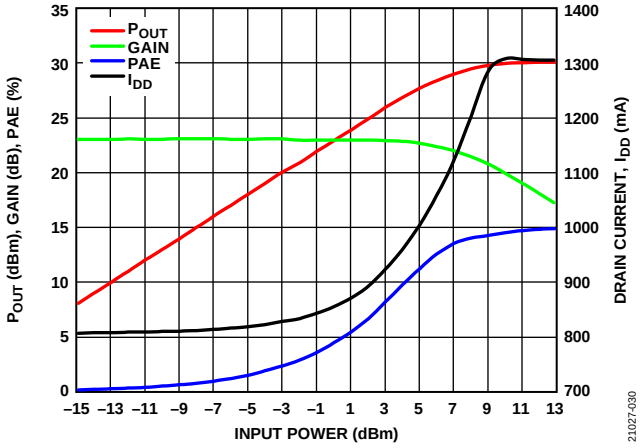

Figure 30. P_{OUT}, Gain, PAE, and I_{DD} vs. Input Power, 26 GHz, V_{DD} = 5 V, I_{DQ} = 800 mA

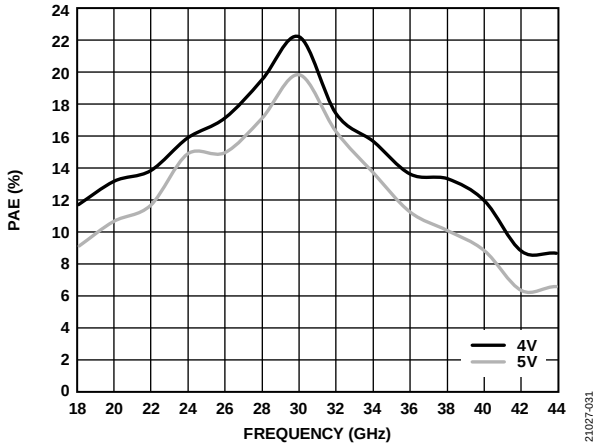

Figure 31. PAE vs. Frequency for Various V_{DD}, I_{DQ} = 800 mA, PAE Measured at P_{SAT}

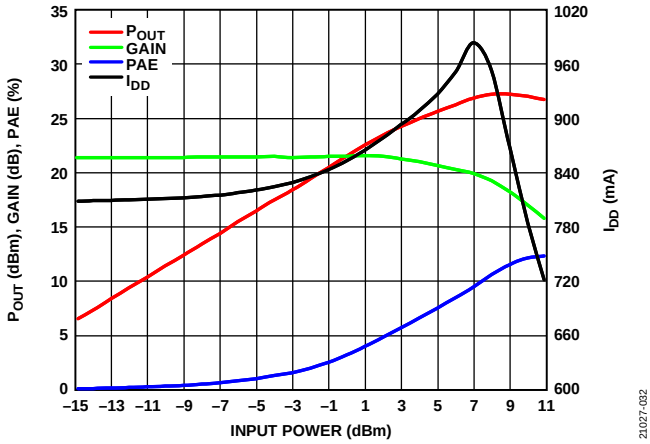

Figure 32. P_{OUT}, Gain, PAE, and I_{DD} vs. Input Power, 20 GHz, V_{DD} = 5 V, I_{DQ} = 800 mA

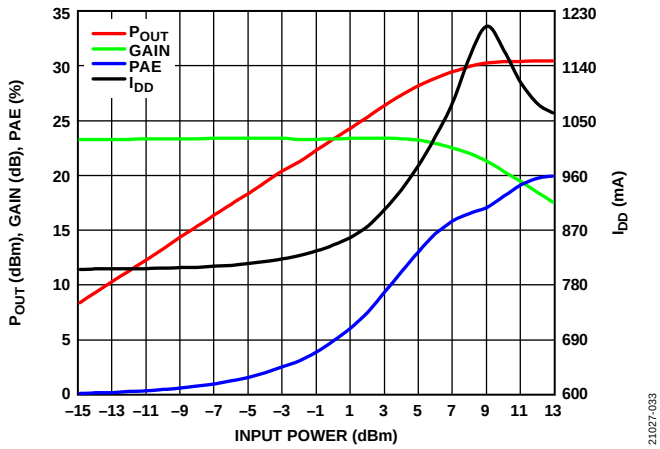

Figure 33. P_{OUT}, Gain, PAE, and I_{DD} vs. Input Power, 30 GHz, V_{DD} = 5 V, I_{DQ} = 800 mA

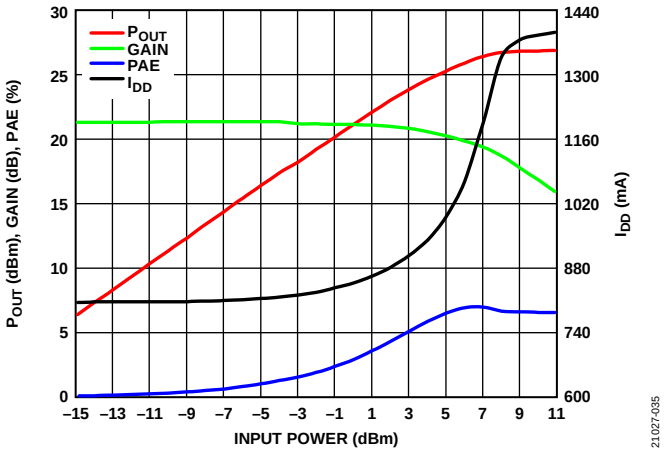

Figure 34. P_{OUT}, Gain, PAE, and I_{DD} vs. Input Power, 44 GHz, V_{DD} = 5 V, I_{DQ} = 800 mA

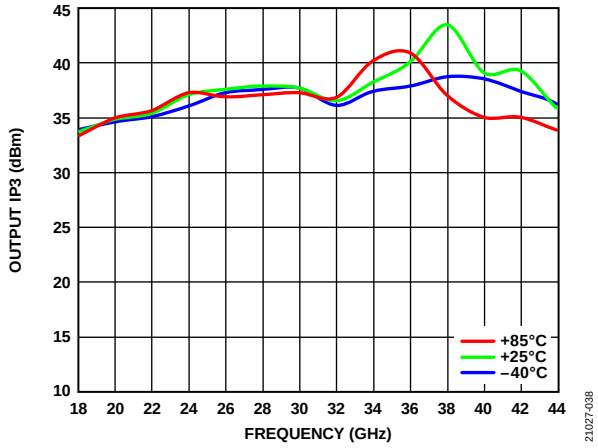

Figure 37. Output IP3 vs. Frequency for Various Temperatures, P_{OUT} per Tone = 16 dBm, V_{DD} = 5 V, I_{DQ} = 800 mA

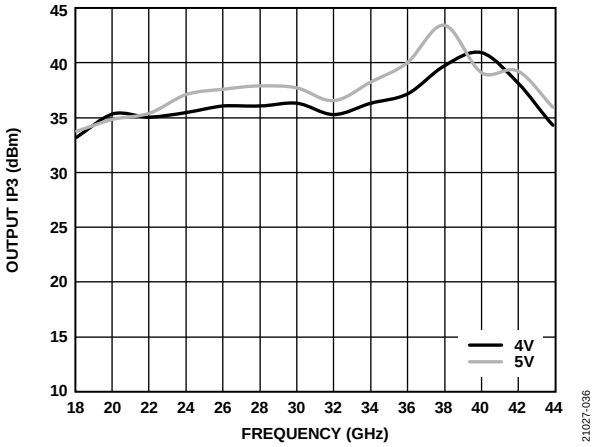

Figure 35. Output IP3 vs. Frequency for Various V_{DD}, P_{OUT} per Tone = 16 dBm, I_{DQ} = 800 mA

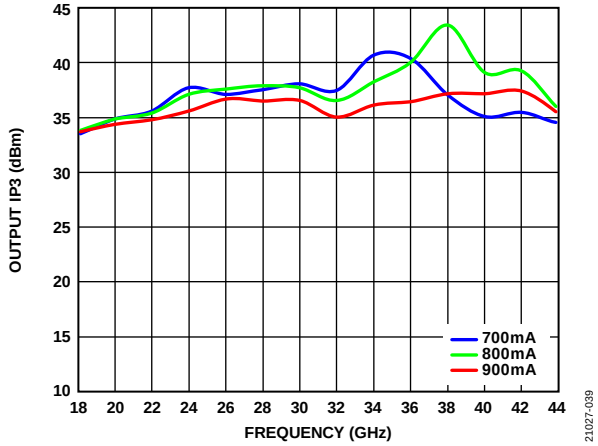

Figure 38. Output IP3 vs. Frequency for Various I_{DQ}, P_{OUT} per Tone = 16 dBm, V_{DD} = 5 V

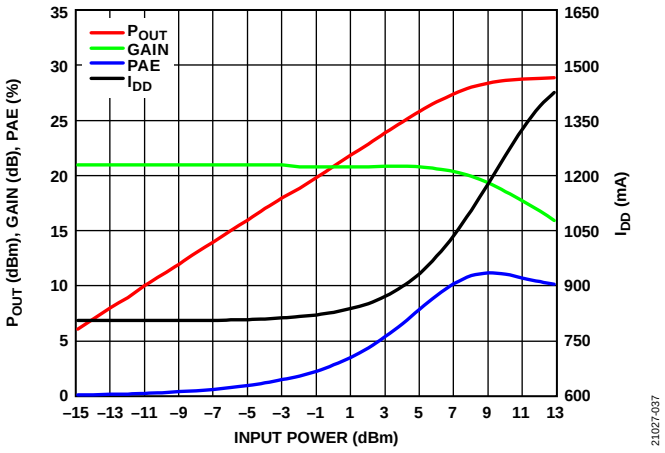

Figure 36. P_{OUT}, Gain, PAE, and I_{DD} vs. Input Power, 38 GHz, V_{DD} = 5 V, I_{DQ} = 800 mA

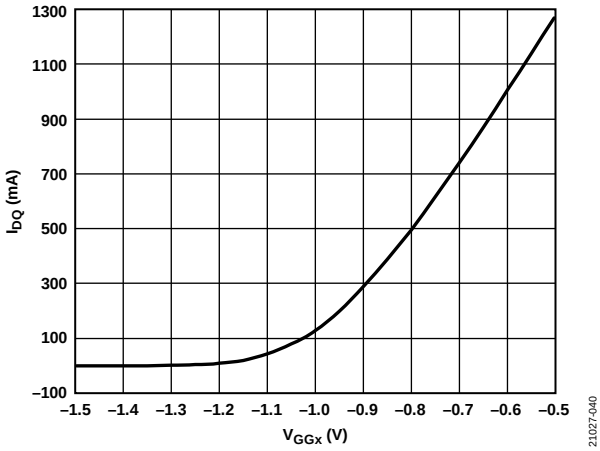

Figure 39. I_{DQ} vs. V_{GGx}

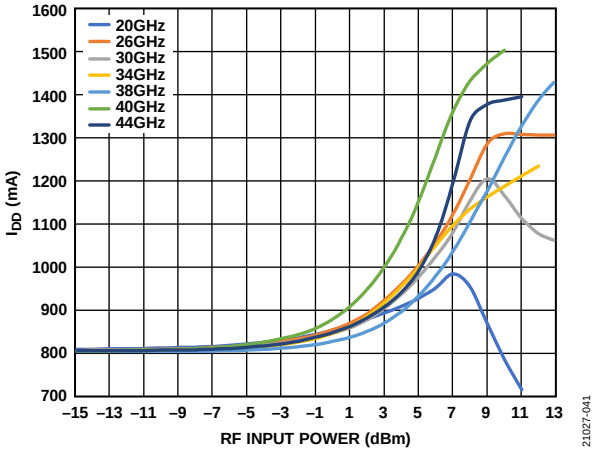

Figure 40. I_{DD} vs. RF Input Power at Various Frequencies, V_{DD} = 5 V, I_{DQ} = 800 mA

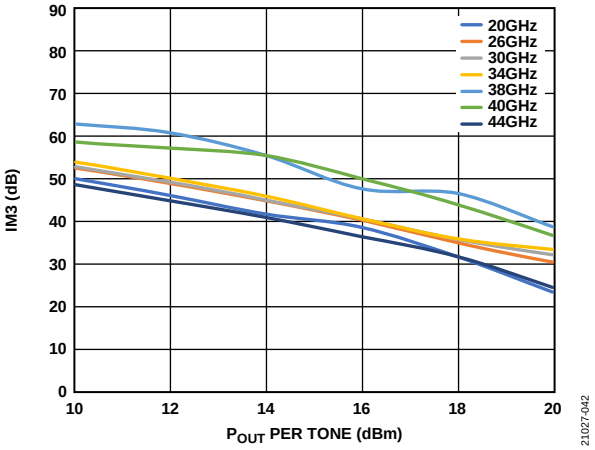

Figure 41. IM3 vs. P_{OUT} per Tone at Various Frequencies, V_{DD} = 4 V, I_{DQ} = 800 mA

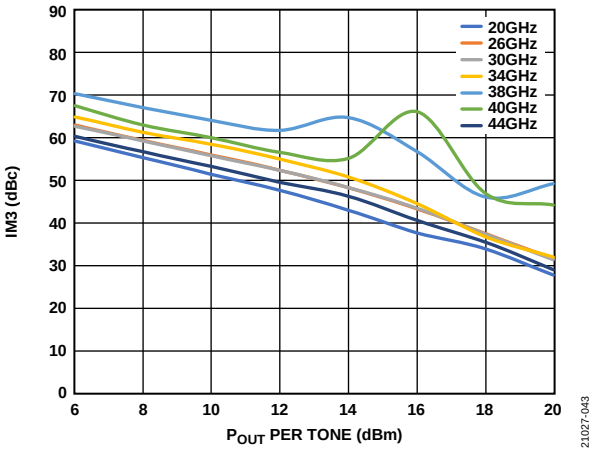

Figure 42. Third-Order Intermodulation Distortion Relative to Carrier (IM3) vs. P_{OUT} per Tone at Various Frequencies, V_{DD} = 5 V, I_{DQ} = 800 mA

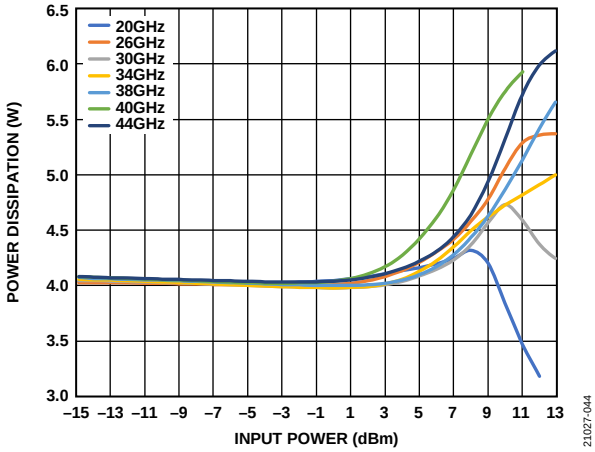

Figure 43. Power Dissipation vs. Input Power at Various Frequencies, T = 85°C, V_{DD} = 5 V, I_{DQ} = 800 mA

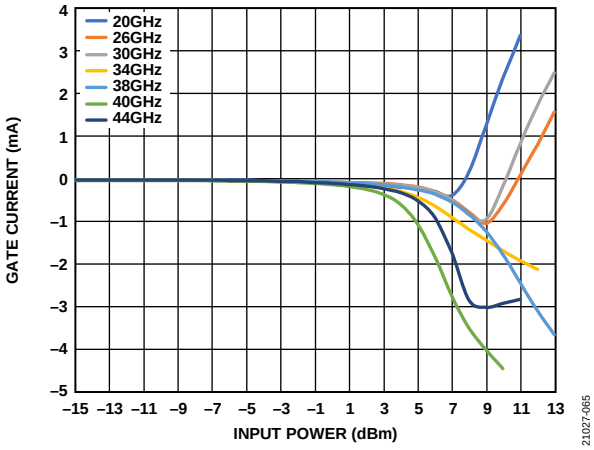

Figure 44. Gate Current vs. Input Power at Various Frequencies, V_{DD} = 5 V, I_{DQ} = 800 mA

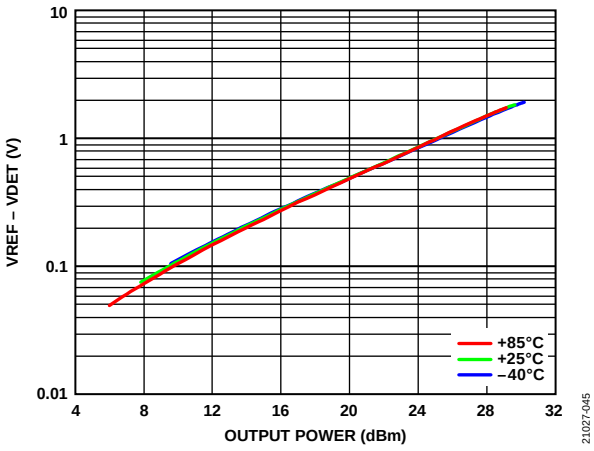

Figure 45. Detector Voltage (VREF − VDET) vs. Output Power for Various Temperatures at 32 GHz, V_{DD} = 5 V, I_{DQ} = 800 mA

CONSTANT I_{DD} OPERATION

T_A = 25°C, V_{DD} = 5 V, and I_{DD} = 1000 mA for nominal operation, unless otherwise noted. Figure 46 through Figure 49 are biased with the HMC980LP4E active bias controller. See the Biasing the ADPA7006 with the HMC980LP4E section for biasing details.

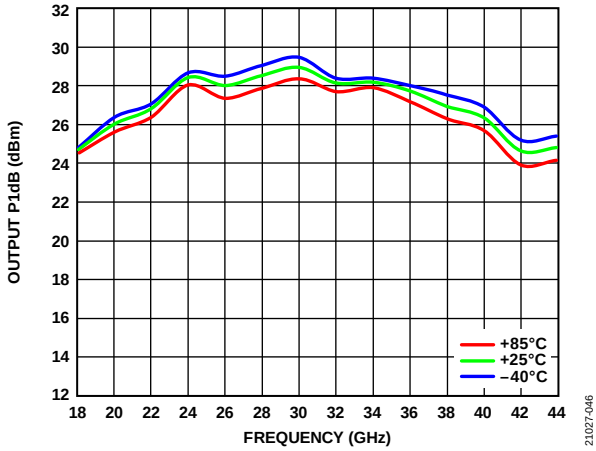

Figure 46. Output P1dB vs. Frequency for Various Temperatures, V_{DD} = 5 V, Data Measured with Constant I_{DD}

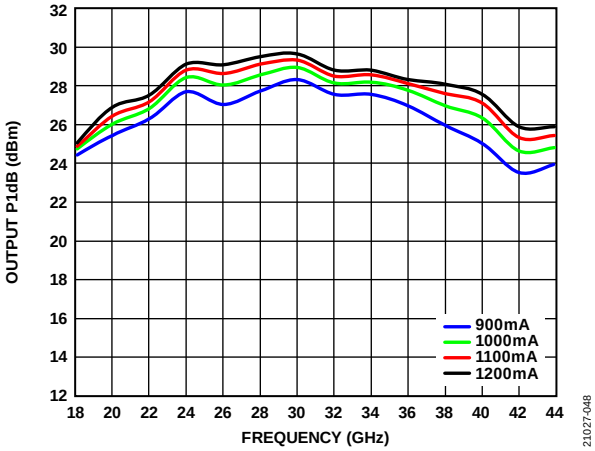

Figure 48. Output P1dB vs. Frequency for Various Drain Currents, V_{DD} = 5 V, Data Measured with Constant I_{DD}

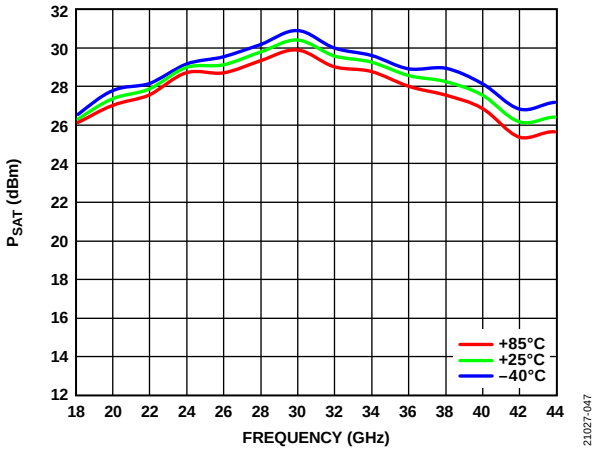

Figure 47. P_{SAT} vs. Frequency for Various Temperatures, V_{DD} = 5 V, Data Measured with Constant I_{DD}

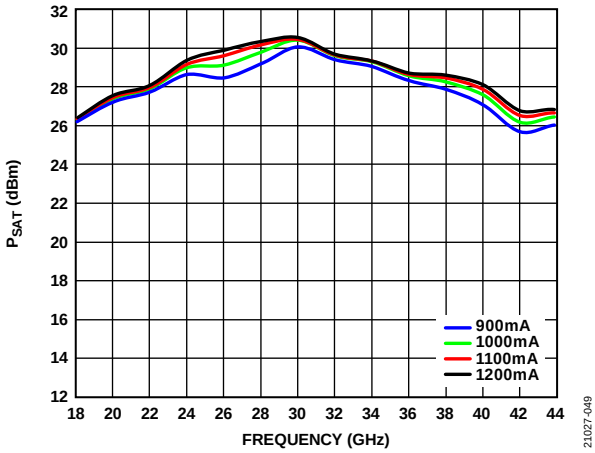

Figure 49. P_{SAT} vs. Frequency for Various Drain Currents, V_{DD} = 5 V, Data Measured with Constant I_{DD}

THEORY OF OPERATION

The simplified architecture of the ADPA7006 power amplifier is shown in Figure 50. The ADPA7006 uses two, three-stage amplifiers operating in quadrature between two 90° hybrids. The drain current is controlled by the voltage on the V_{GG1} pin. This pin must be driven by a negative voltage in the −1.5 V to 0 V range (typical gate bias voltage for a quiescent drain bias current of 800 mA is −0.68 V). Simplified bias pin connections to the dedicated gain stages are shown in Figure 50.

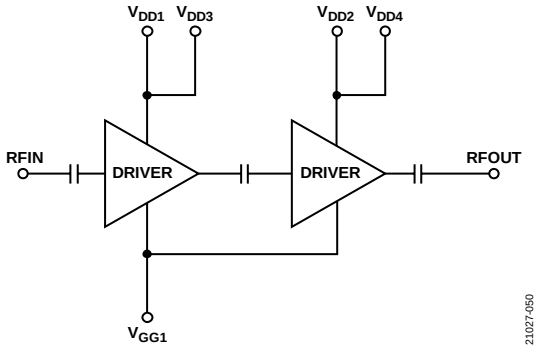

Figure 50. Simplified Architecture

A portion of the RF output signal is directionally coupled to a diode to detect the RF output power (see Figure 51). When the diode is dc biased, the diode rectifies the RF power and makes the RF power available for measurement as a dc voltage at the VDET pin. Temperature compensation is accomplished by referencing a symmetrical diode circuit that is not coupled to the RF output, which contains a dc voltage output at the VREF pin, as shown in Figure 51. The difference of VREF − VDET provides a temperature compensated signal that is proportional to the RF output.

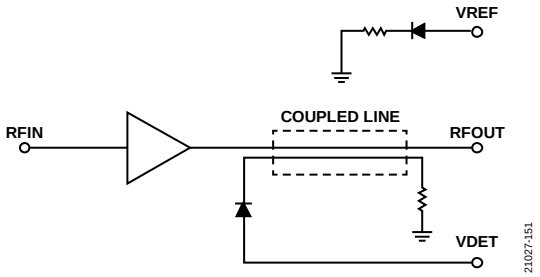

Figure 51. Power Detector Circuit

The 90° hybrids ensure that the input and output return losses are >12 dB. See the application circuit in Figure 52 for further details on biasing the various blocks.

To obtain optimal performance from the ADPA7006 and to avoid damaging the device, follow the recommended biasing sequences described in the Biasing Procedures section.

APPLICATIONS INFORMATION

Figure 52, Figure 53, and Figure 54 show schematics of basic connections for operating the ADPA7006. Pin 3 and Pin 9 are V_{GG1} gate bias pins that are connected internally. A gate bias voltage can be applied to either Pin 3 or Pin 9. V_{DD1} and V_{DD2} are drain bias pins for the driver stage and are internally connected. V_{DD3} and V_{DD4} are drain bias pins for the output stage and are also internally connected. Drain bias can be applied to either V_{DD1} and V_{DD3} or to V_{DD2} and V_{DD4}. As a result, the simplified biasing schemes shown in Figure 53 and Figure 54 can be used (Bias Option 1 and Bias Option 2, respectively). Bias Option 1 uses V_{GG1} for the gate control and V_{DD1} and V_{DD3} for the drain bias (see Figure 53). Bias Option 2 uses V_{GG1} for gate control and V_{DD2} and V_{DD4} for the drain bias (see Figure 54).

Connect all used V_{DDx} pins to a single source. Likewise, connect all used V_{GG1} pins together to a single source. Capacitive bypassing is required for all V_{GG1} and V_{DDx} pins in use. There may be a scope to reduce the number of capacitors, but scopes vary from system to system. It is recommended to first remove or combine the largest capacitors that are farthest from the device.

BIASING PROCEDURES

Adhere to the following bias sequence during power-up:

1. Connect GND to RF and dc ground.
2. Set the V_{GG1} to −1.5 V.
3. Set all the drain bias voltages (V_{DDx}) to 5 V.
4. Increase V_{GG1} to achieve I_{DQ} = 800 mA.
5. Apply the RF signal.

Adhere to the following bias sequence during power-down:

1. Turn off the RF signal.
2. Decrease V_{GG1} to −1.5 V to achieve I_{DQ} = 0 mA (approximately).
3. Decrease all drain bias voltages to 0 V.
4. Decrease V_{GG1} to 0 V.

The V_{DD} = 5 V and I_{DQ} = 800 mA bias conditions are recommended to optimize overall performance when the gate voltage is being held at a fixed value (note that with the gate voltage held at a fixed value, the drain current, I_{DD}, increases as the RF input power level is increased, as shown in Figure 40). Unless otherwise noted, the data shown was taken using the recommended bias conditions. Operation of the ADPA7006 at different quiescent drain current conditions can result in different performance. Biasing the ADPA7006 for higher quiescent drain current typically results in higher gain and output P1dB at the expense of increased power consumption (see Table 8).

Table 8. Power Selection Table[1, 2]

I_{DQ} (mA)	Gain (dB)	Output P1dB (dBm)	Output IP3 (dBm)	P_{DISS} (W)	V_{GGx} (V)
600	21.5	29.63	36.6	3	−0.752
700	22.0	29.68	38.0	3.5	−0.712
800	22.4	29.70	37.7	4	−0.674
900	22.7	29.80	36.6	4.5	−0.637
1000	23.0	29.94	35.4	5	−0.600

[1] Data taken at the following nominal bias conditions: V_{DD} = 5 V, T_A = 25°C, and frequency = 30 GHz.
[2] Adjust V_{GG1} from −1.5 V to 0 V to achieve the desired quiescent drain current, I_{DQ}.

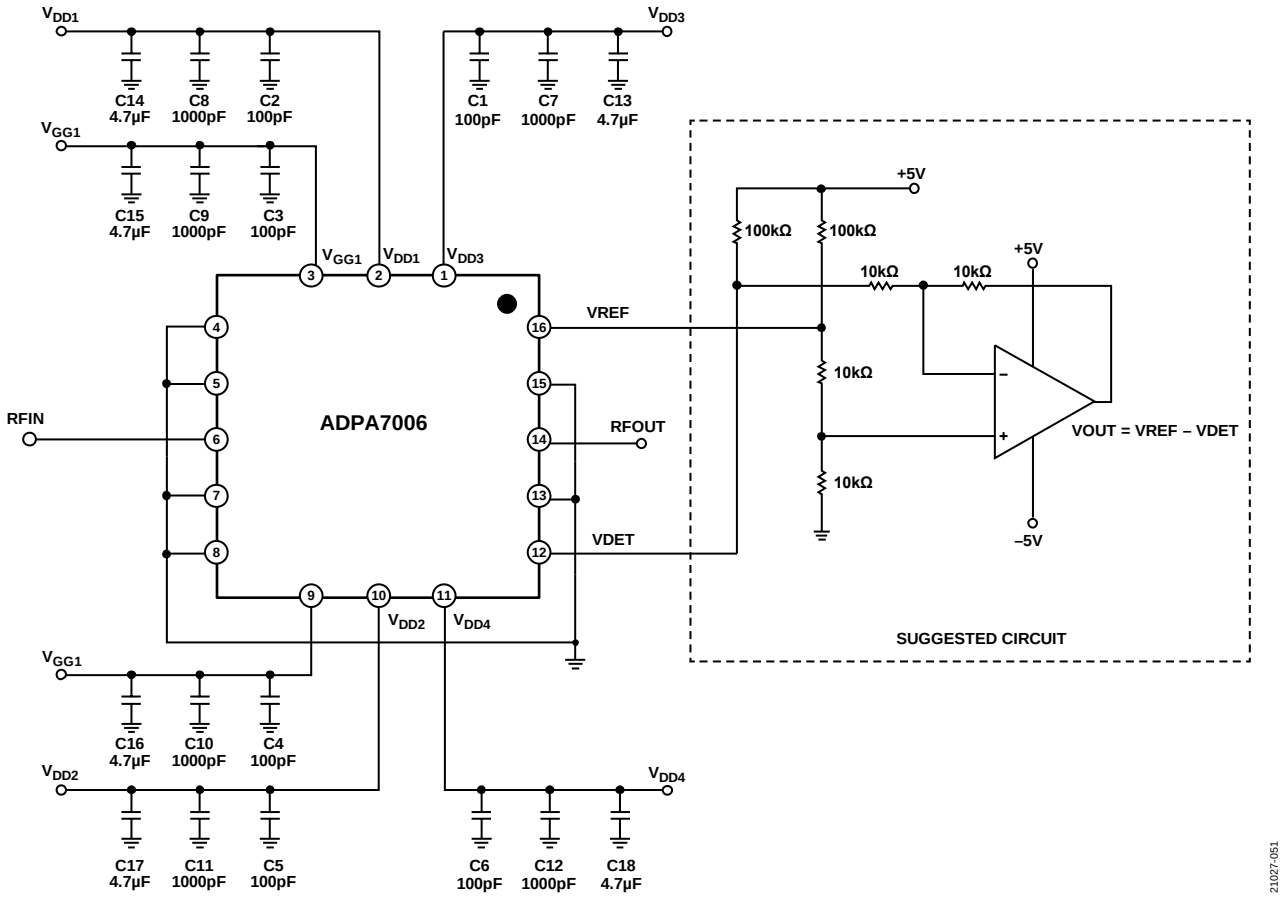

Figure 52. Typical Application Circuit

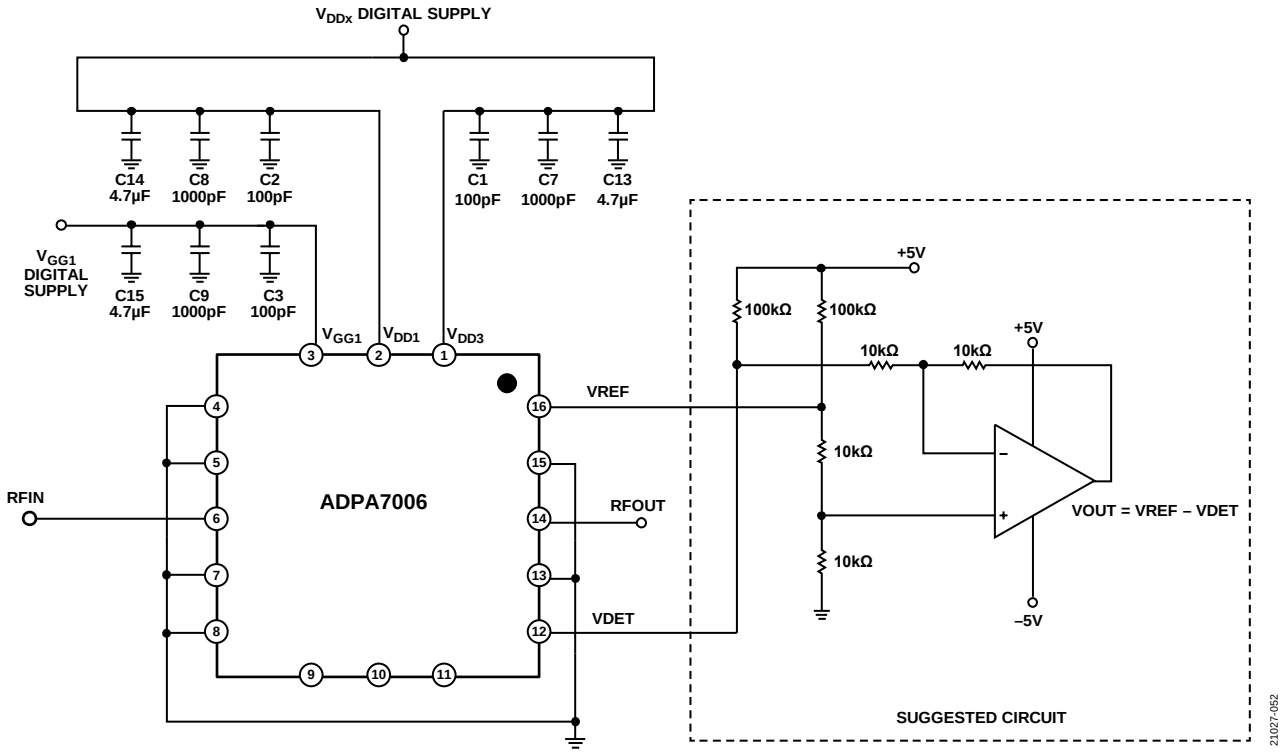

Figure 53. Bias Option 1

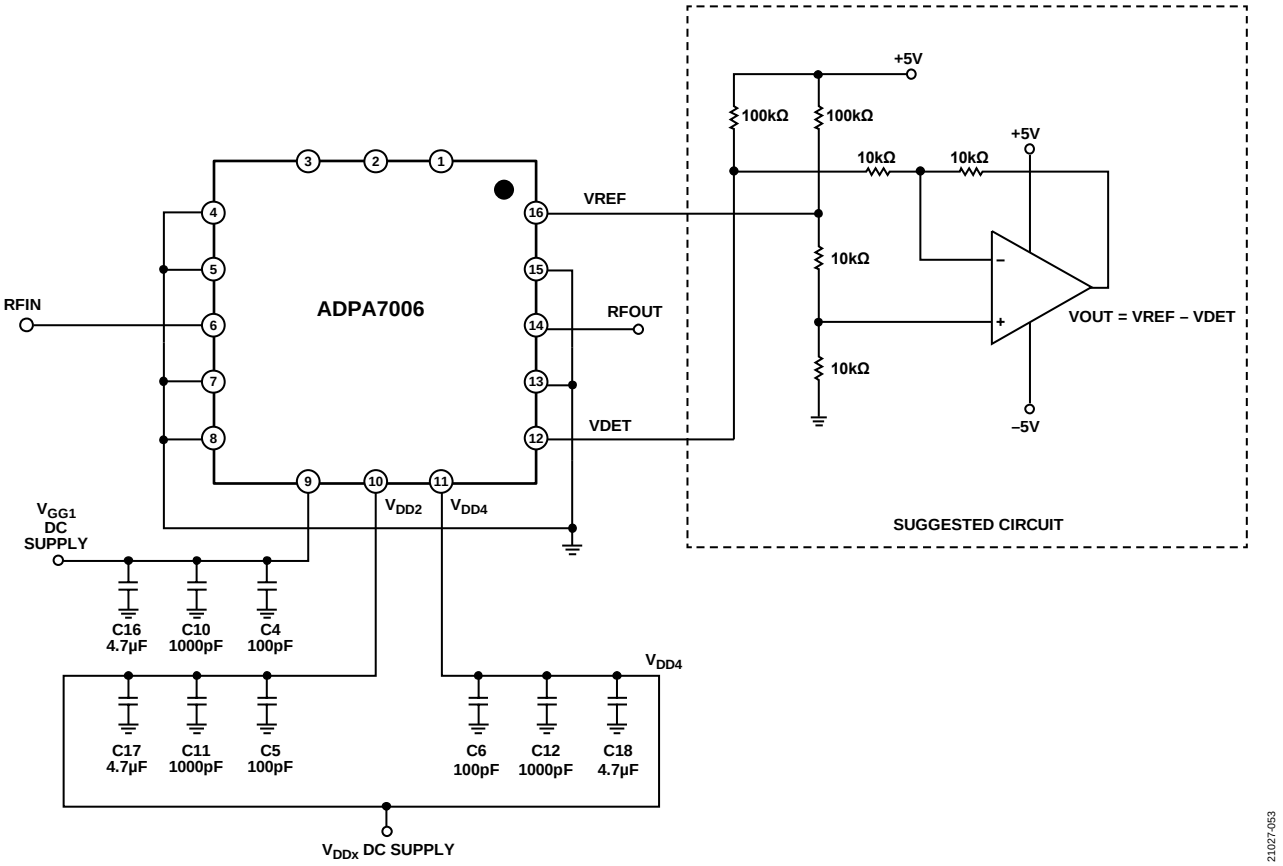

Figure 54. Bias Option 2

BIASING THE ADPA7006 WITH THE HMC980LP4E

The HMC980LP4E is an active bias controller that measures and regulates drain current by automatically adjusting the gate voltage. The HMC980LP4E can control the biasing of RF amplifiers with drain voltages up to 16.5 V and currents up to 1.6 A. The controller provides constant drain current biasing over temperature and device to device variation, and properly sequences gate and drain voltages to ensure the safe operation of the amplifier.

The HMC980LP4E offers self protection in the event of a short circuit, as well as an internal charge pump that generates the negative voltage required on the gate of the ADPA7006. The HMC980LP4E also provides the option to use an external negative voltage source. The HMC980LP4E is also available in die form as the HMC980-DIE.

APPLICATION CIRCUIT SETUP

When using an external negative supply for VNEG, refer to the schematic in Figure 56.

Although the ADPA7006 is specified with a quiescent drain current of 800 mA, the operational drain current, I_{DRAIN}, required to achieve the maximum output power from the ADPA7006 must be set closer to 1000 mA. The I_{DRAIN} current increases to approximately 1000 mA when the RF input power is 5 dBm, the approximate input compression point (see Figure 40). As a result, a target drain current of 1000 mA is chosen.

In the application circuit, the ADPA7006 drain voltage and drain current are set by the following equations:

$$VDRAIN = V_{DD} - I_{DRAIN} \times 0.85\ \Omega \quad (1)$$

where:

$VDRAIN$ = 5 V, the drain voltage from Pin 17 and Pin 18 of the HMC980LP4E.

V_{DD} = 5.85 V, the supply voltage to the HMC980LP4E.

I_{DRAIN} = 1000 mA, the constant drain current from Pin 17 and Pin 18 on the HMC980LP4E.

$$R10 = \frac{150\ \Omega}{I_{DRAIN}} \quad (2)$$

where:

I_{DRAIN} = 1000 mA.

$R10$ = 150 Ω.

LIMITING VGATE AND VNEG TO MEET ADPA7006 V_{GG1} ABSOLUTE MAXIMUM RATINGS REQUIREMENT

When using the ADPA7006 to control the HMC980LP4E, the minimum voltages for the VNEG and VGATE pins of the HMC980LP4E must be set to −1.5 V to keep these voltages within the absolute maximum ratings limit for the ADPA7006 V_{GG1} pin. To set the minimum voltages, set the R15 and R16 resistors to the values shown in Figure 55 and Figure 56. Refer to the AN-1363 Application Note, *Meeting Biasing Requirements of Externally Biased RF/Microwave Amplifiers with Active Bias Controllers*, for more information and calculations for R15 and R16.

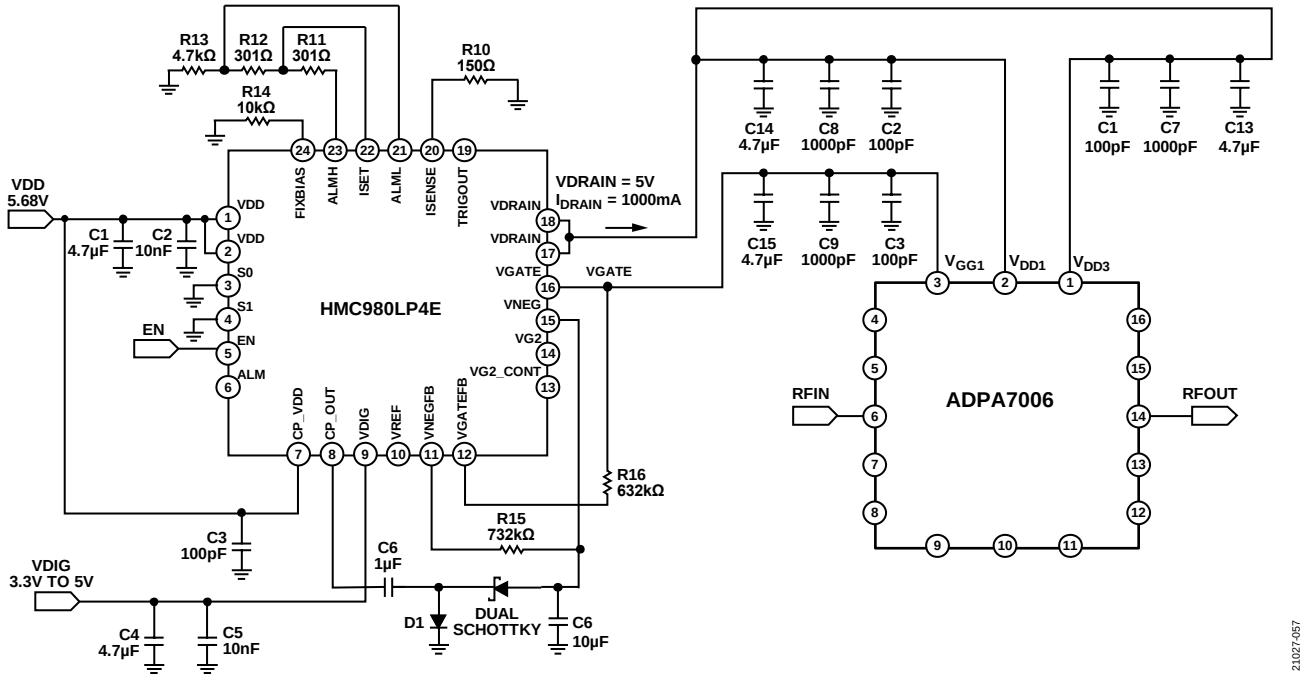

Figure 55. Application Circuit Using the HMC980LP4E with the ADPA7006

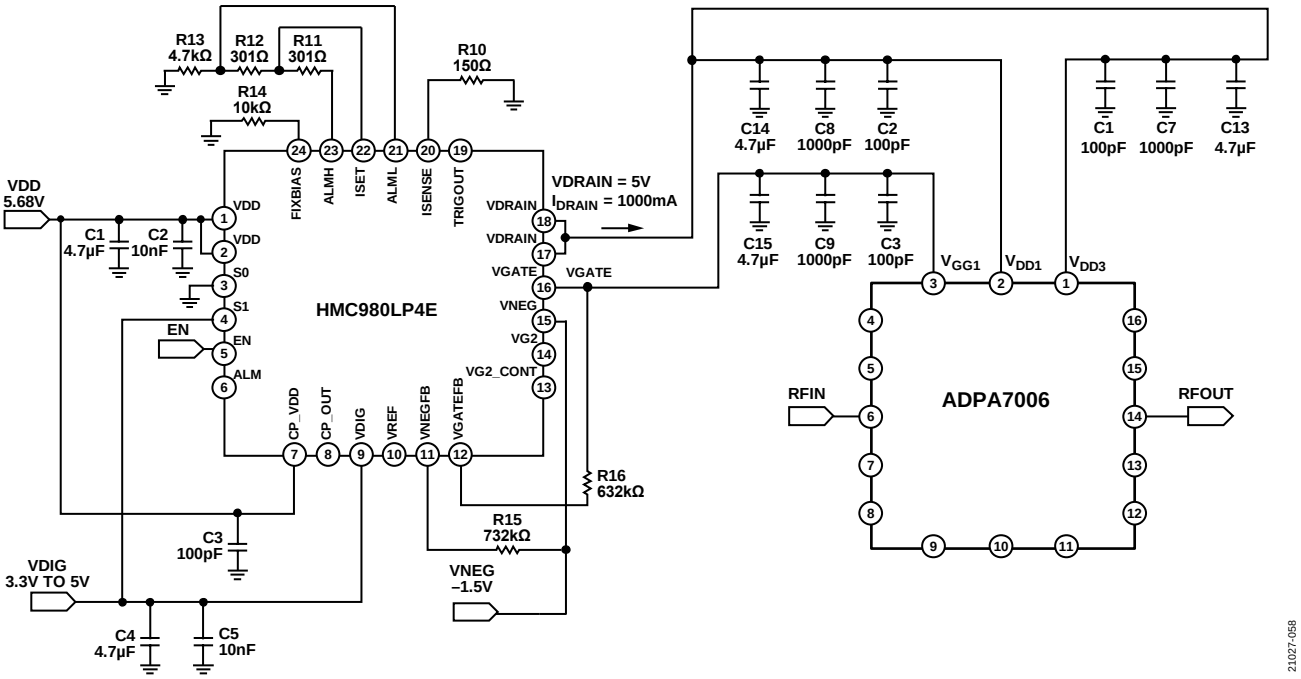

Figure 56. Application Circuit Using the HMC980LP4E with the ADPA7006 as an External Negative Voltage Source

HMC980LP4E BIAS SEQUENCE

Proper dc supply sequencing is required to prevent damage to the HMC980LP4E. Adhere to the following power-up sequence steps:

1. Set VDIG, the voltage supply input (Pin 9) for the HMC980LP4E digital circuit (see Figure 56), to 3.3 V.
2. Connect S0 (Pin 3) to ground.
3. Connect S1, the digital control pin (Pin 4) that sets the internal field effect transistor (FET) and the internal HMC980LP4E resistor (R_{DS_ON}) resistance (see Figure 56), to VDIG (3.3 V).
4. Set the VDD pins of the HMC980LP4E to 5.85 V.
5. Set VNEG (Pin 15 of the HMC980LP4E) to −1.5 V. This step is not needed if using an internally generated voltage.
6. Set EN (Pin 5) of the HMC980LP4E to 3.3 V. Transitioning from 0 V to 3.3 V turns on the VGATE and VDRAIN pins of the HMC980LP4E.

Adhere to the following power-down sequence steps:

1. Set EN (Pin 5 of the HMC980LP4E) to 0 V. Transitioning from 3.3 V to 0 V turns off the VDRAIN and VGATE pins of the HMC980LP4E.
2. Set VNEG (Pin 15 of the HMC980LP4E) to 0 V. This step is not required if using an internally generated voltage.
3. Set the VDD pins of the HMC980LP4E to 0 V.
4. Set S1 (Pin 4 of the HMC980LP4E) to 0 V.
5. Set VDIG (Pin 9 of the HMC980LP4E) to 0 V.

When the HMC980LP4E bias control circuit is set up, the ADPA7006 bias can be toggled on and off by applying 3.3 V or 0 V to the EN pin of the HMC980LP4E. If the EN pin is set to 3.3 V, the VGATE pin of the HMC980LP4E drops to −1.5 V, and the VDRAIN pin of the HMC980LP4E turns on at 5 V. The VGATE pin of the HMC980LP4E rises in voltage until I_{DRAIN} = 1000 mA. The closed control loop then regulates I_{DRAIN} at 1000 mA. When the EN = 0 V, the VGATE pin is automatically set to −1.5 V and the VDRAIN pin is set to 0 V (see Figure 57 and Figure 58).

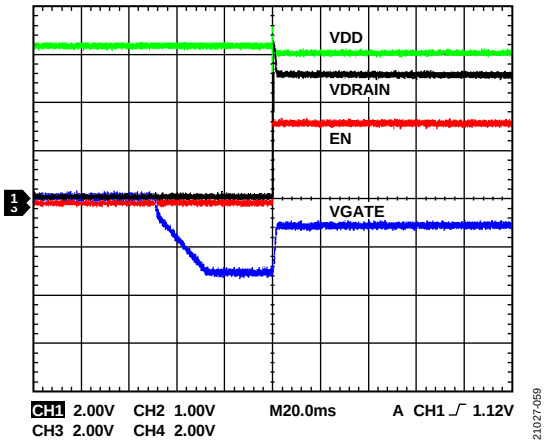

Figure 57. Turn On HMC980LP4E Outputs to the ADPA7006

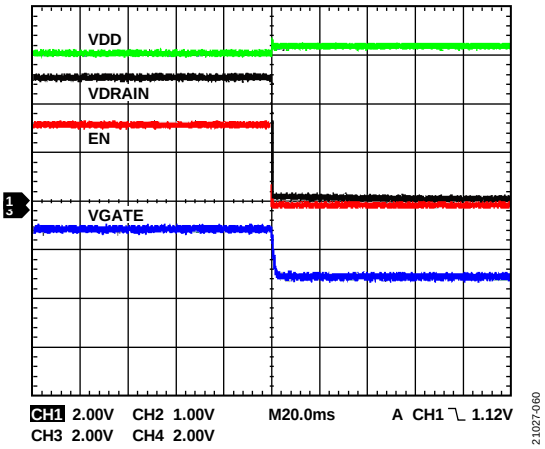

Figure 58. Turn Off HMC980LP4E Outputs to the ADPA7006

CONSTANT DRAIN CURRENT BIASING vs. CONSTANT GATE VOLTAGE BIASING

The HMC980LP4E uses a feedback loop to continuously adjust VGATE to maintain a constant drain current over dc supply, variation, temperature, RF input/output level, and device to device variation. Constant drain current bias is the preferred method for reducing time in calibration procedures and for maintaining consistent performance over time.

Figure 59 through Figure 62 compare the performance of the ADPA7006 with drain current control and gate voltage control.

In comparison to a constant gate voltage bias, where the current increases when RF power is applied, a constant drain current has a slightly lower output P1dB. This output P1dB is shown in Figure 62, where the RF performance is slightly lower than constant gate bias voltage operation due to a lower drain current at high input power (see Figure 59) as the HMC980LP4E reaches 1 dB compression.

The output P1dB performance for constant drain current bias can be increased toward the constant gate voltage bias performance by increasing the set current toward the I_{DD} value it reaches under RF drive in the constant gate voltage bias condition (see Figure 62).

The limit of increasing drain current under the constant current operation is set by the thermal limitations found in Table 5 with the maximum power dissipation specification. As the I_{DD} increase continues, the actual output P1dB does not continue to increase indefinitely but the power dissipation increases linearly. Therefore, take the trade-off between the power dissipation and output P1dB performance into consideration when using constant drain current biasing.

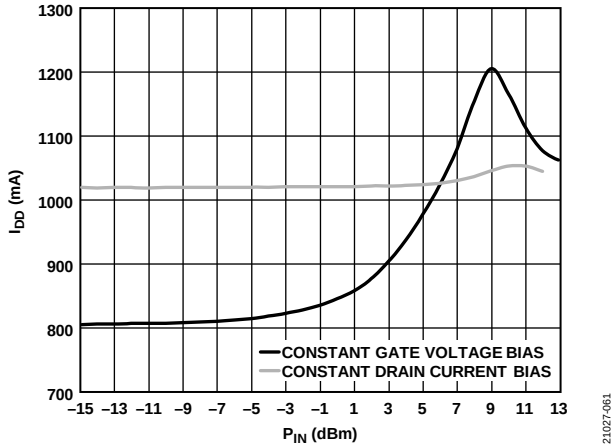

Figure 59. I_{DD} vs. P_{IN}, V_{DD} = 5 V, Frequency = 30 GHz, Constant Drain Current Bias (I_{DRAIN} Setpoint = 1000 mA) and Constant Gate Voltage Bias (V_{GG1} ≈ −0.68 V)

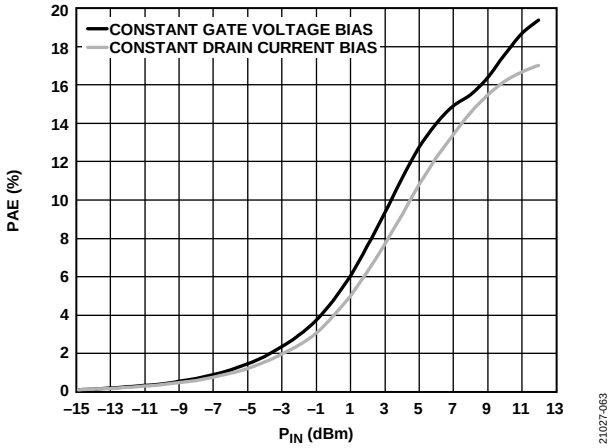

Figure 61. PAE vs. Input Power, V_{DD} = 5 V, Frequency = 30 GHz, Constant Drain Current Bias (I_{DRAIN} Setpoint = 1000 mA) and Constant Gate Voltage Bias (V_{GG1} ≈ −0.68 V)

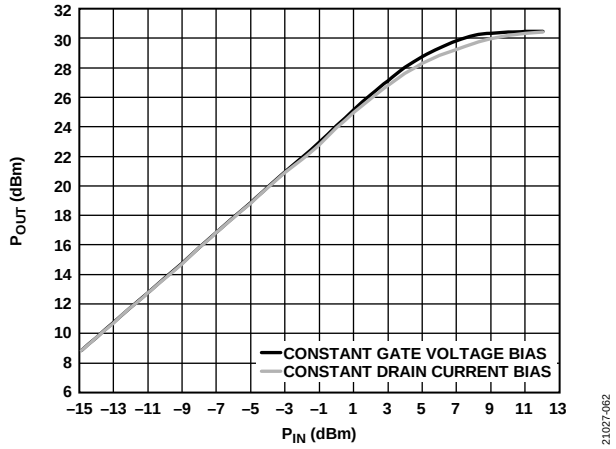

Figure 60. P_{OUT} vs. P_{IN}, V_{DD} = 5 V, Frequency = 32 GHz, Constant Drain Current Bias (I_{DRAIN} Setpoint = 1000 mA) and Constant Gate Voltage Bias (V_{GG1} ≈ −0.68 V)

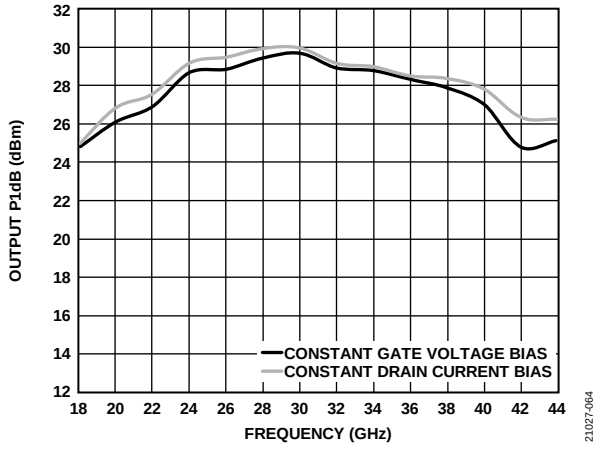

Figure 62. Output P1dB vs. Frequency, V_{DD} = 5 V, Constant Drain Current Bias (I_{DRAIN} Setpoint = 1000 mA) and Constant Gate Voltage Bias (V_{GG1} ≈ −0.68 V)

OUTLINE DIMENSIONS

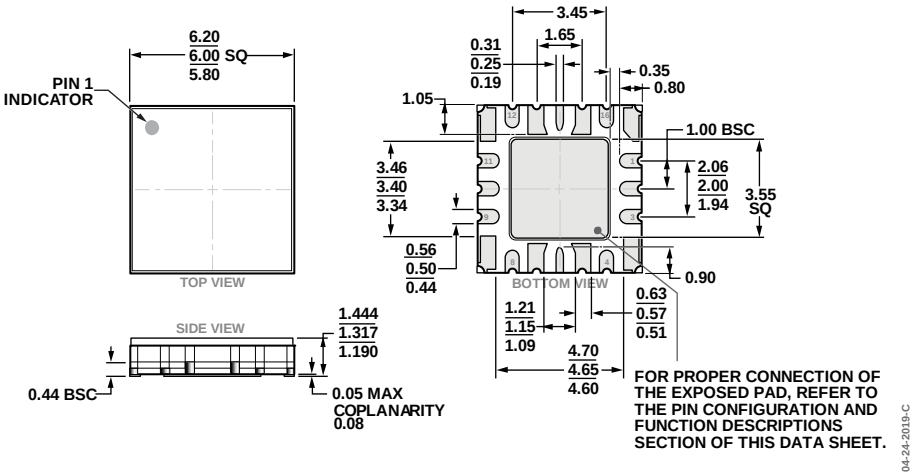

Figure 63. 16-Terminal Ceramic Leadless Chip Carrier with Heat Sink [LCC_HS] (EH-16-1)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	MSL Rating[2]	Package Description	Package Option
ADPA7006AEHZ	−40°C to +85°C	MSL3	16-Terminal Ceramic Leadless Chip Carrier with Heat Sink [LCC_HS]	EH-16-1
ADPA7006AEHZ-R7	−40°C to +85°C	MSL3	16-Terminal Ceramic Leadless Chip Carrier with Heat Sink [LCC_HS]	EH-16-1
ADPA7006-EVALZ			Evaluation PCB	

[1] Z = RoHS Compliant Part
[2] See the Absolute Maximum Ratings section for further information on the moisture sensitivity level (MSL) rating.

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