VS-702-1005-805M664062

Voltage Controlled SAW Oscillator

Description

The VS-702 is a SAW Based Voltage Controlled Oscillator that achieves low phase noise and very low jitter performance. The VS-702 is housed in an industry standard hermetically sealed LCC package and available in tape and reel.

Features

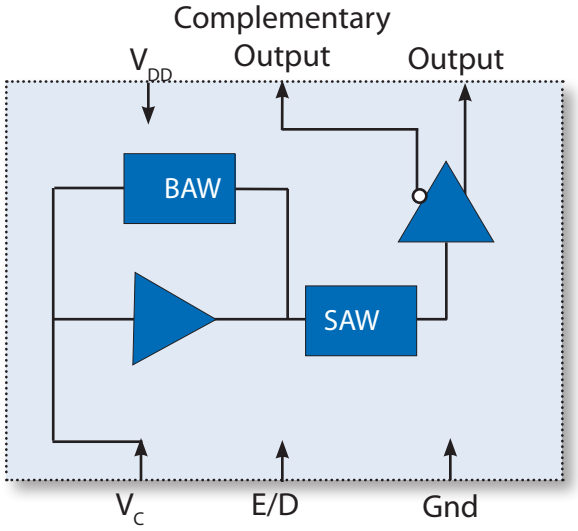
- Industry Standard Package, 5.0 x 7.5 x 2.0 mm
- 805.664062MHz
- 3.3 V Operation
- LV-PECL
- Improved Temperature Stability over Standard VCSO (±20 ppm)
- Output Power Down Feature
- -40/85°C operating temperature
- Product is free of lead and compliant to EC RoHS Directive

Applications

Ideal for PLL circuits for clock smoothing and frequency translation

- SONET, SDH
- Synchronous Ethernet
- Fiber Channel
- LAN / WAN
- Test and Measurement

Block Diagram



Performance Specifications

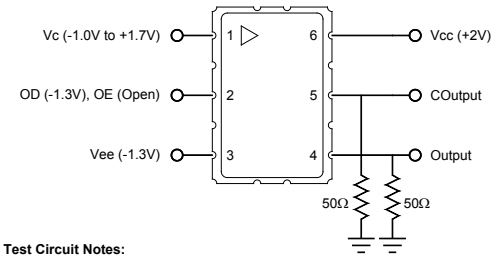
Table 1. Electrical Performance

Parameter	Symbol	Min	Typical	Maximum	Units
Supply					
Voltage[1]	V_{DD}	2.97	3.3	3.63	V
Current (No Load)	I_{DD}		55	70	mA
Current power down mode			10		mA
Frequency					
Nominal Frequency[2]	f_N		805.664062		MHz
Absolute Pull Range [3,6]	APR	±110			ppm
Linearity[3]	Lin		5	10	%
Gain Transfer Positive[3] (See pg 5)	K_V		+100		ppm/V
Temperature Stability[3]	f_{STAB}		±20		ppm
Outputs					
Mid Level - LVPECL [2, 3]		V_{CC}-1.4	V_{CC}-1.25	V_{CC}-1.0	V
Swing - LVPECL [2, 3]		450	600	750	mV-pp
Current	I_{OUT}			20	mA
Rise Time[4] Fall Time[4]	t_R t_F			500 500	ps ps
Symmetry[3]	SYM	45	50	55	%
Jitter (12 kHz - 20 MHz BW)[5]	ϕJ		0.1	0.250	ps-rms
Period Jitter, RMS[7]	ϕJ		2.5	3.0	ps
Period Jitter, Peak - Peak[7]	ϕJ		16	24	ps
Phase Noise (881.28 MHz)[8]					
1kHz				-104	dBc/Hz
10kHz				-114	dBc/Hz
100kHz				-129	dBc/Hz
1MHz				-132	dBc/Hz
10MHz				-133	dBc/Hz
Spurious Suppression[2]			-60	-50	dBc
Control Voltage					
Control Voltage Range for APR	V_C	0.3		3.0	V
Control Voltage Input Impedance	Z_{IN}	75			KΩ
Control Voltage Modulation BW	BW	50			kHz
Enable/Disable					
Power Up Power Down	V_{IH} V_{IL}	0.7*V_{DD}		 0.3*V_{DD}	V V
Operating Temperature	T_{OP}	-40/85			°C
Package Size		5.0 x 7.5 x 2.0			mm

1] The VS-702 power supply should be filtered, eg, 0.1 and 0.01uF to ground
2] See Standard Frequencies and Ordering Information tables for more specific information
3] Parameters are tested with production test circuit below (Fig 1).
4] Measured from 20% to 80% of a full output swing (Fig 2).
5] Integrated across stated bandwidth.
6] Tested with Vc = 0.3V to 3.0V unless otherwise stated in part description
7] Broadband Period Jitter measured using Lecroy Wavemaster 8600A 6 GHz Oscilloscope, 25K samples taken. See application note.
8] Not tested in production, guaranteed by design

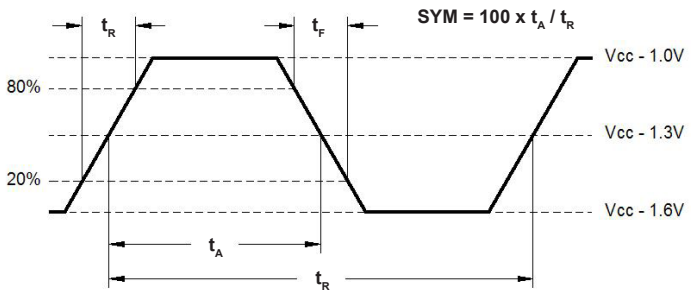
LVPECL Test Circuit

Fig 1: Test Circuit

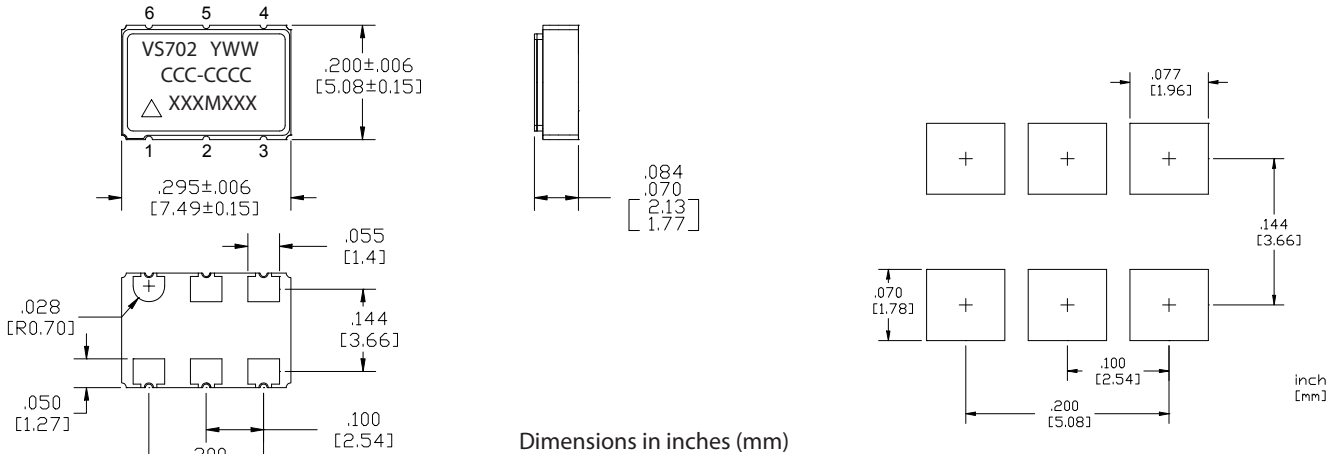


Test Circuit Notes:
1) To Permit 50Ω Measurement of Outputs, all DC Inputs are Biased Down 1.3V.
2) All Voltage Sources Contain Bypass Capacitors to Minimize Supply Noise.
3) 50Ω Terminations are Within Test Equipment.

Fig 2: LVPECL Waveform



Outline Drawing & Pad Layout



Dimensions in inches (mm)

Table 2. Pin Out

Pin	Symbol	Function
1	V_C	VCXO Control Voltage
2	E/D	High = Enable Low = Disable (power down mode)
3	GND	Case and Electrical Ground
4	Output	Output
5	COutput	Complementary Output
6	V_{DD}	Power Supply Voltage (3.3V ±10%)

Ordering Information

VS - 702 - 1005 - 805M664062

Product Family
VS: VCSO

Package
702: 5 x 7.5 x 2.0 mm

Input
E: 3.3 Vdc ±10%

Output
LVPECL (45/55% Symmetry)

Operating Temperature
-40/85°C

Performance Options
Improved Phase Noise

Enable/Disable
High = Enable, Low = Disable (power down mode)

Stability
Standard

Absolute Pull Range
±110ppm

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