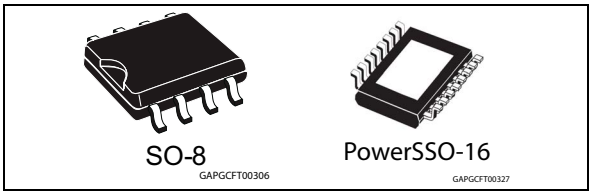
VN7050AS-E
VN7050AJ-E

High-side driver with MultiSense analog feedback for automotive application

Datasheet - preliminary data



Features

Max transient supply voltage	V_{CC}	40 V
Operating voltage range	V_{CC}	4 to 28 V
Typ. on-state resistance (per Ch)	R_{ON}	50 mΩ
Current limitation (typ)	I_{LIMH}	30 A
Stand-by current (max)	I_{STBY}	0.5 µA

- General
  - Single channel smart high-side driver with MultiSense analog feedback
  - Very low standby current
  - Compatible with 3 V and 5 V CMOS outputs
- MultiSense diagnostic functions
  - Multiplexed analog feedback of: load current with high precision proportional current mirror, V_{CC} supply voltage and T_{CHIP} device temperature
  - Overload and short to ground (power limitation) indication
  - Thermal shutdown indication
  - OFF-state open-load detection
  - Output short to V_{CC} detection
  - Sense enable/ disable
- Protections
  - Undervoltage shutdown
  - Overvoltage clamp
  - Load current limitation
  - Self limiting of fast thermal transients
  - Loss of ground and loss of V_{CC}
  - Configurable latch-off on overtemperature or power limitation with dedicated fault reset pin
  - Reverse battery with external components
  - Electrostatic discharge protection

Applications

- All types of automotive resistive, inductive and capacitive loads
- Specially intended for Automotive Turn Indicators (up to P27W or SAE1156 or LED Rear Combinations)

Description

The VN7050AS-E and VN7050AJ-E are single channel high-side driver manufactured using ST proprietary VIPower® technology and housed in PowerSSO-16 and SO-8 packages. The devices are designed to drive 12 V automotive grounded loads through a 3 V and 5 V CMOS-compatible interface, and to provide protection and diagnostics.

The devices integrate advanced protective functions such as load current limitation, overload active management by power limitation and overtemperature shutdown with configurable latch-off. A $\overline{\text{FaultRST}}$ pin unlatches the output in case of fault or disables the latch-off functionality.

A dedicated multifunction multiplexed analog output pin delivers sophisticated diagnostic functions including high precision proportional load current sense, supply voltage feedback and chip temperature sense, in addition to the detection of overload and short circuit to ground, short to V_{CC} and OFF-state open-load.

A sense enable pin allows OFF-state diagnosis to be disabled during the module low-power mode as well as external sense resistor sharing among similar devices.

This is preliminary information on a new product now in development or undergoing evaluation. Details are subject to change without notice.

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1 Block diagram and pin description

Figure 1. Block diagram

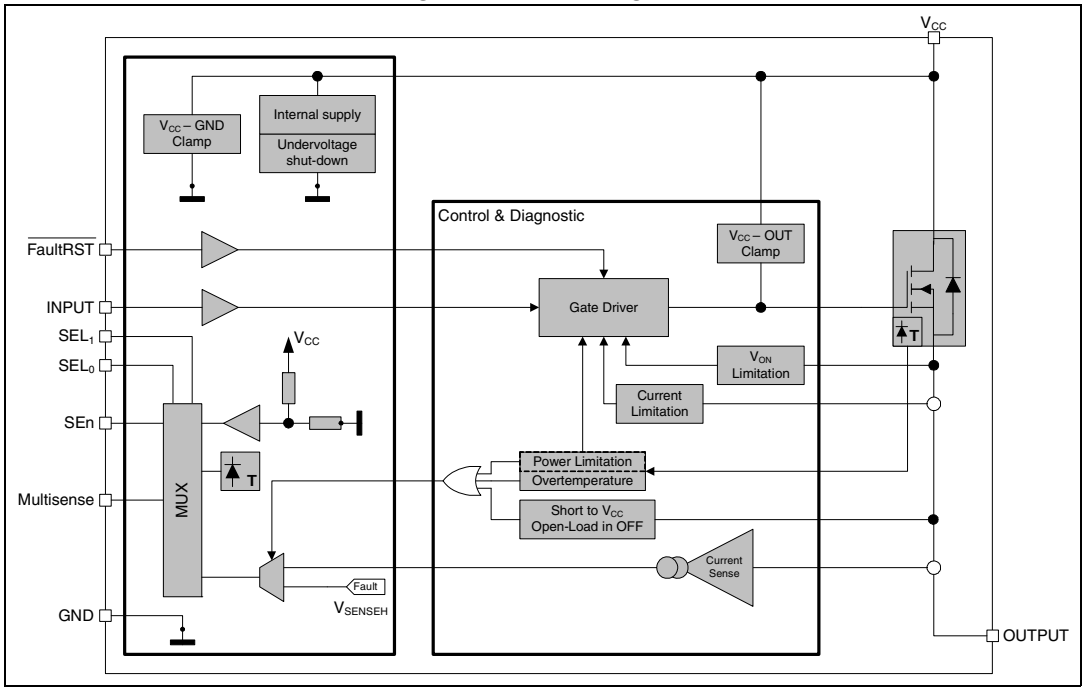


Table 1. Pin functions

Name	Function
V_{CC}	Battery connection.
OUTPUT	Power output.
GND	Ground connection. Must be reverse battery protected by an external diode / resistor network.
INPUT	Voltage controlled input pin with hysteresis, compatible with 3 V and 5 V CMOS outputs. It controls output switch state.
MultiSense	Multiplexed analog sense output pin; it delivers a current proportional to the selected diagnostic: load current, supply voltage or chip temperature.
SEn	Active high compatible with 3 V and 5 V CMOS output pin; it enables the MultiSense diagnostic pin.
$SEL_{0,1}$	Active high compatible with 3 V and 5 V CMOS output pin; they address the MultiSense multiplexer.
$\overline{FaultRST}$	Active low compatible with 3 V and 5 V CMOS output pin; unlatches the output in case of fault; If kept low, sets the outputs in auto-restart mode.

Figure 2. Configuration diagram (top view)

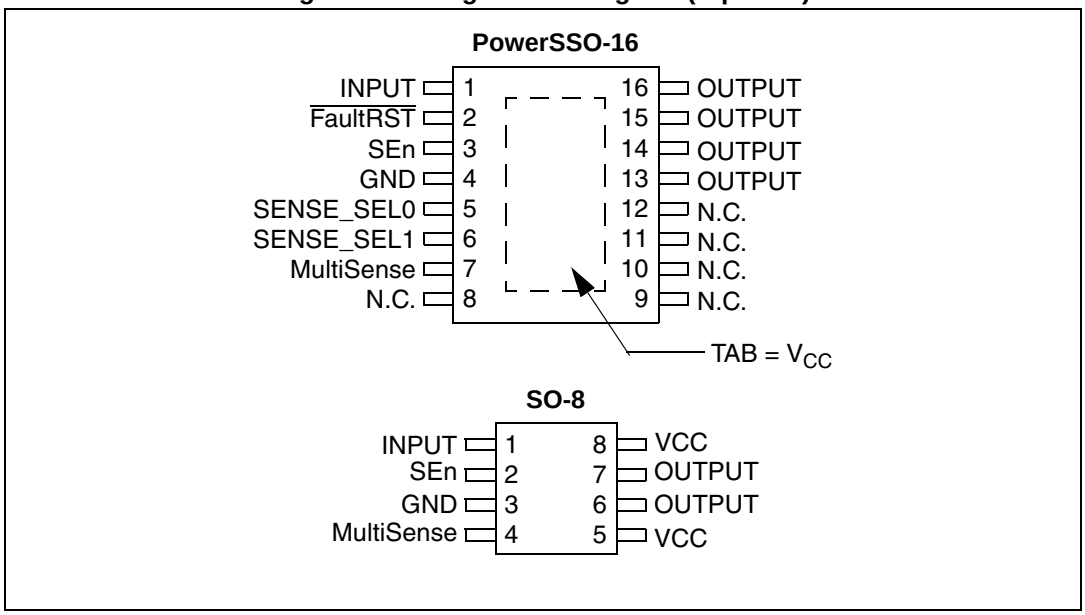


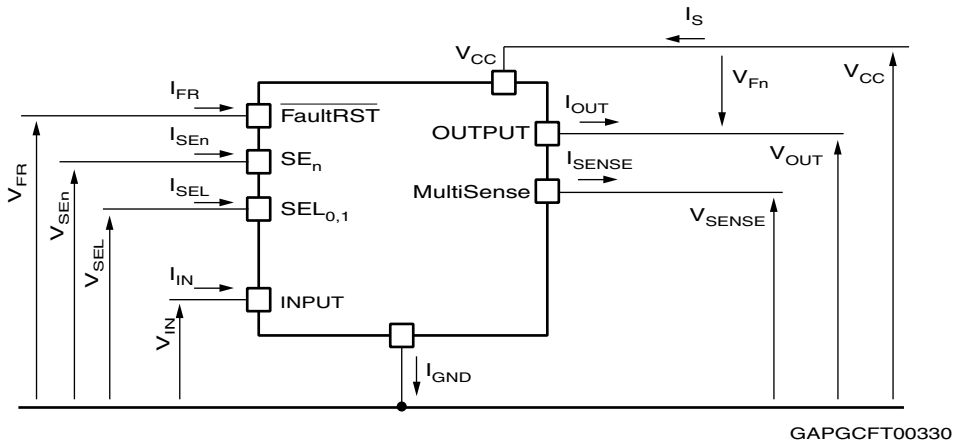
Table 2. Suggested connections for unused and not connected pins

Connection / pin	MultiSense	N.C.	Output	Input	SEn, SELx, $\overline{\text{FaultRST}}$
Floating	Not allowed	X(1)	X	X	X
To ground	Through 1 kΩ resistor	X	Not allowed	Through 15 kΩ resistor	Through 15 kΩ resistor

1. X: do not care.

2 Electrical specification

Figure 3. Current and voltage conventions



Note: $V_F = V_{OUT} - V_{CC}$ during reverse battery condition.

2.1 Absolute maximum ratings

Stressing the device above the rating listed in *Table 3* may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to the conditions in table below for extended periods may affect device reliability.

Table 3. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	DC supply voltage	38	V
$-V_{CC}$	Reverse DC supply voltage	0.3	
V_{CCPK}	Maximum transient supply voltage (ISO 16750-2:2010 Test B clamped to 40 V; R_L = 4 Ω)	40	
V_{CCJS}	Maximum jump start voltage for single pulse short circuit protection	28	
$-I_{GND}$	DC reverse ground pin current	200	mA
I_{OUT}	OUTPUT DC output current	Internally limited	A
$-I_{OUT}$	Reverse DC output current	10	
I_{IN}	INPUT DC input current	-1 to 10	mA
I_{SEn}	SEn DC input current		
I_{SEL}	$SEL_{0,1}$ DC input current		
I_{FR}	FaultRST DC input current	-1 to 10	
V_{FR}	FaultRST DC input voltage	7.5	V

Table 3. Absolute maximum ratings (continued)

Symbol	Parameter	Value	Unit
I_{SENSE}	MultiSense pin DC output current (V_{GND} = V_{CC} and V_{SENSE} < 0 V)	10	mA
	MultiSense pin DC output current in reverse (V_{CC} < 0 V)	-20	
E_{MAX}	Maximum switching energy (single pulse) (T_{DEMAG} = 0.4 ms; T_{jstart} = 150 °C)	30	mJ
V_{ESD}	Electrostatic discharge (JEDEC 22A-114F) – INPUT – MultiSense – SEn, $SEL_{0,1}$, FaultRST – OUTPUT – V_{CC}	 4000 2000 4000 4000 4000	 V V V V V
V_{ESD}	Charge device model (CDM-AEC-Q100-011)	750	V
T_j	Junction operating temperature	-40 to 150	°C
T_{stg}	Storage temperature	-55 to 150	

2.2 Thermal data

Table 4. Thermal data

Symbol	Parameter	Typ. value		Unit
		SO-8	PSSO-16	
$R_{thj\text{-}board}$	Thermal resistance junction-board (JEDEC JESD 51-5/51-8) (1)	29.4	6.8	°C/W
$R_{thj\text{-}amb}$	Thermal resistance junction-ambient (JEDEC JESD 51-5) (2)	67.5	58.5	
$R_{thj\text{-}amb}$	Thermal resistance junction-ambient (JEDEC JESD 51-7) (1)	45.8	24.5	

1. Device mounted on four-layers 2s2p PCB.
2. Device mounted on two-layers 2s0p PCB with 2 cm^2 heatsink copper trace.

2.3 Main electrical characteristics

7 V < V_{CC} < 28 V; -40 °C < T_j < 150 °C, unless otherwise specified.

All typical values refer to V_{CC} = 13 V; T_j = 25°C, unless otherwise specified.

Table 5. Power section

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{CC}	Operating supply voltage		4	13	28	V
V_{USD}	Undervoltage shutdown				4	
$V_{USDReset}$	Undervoltage shutdown reset				5	
$V_{USDhyst}$	Undervoltage shutdown hysteresis			0.3		
R_{ON}	On-state resistance	I_{OUT} = 2 A; T_j = 25 °C		50		mΩ
		I_{OUT} = 2 A; T_j = 150 °C			100	
		I_{OUT} = 2 A; V_{CC} = 4 V; T_j = 25 °C			75	
V_{clamp}	Clamp voltage	I_S = 20 mA; T_j = -40 °C	38			V
		I_S = 20 mA; 25°C < T_j < 150°C	41	46	52	
I_{STBY}	Supply current in standby at V_{CC} = 13 V(1)	V_{CC} = 13 V; V_{IN} = V_{OUT} = V_{SEn} 0 V; V_{FR} = $V_{SEL0,1}$ = 0 V; T_j = 25 °C			0.5	µA
		V_{CC} = 13 V; V_{IN} = V_{OUT} = V_{SEn} 0 V; V_{FR} = $V_{SEL0,1}$ = 0 V; T_j = 85 °C (2)			0.5	
		V_{CC} = 13 V; V_{IN} = V_{OUT} = V_{SEn} 0 V; V_{FR} = $V_{SEL0,1}$ = 0 V; T_j = 125 °C			3	
t_{D_STBY}	Standby mode blanking time	V_{CC} = 13 V; V_{IN} = V_{OUT} = V_{FR} = $V_{SEL0,1}$ = 0V; V_{SEn} = 5 V to 0 V	60	300	550	µs
$I_{S(ON)}$	Supply current	V_{CC} = 13 V; V_{SEn} = 0 V; $V_{SEL0,1}$ = V_{FR} = 0V; V_{IN} = 5 V; I_{OUT} = 0 A		3	5	mA
$I_{GND(ON)}$	Control stage current consumption in ON-state. All channels active.	V_{CC} = 13 V; V_{SEn} = 5 V; $V_{SEL0,1}$ = V_{FR} = 0 V; V_{IN} = 5 V; I_{OUT} = 2 A			6	mA
$I_{L(off)}$	Off-state output current at V_{CC} = 13 V	V_{IN} = V_{OUT} = 0 V; V_{CC} = 13 V; T_j = 25 °C	0	0.01	0.5	µA
		V_{IN} = V_{OUT} = 0 V; V_{CC} = 13 V; T_j = 125 °C	0		3	
V_F	Output - V_{CC} diode voltage	I_{OUT} = -2 A; T_j = 150 °C			0.7	V

1. PowerMOS leakage included.
2. Parameter specified by design; not subject to production test.

Table 6. Switching (V_{CC} = 13 V; -40°C < T_j < 150°C, unless otherwise specified[1])

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time at T_j = 25°C	R_L = 6.5 Ω	10	60	120	µs
$t_{d(off)}$	Turn-off delay time at T_j = 25°C	R_L = 6.5 Ω	10	40	100	
$(dV_{OUT}/dt)_{on}$	Turn-on voltage slope at T_j = 25°C	R_L = 6.5 Ω	0.1	0.32	0.7	V/µs
$(dV_{OUT}/dt)_{off}$	Turn-off voltage slope at T_j = 25°C	R_L = 6.5 Ω	0.1	0.32	0.7	
W_{ON}	Switching energy losses at turn-on (t_{won})	R_L = 6.5 Ω	—	0.3	0.38[2]	mJ
W_{OFF}	Switching energy losses at turn-off (t_{woff})	R_L = 6.5 Ω	—	0.23	0.29[2]	mJ
t_{SKEW}	Differential Pulse skew (t_{PHL} - t_{PLH}) see *Figure 4*	R_L = 6.5 Ω	-80	-30	20	µs

1. See *Figure 4: Switching times and Pulse skew*.
2. Parameter guaranteed by design and characterization; not subject to production test.

Table 7. Logic Inputs (7 V < V_{CC} < 28 V; -40°C < T_j < 150°C)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
INPUT characteristics						
V_{IL}	Input low level voltage				0.9	V
I_{IL}	Low level input current	V_{IN} = 0.9 V	1			µA
V_{IH}	Input high level voltage		2.1			V
I_{IH}	High level input current	V_{IN} = 2.1 V			10	µA
$V_{I(hyst)}$	Input hysteresis voltage		0.2			V
V_{ICL}	Input clamp voltage	I_{IN} = 1 mA	5.3		7.2	V
		I_{IN} = -1 mA		-0.7		
$\overline{\text{FaultRST}}$ characteristics (VN7050AJ-E only)						
V_{FRL}	Input low level voltage				0.9	V
I_{FRL}	Low level input current	V_{IN} = 0.9 V	1			µA
V_{FRH}	Input high level voltage		2.1			V
I_{FRH}	High level input current	V_{IN} = 2.1 V			10	µA
$V_{FR(hyst)}$	Input hysteresis voltage		0.2			V
V_{FRCL}	Input clamp voltage	I_{IN} = 1 mA	5.3		7.5	V
		I_{IN} = -1 mA		-0.3		
$SEL_{0,1}$ characteristics (VN7050AJ-E only) (7 V < V_{CC} < 18 V)						
V_{SELL}	Input low level voltage				0.9	V
I_{SELL}	Low level input current	V_{IN} = 0.9 V	1			µA
V_{SELH}	Input high level voltage		2.1			V

Table 7. Logic Inputs (7 V < V_{CC} < 28 V; -40°C < T_j < 150°C) (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SELH}	High level input current	V_{IN} = 2.1 V			10	µA
$V_{SEL(hyst)}$	Input hysteresis voltage		0.2			V
V_{SELCL}	Input clamp voltage	I_{IN} = 1 mA	5.3		7.2	V
		I_{IN} = -1 mA		-0.7		
SEn characteristics (7 V < V_{CC} < 18 V)						
V_{SEnL}	Input low level voltage				0.9	V
I_{SEnL}	Low level input current	V_{IN} = 0.9 V	1			µA
V_{SEnH}	Input high level voltage		2.1			V
I_{SEnH}	High level input current	V_{IN} = 2.1 V			10	µA
$V_{SEn(hyst)}$	Input hysteresis voltage		0.2			V
V_{SEnCL}	Input clamp voltage	I_{IN} = 1 mA	5.3		7.2	V
		I_{IN} = -1 mA		-0.7		

Table 8. Protections (7 V < V_{CC} < 18 V; -40°C < T_j < 150°C)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{LIMH}	DC short circuit current	V_{CC} = 13 V	21	30	42	A
		4 V < V_{CC} < 18 V(1)			42	A
I_{LIML}	Short circuit current during thermal cycling	V_{CC} = 13 V; $T_R < T_j < T_{TSD}$		10		A
T_{TSD}	Shutdown temperature		150	175	200	°C
T_R	Reset temperature(1)		T_{RS} + 1	T_{RS} + 7		
T_{RS}	Thermal reset of fault diagnostic indication	V_{FR} = 0 V; V_{SEn} = 5 V;	135			
T_{HYST}	Thermal hysteresis (T_{TSD} - T_R)(1)			7		
ΔT_{J_SD}	Dynamic temperature	T_j = -40 °C; V_{CC} = 13 V		60		K
t_{LATCH_RST}	Fault reset time for output unlatch(1) (VN7050AJ-E only)	V_{FR} = 5 V to 0 V; V_{SEn} = 5 V; V_{IN} = 5 V; $V_{SEL0,1}$ = 0 V	3	10	20	µs
V_{DEMAG}	Turn-off output voltage clamp	I_{OUT} = 2 A; L = 6 mH; T_j = -40 °C	V_{CC} - 38			V
		I_{OUT} = 2 A; L = 6 mH; T_j = 25 °C to 150 °C	V_{CC} - 41	V_{CC} - 46	V_{CC} - 52	V
V_{ON}	Output voltage drop limitation	I_{OUT} = 0.2 A		20		mV

1. Parameter guaranteed by design and characterization; not subject to production test.

Table 9. MultiSense (7 V < V_{CC} < 18 V; -40°C < T_j < 150°C)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{SENSE_CL}	MultiSense clamp voltage	V_{SEn} = 0 V; I_{SENSE} = 1 mA	-17		-12	V
		V_{SEn} = 0 V; I_{SENSE} = -1 mA		7		V
Current Sense characteristics						
K_{OL}	I_{OUT}/I_{SENSE}	I_{OUT} = 0.01 A; V_{SENSE} = 0.5 V; V_{SEn} = 5 V	470			
dK_{cal}/K_{cal} (1)(2)	Current sense ratio drift at calibration point	I_{OUT} = 0.01 A to 0.03 A; I_{cal} = 17.5 mA; V_{SENSE} = 0.5 V; V_{SEn} = 5 V	-30		30	%
K_{LED}	I_{OUT}/I_{SENSE}	I_{OUT} = 0.05 A; V_{SENSE} = 0.5 V; V_{SEn} = 5 V	575	1465	2360	
dK_{LED}/K_{LED} (1)(2)	Current sense ratio drift	I_{OUT} = 0.05 A; V_{SENSE} = 0.5 V; V_{SEn} = 5 V	-25		25	%
K_0	I_{OUT}/I_{SENSE}	I_{OUT} = 0.2 A; V_{SENSE} = 0.5 V; V_{SEn} = 5 V	830	1365	1935	
dK_0/K_0 (1)(2)	Current sense ratio drift	I_{OUT} = 0.2 A; V_{SENSE} = 0.5 V; V_{SEn} = 5 V	-20		20	%
K_1	I_{OUT}/I_{SENSE}	I_{OUT} = 0.4 A; V_{SENSE} = 4 V; V_{SEn} = 5 V	875	1250	1615	
dK_1/K_1 (1)(2)	Current sense ratio drift	I_{OUT} = 0.4 A; V_{SENSE} = 4 V; V_{SEn} = 5 V	-15		15	%
K_2	I_{OUT}/I_{SENSE}	I_{OUT} = 1.5 A; V_{SENSE} = 4 V; V_{SEn} = 5 V	980	1215	1470	
dK_2/K_2 (1)(2)	Current sense ratio drift	I_{OUT} = 1.5 A; V_{SENSE} = 4 V; V_{SEn} = 5 V	-10		10	%
K_3	I_{OUT}/I_{SENSE}	I_{OUT} = 4.5 A; V_{SENSE} = 4 V; V_{SEn} = 5 V	1000	1110	1220	
dK_3/K_3 (1)(2)	Current sense ratio drift	I_{OUT} = 4.5 A; V_{SENSE} = 4 V; V_{SEn} = 5 V	-5		5	%

Table 9. MultiSense (7 V < V_{CC} < 18 V; -40°C < T_j < 150°C) (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SENSE0}	MultiSense leakage current	MultiSense disabled: V_{SEn} = 0 V	0		0.5	µA
		MultiSense disabled: -1 V < V_{SENSE} < 5 V(1)	-0.5		0.5	
		MultiSense enabled: V_{SEn} = 5 V; Channel ON; I_{OUT} = 0 A; Diagnostic selected; V_{IN} = 5 V; V_{SEL0} = 0 V; V_{SEL1} = 0 V; I_{OUT} = 0 A;	0		2	
		MultiSense enabled: V_{SEn} = 5 V Channel OFF; Diagnostic selected: V_{IN} = 0 V; V_{SEL0} = 0 V; V_{SEL1} = 0 V	0		2	
V_{OUT_MSD}(1)	Output Voltage for MultiSense shutdown	V_{SEn} = 5 V; R_{SENSE} = 2.7 KΩ – E.g. Ch_0: V_{IN0} = 5 V; V_{SEL0} = 0 V; V_{SEL1} = 0 V; I_{OUT} = 2 A		5		V
V_{SENSE_SAT}	MultiSense saturation voltage	V_{CC} = 7 V; R_{SENSE} = 2.7 KΩ; V_{SEn} = 5 V; V_{IN} = 5 V; V_{SEL0} = 0 V; V_{SEL1} = 0 V; I_{OUT} = 2 A; T_j = 150°C	5			V
I_{SENSE_SAT}(1)	CS saturation current	V_{CC} = 7 V; V_{SENSE} = 4 V; V_{IN} = 5 V; V_{SEn} = 5 V; V_{SEL0} = 0 V; V_{SEL1} = 0 V; T_j = 150°C	4			mA
I_{OUT_SAT}(1)	Output saturation current	V_{CC} = 7 V; V_{SENSE} = 4 V; V_{IN} = 5 V; V_{SEn} = 5 V; V_{SEL0} = 0 V; V_{SEL1} = 0 V; T_j = 150°C	6			A
OFF-state diagnostic						
V_{OL}	OFF-state open-load voltage detection threshold	V_{IN} = 0 V; V_{SEn} = 5 V; V_{SEL0} = 0 V; V_{SEL1} = 0 V;	2	3	4	V
$I_{L(off2)}$	OFF-state output sink current	V_{IN} = 0 V; V_{OUT} = V_{OL}	-100		-15	µA
t_{DSTKON}	OFF-state diagnostic delay time from falling edge of INPUT (see *Figure 7*)	V_{IN} = 5 V to 0 V; V_{SEn} = 5 V; V_{SEL0} = 0 V; V_{SEL1} = 0 V; I_{OUT} = 0 A; V_{OUT} = 4 V	100	350	700	µs

Table 9. MultiSense (7 V < V_{CC} < 18 V; -40°C < T_j < 150°C) (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{D_OL_V}$	Settling time for valid OFF-state open load diagnostic indication from rising edge of SEn	V_{IN} = 0 V; V_{FR} = 0 V; V_{SEL0} = 0 V; V_{SEL1} = 0 V; V_{OUT} = 4 V; V_{SEn} = 0 V to 5 V			60	µs
t_{D_VOL}	OFF-state diagnostic delay time from rising edge of V_{OUT}	V_{IN} = 0 V; V_{SEn} = 5 V; V_{SEL0} = 0 V; V_{SEL1} = 0 V; V_{OUT} = 0 V to 4 V		5	30	µs
Chip temperature analog feedback (VN7050AJ-E only)						
V_{SENSE_TC}	MultiSense output voltage proportional to chip temperature	V_{SEn} = 5 V; V_{SEL0} = 0 V; V_{SEL1} = 5 V; V_{IN} = 0 V; R_{SENSE} = 1 KΩ; T_j = -40 °C	2.325	2.41	2.495	V
		V_{SEn} = 5 V; V_{SEL0} = 0 V; V_{SEL1} = 5 V; V_{IN} = 0 V; R_{SENSE} = 1 KΩ; T_j = 25 °C	1.985	2.07	2.155	V
		V_{SEn} = 5 V; V_{SEL0} = 0 V; V_{SEL1} = 5 V; V_{IN} = 0 V; R_{SENSE} = 1 KΩ; T_j = 125 °C	1.435	1.52	1.605	V
dV_{SENSE_TC}/dT(1)	Temperature coefficient	T_j = -40 °C to 150 °C		-5.5		mV/K
Transfer function		V_{SENSE_TC} (T) = V_{SENSE_TC} (T_0) + dV_{SENSE_TC} / dT * (T - T_0)				
V_{CC} supply voltage analog feedback (VN7050AJ-E only)						
V_{SENSE_VCC}	MultiSense output voltage proportional to V_{CC} supply voltage	V_{CC} = 13 V; V_{SEn} = 5 V; V_{SEL0} = 5 V; V_{SEL1} = 5 V; V_{IN} = 0 V; R_{SENSE} = 1 KΩ	3.16	3.23	3.3	V
Transfer function(3)		V_{SENSE_VCC} = V_{CC} / 4				
Fault diagnostic feedback (see *Table 10*)						
V_{SENSEH}	MultiSense output voltage in fault condition	V_{CC} = 13 V; R_{SENSE} = 1 kΩ; V_{SEn} = 5 V; V_{IN} = 0 V; V_{SEL0} = 0 V; V_{SEL1} = 0 V; I_{OUT} = 0 A; V_{OUT} = 4 V	5		6.6	V
I_{SENSEH}	MultiSense output current in fault condition	V_{CC} = 13 V; V_{SENSE} = 5 V	7	20	30	mA

Table 9. MultiSense (7 V < V_{CC} < 18 V; -40°C < T_j < 150°C) (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
MultiSense timings (current sense mode - see *Figure 5*)						
$t_{DSENSE1H}$	Current sense settling time from rising edge of SEn	V_{IN} = 5 V; V_{SEn} = 0 V to 5 V; R_{SENSE} = 1 KΩ; R_L = 6.5 Ω			60	µs
$t_{DSENSE1L}$	Current sense disable delay time from falling edge of SEn	V_{IN} = 5 V; V_{SEn} = 5 V to 0 V; R_{SENSE} = 1 KΩ; R_L = 6.5 Ω		5	20	
$t_{DSENSE2H}$	Current sense settling time from rising edge of INPUT	V_{IN} = 0 V to 5 V; V_{SEn} = 5 V; R_{SENSE} = 1 KΩ; R_L = 6.5 Ω		100	250	
$\Delta t_{DSENSE2H}$	Current sense settling time from rising edge of I_{OUT} (dynamic response to a step change of I_{OUT})	V_{IN} = 5 V; V_{SEn} = 5 V; R_{SENSE} = 1 KΩ; I_{SENSE} = 90 % of $I_{SENSEMAX}$; R_L = 6.5 Ω			100	
$t_{DSENSE2L}$	Current sense turn-off delay time from falling edge of INPUT	V_{IN} = 5 V to 0 V; V_{SEn} = 5 V; R_{SENSE} = 1 KΩ; R_L = 6.5 Ω		50	250	
MultiSense timings (chip temperature sense mode - see *Figure 6*) (VN7050AJ-E only)						
$t_{DSENSE3H}$	V_{SENSE_TC} settling time from rising edge of SEn	V_{SEn} = 0 V to 5 V; V_{SEL0} = 0 V; V_{SEL1} = 5 V; R_{SENSE} = 1 kΩ			60	µs
$t_{DSENSE3L}$	V_{SENSE_TC} disable delay time from falling edge of SEn	V_{SEn} = 5 V to 0 V; V_{SEL0} = 0 V; V_{SEL1} = 5 V; R_{SENSE} = 1 kΩ			20	µs
MultiSense timings (V_{CC} voltage sense mode - see *Figure 6*) (VN7050AJ-E only)						
$t_{DSENSE4H}$	V_{SENSE_VCC} settling time from rising edge of SEn	V_{SEn} = 0 V to 5 V; V_{SEL0} = 5 V; V_{SEL1} = 5 V; R_{SENSE} = 1 kΩ			60	µs
$t_{DSENSE4L}$	V_{SENSE_VCC} disable delay time from falling edge of SEn	V_{SEn} = 5 V to 0 V; V_{SEL0} = 5 V; V_{SEL1} = 5 V; R_{SENSE} = 1 kΩ			20	µs
MultiSense timings (Multiplexer transition times)(4) (VN7050AJ-E only)						
t_{D_CStoTC}	MultiSense transition delay from current sense to T_C sense	V_{IN} = 5 V; V_{SEn} = 5 V; V_{SEL0} = 0 V; V_{SEL1} = 0 V to 5 V; I_{OUT} = 1 A; R_{SENSE} = 1 kΩ			60	µs

Table 9. MultiSense (7 V < V_{CC} < 18 V; -40°C < T_j < 150°C) (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
t_{D_TCtoCS}	MultiSense transition delay from T_C sense to current sense	V_{IN} = 5 V; V_{SEn} = 5 V; V_{SEL0} = 0 V; V_{SEL1} = 5 V to 0 V; I_{OUT} = 1 A; R_{SENSE} = 1 kΩ			20	µs
$t_{D_CStoVCC}$	MultiSense transition delay from current sense to V_{CC} sense	V_{IN} = 5 V; V_{SEn} = 5 V; V_{SEL0} = 5 V; V_{SEL1} = 0 V to 5 V; I_{OUT} = 1 A; R_{SENSE} = 1 kΩ			60	µs
$t_{D_VCCtoCS}$	MultiSense transition delay from V_{CC} sense to current sense	V_{IN} = 5 V; V_{SEn} = 5 V; V_{SEL0} = 5 V; V_{SEL1} = 5 V to 0 V; I_{OUT} = 1 A; R_{SENSE} = 1 kΩ			20	µs
$t_{D_TCtoVCC}$	MultiSense transition delay from T_C sense to V_{CC} sense	V_{CC} = 13 V; T_j = 125 °C; V_{SEn} = 5 V; V_{SEL1} = 5 V; V_{SEL0} = 0 V to 5 V; R_{SENSE} = 1 kΩ			20	µs
$t_{D_VCCtoTC}$	MultiSense transition delay from V_{CC} sense to T_C sense	V_{CC} = 13 V; T_j = 125 °C; V_{SEn} = 5 V; V_{SEL1} = 5 V; V_{SEL0} = 5 V to 0 V; R_{SENSE} = 1 kΩ			20	µs

1. Parameter guaranteed by design and characterization; not subject to production test.
2. All values refer to V_{CC} = 13 V; T_j = 25°C, unless otherwise specified.
3. V_{CC} sensing and T_C are referred to GND potential.
4. Transition delay are measured up to +/- 10% of final conditions.

Figure 4. Switching times and Pulse skew

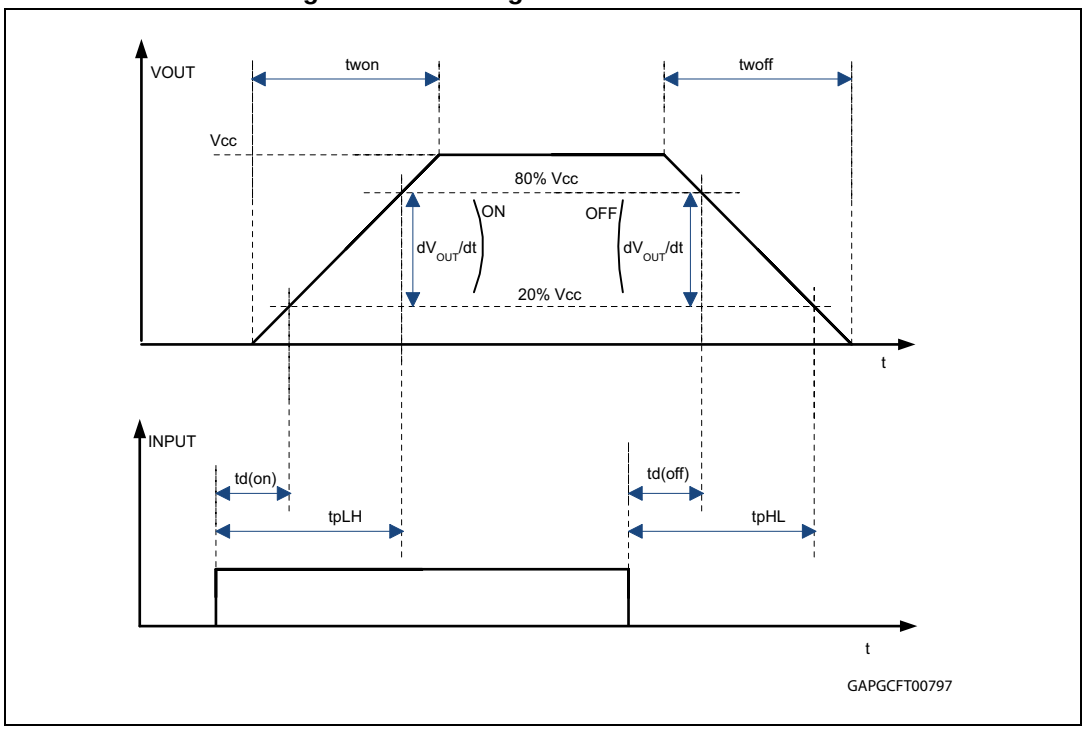


Figure 5. MultiSense timings (current sense mode)

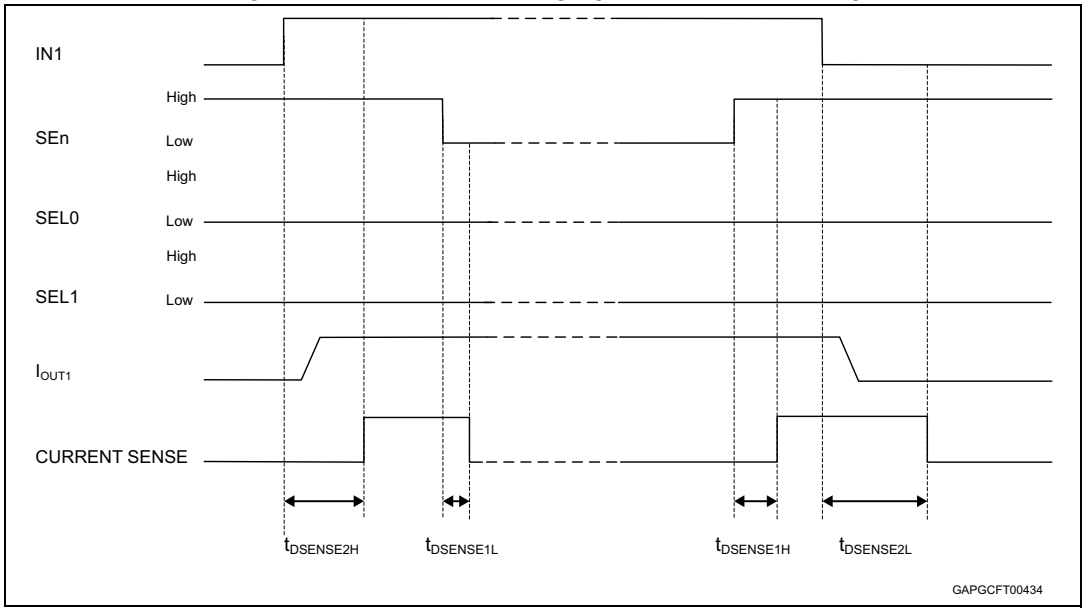


Figure 6. Multisense timings (chip temperature and V_{CC} sense mode)(VN7050AJ-E only)

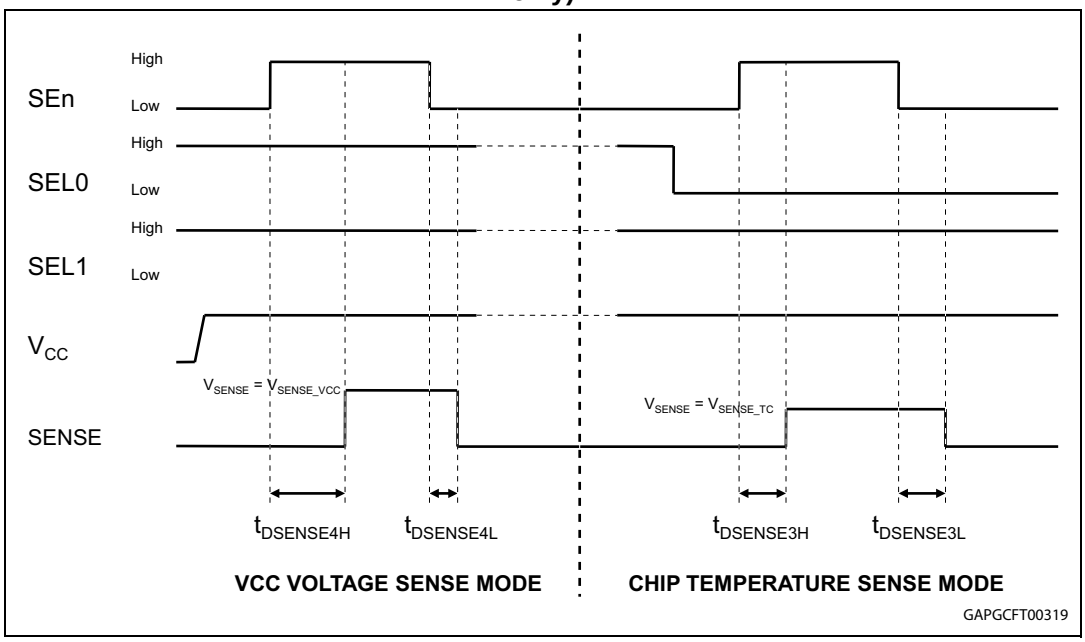


Figure 7. T_{DSTKON}

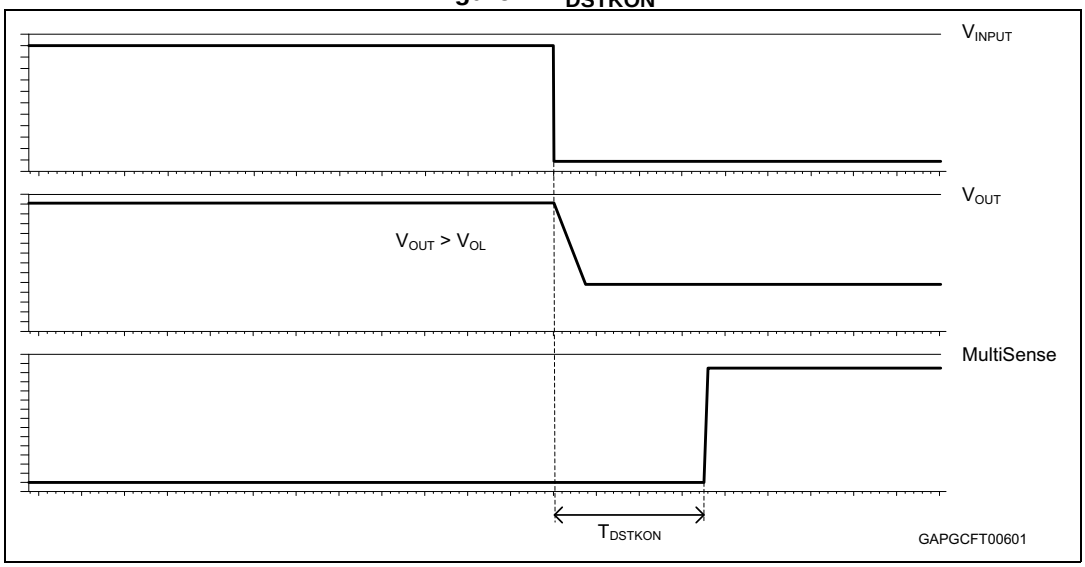


Table 10. Truth table

Mode	Conditions	IN_X	$FR^{(1)}$	SEn	$SEL_X^{(1)}$	OUT_X	MultiSense	Comments
Standby	All logic inputs low	L	L	L	L	L	Hi-Z	Low quiescent current consumption
Normal	Nominal load connected; T_j < 150°C	L	X	Refer to *Table 11*		L	Refer to *Table 11*	
		H	L			H		Outputs configured for auto-restart
		H	H			H		Outputs configured for Latch-off[1]
Overload	Overload or short to GND causing: $T_j > T_{TSD}$ or $\Delta T_j > \Delta T_{j_SD}$	L	X	Refer to *Table 11*		L	Refer to *Table 11*	
		H	L			H		Output cycles with temperature hysteresis
		H	H			L		Output latches-off[1]
Undervoltage	$V_{CC} < V_{USD}$ (falling)	X	X	X	X	L L	Hi-Z Hi-Z	Re-start when $V_{CC} > V_{USD} + V_{USDhyst}$ (rising)
OFF-state diagnostics	Short to V_{CC}	L	X	Refer to *Table 11*		H	Refer to *Table 11*	
	Open-load	L	X			H		External pull-up
Negative output voltage	Inductive loads turn-off	L	X	Refer to *Table 11*		< 0 V	Refer to *Table 11*	

1. VN7050AJ-E only.

Table 11. MultiSense multiplexer addressing

SEn	SEL_1	SEL_0	MUX channel	MultiSense output			
				Nomal mode	Overload	OFF-state diag.[1]	Negative output
SO-8							
L	n.a.	n.a.	n.a.	Hi-Z			
H	n.a.	n.a.	Channel diagnostic	I_{SENSE} = 1/K * I_{OUT}	V_{SENSE} = V_{SENSEH}	$V_{SENSE} = V_{SENSEH}$	Hi-Z
PowerSSO-16							
H	L	L	Channel diagnostic	I_{SENSE} = 1/K * I_{OUT}	V_{SENSE} = V_{SENSEH}	$V_{SENSE} = V_{SENSEH}$	Hi-Z
H	L	H	Channel diagnostic	I_{SENSE} = 1/K * I_{OUT}	V_{SENSE} = V_{SENSEH}	$V_{SENSE} = V_{SENSEH}$	Hi-Z
H	H	L	T_{CHIP} Sense	$V_{SENSE} = V_{SENSE_TC}$			
H	H	H	V_{CC} Sense	$V_{SENSE} = V_{SENSE_VCC}$			

1. In case the output channel corresponding to the selected MUX channel is latched off while the relevant input is low, Multisense pin delivers feedback according to OFF-State diagnostic.
Example 1: FR = 1; IN_0 = 0; OUT_0 = L (latched); MUX channel = channel 0 diagnostic; Mutisense = 0
Example 2: FR = 1; IN_0 = 0; OUT_0 = latched, $V_{OUT0} > V_{OL}$; MUX channel = channel 0 diagnostic; Mutisense = V_{SENSEH}

2.4 Waveforms

Figure 8. Latch functionality - behavior in hard short circuit condition (T_{AMB} << T_{TSD})



Figure 9. Latch functionality - behavior in hard short circuit condition

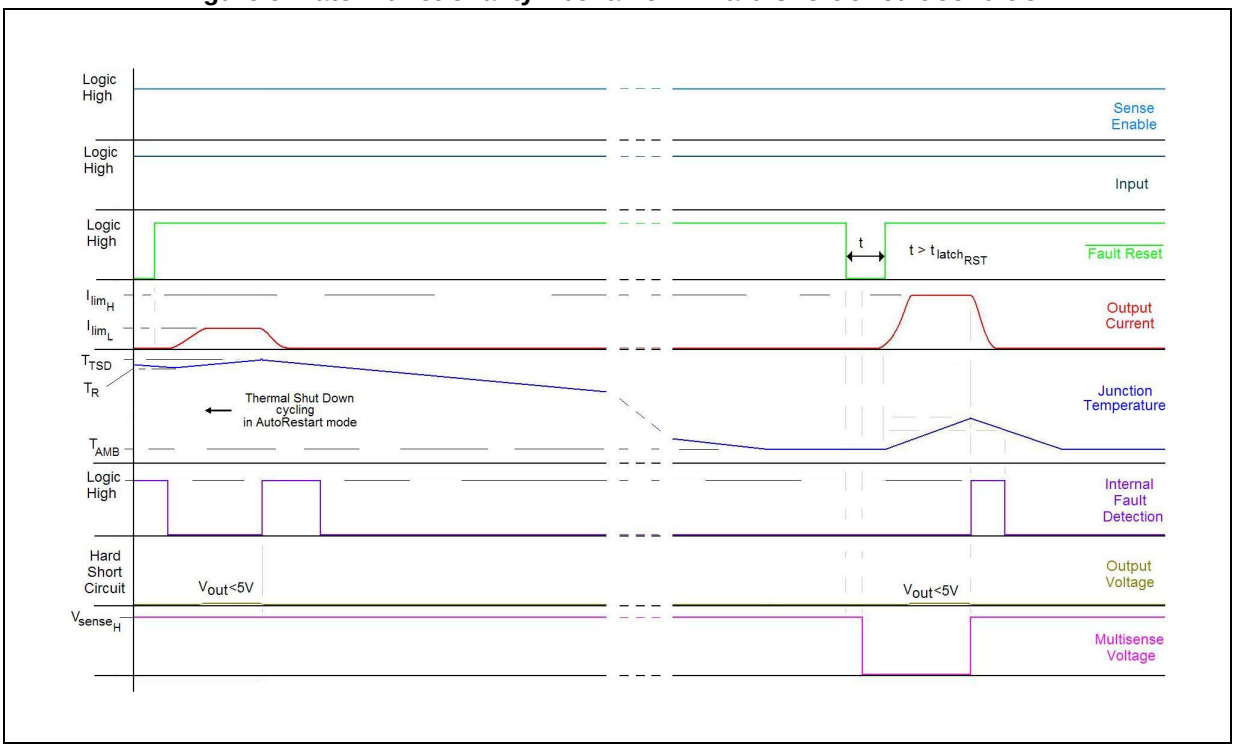


Figure 10. Latch functionality - behavior in hard short circuit condition (autorestart mode + latch off)

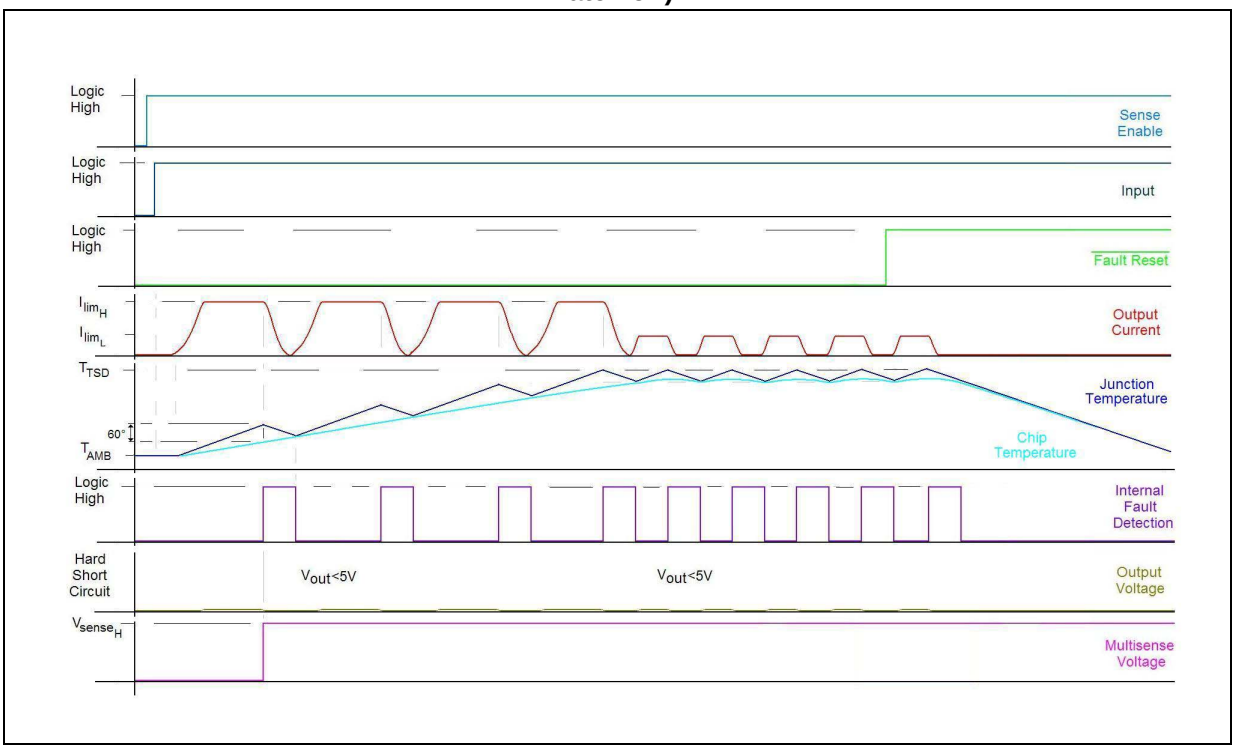


Figure 11. Standby mode activation

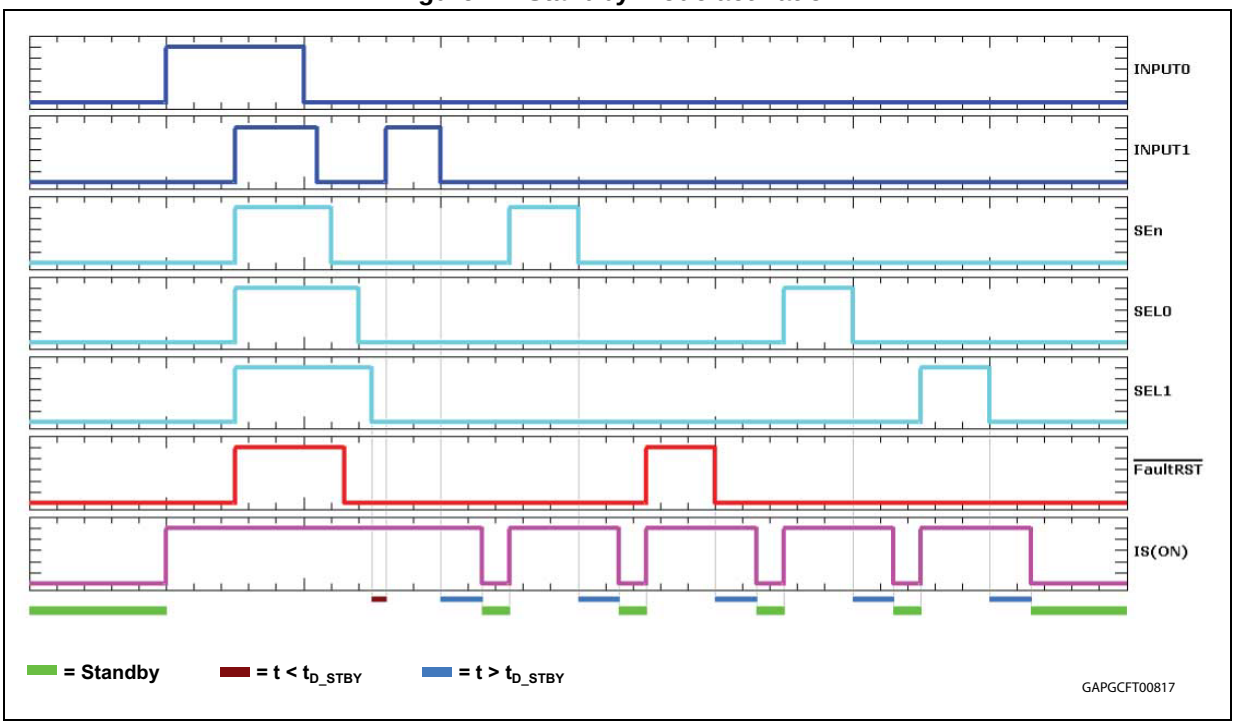
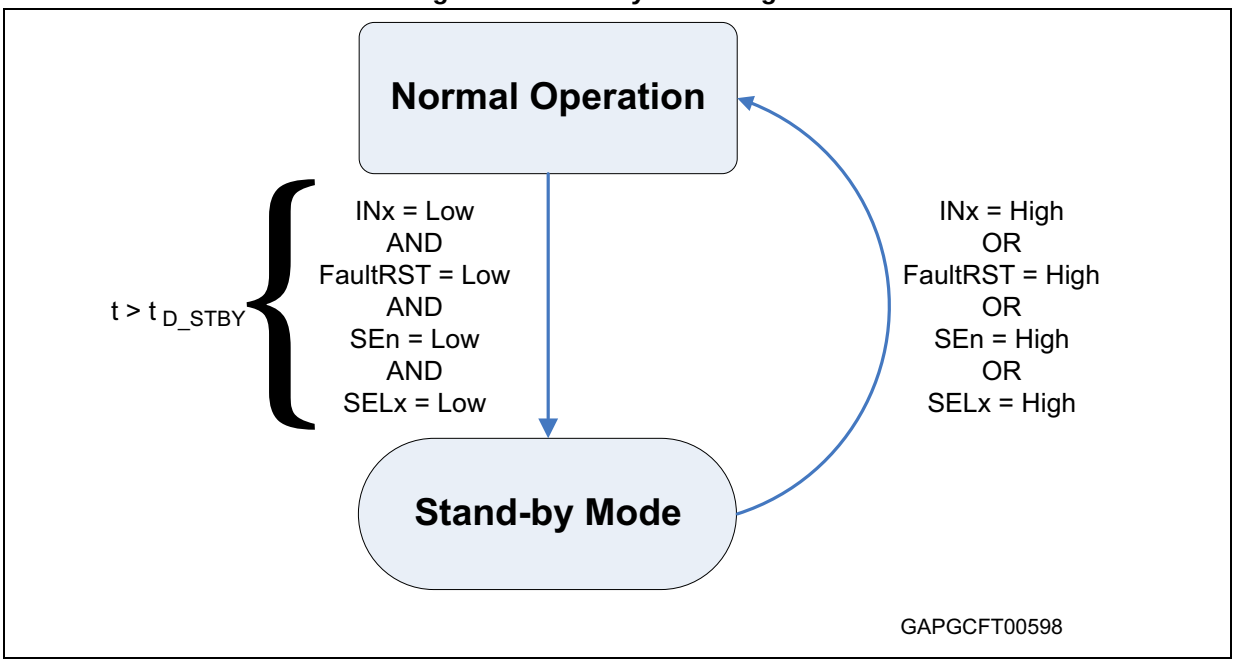


Figure 12. Standby state diagram



3 Protections

3.1 Power limitation

The basic working principle of this protection consists of an indirect measurement of the junction temperature swing ΔT_j through the direct measurement of the spatial temperature gradient on the device surface in order to automatically shut off the output MOSFET as soon as ΔT_j exceeds the safety level of ΔT_{j_SD}. According to the voltage level on the FaultRST pin, the output MOSFET switches on and cycles with a thermal hysteresis according to the maximum instantaneous power which can be handled (FaultRST = Low) or remains off (FaultRST = High). The protection prevents fast thermal transient effects and, consequently, reduces thermo-mechanical fatigue.

3.2 Thermal shutdown

In case the junction temperature of the device exceeds the maximum allowed threshold (typically 175°C), it automatically switches off and the diagnostic indication is triggered. According to the voltage level on the FaultRST pin, the device switches on again as soon as its junction temperature drops to T_R (see *Table 8*, FaultRST = Low) or remains off (FaultRST = High).

3.3 Current limitation

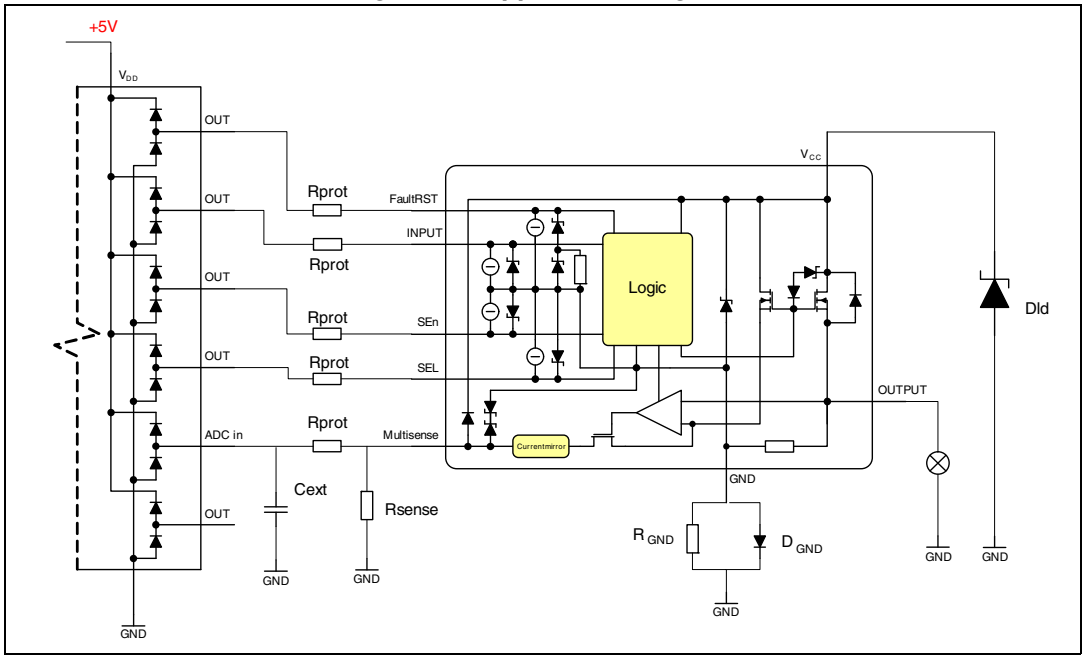
The device is equipped with an output current limiter in order to protect the silicon as well as the other components of the system (e.g. bonding wires, wiring harness, connectors, loads, etc.) from excessive current flow. Consequently, in case of short circuit, overload or during load power-up, the output current is clamped to a safety level, I_{LIMH}, by operating the output power MOSFET in the active region.

3.4 Negative voltage clamp

In case the device drives inductive load, the output voltage reaches negative value during turn off. A negative voltage clamp structure limits the maximum negative voltage to a certain value, V_{DEMAG} (see *Table 8*), allowing the inductor energy to be dissipated without damaging the device.

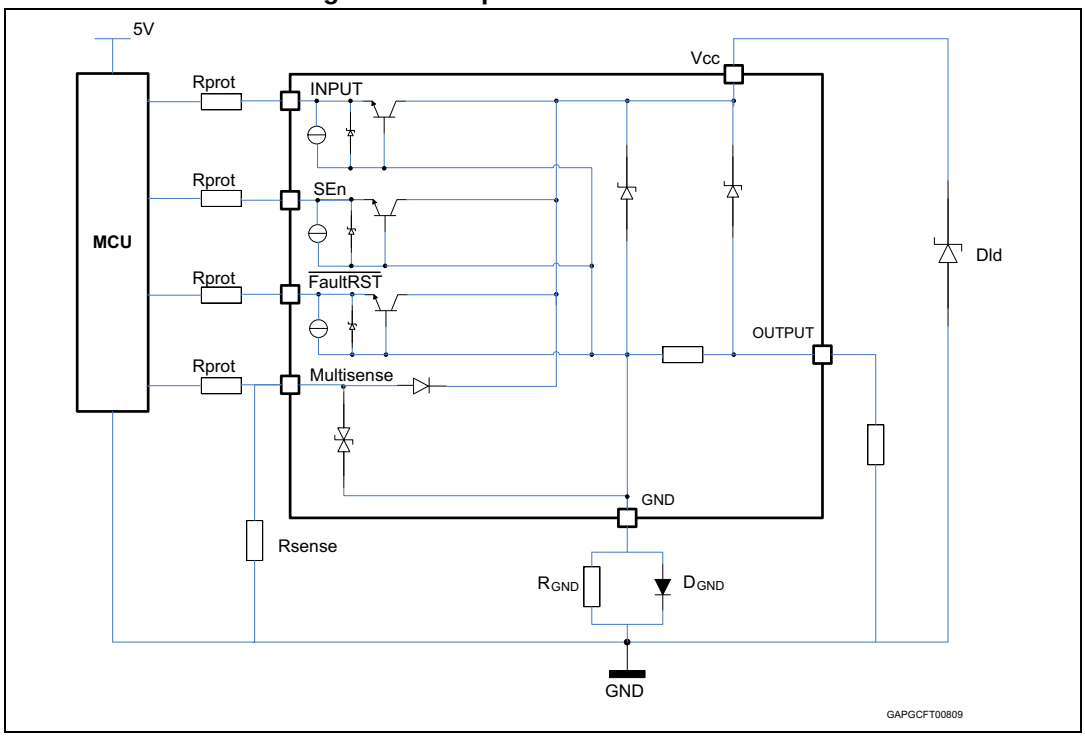
4 Application information

Figure 13. Application diagram



4.1 GND protection network against reverse battery

Figure 14. Simplified internal structure



4.1.1 Diode (D_{GND}) in the ground line

A resistor (typ. R_{GND} = 4.7 kΩ) should be inserted in parallel to D_{GND} if the device drives an inductive load.

This small signal diode can be safely shared amongst several different HSDs. Also in this case, the presence of the ground network produces a shift (≈600 mV) in the input threshold and in the status output values if the microprocessor ground is not common to the device ground. This shift does not vary if more than one HSD shares the same diode/resistor network.

4.2 Immunity against transient electrical disturbances

The immunity of the device against transient electrical emissions, conducted along the supply lines and injected into the V_{CC} pin, is tested in accordance with ISO7637-2:2011 (E) and ISO 16750-2:2010.

The related function performance status classification is shown in *Table 12*.

Test pulses are applied directly to DUT (Device Under Test) both in ON and OFF-state and in accordance to ISO 7637-2:2011(E), chapter 4. The DUT is intended as the present device only, without components and accessed through V_{CC} and GND terminals.

Status II is defined in ISO 7637-1 Function Performance Status Classification (FPSC) as follows: “The function does not perform as designed during the test but returns automatically to normal operation after the test”.

Table 12. ISO 7637-2 - electrical transient conduction along supply line

Test Pulse 2011(E)	Test pulse severity level with Status II functional performance status		Minimum number of pulses or test time	Burst cycle / pulse repetition time		Pulse duration and pulse generator internal impedance
	Level	U_S(1)		min	max	
1	III	-112V	500 pulses	0,5 s		2ms, 10Ω
2a	III	+55V	500 pulses	0,2 s	5 s	50µs, 2Ω
3a	IV	-220V	1h	90 ms	100 ms	0.1µs, 50Ω
3b	IV	+150V	1h	90 ms	100 ms	0.1µs, 50Ω
4(2)	IV	-7V	1 pulse			100ms, 0.01Ω
Load dump according to ISO 16750-2:2010						
Test B(3)		40V	5 pulse	1 min		400ms, 2Ω

1. U_S is the peak amplitude as defined for each test pulse in ISO 7637-2:2011(E), chapter 5.6.
2. Test pulse from ISO 7637-2:2004(E).
3. With 40 V external suppressor referred to ground (-40°C < T_j < 150°C).

4.3 MCU I/Os protection

If a ground protection network is used and negative transients are present on the V_{CC} line, the control pins will be pulled negative. ST suggests to insert a resistor (R_{prot}) in line both to prevent the microcontroller I/O pins to latch-up and to protect the HSD inputs.

The value of these resistors is a compromise between the leakage current of microcontroller and the current required by the HSD I/Os (Input levels compatibility) with the latch-up limit of microcontroller I/Os.

Equation 1

$V_{CCpeak}/I_{latchup} \leq R_{prot} \leq (V_{OH\mu C}-V_{IH}-V_{GND}) / I_{IHmax}$

Calculation example:

For V_{CCpeak} = -150 V; $I_{latchup} \geq$ 20mA; $V_{OH\mu C} \geq$ 4.5V

$$7.5\ k\Omega \leq R_{prot} \leq 140\ k\Omega.$$

Recommended values: R_{prot} = 15 kΩ

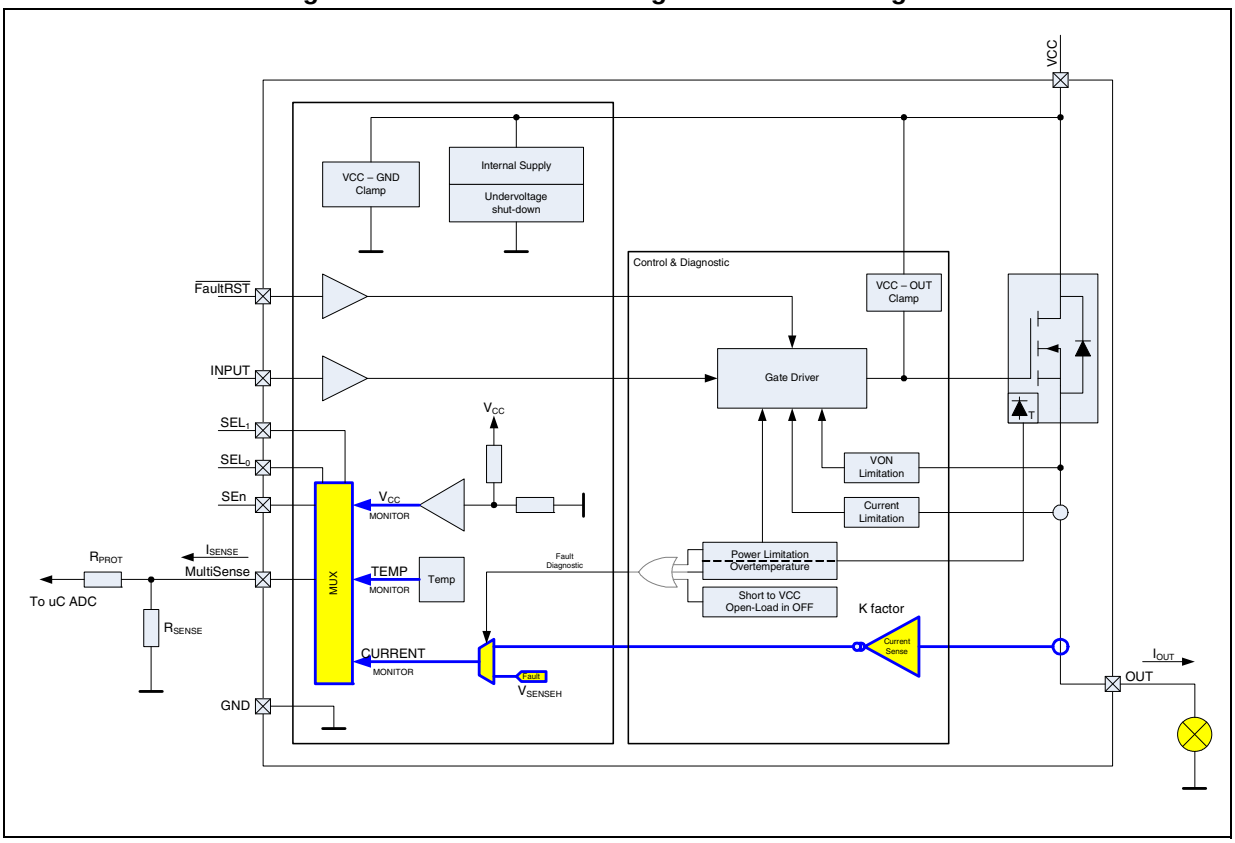
4.4 Multisense - analog current sense

Diagnostic information on device and load status are provided by an analog output pin (Multisense) delivering the following signals:

- Current monitor: current mirror of channel output current
- V_{CC} monitor: voltage propotional to V_{CC}
- T_{CASE}: voltage propotional to chip temperature

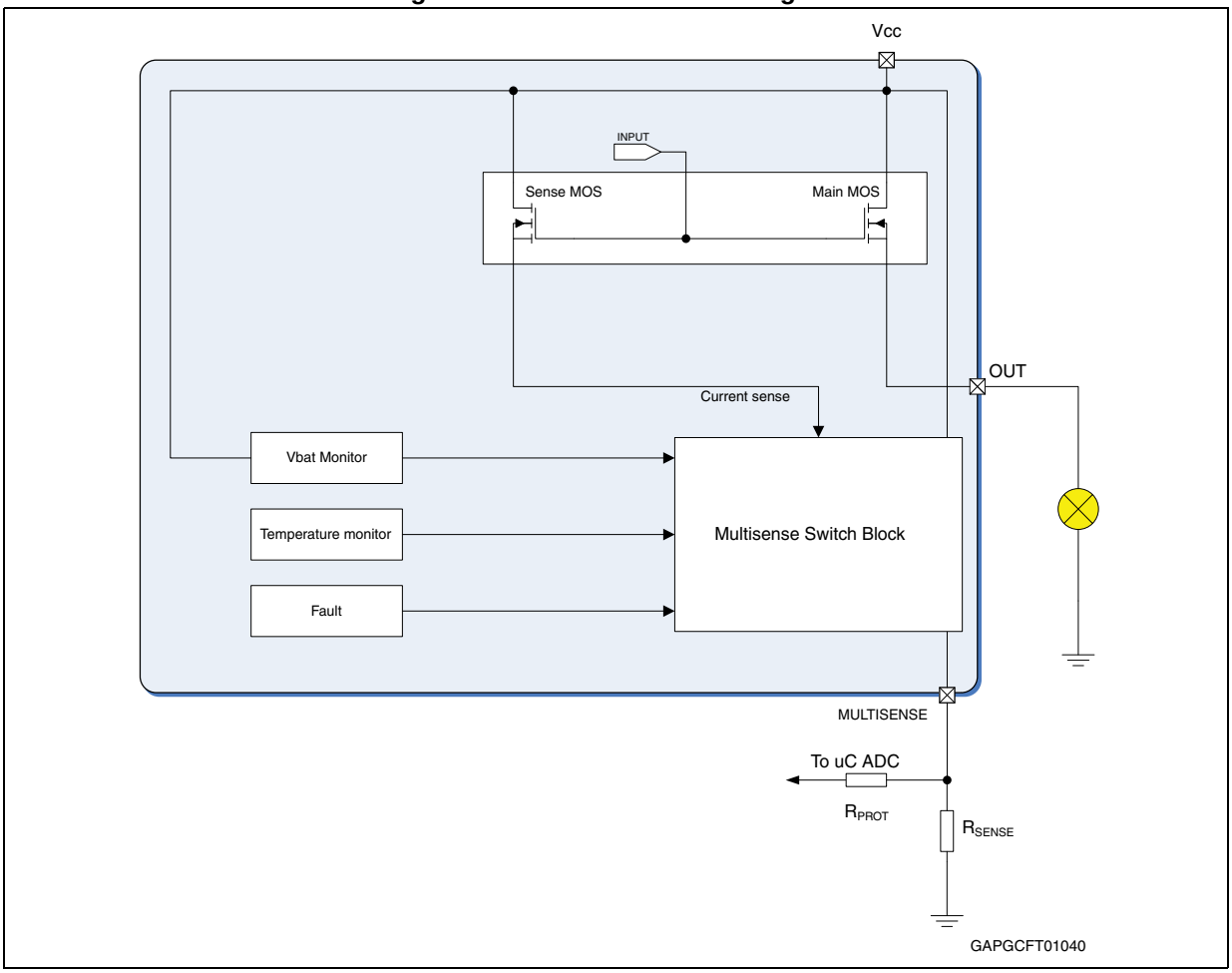
Those signals are routed through an analog multiplexer which is configured and controlled by means of SELx and SEn pins, according to the address map in *Table 11*.

Figure 15. Multisense and diagnostic – block diagram



4.4.1 Principle of Multisense signal generation

Figure 16. Multisense block diagram



Current monitor

When current mode is selected in the Multisense, this output is capable to provide:

- **Current mirror proportional to the load current in normal operation**, delivering current proportional to the load according to known ratio named **K**
- **Diagnostics flag in fault conditions** delivering fixed voltage V_{SENSEH}

The current delivered by the current sense circuit, I_{SENSE}, can be easily converted to a voltage V_{SENSE} by using an external sense resistor, R_{SENSE}, allowing continuous load monitoring and abnormal condition detection.

Normal operation (channel ON, no fault, SEn active)

While device is operating in normal conditions (no fault intervention), V_{SENSE} calculation can be done using simple equations

Current provided by Multisense output: $I_{SENSE} = I_{OUT}/K$

Voltage on R_{SENSE}: $V_{SENSE} = R_{SENSE} \cdot I_{SENSE} = R_{SENSE} \cdot I_{OUT}/K$

Where:

- V_{SENSE} is voltage measurable on R_{SENSE} resistor
- I_{SENSE} is current provided from MultiSense pin in current output mode
- I_{OUT} is current flowing through output
- K factor represent the ratio between PowerMOS cells and SenseMOS cells; its spread includes geometric factor spread, current sense amplifier offset and process parameters spread of overall circuitry specifying ratio between I_{OUT} and I_{SENSE}.

Failure flag indication

In case of power limitation/overtemperature, the fault is indicated by the Multisense pin which is switched to a “current limited” voltage source, V_{SENSEH} (see *Table 9*).

In any case, the current sourced by the Multisense in this condition is limited to I_{SENSEH} (see *Table 9*).

The typical behavior in case of overload or hard short circuit is shown in *Figure 8*, *Figure 9* and *Figure 10*.

Figure 17. Analogue HSD – open-load detection in off-state

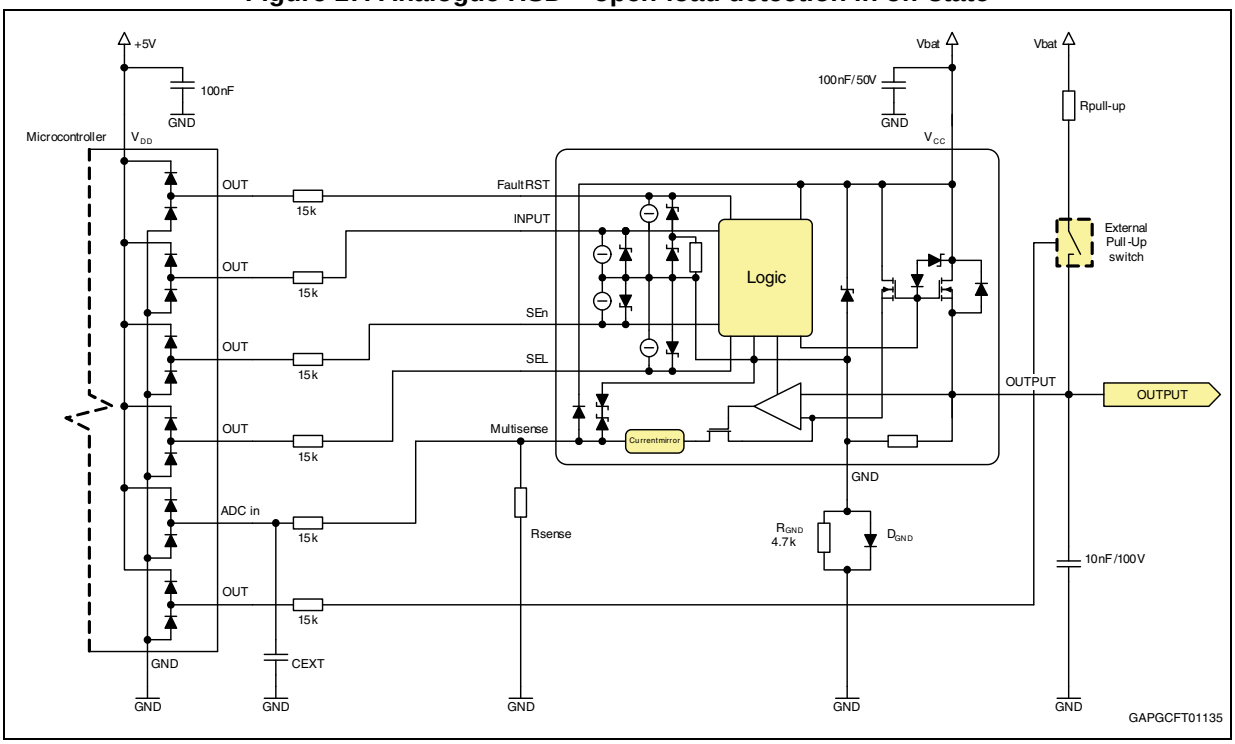


Figure 18. Open-load / short to V_{CC} condition

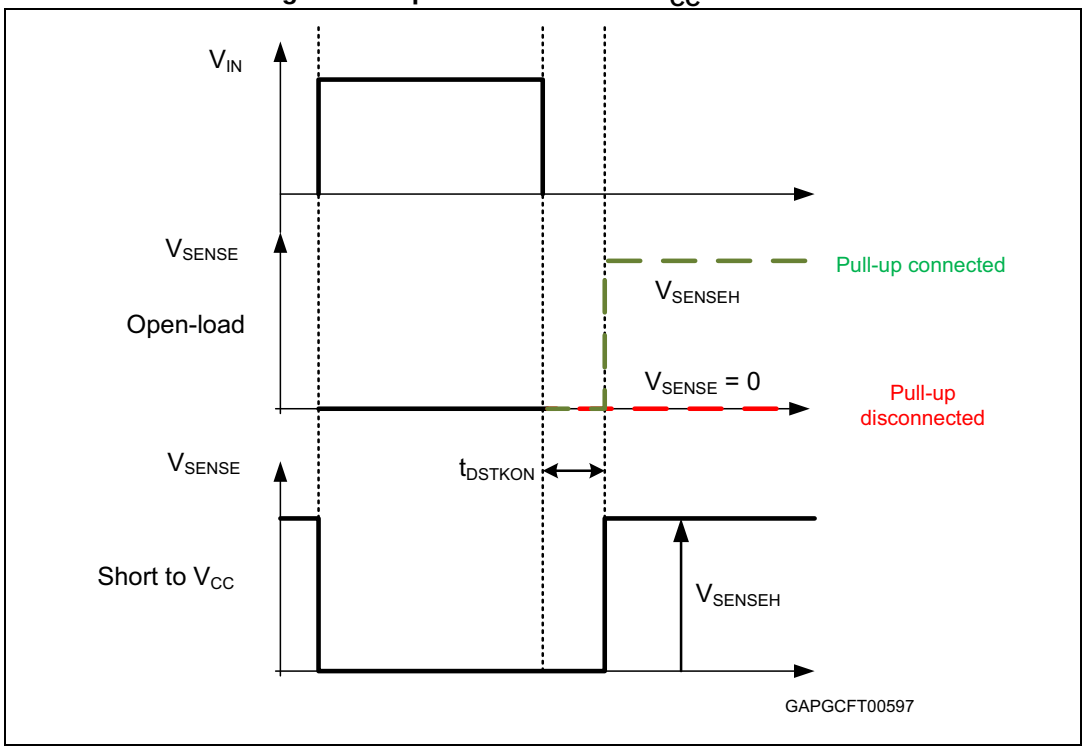


Table 13. Multisense pin levels in off-state

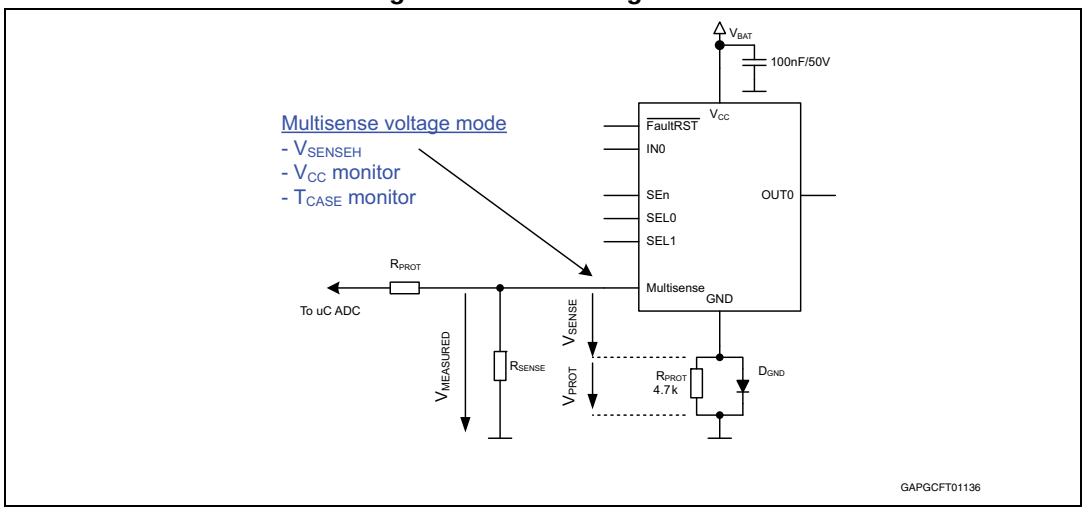
Condition	Output	Multisense	SEn
Open-load	$V_{OUT} > V_{OL}$	Hi-Z	L
		V_{SENSEH}	H
	$V_{OUT} < V_{OL}$	Hi-Z	L
		0	H
Short to V_{CC}	$V_{OUT} > V_{OL}$	Hi-Z	L
		V_{SENSEH}	H
Nominal	$V_{OUT} < V_{OL}$	Hi-Z	L
		0	H

4.4.2 T_{CASE} and V_{CC} monitor

In this case, MultiSense output operates in voltage mode and output level is referred to device GND. Care must be taken in case a GND network protection is used, because of a voltage shift is generated between device GND and the microcontroller input GND reference.

Figure 19 shows link between $V_{MEASURED}$ and real V_{SENSE} signal.

Figure 19. GND voltage shift



V_{CC} monitor

Battery monitoring channel provides $V_{SENSE} = V_{CC} / 4$.

Case temperature monitor

Case temperature monitor is capable to provide information about actual device temperature. Since diode is used for temperature sensing, following equation describe link between temperature and output V_{SENSE} level:

$V_{SENSE_TC}(T) = V_{SENSE_TC}(T_0) + dV_{SENSE_TC} / dT * (T - T_0)$

where dV_{SENSE_TC} / dT ~ typically -5.5 mV/K (for temperature range (-40°C to +150°C).

4.4.3 Short to V_{CC} and OFF-state open-load detection

Short to V_{CC}

A short circuit between V_{CC} and output is indicated by the relevant current sense pin set to V_{SENSEH} during the device off-state. Small or no current is delivered by the current sense during the on-state depending on the nature of the short circuit.

OFF-state open-load with external circuitry

Detection of an open-load in off mode requires an external pull-up resistor R_{PU} connecting the output to a positive supply voltage V_{PU}.

It is preferable V_{PU} to be switched off during the module standby mode in order to avoid the overall standby current consumption to increase in normal conditions, i.e. when load is connected.

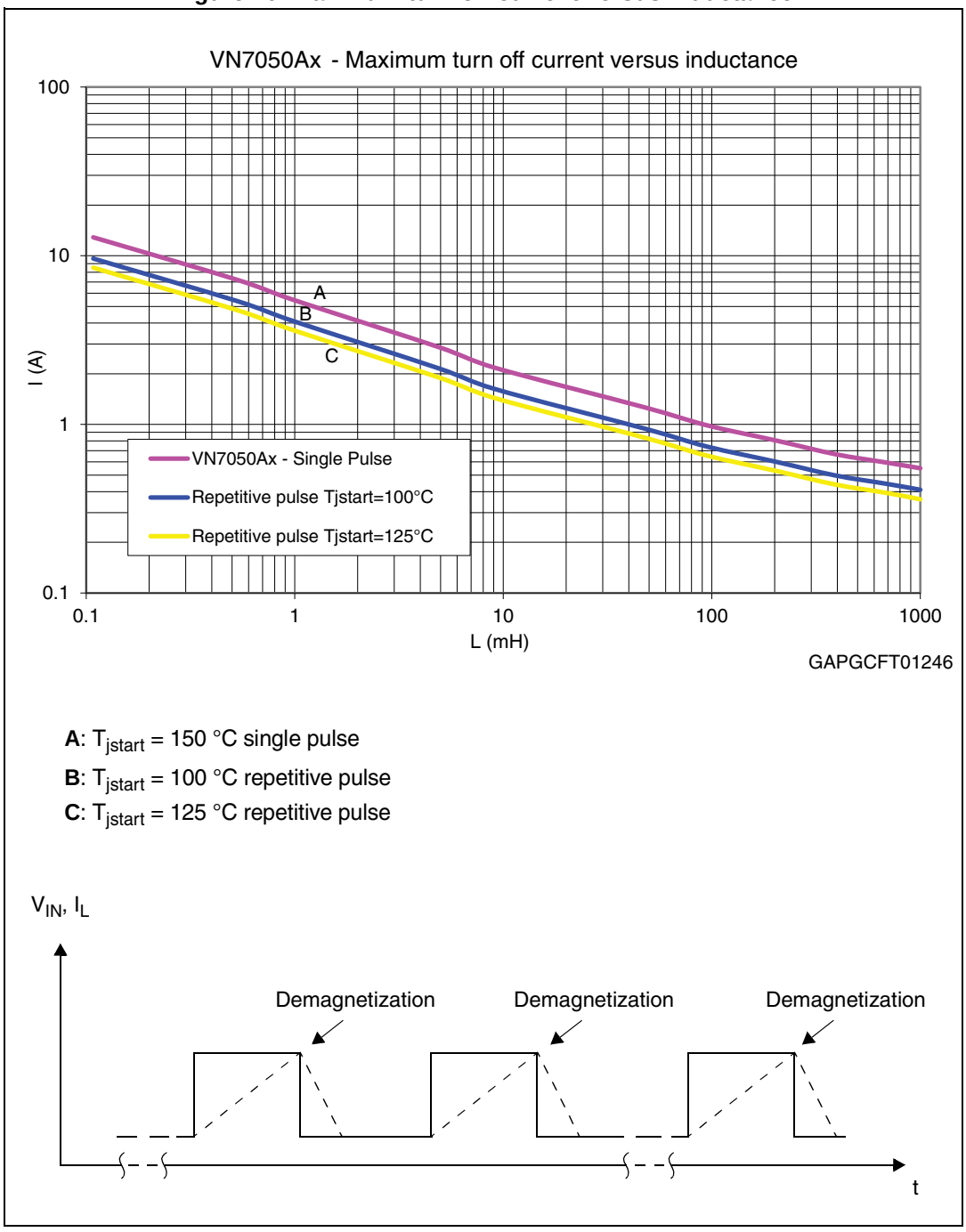
R_{PU} must be selected in order to ensure $V_{OUT} > V_{OLmax}$ in accordance with to following equation:

Equation 2

$$R_{PU} < \frac{V_{PU} - 4}{I_{L(off2)min\ @\ 4V}}$$

4.5 Maximum demagnetization energy (V_{CC} = 16 V)

Figure 20. Maximum turn off current versus inductance



1. Values are generated with R_L = 0 Ω.
In case of repetitive pulses, T_{jstart} (at the beginning of each demagnetization) of every pulse must not exceed the temperature specified above for curves A and B.

5 Package and PCB thermal data

5.1 PowerSSO-16 thermal data

Figure 21. PowerSSO-16 on two-layers PCB (2s0p to JEDEC JESD 51-5)

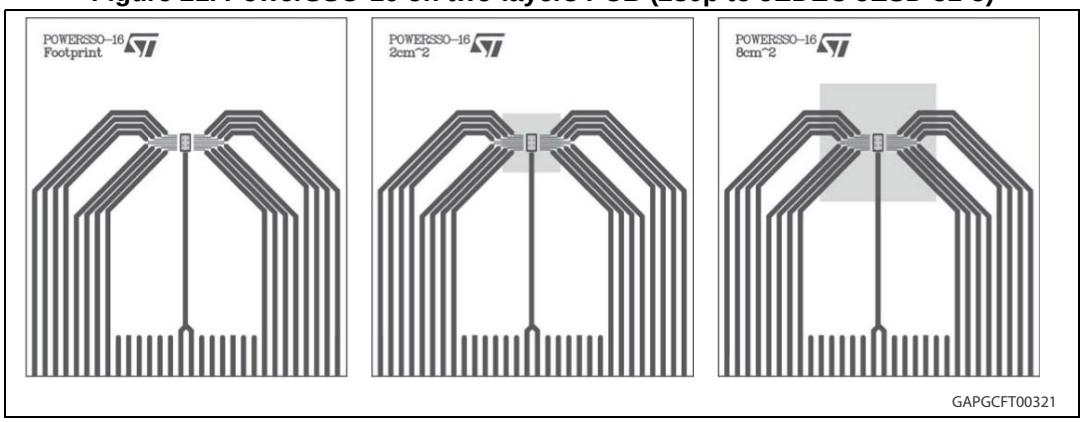


Figure 22. PowerSSO-16 on four-layers PCB (2s2p to JEDEC JESD 51-7)

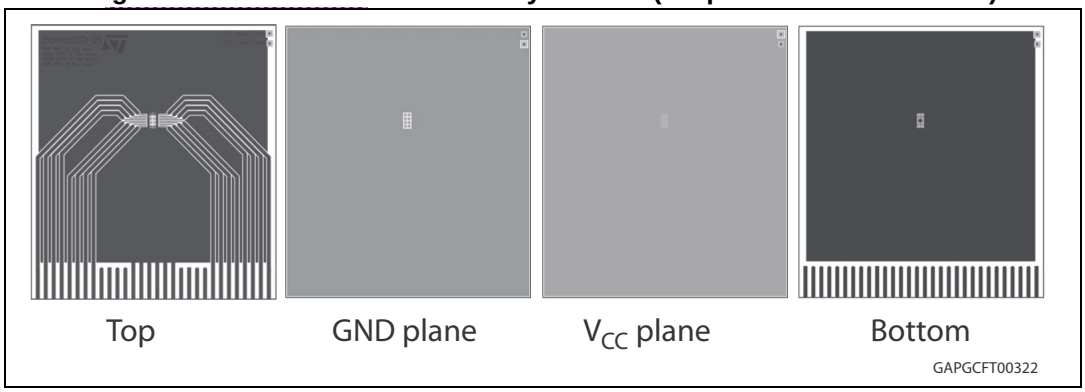


Table 14. PCB properties

Dimension	Value
Board finish thickness	1.6 mm +/- 10%
Board dimension	77 mm x 86 mm
Board Material	FR4
Copper thickness (top and bottom layers)	0.070 mm
Copper thickness (inner layers)	0.035 mm
Thermal vias separation	1.2 mm
Thermal via diameter	0.3 mm +/- 0.08 mm
Copper thickness on vias	0.025 mm
Footprint dimension (top layer)	2.2 mm x 3.9 mm
Heatsink copper area dimension (bottom layer)	Footprint, 2 cm^2 or 8 cm^2

Figure 23. PowerSSO-16 $R_{thj\text{-}amb}$ vs PCB copper area in open box free air conditions

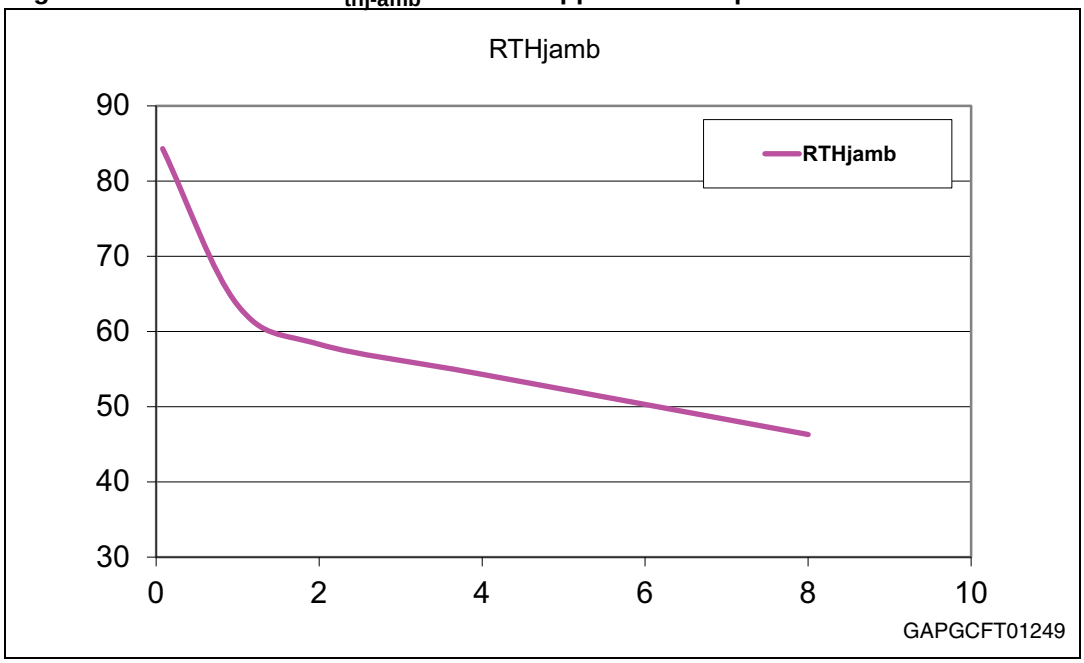
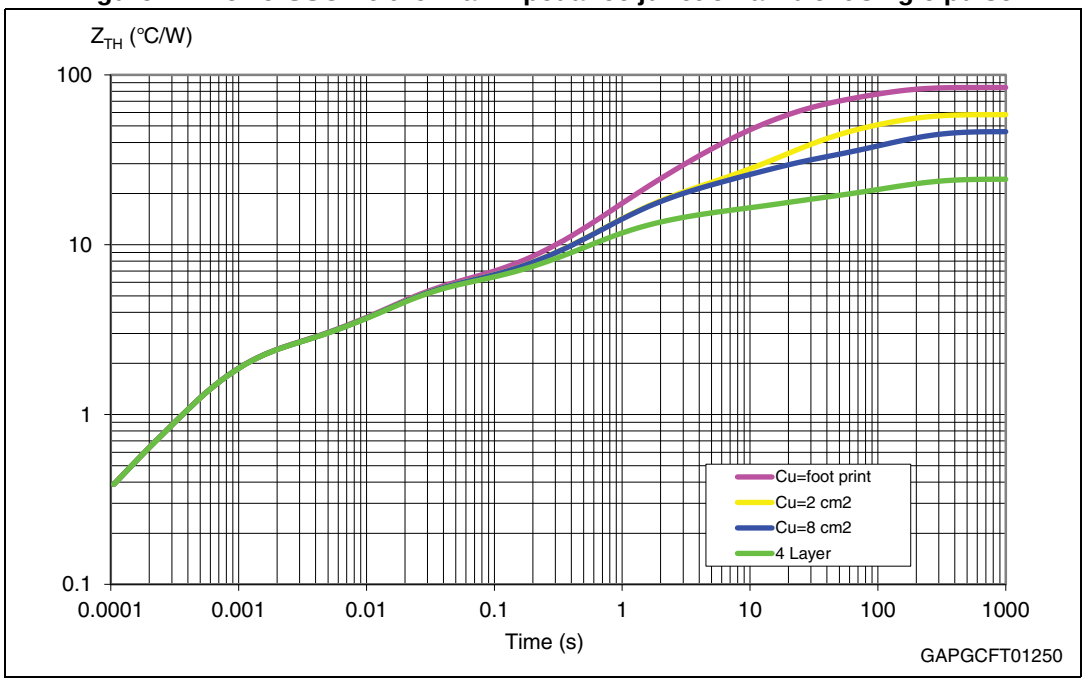


Figure 24. PowerSSO-16 thermal impedance junction ambient single pulse

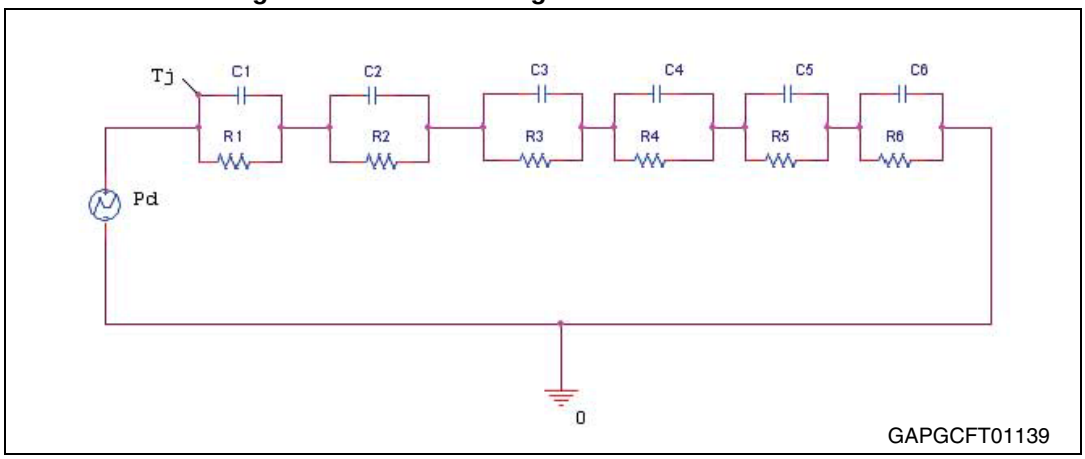


Equation 3: pulse calculation formula

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1 - \delta)$$

where $\delta = t_P/T$

Figure 25. Thermal fitting model for PowerSSO-16



1. The fitting model is a simplified thermal tool and is valid for transient evolutions where the embedded protections (power limitation or thermal cycling during thermal shutdown) are not triggered.

Table 15. Thermal parameters

Area/island (cm^2)	Footprint	2	8	4L
R1 (°C/W)	2.1			
R2 (°C/W)	3.2			
R3 (°C/W)	7	7	7	5
R4 (°C/W)	14	6	6	4
R5 (°C/W)	30	20	10	3
R6 (°C/W)	26	20	18	7
C1 (W.s/°C)	0.0003			
C2 (W.s/°C)	0.005			
C3 (W.s/°C)	0.1			
C4 (W.s/°C)	0.2	0.3	0.3	0.4
C5 (W.s/°C)	0.4	1	1	4
C6 (W.s/°C)	3	5	7	18

5.2 SO-8 thermal data

Figure 26. S0-8 on two-layers PCB (2s0p to JEDEC JESD 51-5)

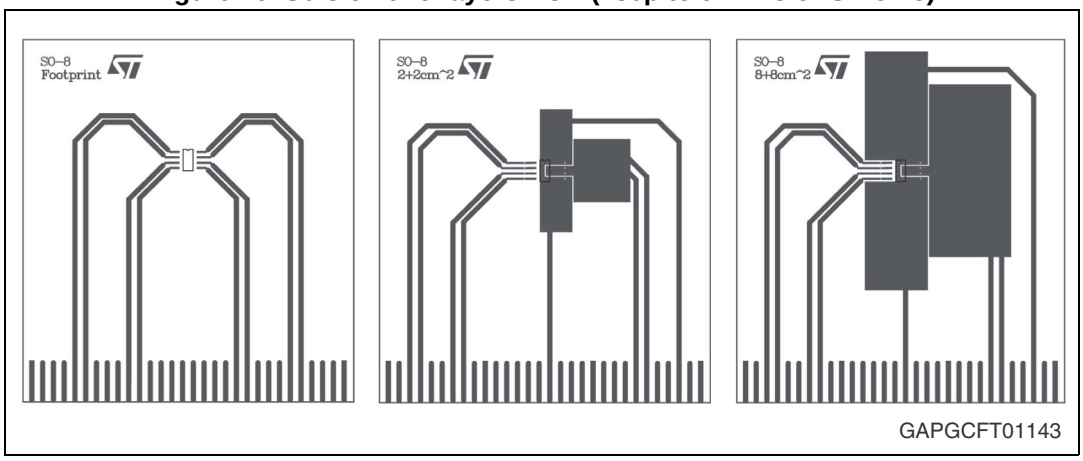


Figure 27. SO-8 on four-layers PCB (2s2p to JEDEC JESD 51-7)

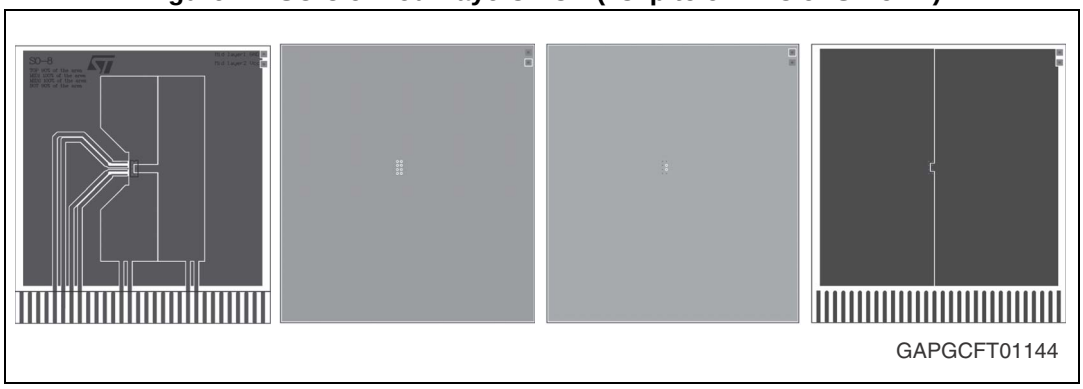


Table 16. PCB properties

Dimension	Value
Board finish thickness	1.6 mm +/- 10%
Board dimension	77 mm x 86 mm
Board Material	FR4
Copper thickness (top and bottom layers)	0.070 mm
Copper thickness (inner layers)	0.035 mm
Thermal vias separation	1.2 mm
Thermal via diameter	0.3 mm +/- 0.08 mm
Copper thickness on vias	0.025 mm
Heatsink copper area dimension (bottom layer)	Footprint, 2 + 2 cm^2 or 8 + 8 cm^2

Figure 28. SO-8 $R_{thj\text{-}amb}$ vs PCB copper area in open box free air conditions

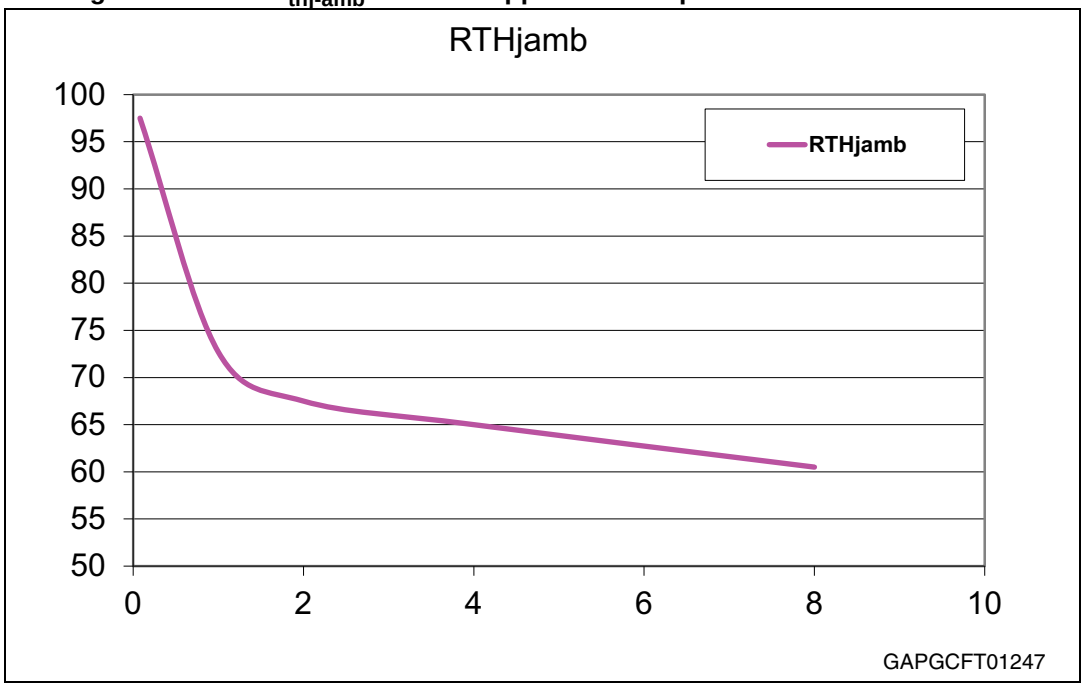
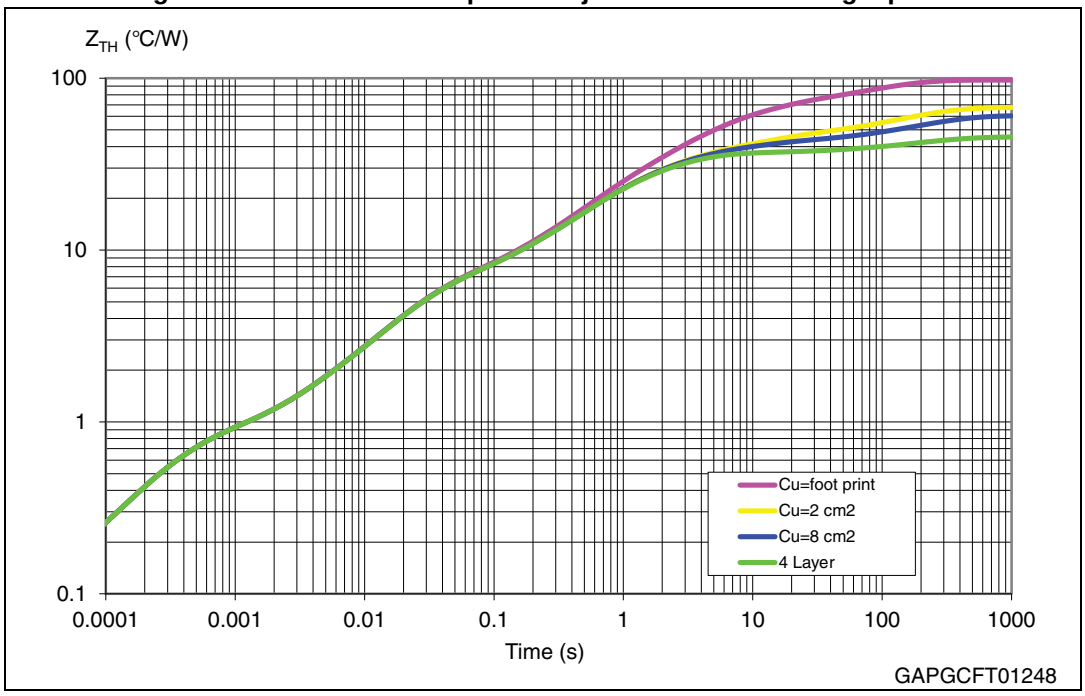


Figure 29. SO-8 thermal impedance junction ambient single pulse

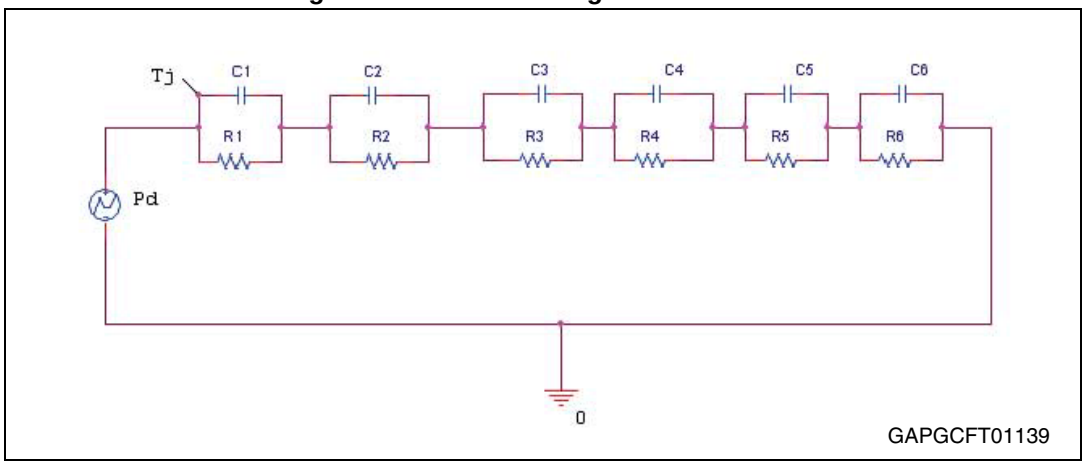


Equation 4: pulse calculation formula

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1 - \delta)$$

where $\delta = t_P/T$

Figure 30. Thermal fitting model for SO-8



1. The fitting model is a simplified thermal tool and is valid for transient evolutions where the embedded protections (power limitation or thermal cycling during thermal shutdown) are not triggered.

Table 17. Thermal parameters

Area/island (cm^2)	Footprint	2	8	4L
R1 (°C/W)	0.7			
R2 (°C/W)	4.8			
R3 (°C/W)	10			
R4 (°C/W)	28	17	17	17
R5 (°C/W)	24	12	9	4
R6 (°C/W)	30	23	19	9
C1 (W.s/°C)	0.0004			
C2 (W.s/°C)	0.0045			
C3 (W.s/°C)	0.05			
C4 (W.s/°C)	0.1			
C5 (W.s/°C)	0.4	0.8	0.8	0.8
C6 (W.s/°C)	3	7	11	22

6 Package information

6.1 ECOPACK®

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com.

ECOPACK® is an ST trademark.

6.2 PowerSSO-16 package information

Figure 31. PowerSSO-16 package dimensions

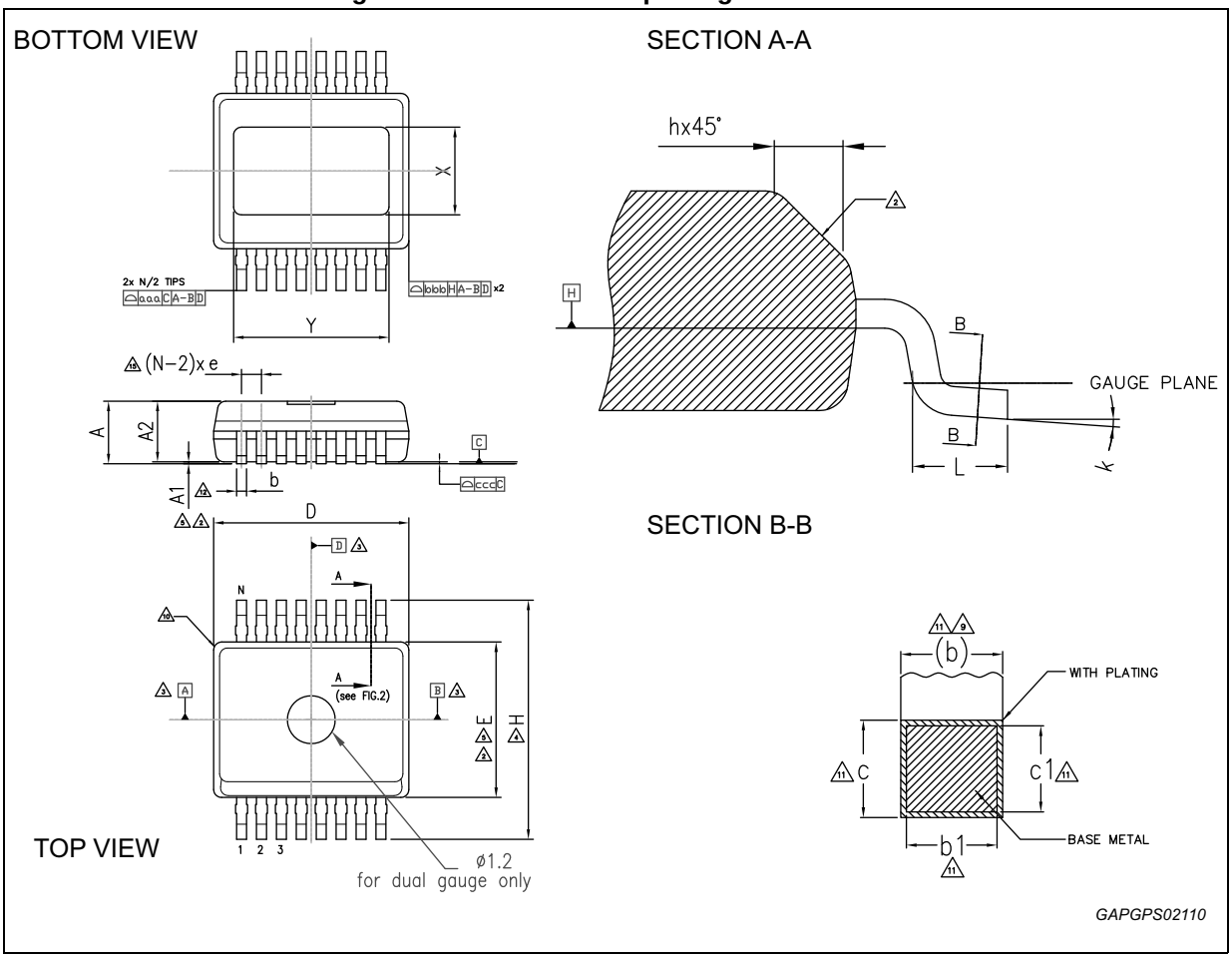


Table 18. PowerSSO-16 mechanical data

Symbol	Millimeters		
	Min.	Typ.	Max.
A	1.25		1.70
A1	0.00		0.10
A2	1.10		1.60
b	0.18		0.33
b1		0.25	
c	0.19		0.25
c1		0.20	
D	4.80		5.00
E	3.80		4.00
e		0.50	
H	5.80		6.20
h	0.25		0.50
L	0.40		1.27
k	0°		8°
X	2.2		2.8
Y	2.9		3.5
aaa	0.20		
bbb	0.20		
ccc	0.10		

Note: 1 Dimensions D does not include mold Flash protrusions or gate burrs.
Mold Flash protrusions or gate burrs shall not exceed 0.15mm in total (both side).

2 Drawings dimensions include Single and Matrix versions.

6.3 SO-8 package information

Figure 32. SO-8 package dimensions

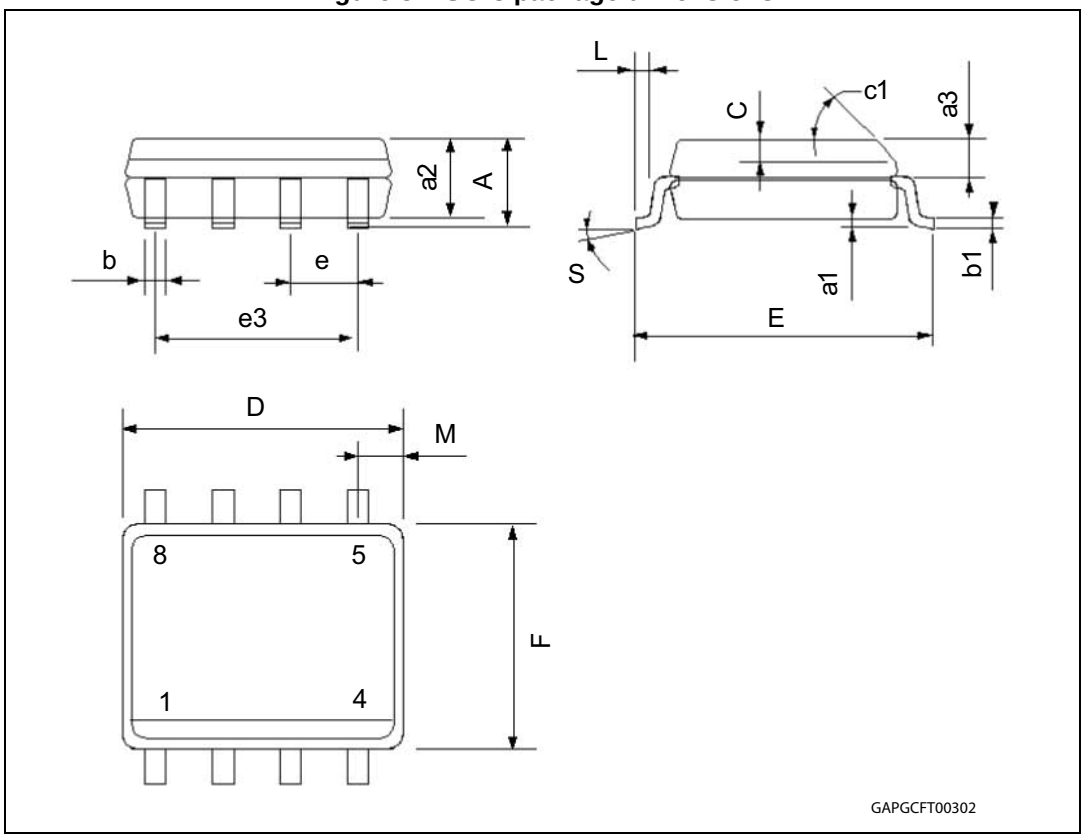
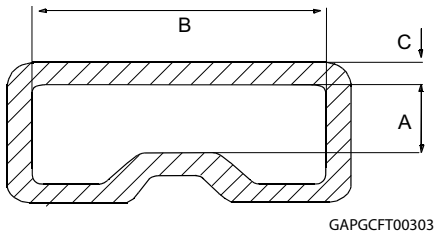


Table 19. SO-8 mechanical data

Dim.	mm.		
	Min.	Typ.	Max.
A			1.75
a1	0.1		0.25
a2			1.65
a3	0.65		0.85
b	0.35		0.48
b1	0.19		0.25
C	0.25		0.5
c1	45 (typ.)		
D	4.8		5
E	5.8		6.2
e		1.27	
e3		3.81	
F	3.8		4
L	0.4		1.27
M			0.6
S	8 (max.)		
L1	0.8		1.2

6.4 Packing information

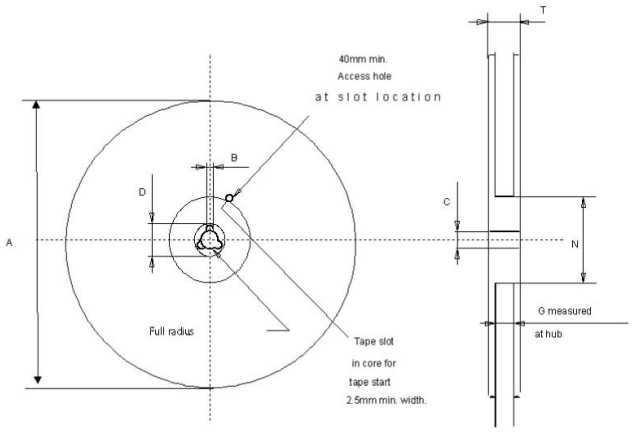
Figure 33. SO-8 tube shipment (no suffix)



Base q.ty	100
Bulk q.ty	2000
Tube length (± 0.5)	532
A	3.2
B	6
C (± 0.1)	0.6

All dimensions are in mm

Figure 34. SO-8 tape and reel shipment (suffix "TR")



REEL DIMENSIONS

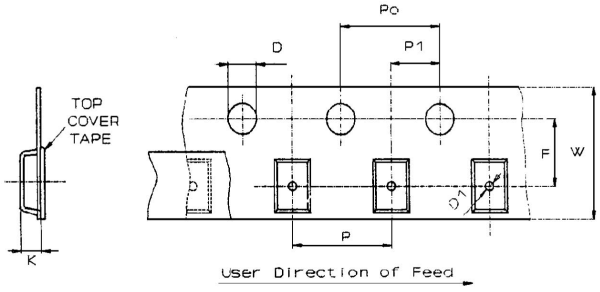
Baseq.ty	2500
Bulk q.ty	2500
A (max)	330
B (min)	1.5
C (± 0.2)	13
F	20.2
G (+ 2 / -0)	12.4
N (min)	60
T (max)	18.4

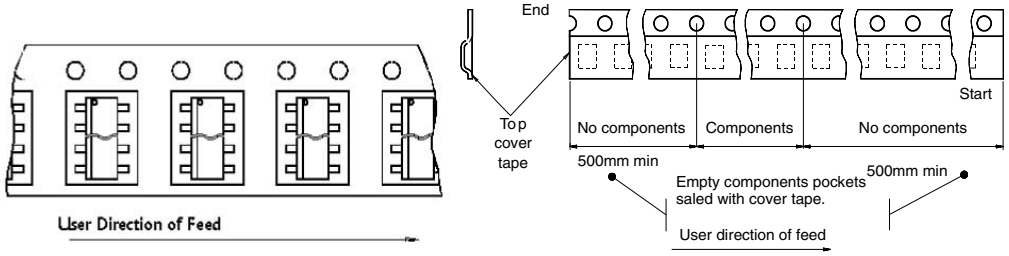
All dimensions are in mm.

TAPE DIMENSIONS
According to Electronic Industries Association (EIA) Standard 481 rev. A, Feb. 1986

Tape width	W	12
Tape hole spacing	P0 (± 0.1)	4
Component spacing	P	8
Hole diameter	D (+ 0.1/-0)	1.5
Hole diameter	D1 (min)	1.5
Hole position	F (± 0.05)	5.5
Compartment depth	K (max)	4.5
Hole spacing	P1 (± 0.1)	2

All dimensions are in mm.





GAPGCFT00304

7 Order codes

Table 20. Device summary

Package	Order codes	
	Tube	Tape and reel
PowerSSO-16	VN7050AJ-E	VN7050AJTR-E
SO-8	VN7050AS-E	VN7050ASTR-E

8 Revision history

Table 21. Document revision history

Date	Revision	Changes
25-Oct-2011	1	Initial release
12-Dec-2012	2	Updated *Features* list Updated *Table 1: Pin functions* and *Table :* *Table 3: Absolute maximum ratings*: – V_{CCPK}, I_{SENSE}, V_{ESD}: updated value – V_{CCJS}: added row – $-V_{SENSE}$: removed row *Table 5: Power section*: – $V_{USDReset}$, $I_{GND(ON)}$: added row – V_{clamp}: updated test conditions Updated *Table 6: Switching (VCC = 13 V; -40°C < Tj < 150°C, unless otherwise specified)* *Table 8: Protections (7 V < VCC < 18 V; -40°C < Tj < 150°C)*: – I_{LIMH}, T_R: added note – t_{LATCH_RST}: added note, updated typ and max values – V_{ON}: updated test conditions *Table 9: MultiSense (7 V < VCC < 18 V; -40°C < Tj < 150°C)*: – V_{SENSE_CL}: updated values; – K_{OL}, K_{LED}, K_0, K_1, K_2, K_3, I_{SENSE0}, $I_{L(off2)}$, V_{SENSE_TC}, V_{SENSE_VCC}, V_{SENSEH}, $t_{DSENSE1H}$: updated test conditions and values – dK_{LED}/K_{LED}, dK_0/K_0, dK_1/K_1, dK_2/K_2, dK_3/K_3, $t_{D_OL_V}$, I_{SENSEH}: updated values – V_{OUT_MSD}, V_{SENSE_SAT}, I_{SENSE_SAT}, I_{OUT_SAT}, $t_{D_OL_V}$: added rows – I_{SENSE0}, $I_{L(off2)}$, $t_{DSENSE1L}$, $t_{DSENSE2H}$, $\Delta t_{DSENSE2H}$, $t_{DSENSE2L}$, $t_{DSENSE3H}$, $t_{DSENSE3L}$, $t_{DSENSE4H}$, $t_{DSENSE4L}$, t_{D_CStoTC}, t_{D_TCtoCS}, $t_{D_CStoVCC}$, $t_{D_VCCtoCS}$, $t_{D_TCtoVCC}$, $t_{D_VCCtoTC}$: updated test conditions – $t_{D_CStoVSENSEH}$: removed row Updated *Figure 4: Switching times and Pulse skew* and *Figure 6: Multisense timings (chip temperature and VCC sense mode)(VN7050AJ-E only)* Removed *Figure: Pulse skew* Added *Figure 7: TDSTKON* *Table 10: Truth table*: – Updated overload conditions *Table 11: MultiSense multiplexer addressing*: – Added note – Updated Negative output values Updated *Section 2.4: Waveforms* Added *Chapter 3: Protections* and *Chapter 4: Application information* *Table 18: PowerSSO-16 mechanical data*: – X, Y: updated values

Table 21. Document revision history (continued)

Date	Revision	Changes
16-Apr-2013	3	*Table 3: Absolute maximum ratings*: – V_{CCPK}: updated parameter – E_{MAX}: updated parameter and value Updated *Table 4: Thermal data* *Table 6: Switching (VCC = 13 V; -40°C < Tj < 150°C, unless otherwise specified)*: – W_{ON}, W_{OFF}: updated values *Table 9: MultiSense (7 V < VCC < 18 V; -40°C < Tj < 150°C)*: – dK_{cal}/K_{cal}: added row – K_{OL}, K_{LED}, K_0, K_1, K_2, K_3, V_{SENSE_H}: updated values – t_{DSTKON}: updated parameter Removed following tables: *Table: Electrical transient requirements (part 1/3)* *Table: Electrical transient requirements (part 2/3)* *Table: Electrical transient requirements (part 3/3)* Updated *Section 4.1.1: Diode (DGND) in the ground line* Removed *Section: Load dump protection* Added *Section 4.2: Immunity against transient electrical disturbances* Updated *Figure 17: Analogue HSD – open-load detection in off-state* and *Figure 19: GND voltage shift* Updated *Table 13: Multisense pin levels in off-state* Added *Section 4.5: Maximum demagnetization energy (VCC = 16 V)* Updated *Table 14: PCB properties* Updated *Chapter 5: Package and PCB thermal data* and *Chapter 6: Package information*
27-May-2013	4	*Table 3: Absolute maximum ratings*: – $-I_{OUT}$: updated value *Table 6: Switching (VCC = 13 V; -40°C < Tj < 150°C, unless otherwise specified)*: – $t_{d(on)}$, W_{ON}, t_{SKEW}: updated values *Table 9: MultiSense (7 V < VCC < 18 V; -40°C < Tj < 150°C)*: – K_1, K_3: updated values

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