VN7007AH

High-side driver with CurrentSense analog feedback for automotive applications

Datasheet - production data



Features

Max transient supply voltage	V_{CC}	40 V
Operating voltage range	V_{CC}	4 to 28 V
Typ. on-state resistance (per Ch)	R_{ON}	7 mΩ
Current limitation (typ)	I_{LIMH}	100 A
Stand-by current (max)	I_{STBY}	0.5 µA

- Automotive qualified
- General
  - Single channel smart high-side driver with CurrentSense analog feedback
  - Very low standby current
  - Compatible with 3.0 V and 5 V CMOS outputs
- Diagnostic functions
  - Overload and short to ground (power limitation) indication
  - Thermal shutdown indication
  - OFF-state open-load detection
  - Output short to V_{CC} detection
  - Sense enable/ disable
- Protections
  - Undervoltage shutdown
  - Overvoltage clamp
  - Load current limitation
  - Self limiting of fast thermal transients
  - Loss of ground and loss of V_{CC}
  - Reverse battery
  - Electrostatic discharge protection

Applications

- All types of Automotive resistive, inductive and capacitive loads
- Specially intended for Automotive Headlamps

Description

The device is a single channel high-side driver manufactured using ST proprietary VIPower® technology and housed in the Octapak package. The device is designed to drive 12 V automotive grounded loads through a 3 V and 5 V CMOS-compatible interface, providing protection and diagnostics.

The device integrates advanced protective functions such as load current limitation, overload active management by power limitation and overtemperature shutdown.

A sense enable pin allows OFF-state diagnosis to be disabled during the module low-power mode as well as external sense resistor sharing among similar devices.

Table 1: Device summary

Package	Order codes
	Tape and reel
Octapak	VN7007AHTR

This is information on a product in full production.

www.st.com

Contents

1 Block diagram and pin description 5

2 Electrical specification 7

2.1 Absolute maximum ratings 7

2.2 Thermal data 8

2.3 Electrical characteristics 8

2.4 Electrical characteristics curves 15

3 Protections 19

3.1 Power limitation 19

3.2 Thermal shutdown 19

3.3 Current limitation 19

3.4 Negative voltage clamp 19

4 Application information 20

4.1 Protection against reverse battery 20

4.2 Immunity against transient electrical disturbances 21

4.3 MCU I/Os protection 21

4.4 CS - analog current sense 22

4.4.1 Principle of CurrentSense signal generation 23

4.4.2 Short to VCC and OFF-state open-load detection 25

5 Maximum demagnetization energy (Vcc = 16 V) 27

6 Package and PCB thermal data 28

6.1 Octapak thermal data 28

7 Package information 31

7.1 Octapak package information 31

7.2 Octapak packing information 33

7.3 Octapak marking information 35

8 Revision history 36

List of tables

Table 1: Device summary 1
Table 2: Pin functions 5
Table 3: Suggested connections for unused and not connected pins 6
Table 4: Absolute maximum ratings 7
Table 5: Thermal data 8
Table 6: Power section 8
Table 7: Switching 9
Table 8: Logic inputs 10
Table 9: Protection 10
Table 10: CurrentSense 11
Table 11: Truth table 15
Table 12: ISO 7637-2 - electrical transient conduction along supply line 21
Table 13: CurrentSense pin levels in off-state 25
Table 14: PCB properties 28
Table 15: Thermal parameters 30
Table 16: Octapak mechanical data 32
Table 17: Reel dimensions 33
Table 18: Document revision history 36

List of figures

Figure 1: Block diagram 5
Figure 2: Configuration diagram (top view) 6
Figure 3: Current and voltage conventions 7
Figure 4: IOUT/ISENSE versus IOUT 13
Figure 5: Current sense precision vs. IOUT 13
Figure 6: Switching times and Pulse skew 14
Figure 7: tDSTKON 14
Figure 8: OFF-state output current 15
Figure 9: Standby current 15
Figure 10: IGND(ON) vs Tcase 16
Figure 11: Logic Input high level voltage 16
Figure 12: Logic Input low level voltage 16
Figure 13: High level logic input current 16
Figure 14: Low level logic input current 16
Figure 15: Logic Input hysteresis voltage 16
Figure 16: Undervoltage shutdown 17
Figure 17: On-state resistance vs Tcase 17
Figure 18: On-state resistance vs VCC 17
Figure 19: Turn-on voltage slope 17
Figure 20: Turn-off voltage slope 17
Figure 21: Won vs Tcase 17
Figure 22: Woff vs Tcase 18
Figure 23: ILIMH vs. Tcase 18
Figure 24: Turn-off output voltage clamp 18
Figure 25: OFF-state open-load voltage detection threshold 18
Figure 26: Vsense clamp vs. Tcase 18
Figure 27: Vsenseh vs. Tcase 18
Figure 28: Application diagram 20
Figure 29: Simplified internal structure 20
Figure 30: CurrentSense and diagnostic – block diagram 22
Figure 31: CurrentSense block diagram 23
Figure 32: Analogue HSD – open-load detection in off-state 24
Figure 33: Open-load / short to VCC condition 25
Figure 34: Maximum turn off current versus inductance 27
Figure 35: Octapak on two-layers PCB (2s0p to JEDEC JESD 51-5) 28
Figure 36: Octapak on four-layers PCB (2s2p to JEDEC JESD 51-7) 28
Figure 37: Rthj-amb vs PCB copper area in open box free air conditions 29
Figure 38: Octapak thermal impedance junction ambient single pulse 29
Figure 39: Thermal fitting model for Octapak 30
Figure 40: Octapak package dimensions 31
Figure 41: Octapack reel 13" 33
Figure 42: Octapak carrier tape 34
Figure 43: Octapak schematic drawing of leader and trailer tape 34
Figure 44: Octapak marking information 35

1 Block diagram and pin description

Figure 1: Block diagram

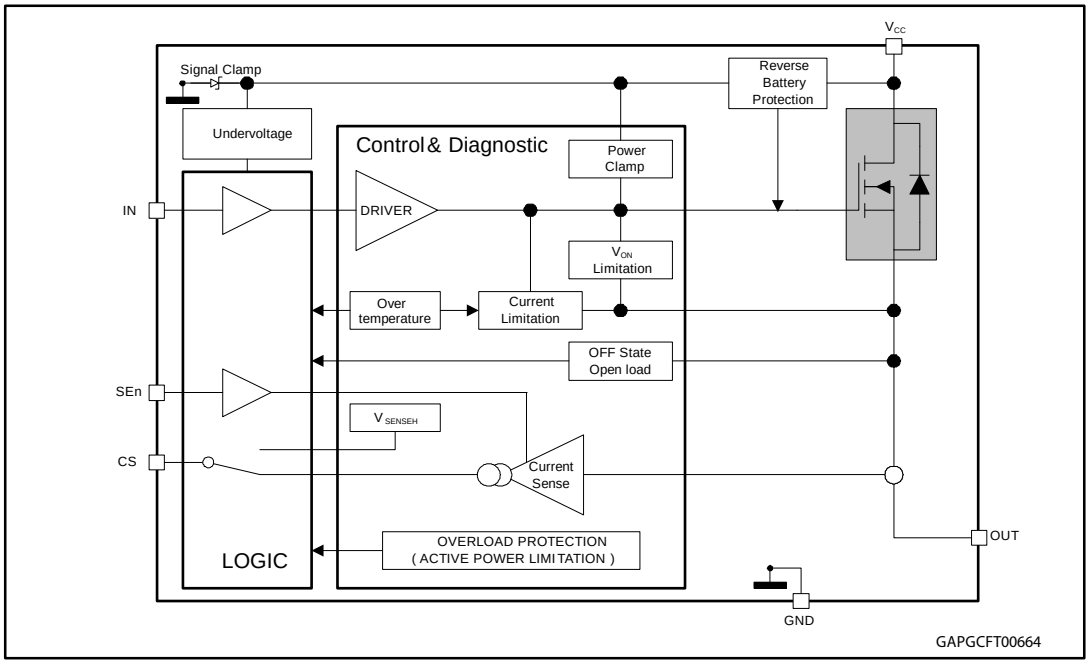


Table 2: Pin functions

Name	Function
V_{CC}	Battery connection.
OUTPUT	Power outputs. All the pins must be connected together.
GND	Ground connection.
INPUT	Voltage controlled input pin with hysteresis. Compatible with 3 V and 5 V CMOS outputs. It controls output switch state.
CS	Analog current sense output pin delivers a current proportional to the load current.
SEn	Active high compatible with 3 V and 5 V CMOS outputs pin; it enables the CurrentSense diagnostic pin.

Figure 2: Configuration diagram (top view)

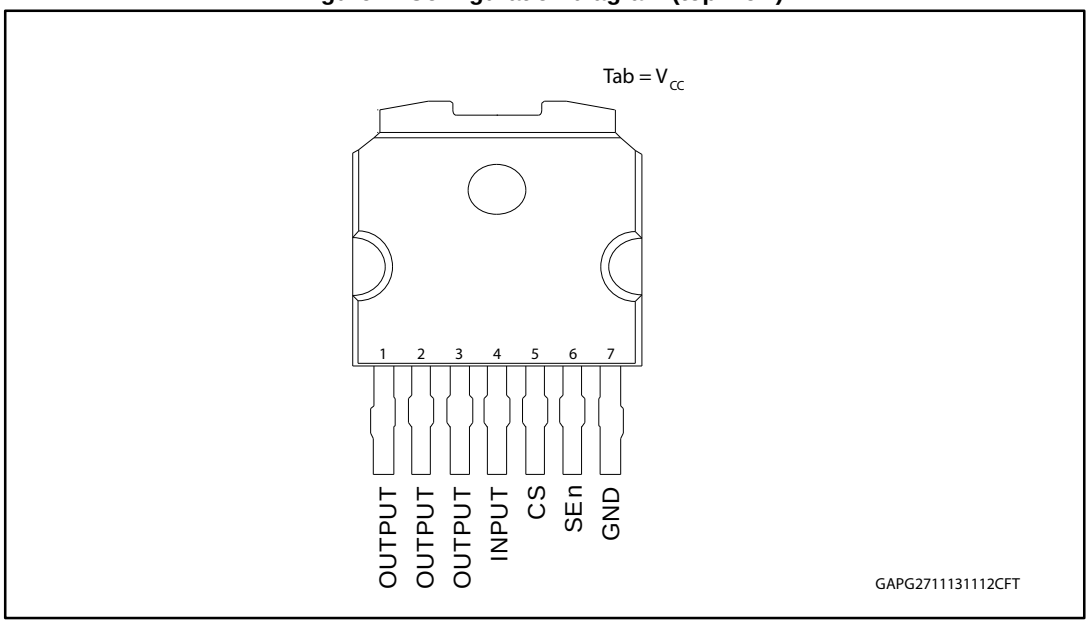


Table 3: Suggested connections for unused and not connected pins

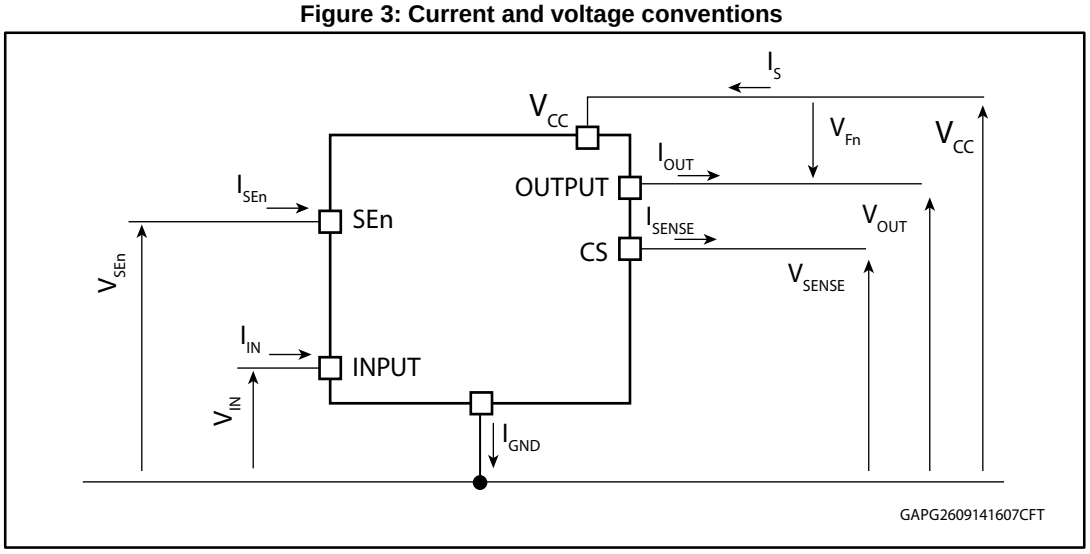
Connection / pin	CurrentSense	N.C.	Output	Input	SEn
Floating	Not allowed	X (1)	X	X	X
To ground	Through 1 kΩ resistor	X	Not allowed	Through 15 kΩ resistor	Through 15 kΩ resistor

Notes:

(1)X: do not care.

2 Electrical specification

Figure 3: Current and voltage conventions



$V_F = V_{OUT} - V_{CC}$ when $V_{OUT} > V_{CC}$ and INPUT = LOW

2.1 Absolute maximum ratings

Stressing the device above the rating listed in *Table 4: "Absolute maximum ratings"* may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to the conditions in table below for extended periods may affect device reliability.

Table 4: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	DC supply voltage	38	V
$-V_{CC}$	Reverse DC supply voltage	16	
V_{CCPK}	Maximum transient supply voltage (ISO7637-2:2004 Pulse 5b level IV clamped to 40 V; R_L = 4Ω)	40	
V_{CCJS}	Maximum jump start voltage for single pulse short circuit protection	28	
$-I_{GND}$	DC reverse ground pin current	200	mA
I_{OUT}	OUTPUT DC output current	Internally limited	A
$-I_{OUT}$	Reverse DC output current	30	
I_{IN}	INPUT DC input current	-1 to 10	mA
I_{SEn}	SEn DC input current		
I_{SENSE}	CS pin DC output current (V_{GND} = V_{CC} and V_{SENSE} < 0 V)	10	mA
	CS pin DC output current in reverse (V_{CC} < 0 V)	-20	

Symbol	Parameter	Value	Unit
E_{MAX}	Maximum switching energy (single pulse) T_{DEMAG} = 0.4 ms; T_{jstart} = 150°C	170	mJ
V_{ESD}	Electrostatic discharge (JEDEC 22A-114F) • INPUT • CurrentSense • SEn • OUTPUT • V_{CC}	 4000 2000 4000 4000 4000	 V V V V V
V_{ESD}	Charge device model (CDM-AEC-Q100-011)	750	V
T_j	Junction operating temperature	-40 to 150	°C
T_{stg}	Storage temperature	-55 to 150	

2.2 Thermal data

Table 5: Thermal data

Symbol	Parameter	Typ. value	Unit
$R_{thj\text{-}board}$	Thermal resistance junction-board (JEDEC JESD 51-8) (1)	2.8	°C/W
$R_{thj\text{-}amb}$	Thermal resistance junction-ambient (JEDEC JESD 51-2) (2)	58.3	
$R_{thj\text{-}amb}$	Thermal resistance junction-ambient (JEDEC JESD 51-2) (1)	15.8	

Notes:

(1)Device mounted on four-layers 2s2p PCB

(2)Device mounted on two-layers 2s0p PCB with 2 cm^2 heatsink copper trace

2.3 Electrical characteristics

7 V < V_{CC} < 28 V; -40°C < T_j < 150°C, unless otherwise specified.

All typical values refer to V_{CC} = 13 V; T_j = 25 °C, unless otherwise specified.

Table 6: Power section

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{CC}	Operating supply voltage		4	13	28	V
V_{USD}	Undervoltage shutdown				4	
$V_{USDReset}$	Undervoltage shutdown reset				5	
$V_{USDhyst}$	Undervoltage shutdown hysteresis			0.3		
R_{ON}	On-state resistance	I_{OUT} = 6 A; T_j = 25 °C		7		mΩ
		I_{OUT} = 6 A; T_j = 150 °C			14.3	
		I_{OUT} = 6 A; V_{CC} = 4 V; T_j = 25 °C			10.5	
R_{ON_Rev}	R_{DSON} in reverse battery condition	V_{CC} = -13 V; I_{OUT} = -6 A; T_j = 25 °C		7		mΩ
V_{clamp}	Clamp voltage	I_S = 20 mA; T_j = -40 °C	38			V
		I_S = 20 mA; 25 °C < T_j < 150 °C	41	46	52	

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{STBY}	Supply current in standby at V_{CC} = 13 V (1)	V_{CC} = 13 V; V_{IN} = V_{OUT} = V_{SEn} = 0 V; T_j = 25°C			0.5	µA
		V_{CC} = 13 V; V_{IN} = V_{OUT} = V_{SEn} = 0 V; T_j = 85 °C (2)			0.5	µA
		V_{CC} = 13 V; V_{IN} = V_{OUT} = V_{SEn} = 0 V; T_j = 125 °C			3	µA
t_{D_STBY}	Standby mode blanking time	V_{CC} = 13 V; V_{IN} = 5 V; V_{SEn} = 0 V; I_{OUT} = 0 A	60	300	550	µs
$I_{S(ON)}$	Supply current	V_{CC} = 13 V; V_{SEn} = 0 V; V_{IN} = 5 V; I_{OUT} = 0 A		3	6.5	mA
$I_{GND(ON)}$	Control stage current consumption in ON-state. All channels active.	V_{CC} = 13 V; V_{SEn} = 5 V; V_{IN} = 5 V; I_{OUT} = 6 A			9	mA
$I_{L(off)}$	Off-state output current at V_{CC} = 13 V	V_{IN} = V_{OUT} = 0 V; V_{CC} = 13 V; T_j = 25 °C	0	0.01	0.5	µA
		V_{IN} = V_{OUT} = 0 V; V_{CC} = 13 V; T_j = 125 °C	0		3	
V_F	Output - V_{CC} diode voltage	I_{OUT} = -6 A; T_j = 150 °C			0.7	V

Notes:

(1)PowerMOS leakage included.

(2)Parameter specified by design; not subject to production test.

Table 7: Switching

V_{CC} = 13 V; -40 °C < T_j < 150 °C, unless otherwise specified						
Symbol	**Parameter**	**Test conditions**	**Min.**	**Typ.**	**Max.**	**Unit**
$t_{d(on)}$(1)	Turn-on delay time at T_j = 25 °C	R_L = 2.2 Ω	10	65	120	µs
$t_{d(off)}$(1)	Turn-off delay time at T_j = 25 °C		10	55	100	
$(dV_{OUT}/dt)_{on}$(1)	Turn-on voltage slope at T_j = 25 °C	R_L = 2.2 Ω	0.1	0.36	0.8	V/µs
$(dV_{OUT}/dt)_{off}$(1)	Turn-off voltage slope at T_j = 25 °C		0.1	0.47	0.8	
W_{ON}	Switching energy losses at turn-on (t_{won})	R_L = 2.2 Ω	—	0.6	1.7(2)	mJ
W_{OFF}	Switching energy losses at turn-off (t_{woff})	R_L = 2.2 Ω	—	0.6	1.7(2)	mJ
t_{SKEW}(1)	Differential Pulse skew (t_{PHL} - t_{PLH})	R_L = 2.2 Ω	-65	-15	35	µs

Notes:

(1)See *Figure 6: "Switching times and Pulse skew"*

(2)Parameter guaranteed by design and characterization; not subject to production test.

Table 8: Logic inputs

7 V < V_{CC} < 28 V; -40 °C < T_j < 150 °C						
Symbol	**Parameter**	**Test conditions**	**Min.**	**Typ.**	**Max.**	**Unit**
INPUT characteristics						
V_{IL}	Input low level voltage				0.9	V
I_{IL}	Low level input current	V_{IN} = 0.9 V	1			µA
V_{IH}	Input high level voltage		2.1			V
I_{IH}	High level input current	V_{IN} = 2.1 V			10	µA
$V_{I(hyst)}$	Input hysteresis voltage		0.2			V
V_{ICL}	Input clamp voltage	I_{IN} = 1 mA	5.3		7.5	V
		I_{IN} = -1 mA		-0.7		
SEn characteristics (7 V < V_{CC} < 18 V)						
V_{SEnL}	Input low level voltage				0.9	V
I_{SEnL}	Low level input current	V_{IN} = 0.9 V	1			µA
V_{SEnH}	Input high level voltage		2.1			V
I_{SEnH}	High level input current	V_{IN} = 2.1 V			10	µA
$V_{SEn(hyst)}$	Input hysteresis voltage		0.2			V
V_{SEnCL}	Input clamp voltage	I_{IN} = 1 mA	5.3		7.5	V
		I_{IN} = -1 mA		-0.7		

Table 9: Protection

7 V < V_{CC} < 18 V; -40 °C < T_j < 150 °C						
Symbol	**Parameter**	**Test conditions**	**Min.**	**Typ.**	**Max.**	**Unit**
I_{LIMH} (1)	DC short circuit current	V_{CC} = 13 V	70	100	140	A
		4 V < V_{CC} < 18 V (2)			140	
I_{LIML}	Short circuit current during thermal cycling	V_{CC} = 13 V; T_R < T_j < T_{TSD}		33		
T_{TSD}	Shutdown temperature		150	175	200	°C
T_R	Reset temperature(2)		T_{RS} + 1	T_{RS} + 7		
T_{RS}	Thermal reset of fault diagnostic indication	V_{SEn} = 5 V	135			
T_{HYST}	Thermal hysteresis (T_{TSD} - T_R)(2)			7		
ΔT_{J_SD}	Dynamic temperature	T_j = -40 °C; V_{CC} = 13 V		60		K
V_{DEMAG}	Turn-off output voltage clamp	I_{OUT} = 2 A; L = 6 mH; T_j = -40 °C	V_{CC} - 38			V
		I_{OUT} = 2 A; L = 6 mH; T_j = 25 °C to 150 °C	V_{CC} - 41	V_{CC} - 46	V_{CC} - 52	V
V_{ON}	Output voltage drop limitation	I_{OUT} = 1.2 A		20		mV

Notes:

(1)Parameter guaranteed by an indirect test sequence.

(2)Parameter guaranteed by design and characterization; not subject to production test.

Table 10: CurrentSense

7 V < V_{CC} < 18 V; -40 °C < T_j < 150 °C						
Symbol	**Parameter**	**Test conditions**	**Min.**	**Typ.**	**Max.**	**Unit**
V_{SENSE_CL}	CurrentSense clamp voltage	V_{SEn} = 0 V; I_{SENSE} = 1 mA	-17		-12	V
		V_{SEn} = 0 V; I_{SENSE} = -1 mA		7		V
Current Sense characteristics						
K_{OL1}	I_{OUT}/I_{SENSE}	I_{OUT} = 10 mA; V_{SENSE} = 0.5 V; V_{SEn} = 5 V	800			
K_{OL2}	I_{OUT}/I_{SENSE}	I_{OUT} = 0.25 A; V_{SENSE} = 0.5 V; V_{SEn} = 5 V			10400	
K_0	I_{OUT}/I_{SENSE}	I_{OUT} = 1 A; V_{SENSE} = 4 V; V_{SEn} = 5 V	3390	6600	10180	
dK_0/K_0 (1)(2)	Current sense ratio drift	I_{OUT} = 1 A; V_{SENSE} = 4 V; V_{SEn} = 5 V	-25		25	%
K_1	I_{OUT}/I_{SENSE}	I_{OUT} = 4.6 A; V_{SENSE} = 4 V; V_{SEn} = 5 V	4080	6570	9530	
dK_1/K_1 (1)(2)	Current sense ratio drift	I_{OUT} = 4.6 A; V_{SENSE} = 4 V; V_{SEn} = 5 V	-20		20	%
K_2	I_{OUT}/I_{SENSE}	I_{OUT} = 9 A; V_{SENSE} = 4 V; V_{SEn} = 5 V	4830	6350	8060	
dK_2/K_2 (1)(2)	Current sense ratio drift	I_{OUT} = 9 A; V_{SENSE} = 4 V; V_{SEn} = 5 V	-13		13	%
K_3	I_{OUT}/I_{SENSE}	I_{OUT} = 27 A; V_{SENSE} = 4 V; V_{SEn} = 5 V	5600	6300	7150	
dK_3/K_3 (1)(2)	Current sense ratio drift	I_{OUT} = 27 A; V_{SENSE} = 4 V; V_{SEn} = 5 V	-8		8	%
I_{SENSE0}	CurrentSense leakage current	CurrentSense disabled: V_{SEn} = 0 V;	0		0.5	µA
		CurrentSense disabled; -1 V < V_{SENSE} < 5 V (1)	-0.5		0.5	µA
		CurrentSense enabled: V_{SEn} = 5 V; V_{IN} = 5 V; I_{OUT} = 0 A;	0		2	µA
V_{OUT_CSD} (1)	Output voltage for CurrentSense shutdown	V_{SEn} = 5 V; R_{SENSE} = 2.7 kΩ; V_{IN} = 5 V; I_{OUT} = 3 A		5		V
V_{SENSE_SAT}	CurrentSense saturation voltage	V_{CC} = 7 V; R_{SENSE} = 2.7 kΩ; V_{SEn} = 5 V; V_{IN} = 5 V; I_{OUT} = 27 A; T_j = 150 °C	5			V
I_{SENSE_SAT} (1)	CS saturation current	V_{CC} = 7 V; V_{SENSE} = 4 V; V_{IN} = 5 V; V_{SEn} = 5 V; T_j = 150 °C	4			mA
I_{OUT_SAT} (1)	Output saturation current	V_{CC} = 7 V; V_{SENSE} = 4 V; V_{IN} = 5 V; V_{SEn} = 5 V; T_j = 150 °C	45			A
OFF-state diagnostic						
V_{OL}	OFF-state open-load voltage detection threshold	V_{IN} = 0 V; V_{SEn} = 5 V	2	3	4	V

7 V < V_{CC} < 18 V; -40 °C < T_j < 150 °C						
Symbol	**Parameter**	**Test conditions**	**Min.**	**Typ.**	**Max.**	**Unit**
$I_{L(off2)}$	OFF-state output sink current	V_{IN} = 0 V; V_{OUT} = V_{OL}; T_j = -40 °C to 125 °C	-100		-15	µA
t_{DSTKON}	OFF-state diagnostic delay time from falling edge of INPUT (see *Figure 7: "tDSTKON"*)	V_{IN} = 5 V to 0 V; V_{SEn} = 5 V; I_{OUT} = 0 A; V_{OUT} = 4 V	100	350	700	µs
$t_{D_OL_V}$	Settling time for valid OFF-state open load diagnostic indication from rising edge of SEn	V_{IN} = 0 V; V_{OUT} = 4 V; V_{SEn} = 0 V to 5 V			60	µs
t_{D_VOL}	OFF-state diagnostic delay time from rising edge of V_{OUT}	V_{IN} = 0 V; V_{SEn} = 5 V; V_{OUT} = 0 V to 4 V		5	30	µs
Fault diagnostic feedback (see *Table 11: "Truth table"*)						
V_{SENSEH}	CurrentSense output voltage in fault condition	V_{CC} = 13 V; V_{IN} = 0 V; V_{SEn} = 5 V; I_{OUT} = 0 A; V_{OUT} = 4 V; R_{SENSE} = 1 kΩ	5		6.6	V
I_{SENSEH}	CurrentSense output current in fault condition	V_{CC} = 13 V; V_{SENSE} = 5 V	7	20	30	mA
CurrentSense timings (current sense mode)[3]						
$t_{DSENSE1H}$	Current sense settling time from rising edge of SEn	V_{IN} = 5 V; V_{SEn} = 0 V to 5 V; R_{SENSE} = 1 kΩ; R_L = 2.2 Ω			60	µs
$t_{DSENSE1L}$	Current sense disable delay time from falling edge of SEn	V_{IN} = 5 V; V_{SEn} = 5 V to 0 V; R_{SENSE} = 1 kΩ; R_L = 2.2 Ω		5	20	µs
$t_{DSENSE2H}$	Current sense settling time from rising edge of INPUT	V_{IN} = 0 V to 5 V; V_{SEn} = 5 V; R_{SENSE} = 1 kΩ; R_L = 2.2 Ω		100	300	µs
$\Delta t_{DSENSE2H}$	Current sense settling time from rising edge of I_{OUT} (dynamic response to a step change of I_{OUT})	V_{IN} = 5 V; V_{SEn} = 5 V; R_{SENSE} = 1 kΩ; I_{SENSE} = 90% of $I_{SENSEMAX}$; R_L = 2.2 Ω			200	µs
$t_{DSENSE2L}$	Current sense turn-off delay time from falling edge of INPUT	V_{IN} = 5 V to 0 V; V_{SEn} = 5 V; R_{SENSE} = 1 kΩ; R_L = 2.2 Ω		50	250	µs

Notes:

(1)Parameter guaranteed by design and characterization; not subject to production test.

(2)All values refer to V_{CC} = 13 V; T_j = 25°C, unless otherwise specified.

(3)Transition delay are measured up to ±10% of final conditions.

Figure 4: IOUT/ISENSE versus IOUT

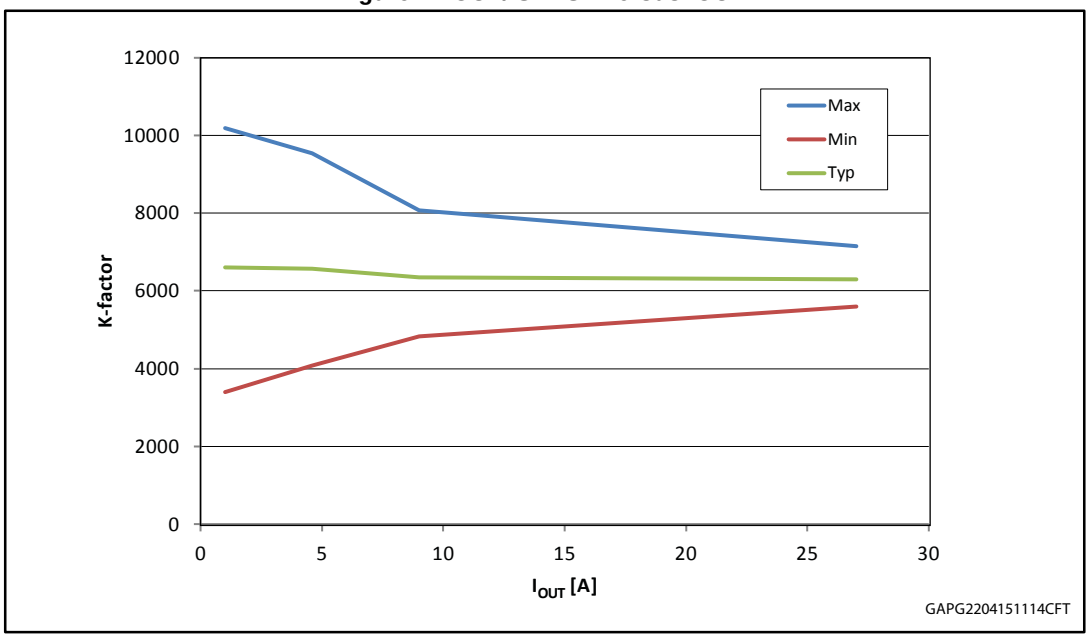


Figure 5: Current sense precision vs. IOUT

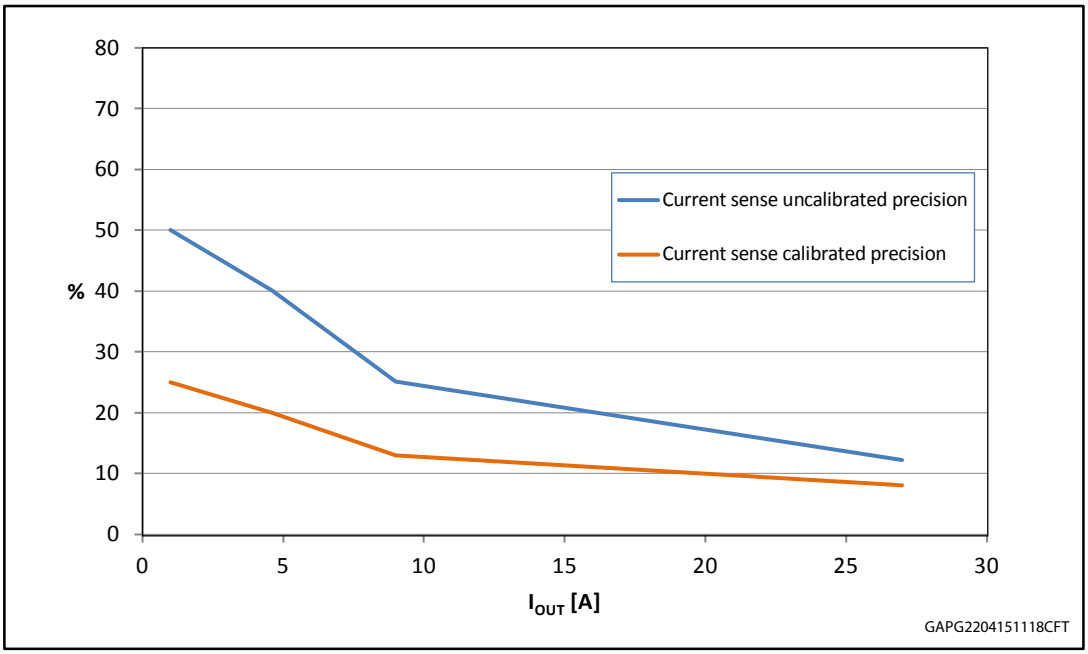


Figure 6: Switching times and Pulse skew

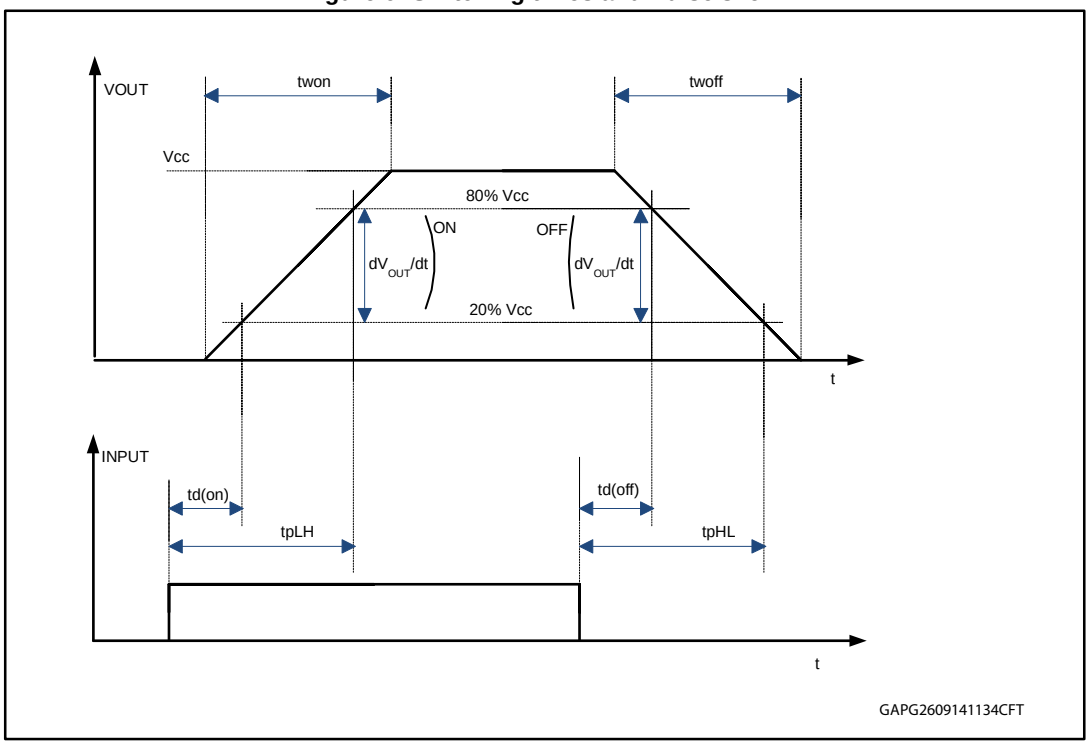


Figure 7: tDSTKON

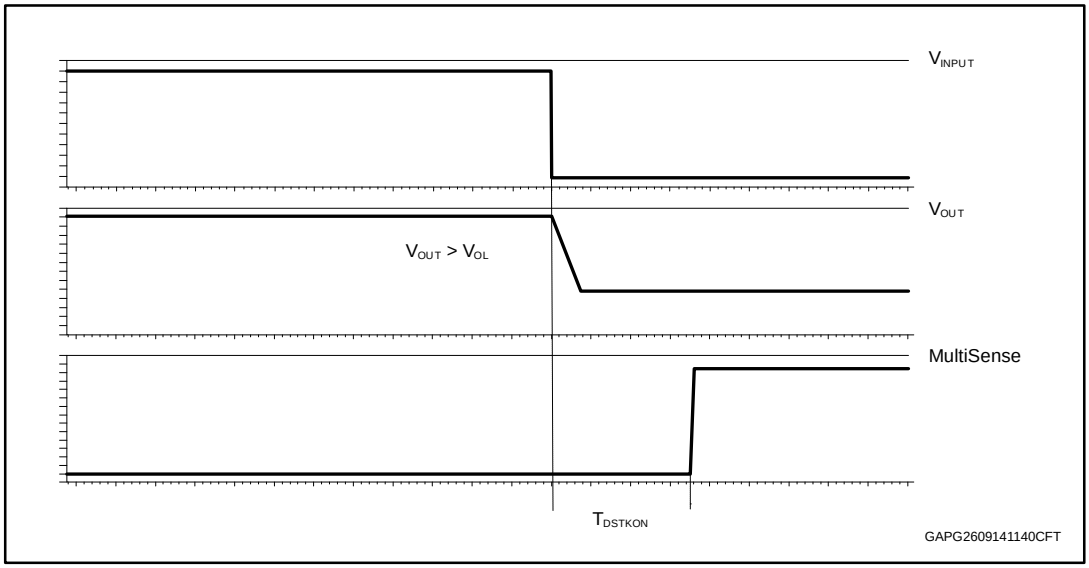


Table 11: Truth table

Mode	Conditions	IN_X	SEn	OUT_X	Current Sense	Comments
Standby	All logic inputs low	L	L	L	Hi-Z	Low quiescent current consumption
Normal	Nominal load connected; T_j < 150°C	L	H	L	0	
		H	L	H	Hi-Z	
		H	H	H	I_{SENSE} = 1/K * I_{OUT}	
Overload	Overload or short to GND causing: $T_j > T_{TSD}$ or $\Delta T_j > \Delta T_{j_SD}$	H	L	H	Hi-Z	Output cycles with temperature hysteresis
		H	H	H	V_{SENSEH}	
Undervoltage	$V_{CC} < V_{USD}$ (falling)	X	X	L L	Hi-Z Hi-Z	Re-start when $V_{CC} > V_{USD} + V_{USDhyst}$ (rising)
OFF-state diagnostics	Short to V_{CC}	L	H	H	V_{SENSEH}	
	Open-load	L	H	H		External pull-up
Negative output voltage	Inductive loads turn-off	L	X	< 0 V	0	

2.4 Electrical characteristics curves

Figure 8: OFF-state output current

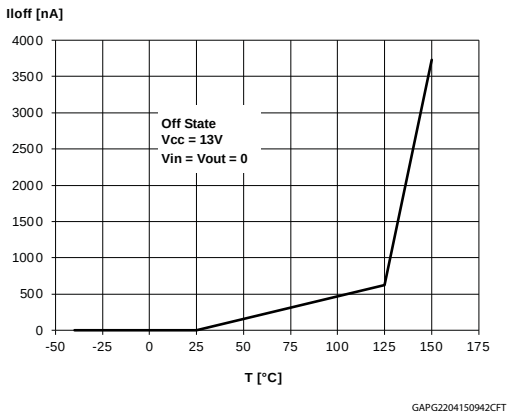


Figure 9: Standby current

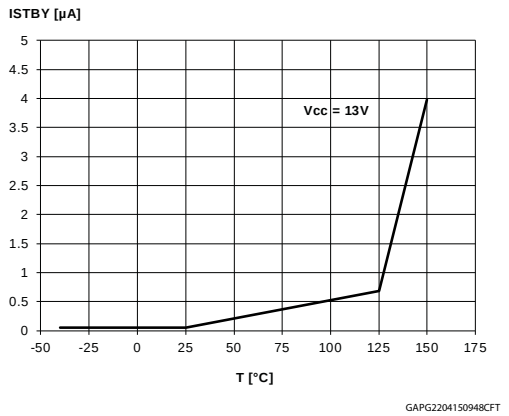


Figure 10: IGND(ON) vs Tcase

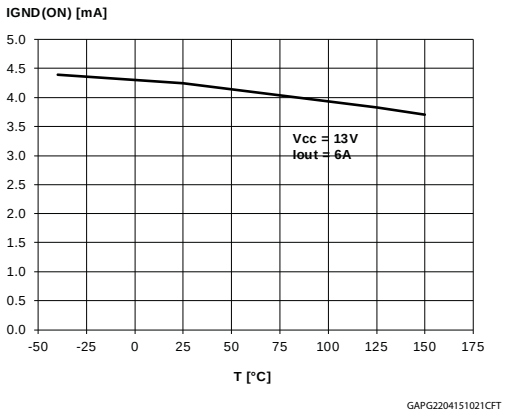


Figure 11: Logic Input high level voltage

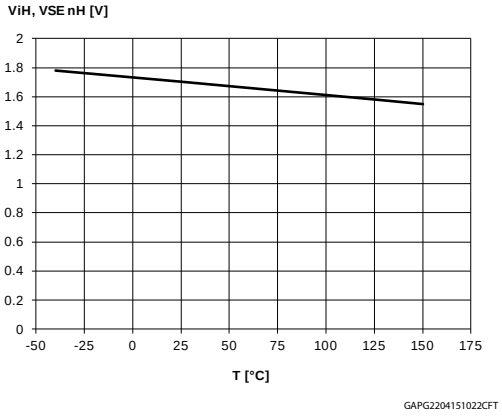


Figure 12: Logic Input low level voltage

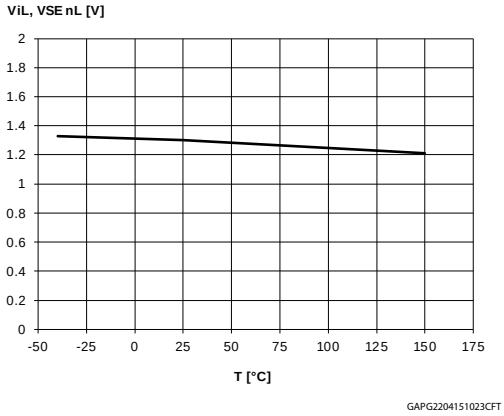


Figure 13: High level logic input current

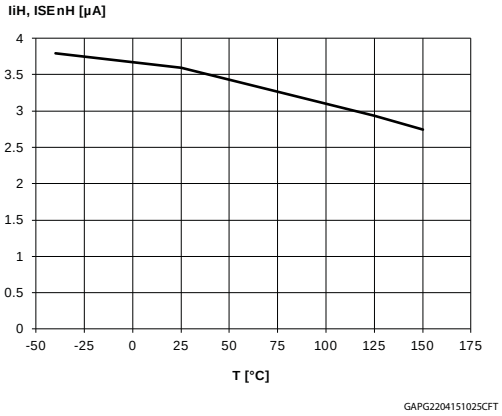


Figure 14: Low level logic input current

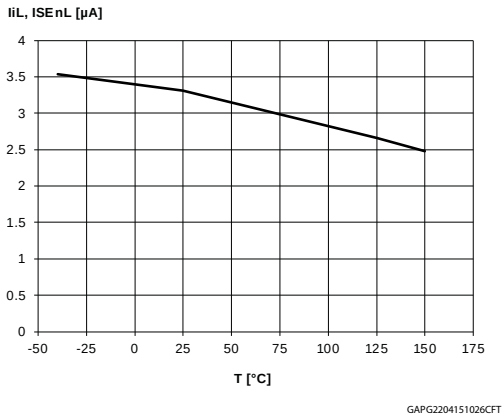


Figure 15: Logic Input hysteresis voltage

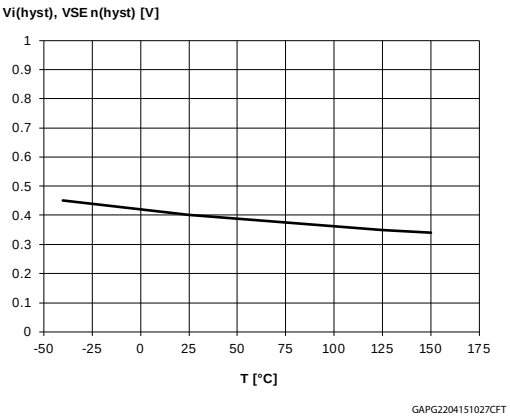


Figure 16: Undervoltage shutdown

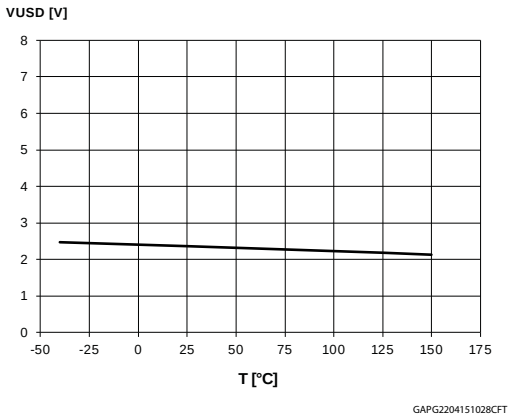


Figure 17: On-state resistance vs Tcase

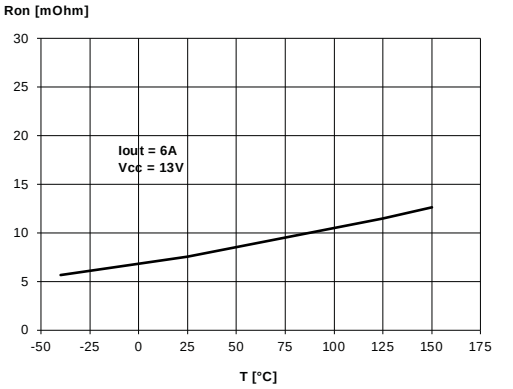


Figure 18: On-state resistance vs VCC

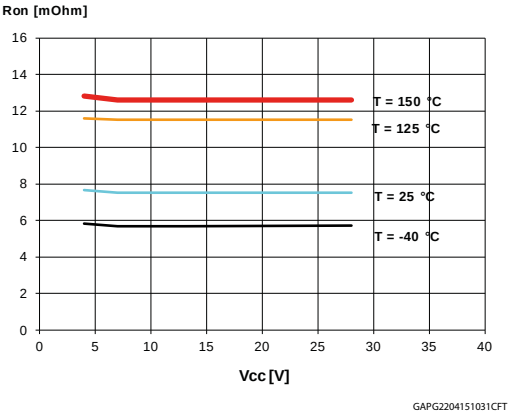


Figure 19: Turn-on voltage slope

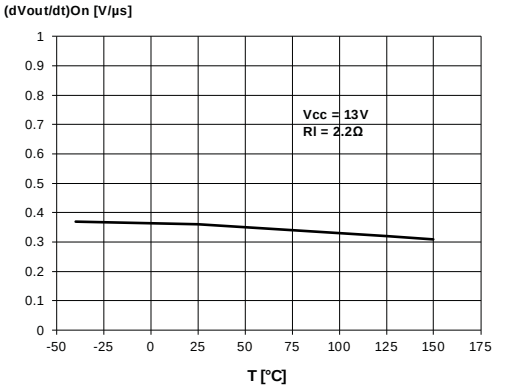


Figure 20: Turn-off voltage slope

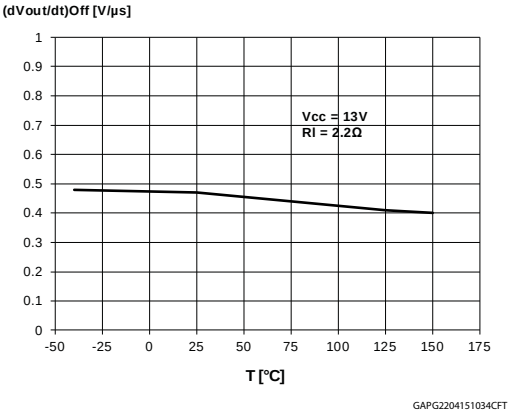


Figure 21: Won vs Tcase

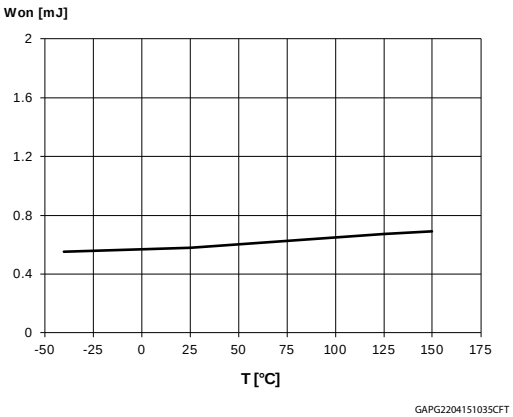


Figure 22: Woff vs Tcase

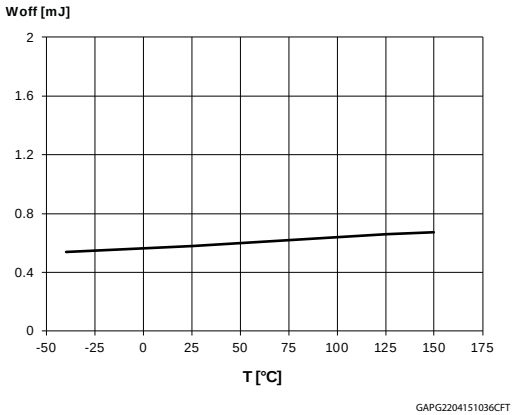


Figure 23: ILIMH vs. Tcase

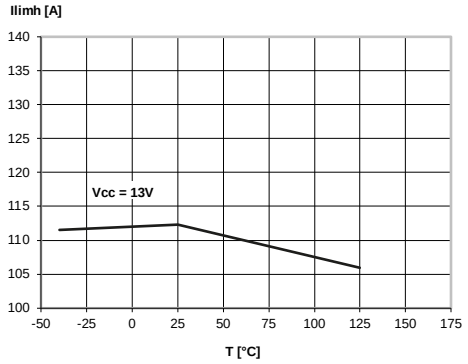


Figure 24: Turn-off output voltage clamp

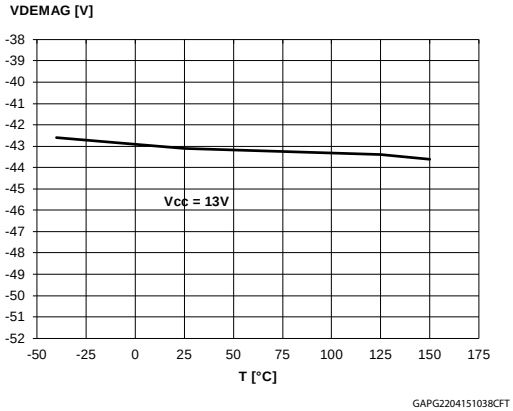


Figure 25: OFF-state open-load voltage detection threshold

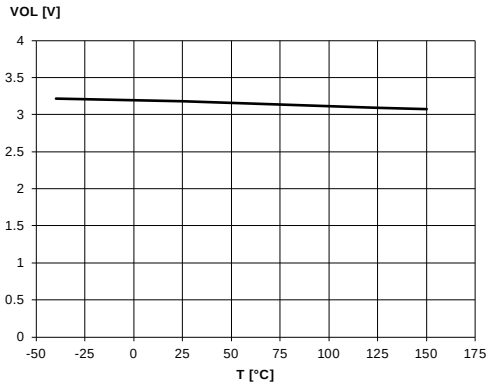


Figure 26: Vsense clamp vs. Tcase

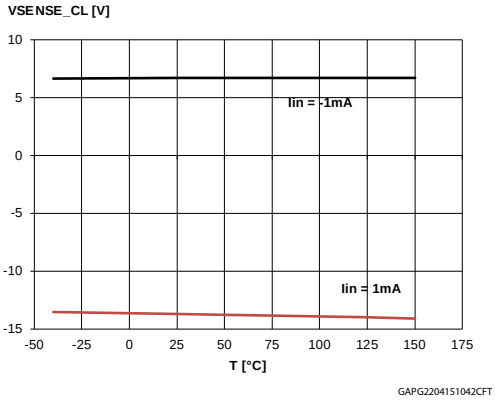
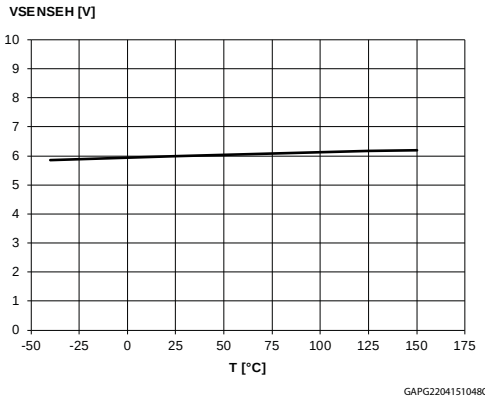


Figure 27: Vsenseh vs. Tcase



3 Protections

3.1 Power limitation

The basic working principle of this protection consists of an indirect measurement of the junction temperature swing ΔT_j through the direct measurement of the spatial temperature gradient on the device surface in order to automatically shut off the output MOSFET as soon as ΔT_j exceeds the safety level of ΔT_{j_SD}. The protection prevents fast thermal transient effects and, consequently, reduces thermo-mechanical fatigue.

3.2 Thermal shutdown

In case the junction temperature of the device exceeds the maximum allowed threshold (typically 175°C), it automatically switches off and the diagnostic indication is triggered. The device switches on again as soon as its junction temperature drops to T_R.

3.3 Current limitation

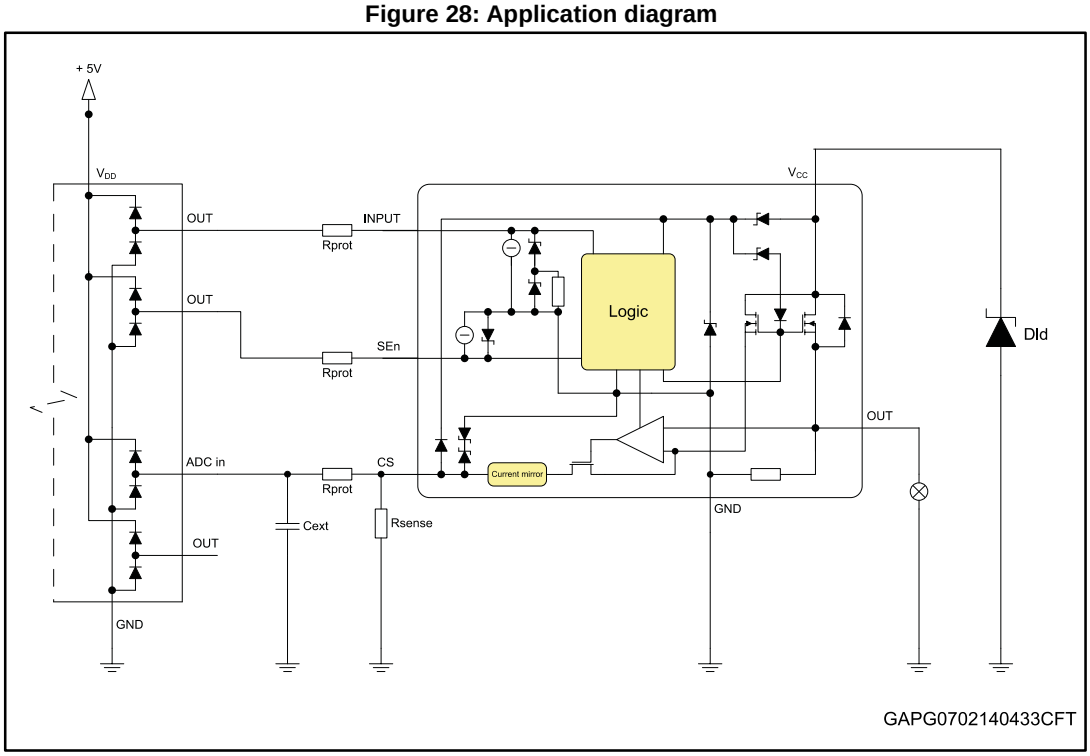
The device is equipped with an output current limiter in order to protect the silicon as well as the other components of the system (e.g. bonding wires, wiring harness, connectors, loads, etc.) from excessive current flow. Consequently, in case of short circuit, overload or during load power-up, the output current is clamped to a safety level, I_{LIMH}, by operating the output power MOSFET in the active region.

3.4 Negative voltage clamp

In case the device drives inductive load, the output voltage reaches negative value during turn off. A negative voltage clamp structure limits the maximum negative voltage to a certain value, V_{DEMAG}, allowing the inductor energy to be dissipated without damaging the device.

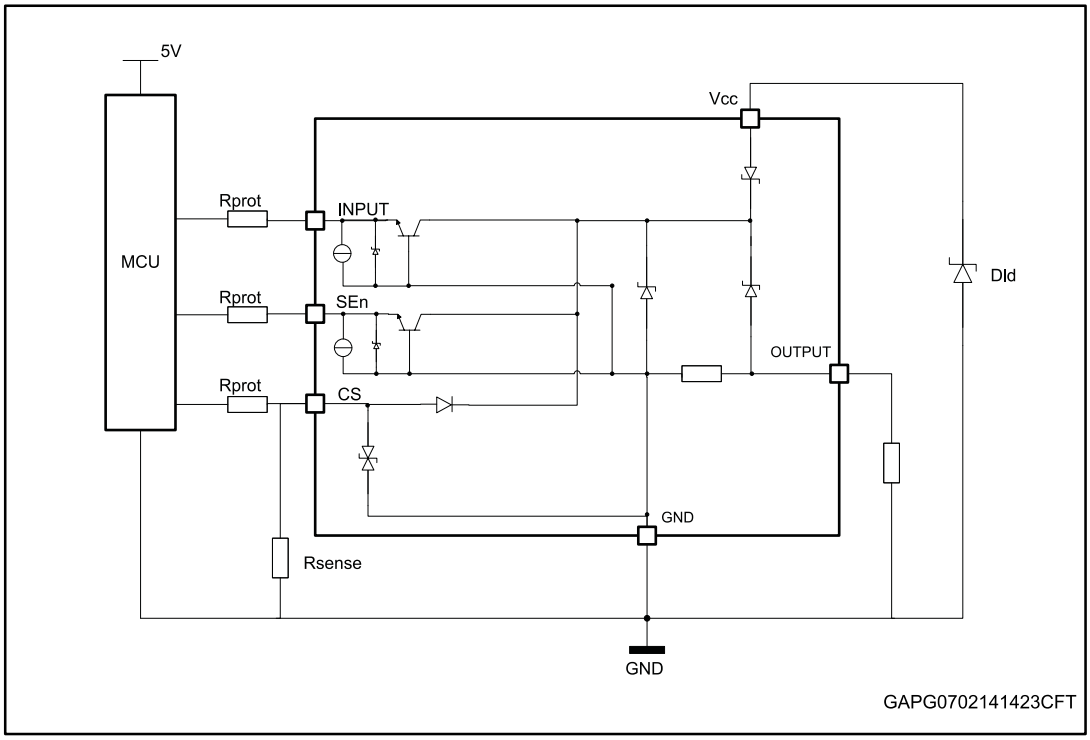
4 Application information

Figure 28: Application diagram



4.1 Protection against reverse battery

Figure 29: Simplified internal structure



The device does not need any external components to protect the internal logic in case of a reverse battery condition. The protection is provided by internal structures.

In addition, due to the fact that the output MOSFET turns on even in reverse battery mode, thus providing the same low ohmic path as in regular operating conditions, no additional power dissipation has to be considered.

4.2 Immunity against transient electrical disturbances

The immunity of the device against transient electrical emissions, conducted along the supply lines and injected into the V_{CC} pin, is tested in accordance with ISO7637-2:2011 (E) and ISO 16750-2:2010.

The related function performance status classification is shown in *Table 12: "ISO 7637-2 - electrical transient conduction along supply line"*.

Test pulses are applied directly to DUT (Device Under Test) both in ON and OFF-state and in accordance to ISO 7637-2:2011(E), chapter 4. The DUT is intended as the present device only, without components and accessed through V_{CC} and GND terminals.

Status II is defined in ISO 7637-1 Function Performance Status Classification (FPSC) as follows: “The function does not perform as designed during the test but returns automatically to normal operation after the test”.

Table 12: ISO 7637-2 - electrical transient conduction along supply line

Test Pulse 2011(E)	Test pulse severity level with Status II functional performance status		Minimum number of pulses or test time	Burst cycle / pulse repetition time		Pulse duration and pulse generator internal impedance
	Level	U_S (1)		min	max	
1	III	-112V	500 pulses	0,5 s		2ms, 10Ω
2a	III	+55V	500 pulses	0,2 s	5 s	50µs, 2Ω
3a	IV	-220V	1h	90 ms	100 ms	0.1µs, 50Ω
3b	IV	+150V	1h	90 ms	100 ms	0.1µs, 50Ω
4 (2)	IV	-7V	1 pulse			100ms, 0.01Ω
Load dump according to ISO 16750-2:2010						
Test B (3)		40V	5 pulse	1 min		400ms, 2Ω

Notes:

(1)U_S is the peak amplitude as defined for each test pulse in ISO 7637-2:2011(E), chapter 5.6.

(2)Test pulse from ISO 7637-2:2004(E).

(3)With 40 V external suppressor referred to ground (-40°C < T_j < 150°C).

4.3 MCU I/Os protection

If a ground protection network is used and negative transients are present on the V_{CC} line, the control pins will be pulled negative. ST suggests to insert a resistor (R_{prot}) in line both to prevent the microcontroller I/O pins from latch-up and to protect the HSD inputs.

The value of these resistors is a compromise between the leakage current of microcontroller and the current required by the HSD I/Os (Input levels compatibility) with the latch-up limit of microcontroller I/Os.

Equation

$V_{CCpeak}/I_{latchup} \leq R_{prot} \leq (V_{OH\mu C}-V_{IH}-V_{GND}) / I_{IHmax}$

Calculation example:

For V_{CCpeak} = -150 V; $I_{latchup} \geq$ 20mA; $V_{OH\mu C} \geq$ 4.5V

7.5 kΩ ≤ R_{prot} ≤ 140 kΩ.

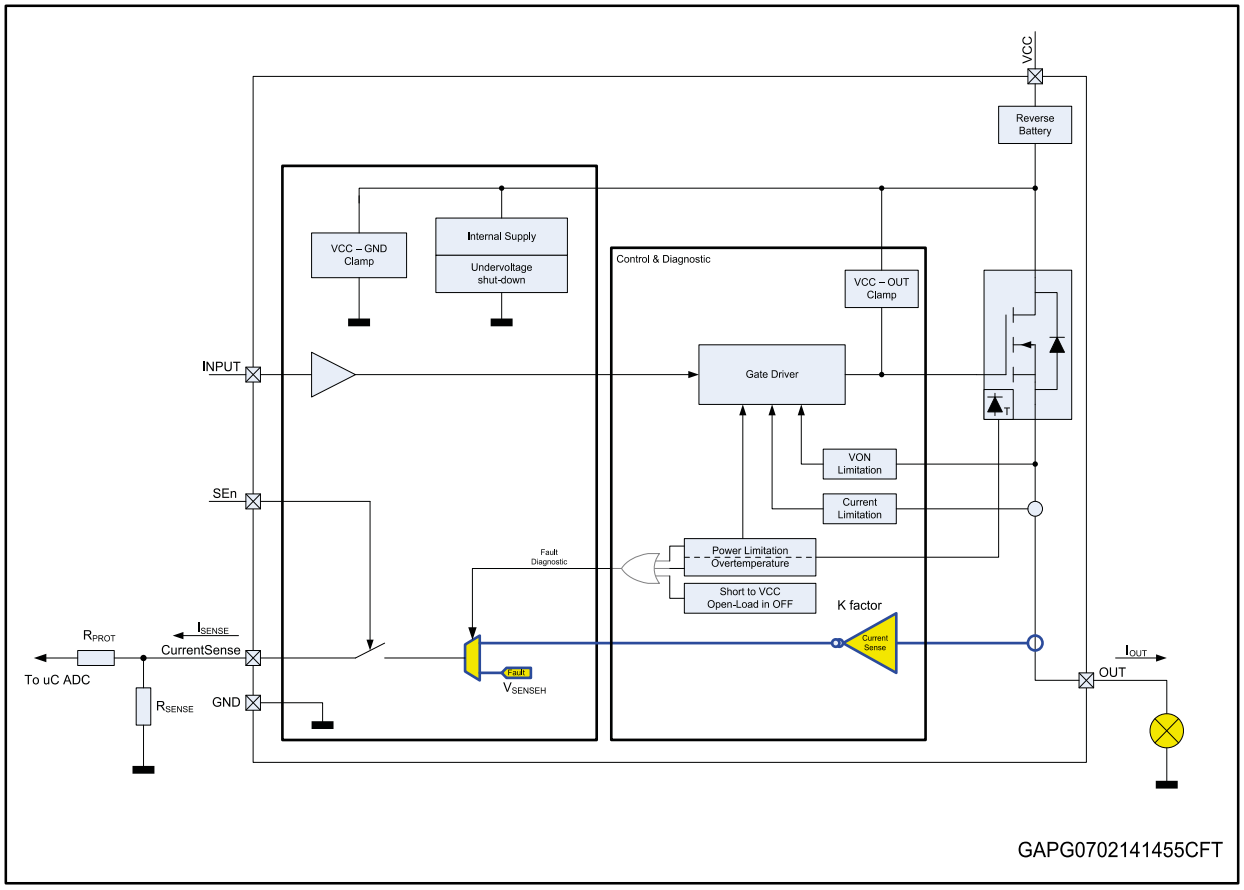
Recommended values: R_{prot} = 15 kΩ

4.4 CS - analog current sense

Diagnostic information on device and load status are provided by an analog output pin (CS) delivering the following signal:

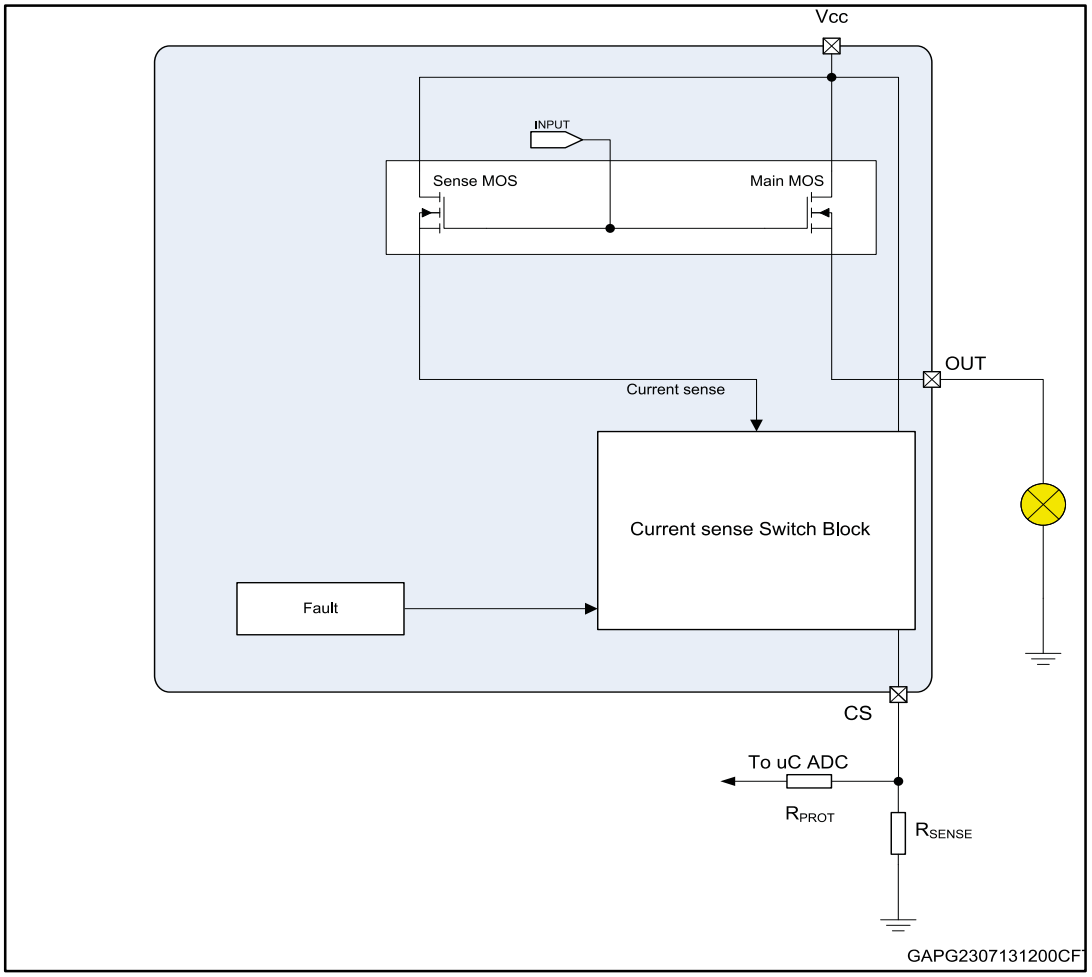
- Current monitor: current monitor of channel output current

Figure 30: CurrentSense and diagnostic – block diagram



4.4.1 Principle of CurrentSense signal generation

Figure 31: CurrentSense block diagram



Current sense

This output is capable of providing:

- Current mirror proportional to the load current in normal operation, delivering current proportional to the load according to known ratio named K
- Diagnostics flag in fault conditions delivering fixed voltage V_{SENSEH}

The current delivered by the current sense circuit, I_{SENSE}, can be easily converted to a voltage V_{SENSE} by using an external sense resistor, R_{SENSE}, allowing continuous load monitoring and abnormal condition detection.

Normal operation (channel ON, no fault, SEn active)

While device is operating in normal conditions (no fault intervention), V_{SENSE} calculation can be done using simple equations

Current provided by CurrentSense output: $I_{SENSE} = I_{OUT}/K$

Voltage on R_{SENSE}: $V_{SENSE} = R_{SENSE} * I_{SENSE} = R_{SENSE} * I_{OUT}/K$

Where :

- V_{SENSE} is voltage measurable on R_{SENSE} resistor

- I_{SENSE} is current provided from CS pin in current output mode
- I_{OUT} is current flowing through output
- K factor represents the ratio between PowerMOS cells and SenseMOS cells; its spread includes geometric factor spread, current sense amplifier offset and process parameters spread of overall circuitry specifying ratio between I_{OUT} and I_{SENSE}.

Failure flag indication

In case of power limitation/overtemperature, the fault is indicated by the CS pin which is switched to a “current limited” voltage source, V_{SENSEH} .

In any case, the current sourced by the CS in this condition is limited to I_{SENSEH}

Figure 32: Analogue HSD – open-load detection in off-state

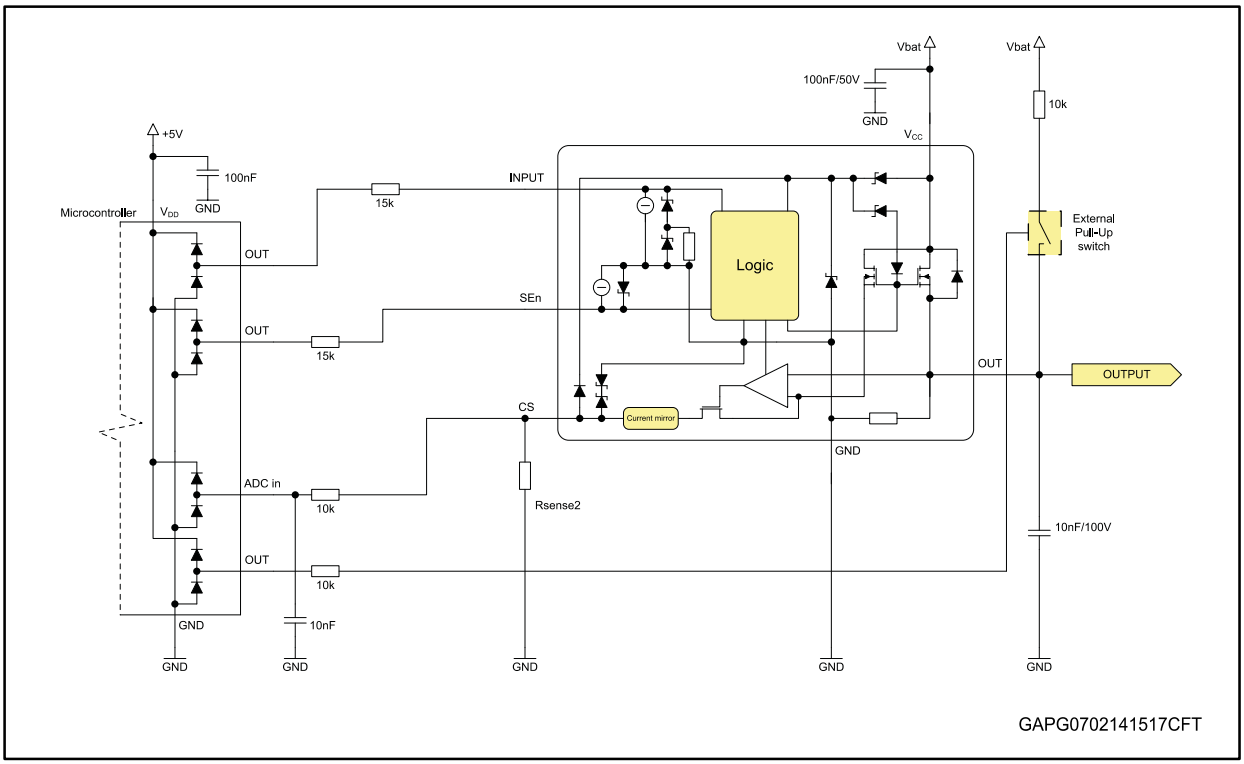


Figure 33: Open-load / short to VCC condition

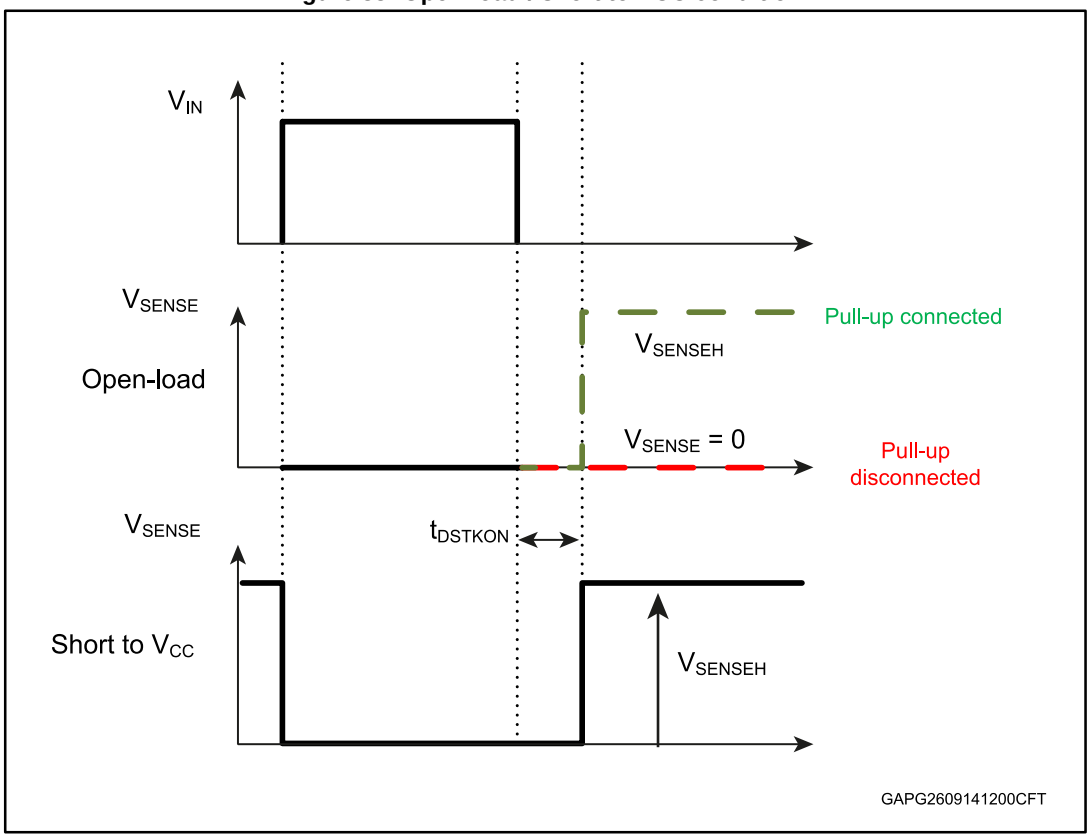


Table 13: CurrentSense pin levels in off-state

Condition	Output	CurrentSense	SEn
Open-load	$V_{OUT} > V_{OL}$	Hi-Z	L
		V_{SENSEH}	H
	$V_{OUT} < V_{OL}$	Hi-Z	L
		0	H
Short to V_{CC}	$V_{OUT} > V_{OL}$	Hi-Z	L
		V_{SENSEH}	H
Nominal	$V_{OUT} < V_{OL}$	Hi-Z	L
		0	H

4.4.2 Short to VCC and OFF-state open-load detection

Short to V_{CC}

A short circuit between V_{CC} and output is indicated by the relevant current sense pin set to V_{SENSEH} during the device off-state. Small or no current is delivered by the current sense during the on-state depending on the nature of the short circuit.

OFF-state open-load with external circuitry

Detection of an open-load in off mode requires an external pull-up resistor R_{PU} connecting the output to a positive supply voltage V_{PU}.

It is preferable V_{PU} to be switched off during the module standby mode in order to avoid the overall standby current consumption to increase in normal conditions, i.e. when load is connected.

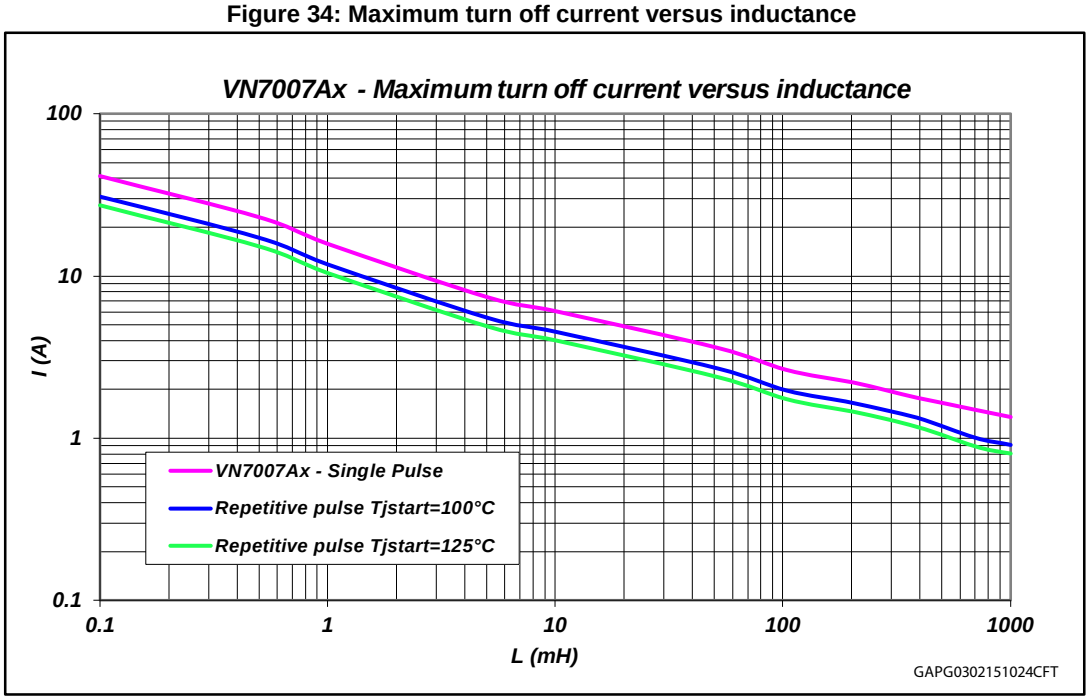
R_{PU} must be selected in order to ensure $V_{OUT} > V_{OLmax}$ in accordance with the following equation:

Equation

$$R_{PU} < \frac{V_{PU} - 4}{I_{L(off2)min\ @\ 4V}}$$

5 Maximum demagnetization energy (Vcc = 16 V)

Figure 34: Maximum turn off current versus inductance



Values are generated with R_L = 0 Ω.

In case of repetitive pulses, T_{jstart} (at the beginning of each demagnetization) of every pulse must not exceed the temperature specified above for curves A and B.

6 Package and PCB thermal data

6.1 Octapak thermal data

Figure 35: Octapak on two-layers PCB (2s0p to JEDEC JESD 51-5)

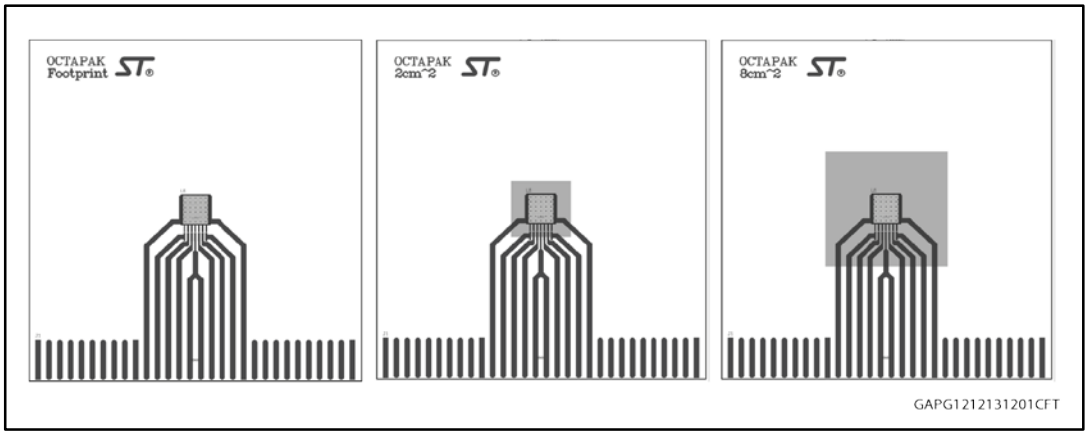


Figure 36: Octapak on four-layers PCB (2s2p to JEDEC JESD 51-7)

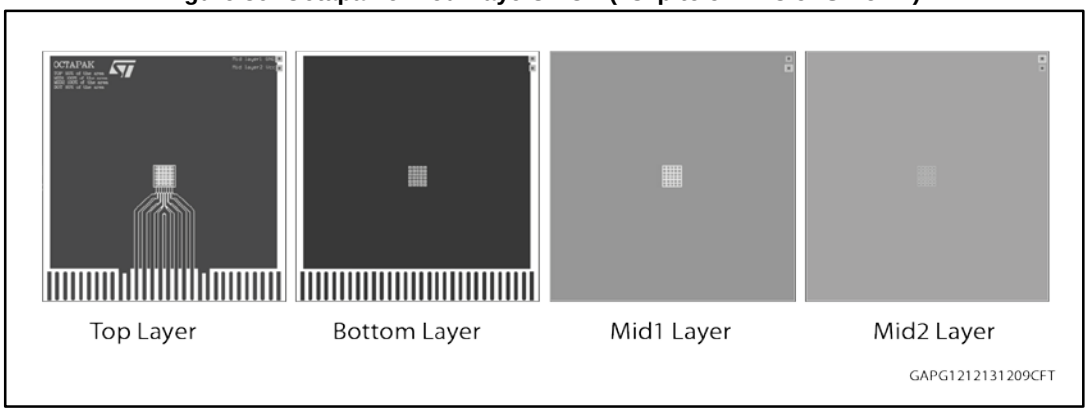


Table 14: PCB properties

Dimension	Value
Board finish thickness	1.6 mm +/- 10%
Board dimension	77 mm x 86 mm
Board Material	FR4
Copper thickness (top and bottom layers)	0.070 mm
Copper thickness (inner layers)	0.035 mm
Thermal vias separation	1.2 mm
Thermal via diameter	0.3 mm +/- 0.08 mm
Copper thickness on vias	0.025 mm
Footprint dimension (top layer)	6.4 mm x 7mm
Heatsink copper area dimension (bottom layer)	Footprint, 2 cm^2 or 8 cm^2

Figure 37: Rthj-amb vs PCB copper area in open box free air conditions

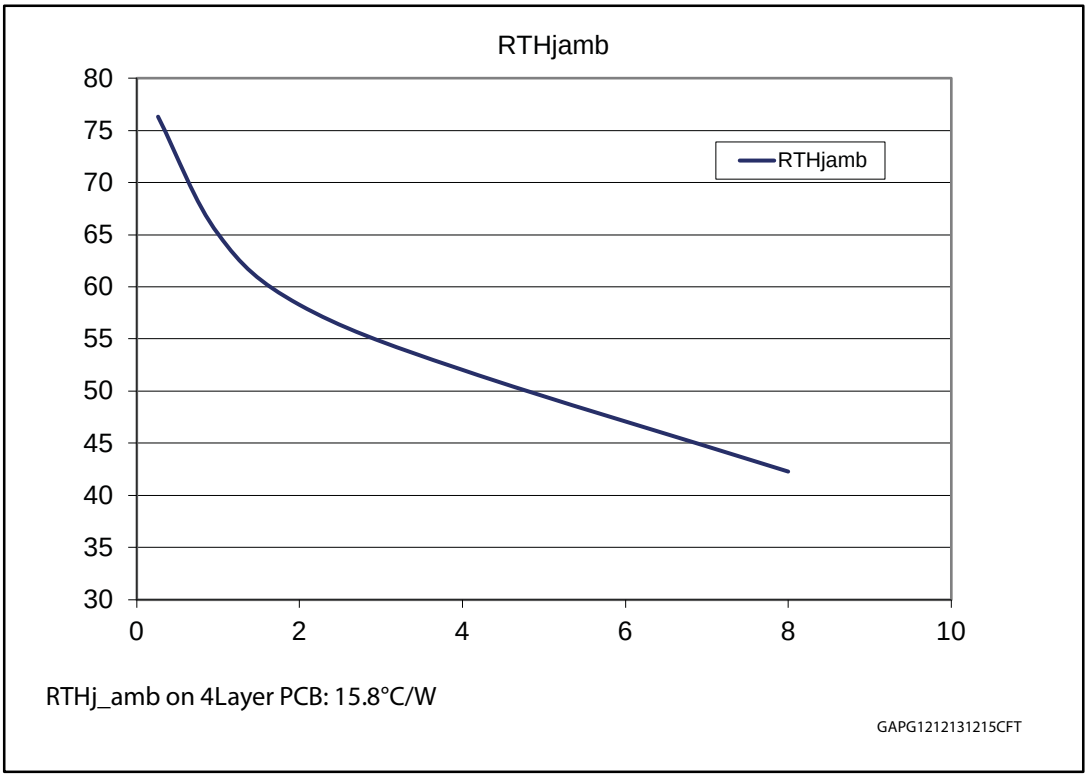
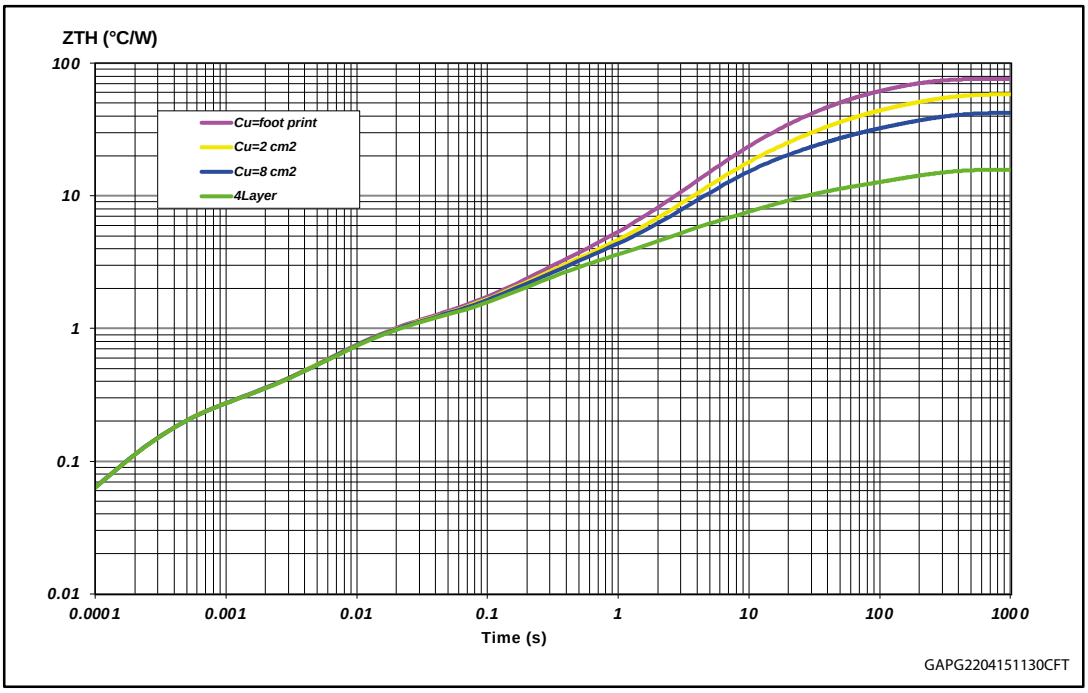


Figure 38: Octapak thermal impedance junction ambient single pulse

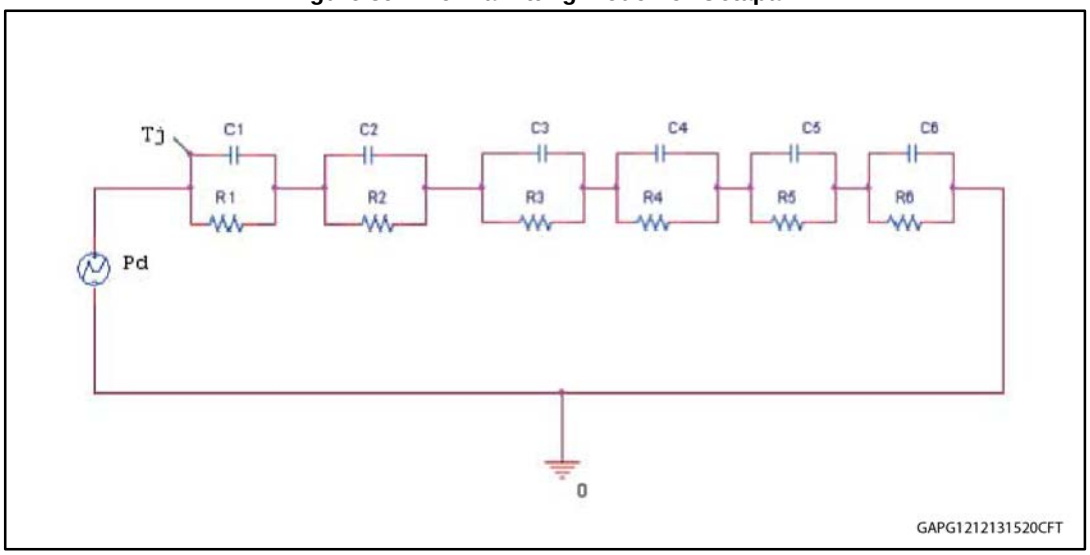


Equation: Pulse calculation formula

$Z_{TH\delta} = R_{TH} \cdot + Z_{THtp} (1 - \delta)$

where $\delta = t_P/T$

Figure 39: Thermal fitting model for Octapak



The fitting model is a simplified thermal tool and is valid for transient evolutions where the embedded protections (power limitation or thermal cycling during thermal shutdown) are not triggered.

Table 15: Thermal parameters

Area/island (cm^2)	Footprint	2	8	4L
R1 (°C/W)	0.2	0.2	0.2	0.2
R2 (°C/W)	0.7	0.7	0.7	0.7
R3 (°C/W)	1.4	1.4	1.4	1.4
R4 (°C/W)	10	10	10	2.5
R5 (°C/W)	28	20	12	5
R6 (°C/W)	36	26	18	6
C1 (W.s/°C)	0.0015	0.0015	0.0015	0.0015
C2 (W.s/°C)	0.013	0.013	0.013	0.013
C3 (W.s/°C)	0.15	0.15	0.15	0.15
C4 (W.s/°C)	0.6	0.6	0.6	0.8
C5 (W.s/°C)	0.8	1.4	2.2	3
C6 (W.s/°C)	3	6	9	25

7 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: ***www.st.com***. ECOPACK® is an ST trademark.

7.1 Octapak package information

Figure 40: Octapak package dimensions

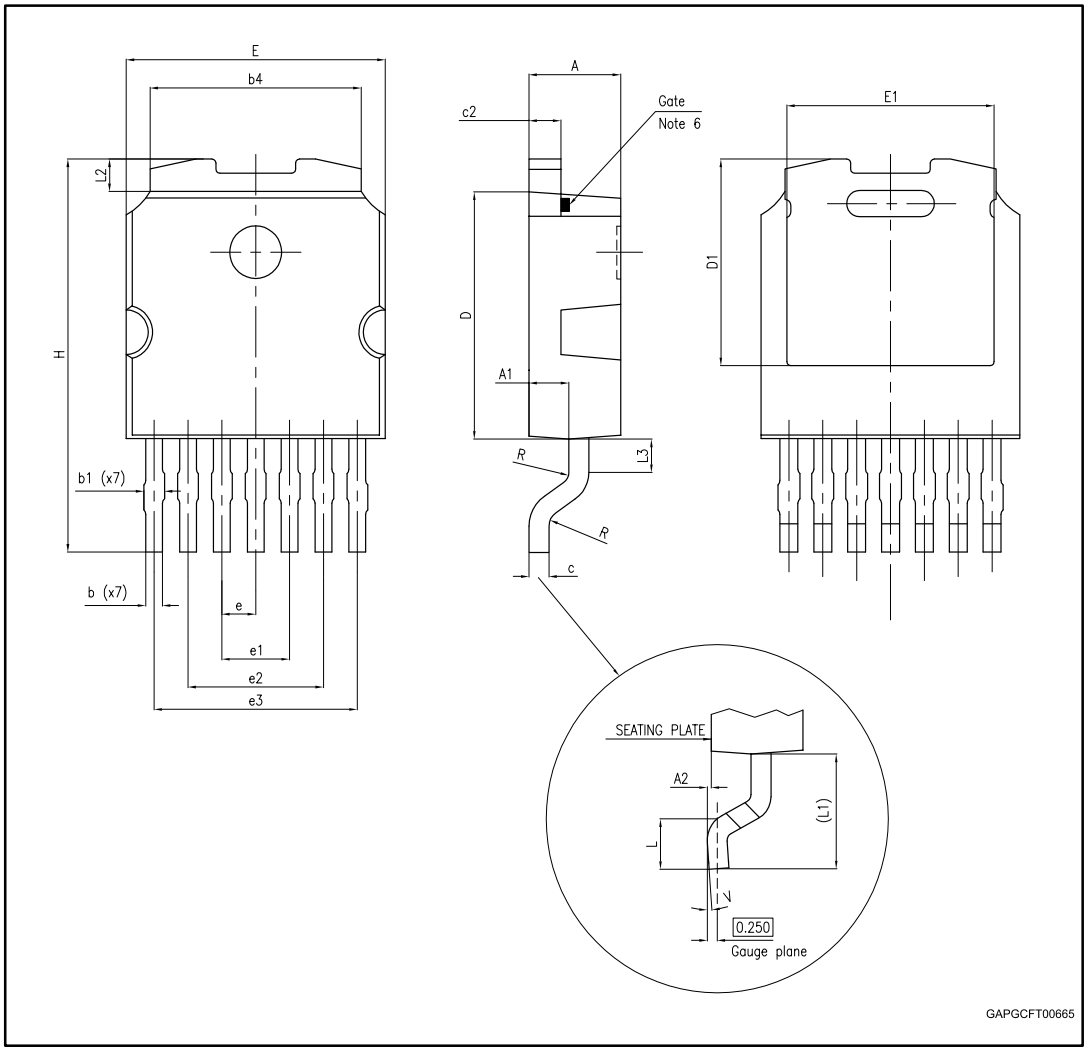


Table 16: Octapak mechanical data

Symbol	Millimeters		
	Min.	Typ.	Max.
A	2.20	2.30	2.40
A1	0.90	1.00	1.10
A2	0.03		0.15
b	0.38	0.45	0.52
b1			0.70
b4	5.20	5.30	5.40
c	0.45	0.50	0.60
c2	0.75	0.80	0.90
D	6.00	6.10	6.20
D1		5.15	
E	6.40	6.50	6.60
E1		5.30	
e	0.85 BSC		
e1	1.60	1.70	1.80
e2	3.30	3.40	3.50
e3	5.00	5.10	5.20
H	9.35	9.70	10.10
L	1.00		—
(L1)		2.80	
L2		0.80	
L3		0.85	
R	0.40 BSC		
V2	0°		8°

7.2 Octapak packing information

Figure 41: Octapack reel 13"

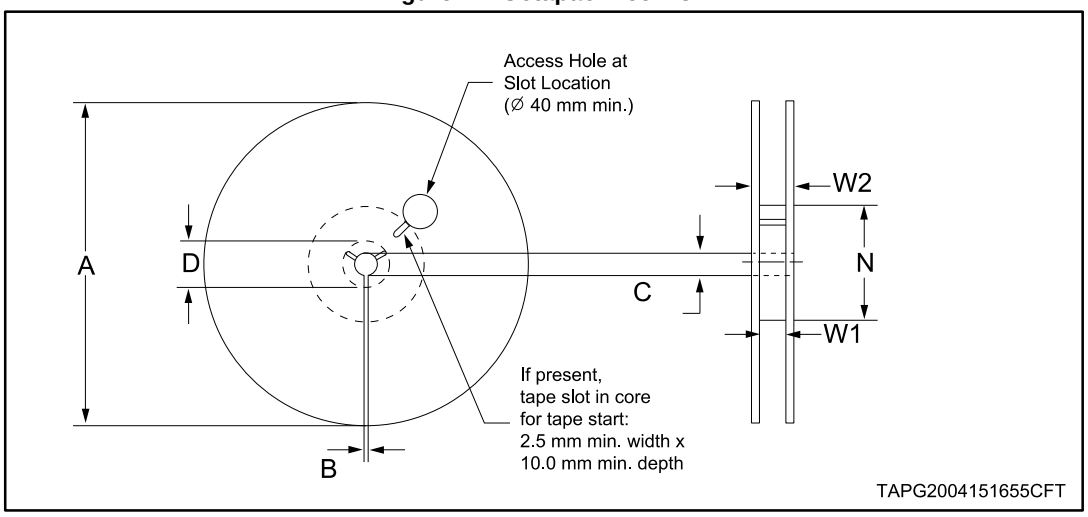


Table 17: Reel dimensions

Description	Value[(1)]
Base quantity	2500
Bulk quantity	2500
A (max)	330
B (min)	1.5
C (+0.5, -0.2)	13
D	20.2
N	100
W1 (+2 /-0)	16.4
W2 (max)	22.4

Notes:

(1)All dimensions are in mm.

Figure 42: Octapak carrier tape

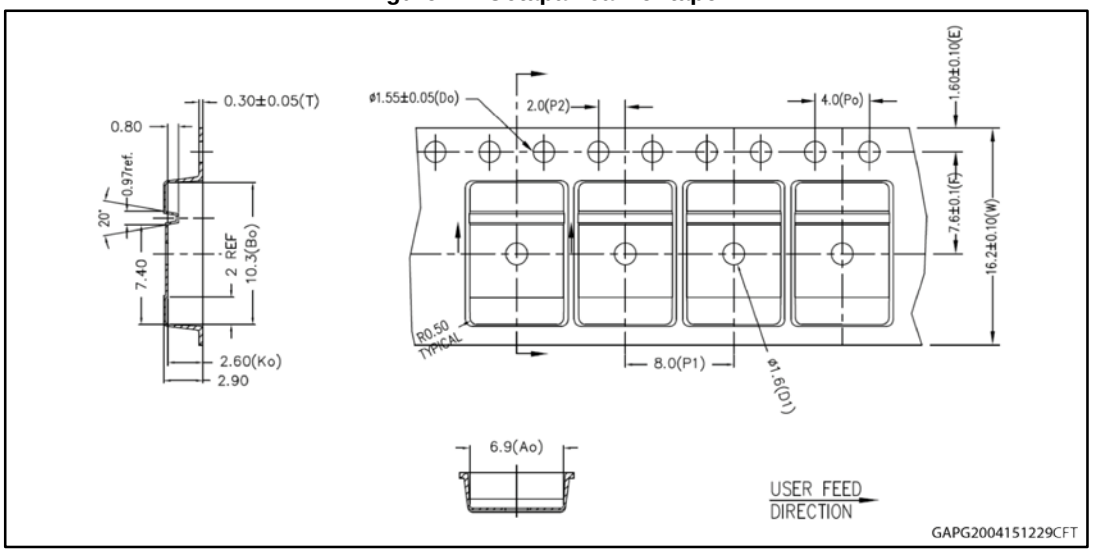
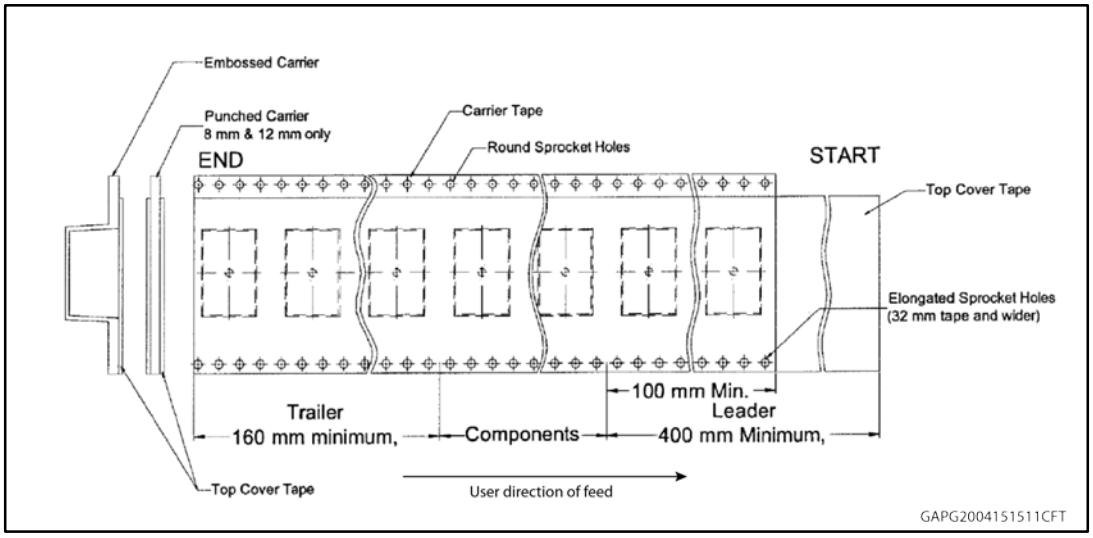
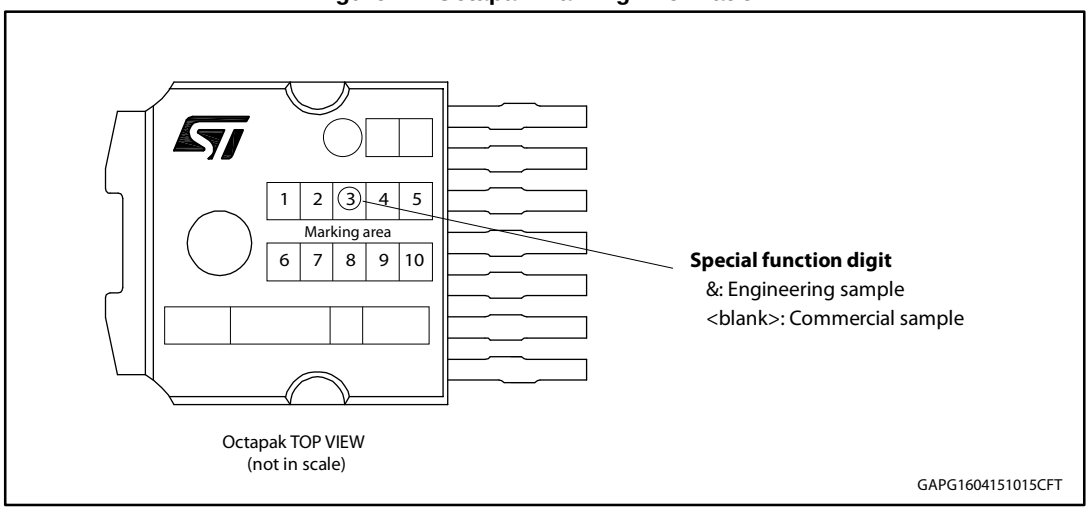


Figure 43: Octapak schematic drawing of leader and trailer tape



7.3 Octapak marking information

Figure 44: Octapak marking information



Engineering Samples: these samples can be clearly identified by a dedicated special symbol in the marking of each unit. These samples are intended to be used for electrical compatibility evaluation only; usage for any other purpose may be agreed only upon written authorization by ST. ST is not liable for any customer usage in production and/or in reliability qualification trials.

Commercial Samples: fully qualified parts from ST standard production with no usage restrictions.

8 Revision history

Table 18: Document revision history

Date	Revision	Changes
17-Jun-2015	1	Initial release
13-Oct-2015	2	*Table 10: "CurrentSense"*: • K_{OL1}: updated test conditions

IMPORTANT NOTICE – PLEASE READ CAREFULLY

STMicroelectronics NV and its subsidiaries (“ST”) reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice. Purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST’s terms and conditions of sale in place at the time of order acknowledgement.

Purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of Purchasers’ products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

ST and the ST logo are trademarks of ST. All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.

© 2015 STMicroelectronics – All rights reserved