UCD7138 4-A and 6-A Single-Channel Synchronous-Rectifier Driver With Body-Diode Conduction Sensing and Reporting

1 Features

- Low-Side Gate Driver With Body-Diode Conduction Sensing
- Gate Turnoff Edge Body-Diode Conduction Reporting
- Gate Turnon Edge Delay Optimization
- Works Together With the Dead-Time Compensation (DTC) Module in the UCD3138A Family of Digital Power Controllers:
  - Automatic or Manual Dead-Time Adjustment of Gate Turnon and Turnoff Edges
  - Negative Current Protection
- -150-mV Body-Diode Conduction Sensing Threshold
- Able to Sense Body Diode Conduction Times as Low as 10 ns
- 4-A Peak-Source and 6-A Peak-Sink Drive Current
- Fast Propagation Delays (14-ns Typical)
- Fast Rise and Fall Times (5-ns Typical)
- Up to 2-MHz Operating Frequency
- 4.5-V to 18-V Supply Range
- Rail-to-Rail Drive Capability
- V_{CC} Undervoltage Lockout (UVLO)
- 6-Pin 3-mm × 3-mm WSON-6 Package

2 Applications

- LLC Converters
- Hard Switching Full-Bridge Converters
- Digital Power-Control Applications

3 Description

The UCD7138 device is a 4-A and 6-A single-channel MOSFET driver with body-diode conduction sensing and reporting and is a high performance driver that allows the Texas Instruments UCD3138A digital PWM controller to achieve advanced synchronous-rectification (SR) control. The device contains a high-speed gate driver, a body-diode conduction-sensing circuit, and a turnon delay optimization circuit. The device is suitable for high-power, high-efficiency isolated converter applications where SR dead-time optimization is desired.

The UCD7138 device offers asymmetrical rail-to-rail 4-A source and 6-A sink peak-current drive capability. The short propagation delay and fast rise and fall time allows efficient operation at high frequencies. An internal high-speed comparator with a –150-mV threshold detects the body-diode conduction and reports the information to the UCD3138A digital-power controller. The UCD7138 device is capable of sensing body-diode conduction time as low as 10 ns. The SR turnon edge is optimized by the UCD7138 device. The SR turnoff edge is optimized by the UCD3138A digital-power controller which analyzes the body-diode conduction information reported by the UCD7138 DTC pin.

The benefits of the chipset include maximizing system efficiency by minimizing body-diode conduction time, robust and fast negative-current protection, and a simple interface.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
UCD7138	WSON (6)	3.00 mm × 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

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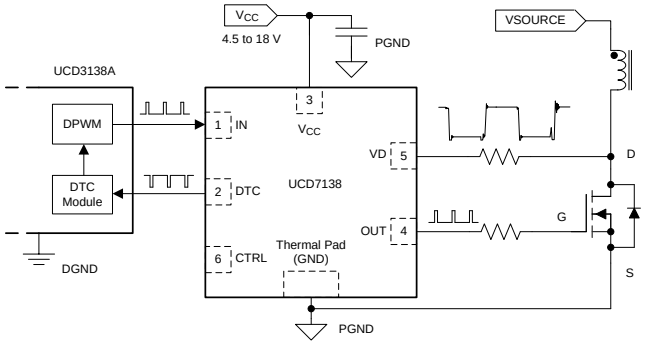
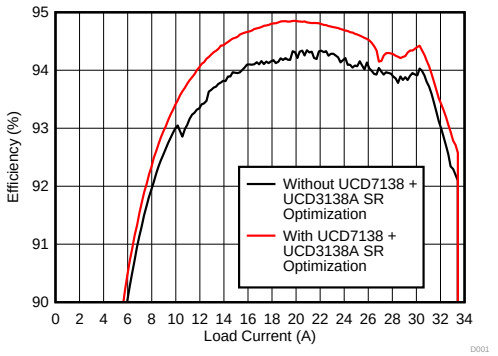
4 Simplified Schematic



Power Savings for a 340-W LLC Application



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCT PREVIEW Information. Product in design phase of development. Subject to change or discontinuance without notice.

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• Released full version of data sheet	1

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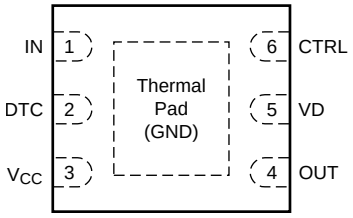
6 Pin Configuration and Functions

DRS Package
6-Pin WSON With Exposed Thermal Pad
Top View



Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	IN	I	**Input:** Gate driver input. This pin should be connected directly to the DPWM output of the digital controller.
2	DTC	O	**Body-diode conduction-time report:** Standard digital IO. Pulled high internally. Output low when the body diode is conducting. This pin should be connected to the DTC0 or DTC1 pin on UCD3138A.
3	V_{CC}	P	**IC supply:** External bias supply input. The supply range is 4.5-V to 18-V. A ceramic bypass capacitor of at least 1 µF should be placed as close as possible to the V_{CC} pin and the thermal pad. Where possible, use thick & wide Cu connections.
4	OUT	O	**Gate driver output:** Integrated push-pull gate driver for one or more external power MOSFETs. Typical 4-A source and 6-A sink capability. This is a rail-to-rail output, with the rails defined by the voltages on V_{CC} and GND. This pin should be connected to the gate terminal of the synchronous rectification MOSFET.
5	VD	I	**Drain voltage:** Connect this pin as close as possible to the controlled-MOSFET drain pad. This pin is internally connected to the diode conduction detection comparator. The comparator has a –0.15-V threshold to detect body-diode conduction. A 20-Ω resistor should be connected between the VD pin and MOSFET drain terminal to limit the current. The maximum voltage of the VD pin should not exceed 45 V. A simple external circuit can enable the usage of much higher voltages, see Figure 34.
6	CTRL	I	**Rising edge optimization control:** Connect this pin to ground to disable rising edge optimization. Leave this pin floating or connect it to logic high to enable rising edge optimization.
—	Thermal Pad (GND)	—	**Exposed thermal pad:** The exposed pad on the bottom of the package enhances the thermal performance of the device. This pad is the device ground reference.

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7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
Input voltage	V_{CC}	–0.3	20	V
	IN, CRTL	–0.3	3.8	
	VD	–1	45	
Maximum V_{CC} continuous input current	DC current		50	mA
Output current, peak (pulse)			6	A
Switching frequency, f_S			2000	kHz
Operating junction temperature, T_J		–40	125	°C
Lead temperature, soldering, 10 s, $T_{(SOL)}$			300	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS–001, all pins(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{CC}	V_{CC} input voltage from a low impedance source	4.5		18	V
V_{IN}	Input voltage	0		3.6	V
$C_{(BP)}$	V_{CC} bypass capacitor	1			µF
T_J	Operating junction temperature	–40		125	°C

7.4 Thermal Information

THERMAL METRIC(1)		UCD7138 DRS (WSON) 6 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	73.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	84.2	
$R_{\theta JB}$	Junction-to-board thermal resistance	46.3	
ψ_{JT}	Junction-to-top characterization parameter	2.6	
ψ_{JB}	Junction-to-board characterization parameter	46.4	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	12.4	

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

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7.5 Electrical Characteristics

At V_{CC} = 12 V_{DC}, –40°C < T_J = T_A < 125°C, 1µF capacitor from V_{CC} to GND, all voltages are with respect to ground and currents are positive into and negative out of the specified terminal, unless otherwise noted. Typical values are at T_J = 25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VCC BIAS SUPPLY						
$I_{CC(UV)}$	V_{CC} current, undervoltage	V_{CC} = 3.4 V		122	186	µA
$I_{CC(ON)}$	V_{CC} current, no switching	V_{CC} = 12 V		0.85	1.1	mA
$I_{CC(OPERATE)}$	V_{CC} current, normal operation (1)	V_{CC} = 12 V, $C_{(LOAD)}$ = 10 nF, f = 100 kHz		13	17	mA
GATE INPUT (IN)						
V_{IH}	Input signal high threshold		1.93	2.03	2.10	V
V_{IL}	Input signal low threshold		0.98	1.03	1.08	V
$V_{I(hys)}$	Input hysteresis		0.90	1.00		V
DTC OUTPUT						
$V_{OL(DTC)}$	Low level output voltage				0.25	V
$V_{OH(DTC)}$	High level output voltage		2.5			V
$I_{OH(DTC)}$	Output sinking current				4	mA
$I_{OL(DTC)}$	Output sourcing current		–4			mA
V_{DTC}	Maximum DTC pin output voltage			3.5	3.6	V
UNDERVOLTAGE LOCKOUT SECTION (UVLO)						
$V_{CC(ON)}$	V_{CC} turnon threshold		3.30	3.80	4.30	V
$V_{CC(OFF)}$	V_{CC} turnoff threshold		3.10	3.56	4.02	V
$V_{CC(hys)}$	UVLO hysteresis	$V_{CC(hys)}$ = $V_{CC(ON)}$ – $V_{CC(OFF)}$		0.24		V
COMPARATOR						
V_{TH}	Body diode conduction sensing threshold		–179	–147	–113	mV
$C_{I(VD–ground)}$	Differential input capacitance between VD and ground (1)	V_D = –150 mV		20		pF
GATE DRIVER						
V_{CC}-V_{OH}	Output high voltage	I_{OUT} = –10 mA		0.038	0.064	V
V_{OL}	Output low voltage	I_{OUT} = 10 mA		0.0025	0.009	V
$R_{(UP)}$	Pullup resistance	T_A = 25°C, I_{OUT} = –25 mA to –50 mA		5	6.1	Ω
		T_A = –40°C to 125°C, I_{OUT} = –50 mA		5	6.3	Ω
$R_{(DOWN)}$	Pulldown resistance	T_A = 25°C, I_{OUT} = 25 mA to 50 mA		0.31	0.44	Ω
		T_A = –40°C to 125°C, I_{OUT} = 50 mA		0.33	0.45	Ω
$I_{O(source)}$	Output peak current (source) (1)	$C_{(LOAD)}$ = 0.22 µF, f_S = 1 kHz, 5-V output		–4		A
$I_{O(sink)}$	Output peak current (sink) (1)	$C_{(LOAD)}$) = 0.22 µF, f_S = 1 kHz, 5-V output		6		A

(1) Ensured by Design, not tested in Production.

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7.6 Switching Characteristics

At V_{CC} = 12 V_{DC}, –40°C < T_J = T_A < 125°C, 1µF capacitor from V_{CC} to GND, all voltages are with respect to ground and currents are positive into and negative out of the specified terminal, unless otherwise noted. Typical values are at T_J = 25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_r	Rise time	$C_{(LOAD)}$ =1 nF, V_{CC} = 5 V, See Figure 1 and Figure 24		5	8	ns
		$C_{(LOAD)}$ =1 nF, V_{CC} = 12 V, See Figure 1 and Figure 24		4	8	ns
t_f	Fall time	$C_{(LOAD)}$=1 nF, V_{CC} = 5 V, See Figure 1 and Figure 24		3.36	5	ns
		$C_{(LOAD)}$=1 nF, V_{CC} = 12 V, See Figure 1 and Figure 24		3.5	5	ns
$t_{w(VD)}$	Minimum VD pulse duration (width) that changes the DTC output state	V_{CC} = 5 V		10	23	ns
		V_{CC} = 12 V		10	23	ns
$t_{w(IN)}$	Minimum IN duration (width) that changes OUT state	V_{CC} = 5 V		11	13	ns
		V_{CC} = 12 V		11	13	ns
$t_{d(1)}$	Gate driver turn on propagation delay	$C_{(LOAD)}$ = 1 nF, V_{IN} = 0 V to 3.3 V, V_{CC} = 5 V, V_{VD} = –0.5 V, See Figure 1 and Figure 24		14	26.6	ns
		$C_{(LOAD)}$ = 1 nF, V_{IN} = 0 V to 3.3 V, V_{CC} = 12 V, V_{VD} = –0.5 V, See Figure 1 and Figure 24		14	25	ns
$t_{d(2)}$	Gate driver turn off propagation delay	$C_{(LOAD)}$ = 1 nF, V_{IN} = 3.3 V to 0 V, V_{CC} = 5 V, See Figure 1 and Figure 24		14	22.9	ns
		$C_{(LOAD)}$ = 1 nF, V_{IN} = 3.3 V to 0 V, V_{CC} = 12 V, See Figure 1 and Figure 24		14	22	ns
$t_{d(COMP)}$	Body-diode conduction detection-comparator controlled-turnon propagation delay(1)	$C_{(LOAD)}$ = 1 nF, V_{IN} = 3.3 V, V_{CC} = 5 V, V_{VD} = 2 V to –0.5 V, See Figure 24		28	36	ns
		$C_{(LOAD)}$ = 1 nF, V_{IN} = 3.3 V, V_{CC} = 12 V, V_{VD} = 2 V to –0.5 V, See Figure 24		26	33	ns
$t_{d(DTC)}$	DTC output propagation delay	V_{CC} = 5 V		21	27	ns
		V_{CC} = 12 V		18	25	ns

(1) For details about the operation, see the *Gate Turnon and Turnoff* section.

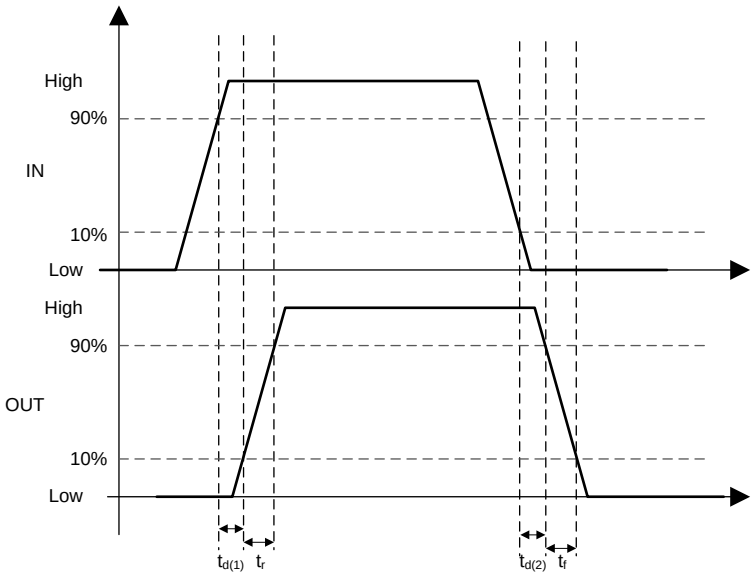

Figure 1. Input Driver Operation

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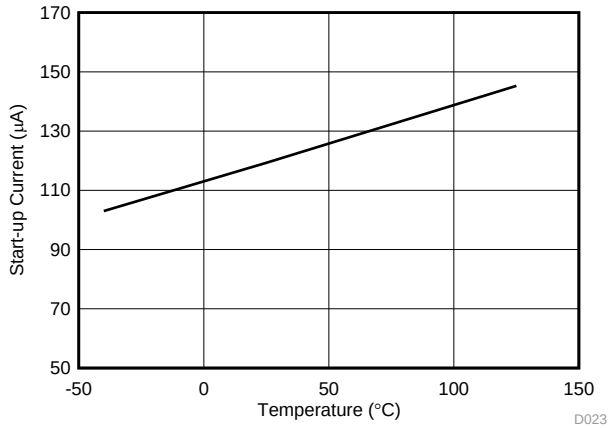
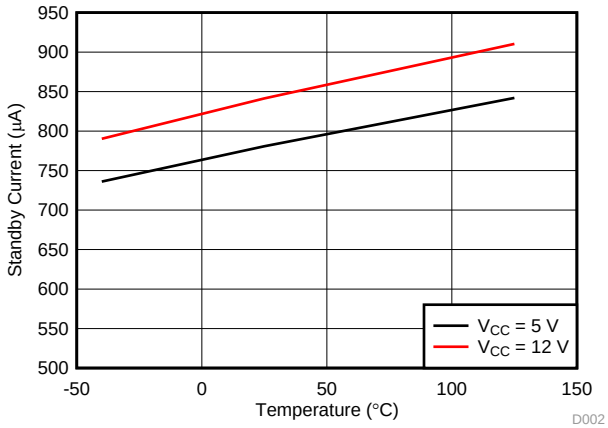
7.7 Typical Characteristics



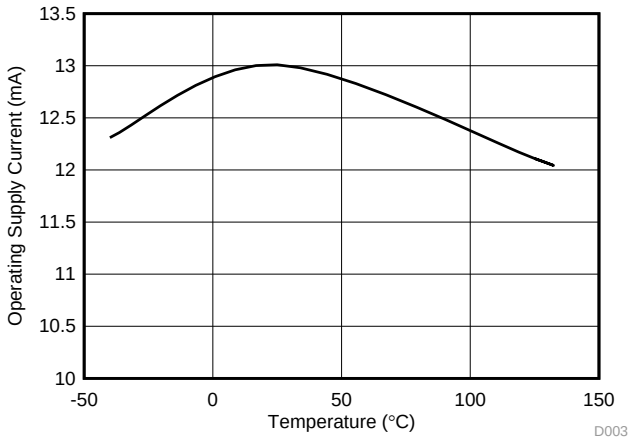
V_{CC} = 3.4 V

Figure 2. Start-Up Current ($I_{CC(UV)}$) vs Temperature



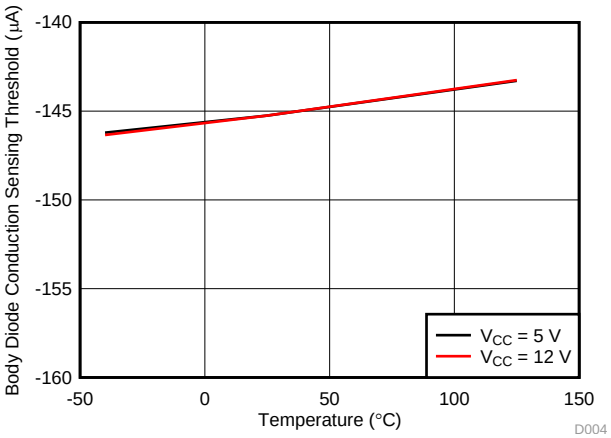
No switching

Figure 3. Standby Current ($I_{CC(ON)}$)vs Temperature



V_{CC} = 12 V $C_{(LOAD)}$ = 10 nF f = 100 kHz

Figure 4. Operating Supply current ($I_{CC(OPERATE)}$) vs Temperature



V_{CC} = 12 V

Figure 5. Body-Diode Conduction Sensing Threshold (V_{TH}) vs Temperature

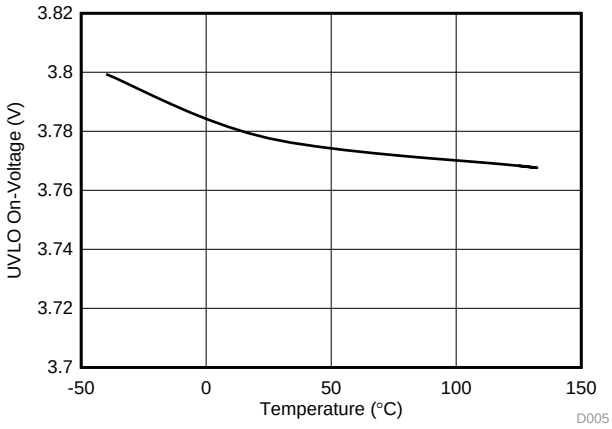


Figure 6. UVLO On-Voltage ($V_{CC(ON)}$)vs Temperature

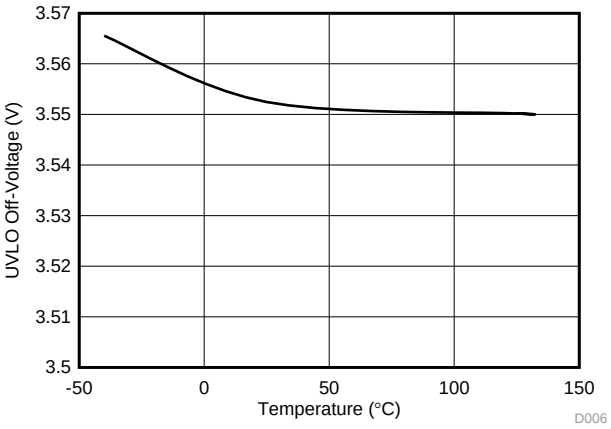


Figure 7. UVLO OFF-Voltage ($V_{CC(OFF)}$) vs Temperature

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Typical Characteristics (continued)

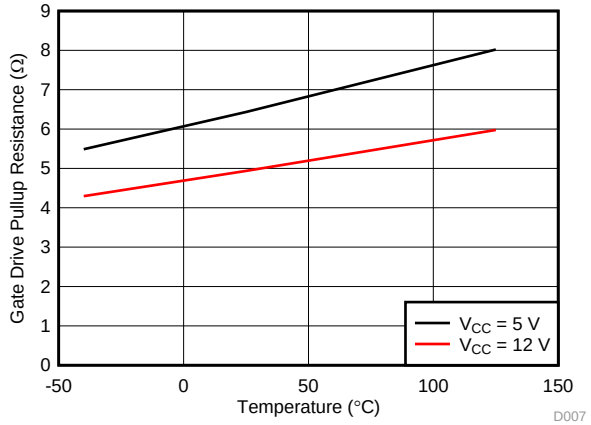

Figure 8. Gate-Driver Pullup Resistance ($R_{(UP)}$) vs Temperature

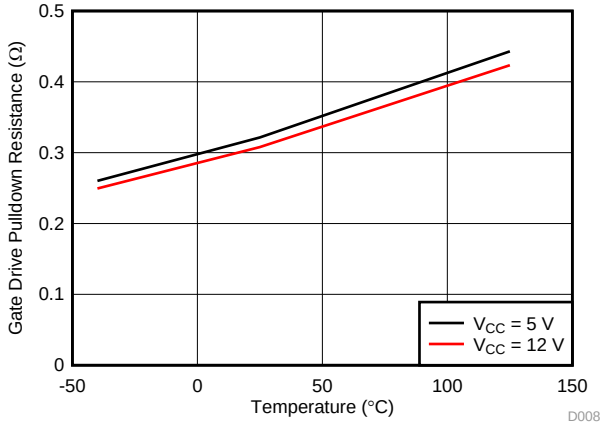

Figure 9. Gate-Driver Pulldown Resistance ($R_{(DOWN)}$) vs Temperature

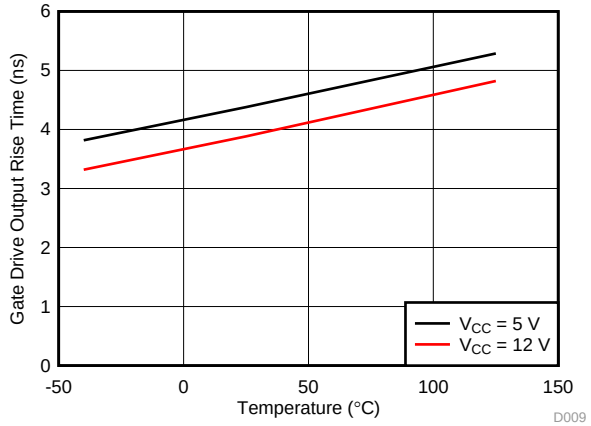

Figure 10. Gate-Drive Output Rise Time (t_r) vs Temperature

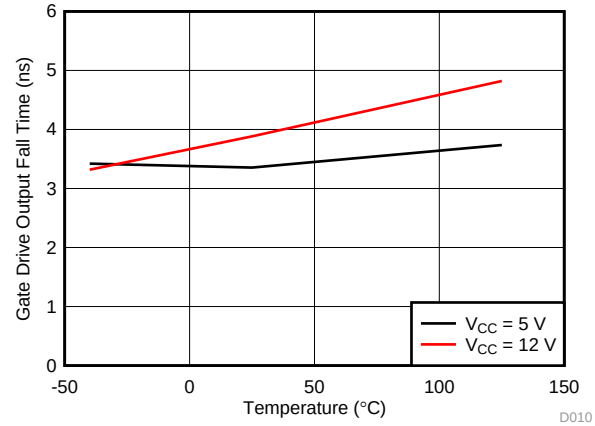

Figure 11. Gate-Drive Output Rise Time (t_f) vs Temperature

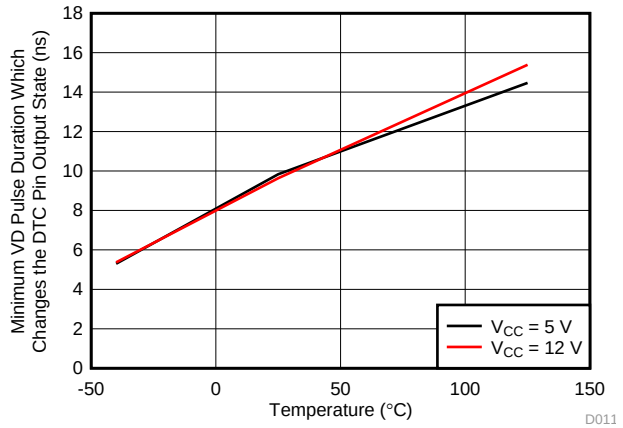

Figure 12. Minimum VD Pulse Duration Which Changes the DTC Pin Output State ($t_{w(VD)}$) vs Temperature

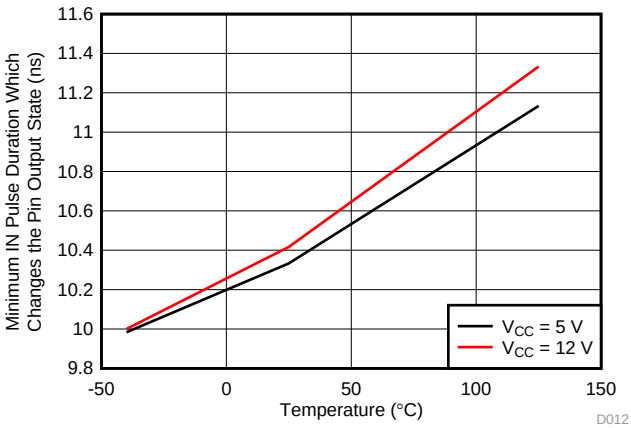

Figure 13. Minimum IN Pulse Duration Which Changes the Pin Output State ($t_{w(IN)}$) vs Temperature

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Typical Characteristics (continued)

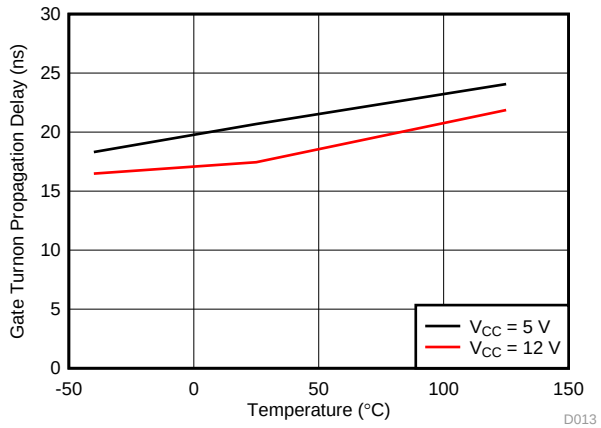

Figure 14. Gate Turnon Propagation Delay ($t_{d(1)}$) vs Temperature

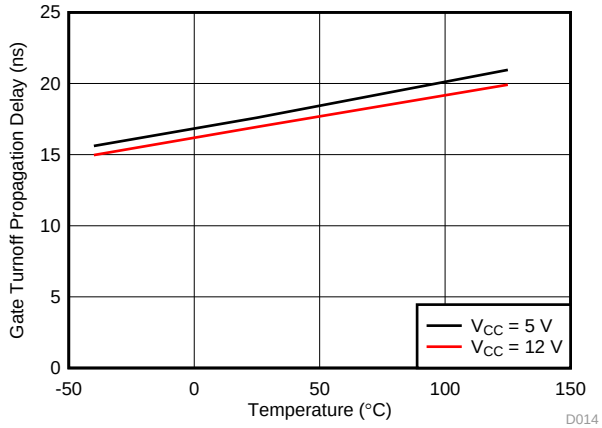

Figure 15. Gate Turnoff Propagation Delay ($t_{d(2)}$) vs Temperature

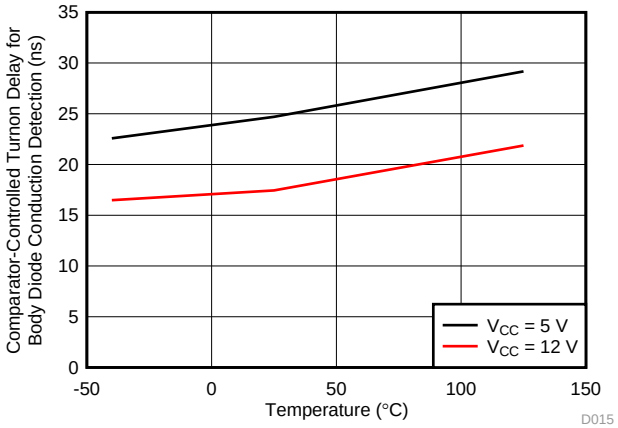

Figure 16. Comparator-Controlled Turnon Delay for Body-Diode Conduction Detection ($t_{d(COMP)}$) vs Temperature

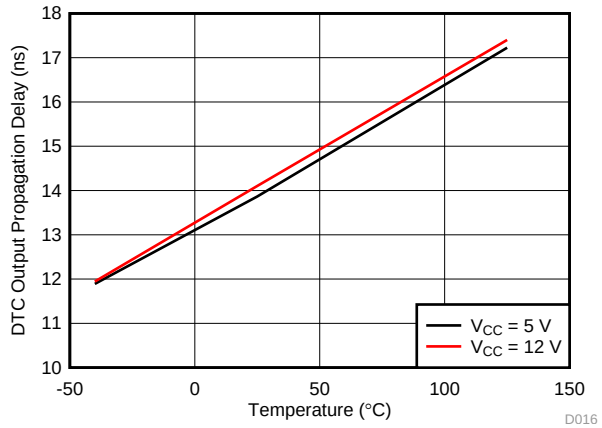

Figure 17. DTC Output Propagation Delay ($t_{d(DTC)}$) vs Temperature

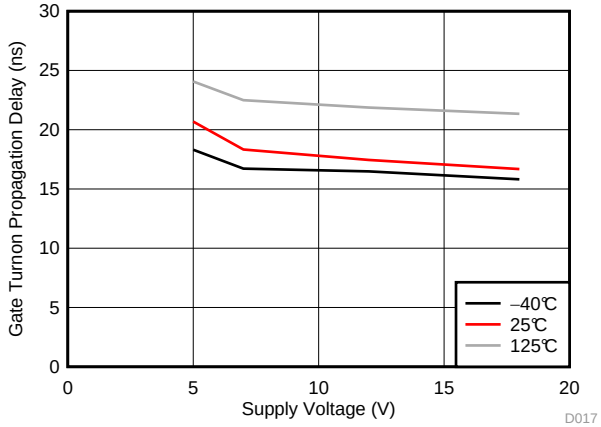

Figure 18. Gate Turnon Propagation Delay ($t_{d(1)}$) vs Supply Voltage (V_{CC})

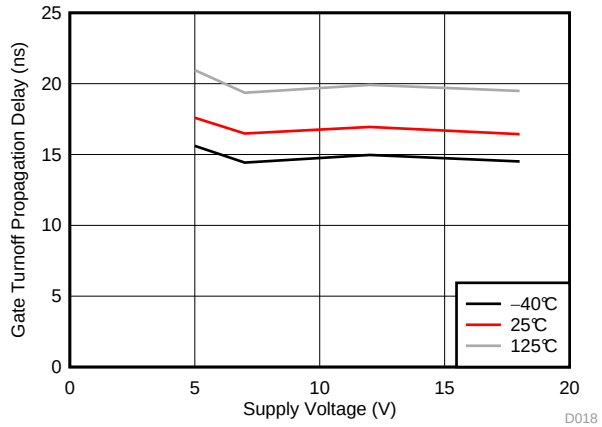

Figure 19. Gate Turnoff Propagation Delay ($t_{d(2)}$) vs Supply Voltage (V_{CC})

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Typical Characteristics (continued)

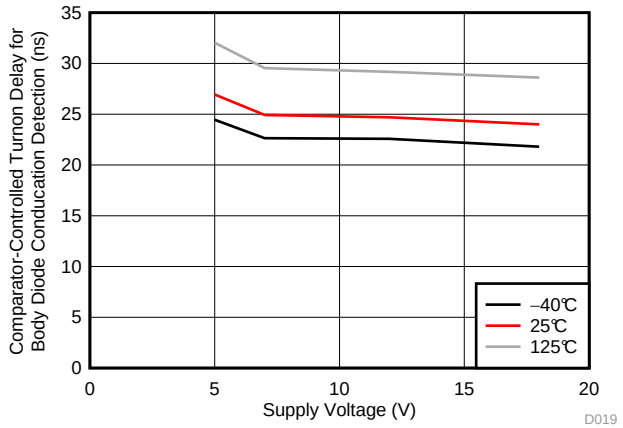

Figure 20. Comparator-Controlled Turnon Delay for Body-Diode Conduction Detection ($t_{d(COMP)}$) vs Supply Voltage (V_{CC})

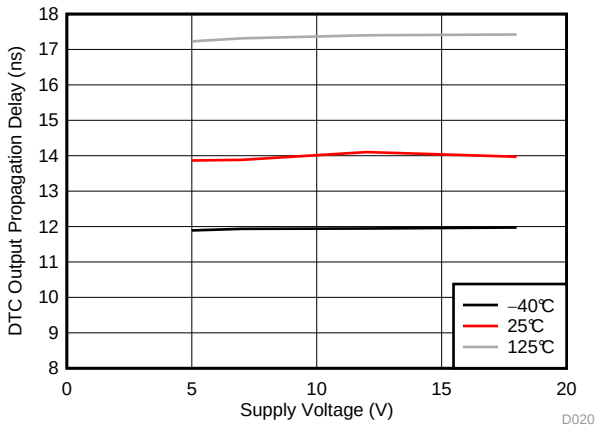

Figure 21. DTC Output Propagation Delay ($t_{d(DTC)}$) vs Supply Voltage (V_{CC})

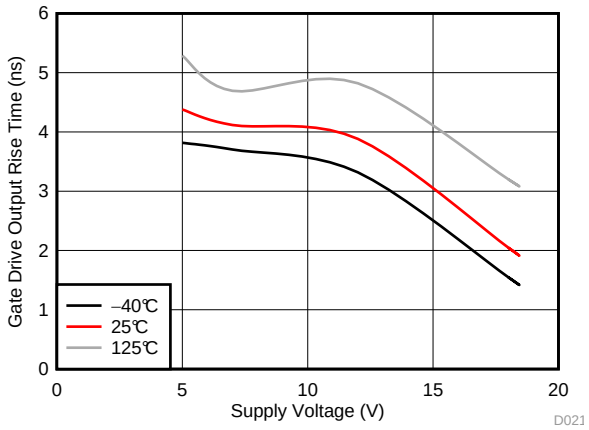

Figure 22. Gate-Drive Output Rise Time (t_r) vs Supply Voltage (V_{CC})

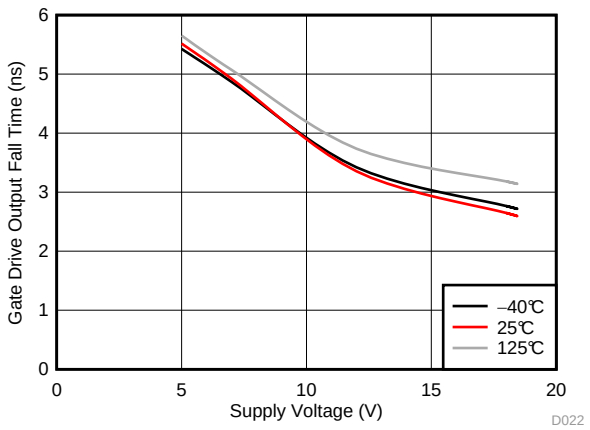

Figure 23. Gate-Drive Output Fall time (t_f) vs Supply Voltage (V_{CC})

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8 Detailed Description

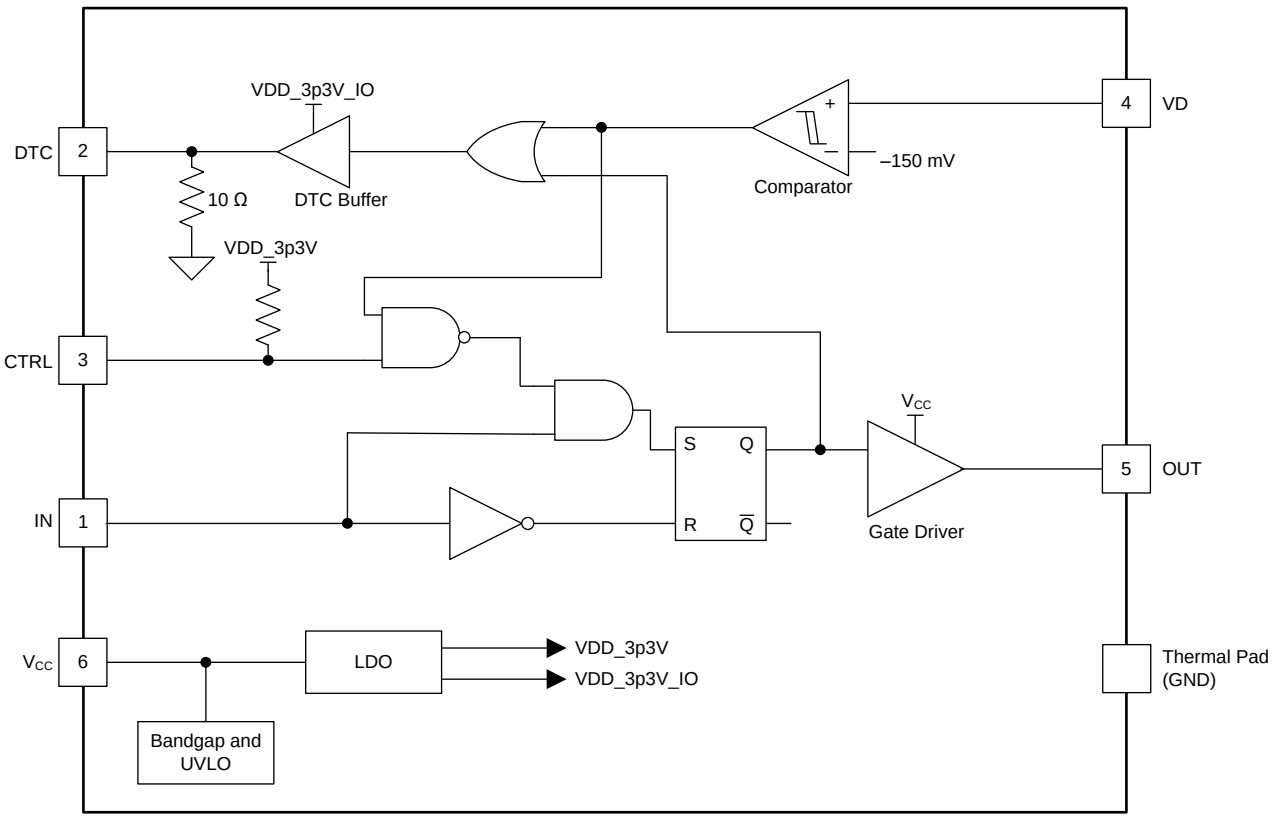
8.1 Overview

The UCD7138 low-side gate driver is a high-performance driver for secondary-side synchronous rectification with body-diode conduction sensing. The device is suitable for high-power high-efficiency isolated converter applications where dead-time optimization is desired. The body-diode conduction is sensed at the falling edge of the gate-drive signal and sent to the UCD3138A digital-power controller through one digital IO pin. The digital controller can adjust the dead-time setting based on this information. The body-diode conduction time is detected in a certain time window in the UCD3138A digital controller. This detection prevents reporting erroneous signals because of noise or reverse current. At the gate turnon edge, the UCD7138 gate driver optimizes the dead time by turning the gate on as soon as diode conduction is detected. The benefits of this driver to the system include, but are not limited to, improved efficiency, improved reliability, and ease of design.

The internal gate driver is a single-channel, high-speed gate driver suitable for both 12-V and 5-V drive. The gate driver offers 4-A source and 6-A sink (asymmetrical drive) peak drive current capability. The package and pin configuration provide minimum parasitic inductances to reduce rise and fall times and to limit ringing. Additionally, the short propagation delay with minimized tolerances and variations allows efficient operation at high frequencies. The 5-Ω and 0.35-Ω pull-up and pull-down resistances boost immunity to hard switching with high slew-rate dV and dt.

The internal body-diode conduction detector is a high-speed comparator with 20-ns propagation delay. The DTC output is internally pulled high by default. When body-diode conduction is sensed, DTC pin drives low.

8.2 Functional Block Diagram



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8.3 Feature Description

8.3.1 Body-Diode Conduction Detection

In Figure 24, V_{DS} is the drain-to-source voltage which is connected to the VD pin. The IN pin is the gate-driver input-command signal from the UCD3138A digital controller. The DTC pin is the sensed body-diode conduction. The OUT pin is the gate-driver output. The body-diode conduction detection comparator has a –150-mV threshold. When the body diode conducts, the DTC pin is low. If the body diode does not conduct, the DTC pin is high.

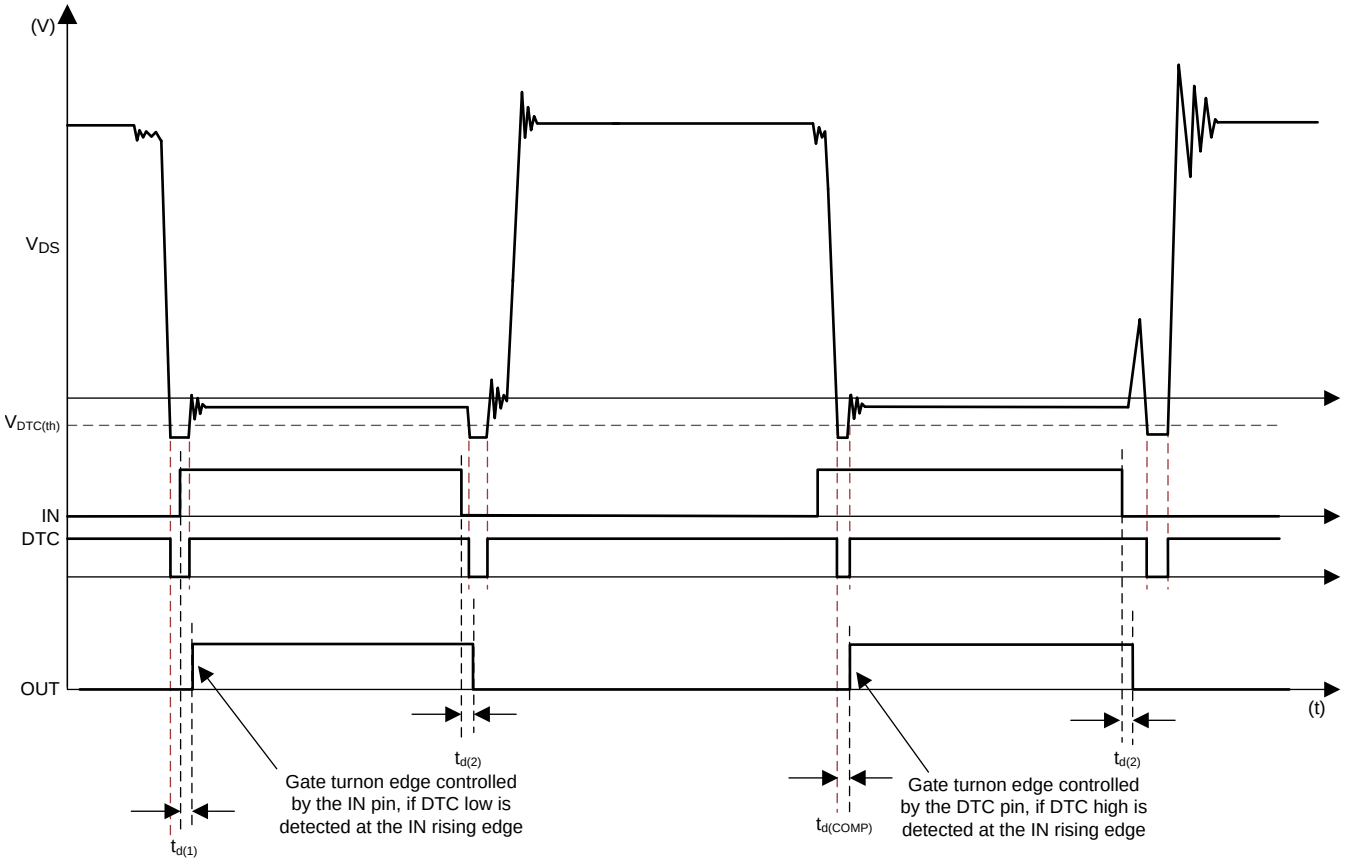

Figure 24. Input-Output Timing Diagram (Turn-On Optimization is Enabled)

To improve noise immunity, the comparator output DTC is blanked when the gate driver output, OUT, is high. The DTC signal always outputs high when OUT is high.

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Feature Description (continued)

8.3.2 Gate Turnon and Turnoff

Gate turnon is controlled by both the gate driver input, IN, and body-diode conduction. System robustness is enhanced through internal logic that guarantees that OUT is only allowed high if IN is also high. At the IN rising edge, the UCD7138 gate-driver analyzes the DTC signal and determines the required course of action. The OUT pin is sent high immediately if the DTC comparator output is low at the rising edge of the IN signal. If the DTC pin is high at the rising edge of the IN signal, OUT is held low until DTC goes low. To allow the gate turnon edge to optimize freely, setting the dead time between the primary side falling edge and the IN rising edge smaller than expected in the UCD3138A digital controller is recommended.

The gate turnoff edge is determined by the IN signal only. The gate is turned off immediately at the IN falling edge.

Table 1. Truth Table for CTRL Pin Function

CTRL PIN CONFIGURATION	FUNCTION
0 V or ground	Turn-on optimization disabled
3.3 V or floating	Turn-on optimization enabled

8.3.3 V_{CC} and Undervoltage Lockout

The UCD7138 device has an internal undervoltage-lockout (UVLO) protection feature based on the V_{CC}-pin voltage. Whenever the driver is in the UVLO condition (such as when the V_{CC} voltage is less than $V_{CC(ON)}$ during power up or when the V_{CC} voltage is less than $V_{CC(OFF)}$ during power down), the device holds all outputs low, regardless of the status of the inputs. The UVLO voltage is typically 3.8 V with a 240-mV hysteresis. This hysteresis helps prevent chatter when low V_{CC} supply voltages have noise from the power supply and also when droops occur in the V_{CC} bias voltage.

For example, at power up, the UCD7138 driver output remains low until the V_{CC} voltage reaches the UVLO threshold. The magnitude of the OUT signal rises with V_{CC} until steady-state V_{CC} is reached. The output remains low until the UVLO threshold is reached. The DTC signal begins to rise when V_{CC} begins to rise. The internal diode conduction detection comparator remains inactive until V_{CC} passes $V_{CC(ON)}$ threshold.

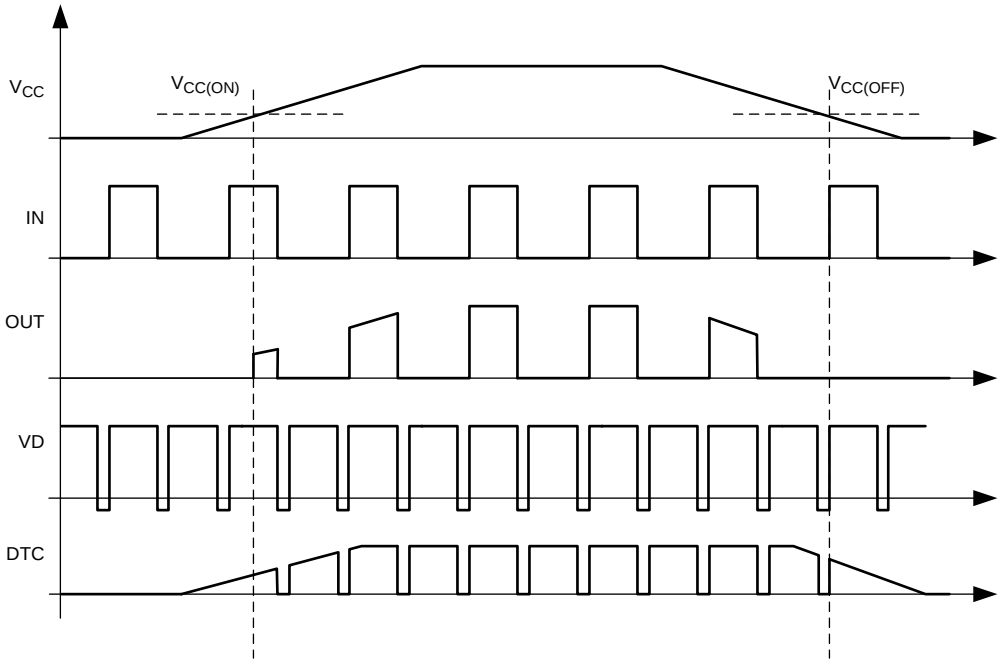

Figure 25. Device Power Up and Power Down

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8.3.4 Operating Supply Current

The UCD7138 device features very-low quiescent supply current. The total supply current is the sum of the quiescent supply current, the average I_{OUT} current from switching, and any current related to pull-up resistors on the unused input pin. Knowing the operating frequency (f_S) and the MOSFET gate (Q_G) charge, the average I_{OUT} current can be calculated as product of Q_G and f_S.

8.3.5 Driver Stage

The input pins of the UCD7138 device are based on a CMOS-compatible input-threshold logic that is independent of the V_{CC} supply voltage. The logic-level thresholds can be conveniently driven with PWM control signals derived from 3.3-V.

The output stage of the UCD7138 device features a unique architecture on the pull-up structure. This architecture delivers the highest peak-source current when needed during the Miller-plateau region of the power switch turnon transition (when the power switch drain or collector voltage experiences dV/dt). The output stage pull-up structure features a P-Channel MOSFET and an additional N-Channel MOSFET in parallel. The function of the N-Channel MOSFET is to provide a brief boost in the peak sourcing current to enable fast turnon. This boost occurs by briefly turning on the N-Channel MOSFET when the output is changing state from LOW to HIGH.

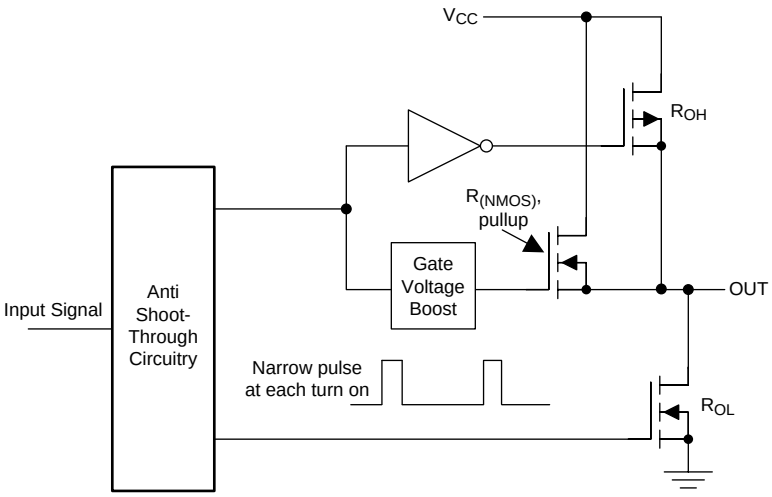

Figure 26. Gate-Driver Output Structure

8.4 Device Functional Modes

8.4.1 UVLO Mode

When the V_{CC} voltage to the device has not reached the $V_{CC(ON)}$ threshold or has fallen below the UVLO threshold, $V_{CC(OFF)}$, the device operates in the low-power UVLO mode. In this mode, most internal functions are disabled and the I_{CC} current is very low. In UVLO mode, the OUT pin is held low. The device passes out of UVLO mode when the V_{CC} voltage increases above the $V_{CC(ON)}$ threshold.

8.4.2 Normal Operation Mode

In this mode, the I_{CC} current is higher because all internal control and timing functions are operating and the gate-driver output, OUT, is driving the controlled MOSFET for synchronous rectification. In this mode, the V_{CC} current is the sum of $I_{CC(ON)}$ plus the average current required to drive the load on the OUT pin.

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9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The UCD7138 device can be used in a wide range of applications. The device can be used on many center-tapped secondary-side rectification topologies. Specifically, the device can be used in half-bridge LLC converters. In these applications, the UCD3138A and UCD7138 chipset enables the synchronous rectifiers to closely approximate the behavior of an ideal diode which is difficult to do in an LLC converter because of the variations in the SR current-conduction time.

The UCD7138 and UCD3138A chipset together can provide an easy-to-use, high-performance and advanced SR-control solution. Without this solution, fine tuning is required for each operation region (including below resonant frequency, at resonant frequency, and above resonant frequency). For LLC converters in production, each power stage may have a different resonant frequency because of tolerances of circuit capacitors and inductors. Calibration is required for each converter to achieve high efficiency. With UCD7138 and UCD3138A advanced SR control, optimal SR operation is easily achieved for every converter without fine tuning and calibration of the resonant tank can be eliminated in production. For more information see *Using UCD7138 and UCD3138A for Advanced Synchronous Rectification Control*, SLUA737.

9.2 Typical Application

9.2.1 Half-Bridge LLC

Figure 27 shows a typical half-bridge LLC application using the UCD7138 device as a secondary-side SR driver and the UCD3138A device as a controller.

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Typical Application (continued)

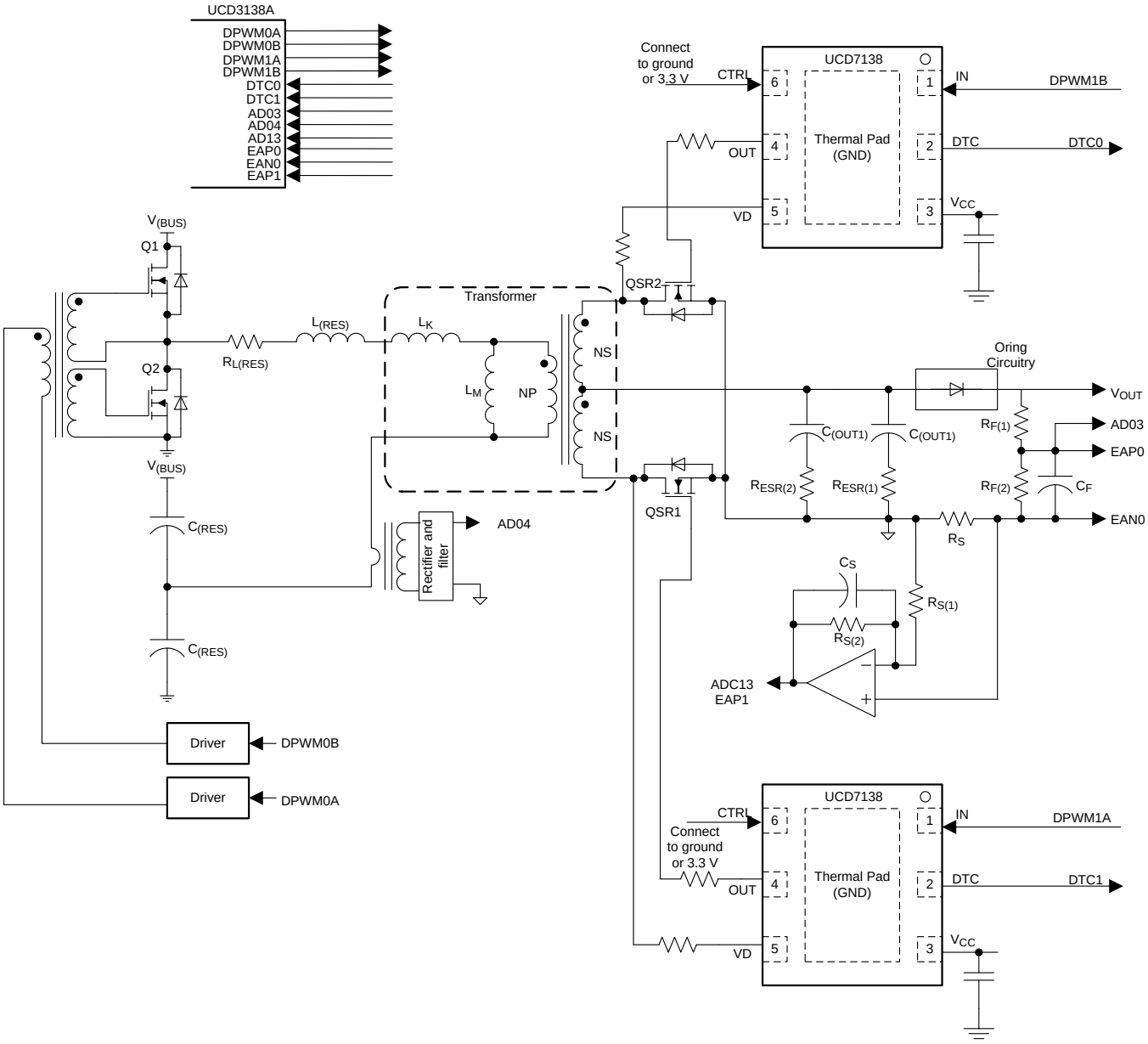

Figure 27. Half-Bridge LLC Typical Application Diagram

In LLC converters, if the SRs are not well optimized, the SR conduction time can either be too long or too short. The duration of the body diode conduction time can be determined by examining the drain-to-source voltage of the MOSFET when it is off. The SR turnon edge is optimized by the UCD7138 device by turning the gate on as soon as body-diode conduction is sensed. The SR turnoff edge is determined when the UCD3138A digital controller analyzes the sensed body-diode conduction time. Figure 28 shows the typical drain-to-source waveforms on a half-bridge LLC converter and the desired waveforms.

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Typical Application (continued)

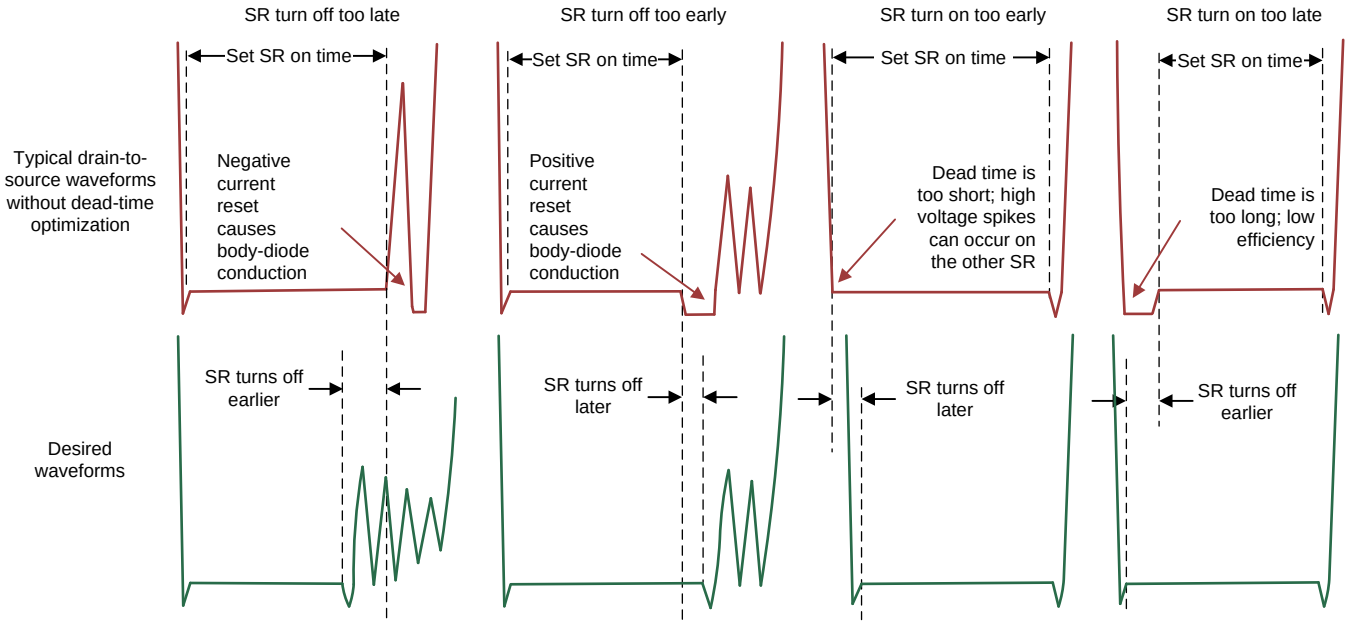

Figure 28. Drain to Source Voltage Waveforms in a Typical Half Bridge LLC Application and Desired Waveforms

As shown in Figure 29, when the SR pulse is on for too long, the drain-to-source voltage shoots up. The upper waveform in Figure 29 shows the SR current. The lower waveform shows the SR drain-to-source voltage. The black segment of the curves show when the SR MOSFET is on. The red and green segments of the curves show when the SR MOSFET is off. The SR current is positive at first, but continues to drop until it is negative. The drain-to-source voltage is close to 0 V when the SR MOSFET is on. As soon as the SR MOSFET is turned off, the negative current must reset. The capacitance across the drain and source terminal is charged, and the drain-to-source voltage increases. The green segments of the curves show when the negative current reset process is complete at which point the body diode of the MOSFET conducts briefly again.

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Typical Application (continued)

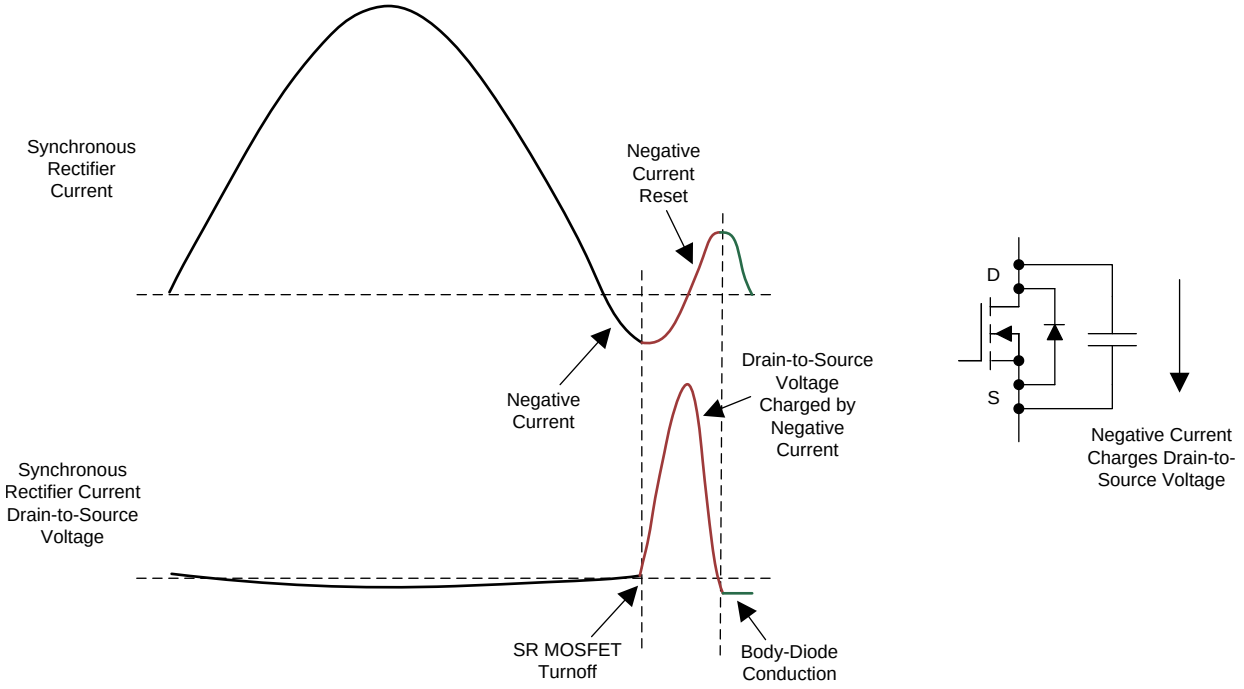

Figure 29. SR Drain-to-Source Voltage Shoot Up When No Negative Current Flow Occurs

For the UCD3138A device, a DTC detection window is generated at the falling edge of the gate drive command IN signal. Only during this detection window is the DTC low time counted by a 4-ns resolution timer capture inside the UCD3138A device. Figure 30 shows the simplified system block diagram. In the two body-diode conduction cases shown in Figure 31, the SR on time should be adjusted in different directions. The detection window identify that these two cases are different. If, during the detection window, a large amount of DTC low time is detected, and the SR turns off too early. If, during the detection window, no or very-short DTC low time is detected and the SR turns off too late.

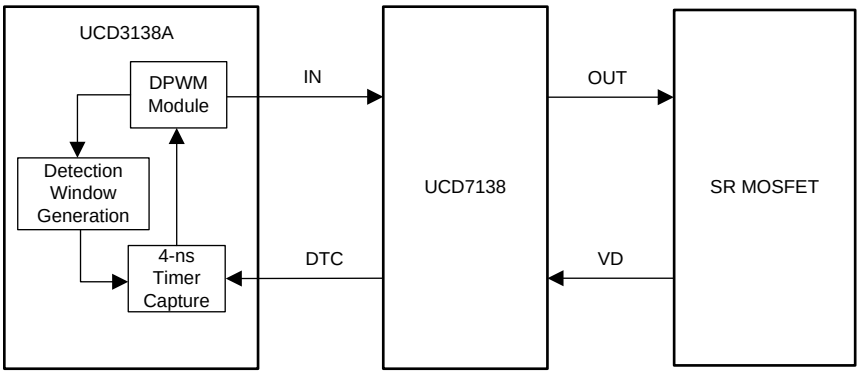

Figure 30. Simplified System Block Diagram

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Typical Application (continued)

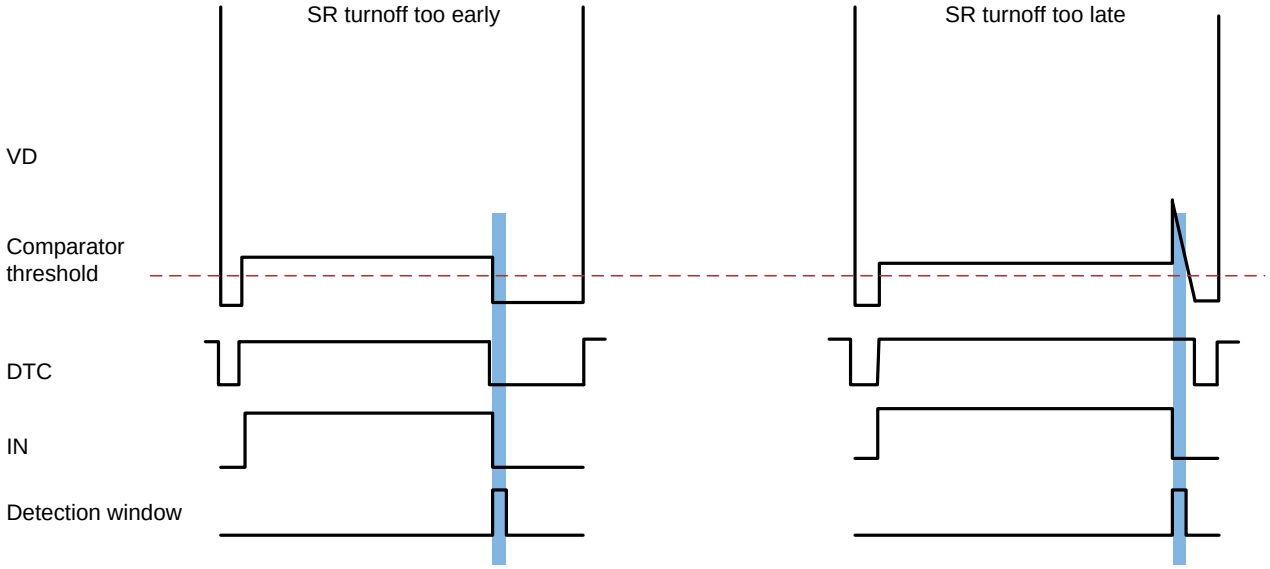

Figure 31. Body-Diode Connection Detection

The UCD3138A digital controller counts the body-diode conduction time of the current cycle and adjusts the SR on time of the next cycle. In Figure 32, the DTC0 and DTC1 signals are the body-diode conduction inputs received from the UCD7138 device. SR0_DPWM and SR1_DPWM are the DPWM waveforms for the SRs. The red and green dashed lines are moving edges controlled by both the UCD3138A digital-compensator output and the DTC interface. In each cycle, directly after the falling edge of the SR DPWM waveform, a detection window is generated for the body-diode conduction time. The detection window is defined by both DETECT_BLANK and DETECT_LEN registers. During this detection window, a 4-ns timer capture counts the conduction time of the body diode. The SR DPWM turnoff edge of the next cycle is then adjusted accordingly.

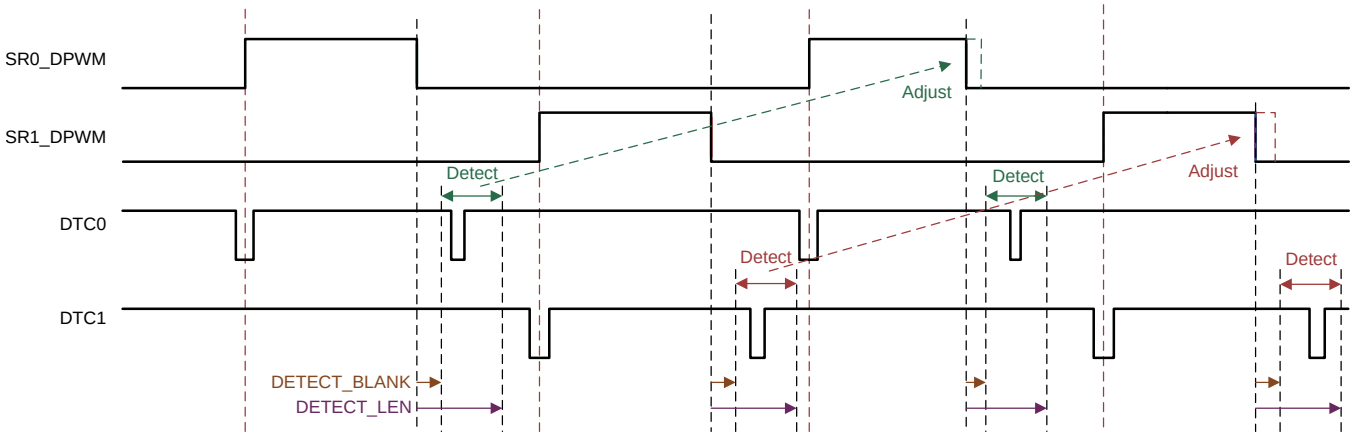

Figure 32. Timing Diagram of the DTC Interface in UCD3138A

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Typical Application (continued)

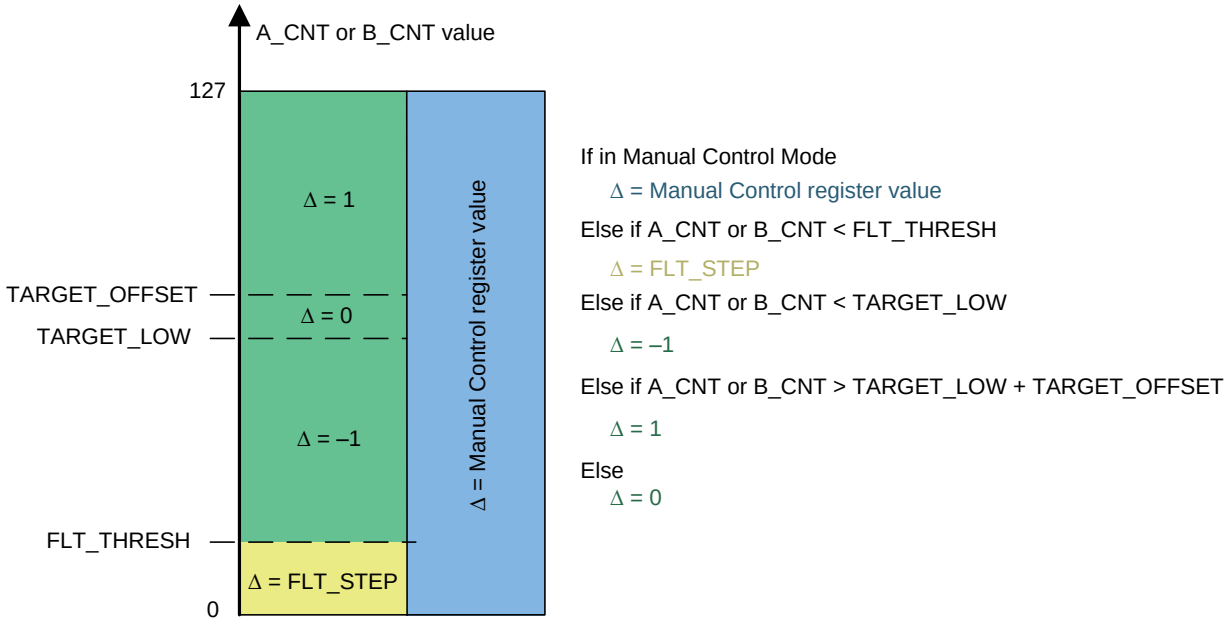

Figure 33. DTC Interface Principle

Figure 33 shows how the SR turnoff edge is adjusted based on the DTC measurement of the previous cycle. The A_CNT or B_CNT is the counted values of diode conduction time of two SRs which ranges from 0 to 127. The two types of SR control modes are automatic-control mode and manual-control mode. If manual-control mode is used, the SR on-time adjustment value is determined by the manual write register. If automatic-control mode is used, the UCD3138A digital controller automatically calculates the SR on-time adjustment amount for the next cycle. The body-diode conduction time at the falling edge of the SR gate is regulated to a target value by step-by-step edge adjustment in the UCD3138A device. The SR on time is reduced by a preprogrammed large amount, when the sensed body-diode conduction time is less than a programmable threshold. This reduction prevents the power supply from damaged caused by negative current in the SRs.

For more information on the DTC interface on UCD3138A see *UCD7138 and UCD3138A for Advanced Synchronous Rectification Control*, SLAU737 and *UCD3138A Highly Integrated Digital Controller for Isolated Power*, SLUSC66.

9.2.1.1 Design Requirements

9.2.1.1.1 Gate Input

The input stage of the driver should be driven by a signal with fast rise and fall times. Caution must be exercised whenever the driver is used with slowly varying input signals, in situations where the device is located in a mechanical socket or PCB layout is not optimal (bad grounding, for example). Ground bounce is often caused by high di/dt current from the driver output, coupled with board-layout parasitic. The differential voltage between the input pin IN and ground pad GND may be modified by ground bounce and trigger an unintended change of output state. Because of short propagation delay, the unintended change of state can ultimately result in high-frequency oscillations, which increases power dissipation and can potentially damage the device. In the worst case, when a slow input signal is used and PCB layout is not optimal, adding a small capacitor (1 nF) between the input pin and ground very close to the driver device may be necessary.

9.2.1.1.2 Gate Output

The output of the gate driver (OUT) must be connected as close to the MOSFET gate as possible. A small resistor may be connected in between to reduce the high-frequency oscillations on the gate. Doing so can also slow down the gate transitions. The DTC detection windows inside UCD3138A may need some adjustment to compensate for the delay caused by the added resistor.

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Typical Application (continued)

9.2.1.1.3 Drain-to-Source Voltage Sensing

When the drain-to-source voltage is below 0 V, current flows out of the VD pin to the drain terminal of the MOSFET. This current flow must be limited to ensure proper operation of the device. The recommended current-limiting resistance value is 20Ω.

The highest voltage that can be applied to VD pin is 45 V which is good for applications where 40-V MOSFETs are used for the secondary-side SRs. If a higher voltage is required for VD pin, an external high-voltage blocking circuit can be used together with the UCD7138 device as shown in Figure 34. Depending on the required voltage rating, a different external high-voltage blocking MOSFET can be selected. Usually a small SOT-23 MOSFET can be used. In this circuit, the gate terminal of the external high-voltage blocking MOSFET is connected to V_{CC} of the UCD7138 gate driver. The source terminal is connected with a current-limiting resistor to the VD pin of the UCD7138 device. The drain terminal is connected to the SR MOSFET drain terminal. When a low voltage is presented at the drain terminal, the blocking MOSFET is turned on because of the positive gate-to-source voltage. When the drain voltage becomes higher and higher, the source terminal voltage rises along with the drain terminal until the gate-to-source voltage falls below the threshold. When the source voltage is high enough so that the blocking MOSFET is turned off, the high voltage on the SR drain is blocked.

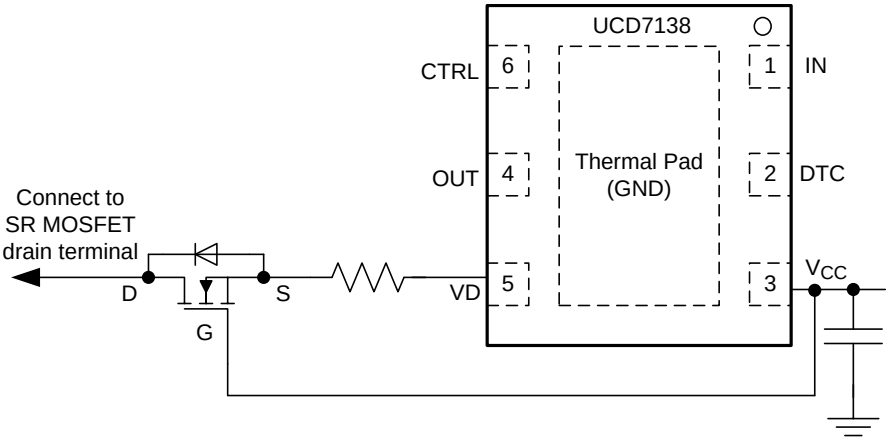

Figure 34. External High-Voltage Blocking Circuit

9.2.1.1.4 DTC Output

The DTC pin is the internal comparator output. This pin should be connected to the DTC0 or DTC1 pin on the UCD3138A device. To keep edges sharp, no filtering is recommended. If noise spikes are observed on the DTC signal, the blanking times in the UCD3138A device can be used to prevent the digital controller from sensing noise. This pin is not designed to drive large current. If filtering must be used, ensure that the sink and source current on this pin is within ±4 mA as specified in the
Electrical Characteristics table.

9.2.1.1.5 Turn-on Edge Optimization

The turnon edge optimization is useful when a positive current flow is at the rising edge of SRs. To maximize the efficiency gain, the dead time between the falling edge of the primary and the rising edge of the secondary should be programmed to a smaller value than expected, so that the rising edge of the SRs can move freely by UCD7138.

9.2.1.2 Detailed Design Procedure

9.2.1.2.1 Design Without SR-Control Optimization

The design procedure of an LLC converter with synchronous rectification can be greatly simplified by using the UCD7138 and UCD3138A chipset. The converter hardware and firmware can initially be designed without advanced SR optimization and then add SR optimization function in.

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Typical Application (continued)

For more information on the UCD3138A-based digital LLC converter, *UCD3138A Highly Integrated Digital Controller for Isolated Power*, SLUSC66.

9.2.1.2.2 Setting the DTC Detection Window

The body-diode conduction should be detected in a specific region for the system to operate correctly. The detection window is defined by a blanking time register DETECT_BLANK and a detection length register DETECT_LEN in the UCD3138A device. To set the detection window, let the LLC converter operate below resonant frequency. measure the VD, IN, and DTC waveforms on an oscilloscope. Use cursors to measure the time, t, difference between the IN falling edge and the starting point of body-diode conduction (first falling edge of DTC excluding noise spike). The blanking time should be set to be less than t. Usually the required blanking time is very short or non existent, so the blanking time can be set to around 10% of t. The detection window length can be set to a few times of the desired body-diode conduction time. For example, if the desired body-diode conduction time is 40 ns, the detection window length can be set to 120 ns. Make sure that the body-diode conduction is well covered inside the detection window when it is at an optimal value. The end point of the detection window should never exceed the first valley on the VD waveform to avoid errors in measurement (see Figure 35).

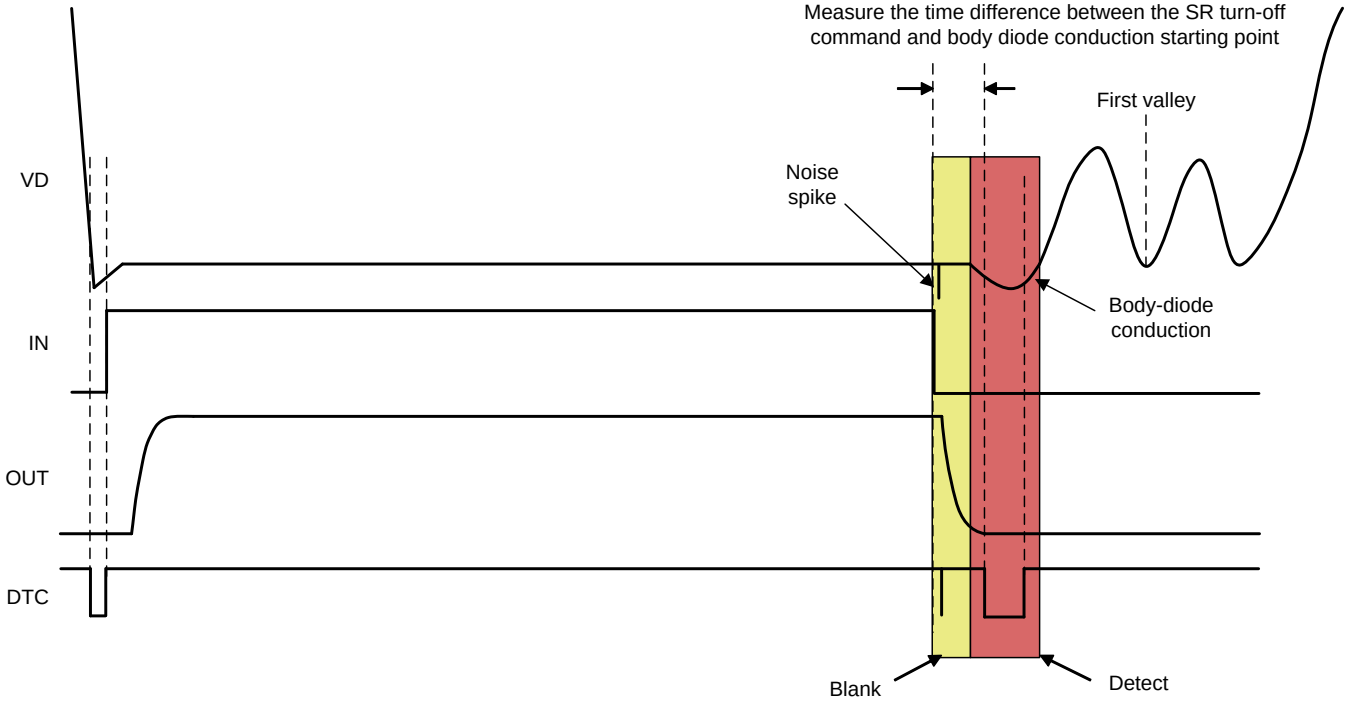

Figure 35. Setting the DTC Detection Window in UCD3138A

After the detection window is set, enable the DTC module in manual control mode. Set the offset in the manual control registers to 0. Change the input voltage and load current to different operation points to verify that the UCD3138A DTC module measures the correct values in the A_CNT and B_CNT registers. See the *UCD3138A64 Programmer's Manual*, SLUUB54 for detailed register information.

9.2.1.2.3 Setting the Clamps

The SR adjustment accumulator clamps defines the maximum SR turnoff edge offset from the calculated value from the UCD3138A compensator. The maximum clamp can be set to prevent the SR on time from going too long and causing shoot through. The minimum clamp can be set based on the light load condition where the desired SR turnoff edge offset is the maximum.

In addition to the SR adjustment accumulator clamps, the SR pulse falling edge is naturally clamped at 50% or 100% or the switching period in UCD3138A. This natural clamp is a default feature of UCD3138A and does not require any special setting.

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Typical Application (continued)

9.2.1.2.4 Setting the DTC Optimization Target and Hysteresis

The body diode must maintain a minimum conduction time for the UCD3138A DTC interface to function properly. The minimum body-diode conduction time is set by the DTC target and target register. A target hysteresis register can also be set to reduce the steady-state output-voltage ripple.

9.2.1.2.5 Setting the DTC Negative Current Fault Protection

If the detected body-diode conduction time is less than the programmed threshold, negative current can occur. This threshold can be set by the fault threshold register in the UCD3138A DTC module. If a DTC fault is detected, the SR on time is reduced by a programed step size in the next switching cycle. This step size is defined by FLT_STEP register in the DTC module. To avoid noise and jitter in the negative current fault detection, a consecutive DTC fault counter can be used. A fault step is executed only after a consecutive number of faults are detected.

After all these registers are set, enable the UCD3138A DTC module in automatic control mode, enable the turnon-edge optimization on the UCD7138 device, and review the different operation conditions to see the overall system performance. The DTC module can be turned on or off by toggling DTC_EN bit in Loop Mux register in UCD3138A. The performance before and after SR optimization control can be compared very easily as shown in the *Application Curves* section.

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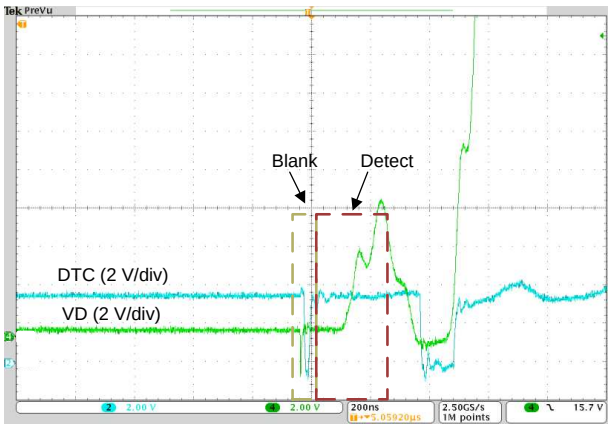
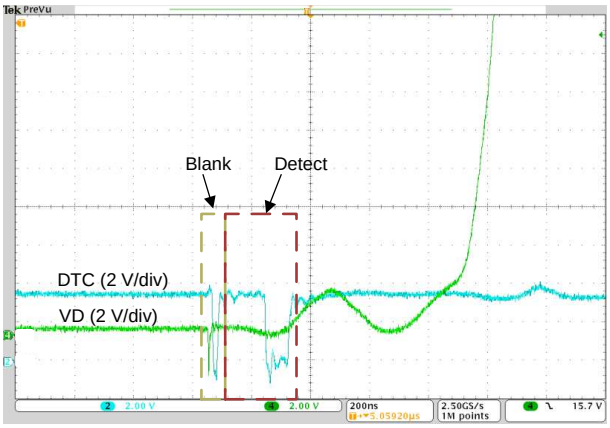
Typical Application (continued)

9.2.1.3 Application Curves



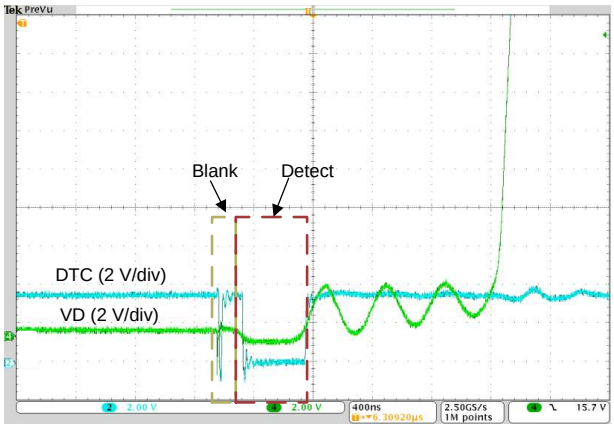
No optimization, SR on time too long.
High V_{DS} stress on the other SR.
Horizontal: 200 ns/div

Figure 36. SR Turnoff Edge Before Optimization



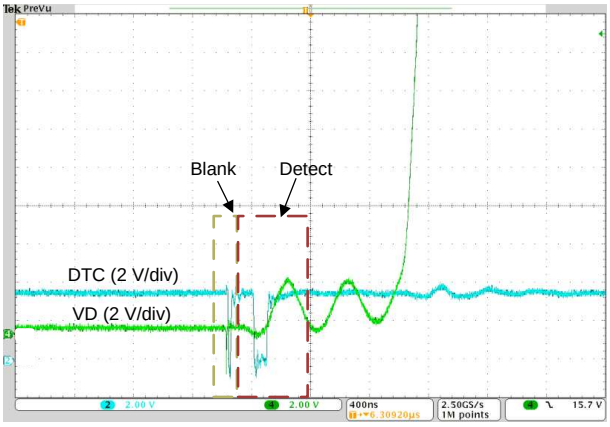
With optimization
Horizontal: 200 ns/div

Figure 37. SR Turnoff Edge After Optimization



No optimization, SR on time too short. Low efficiency.
Horizontal: 200 ns/div

Figure 38. SR Turnoff Edge Before Optimization



With optimization
Horizontal: 200 ns/div

Figure 39. SR Turnoff Edge After Optimization

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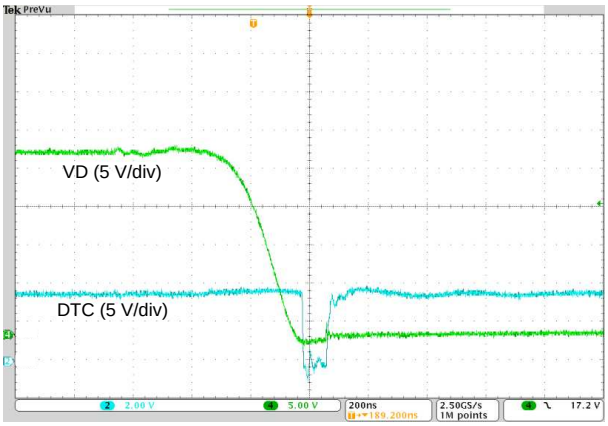
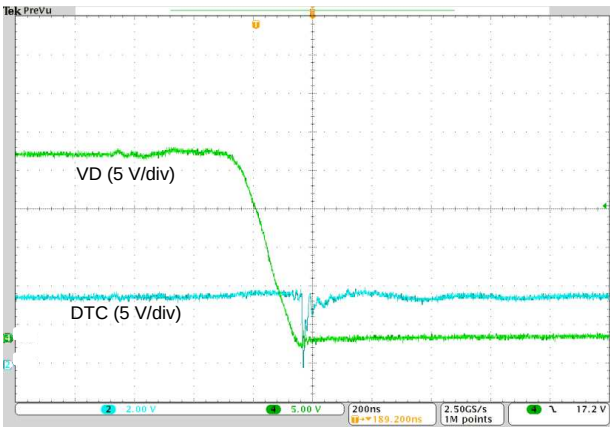
Typical Application (continued)



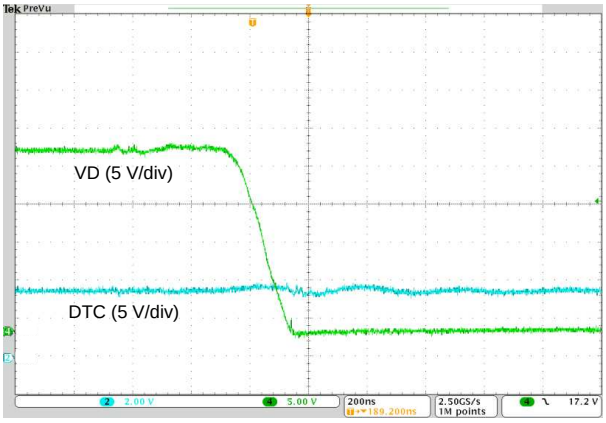
No optimization, SR on turnon too late. Low efficiency.
Horizontal: 200 ns/div

Figure 40. SR Turnon Edge Before Optimization



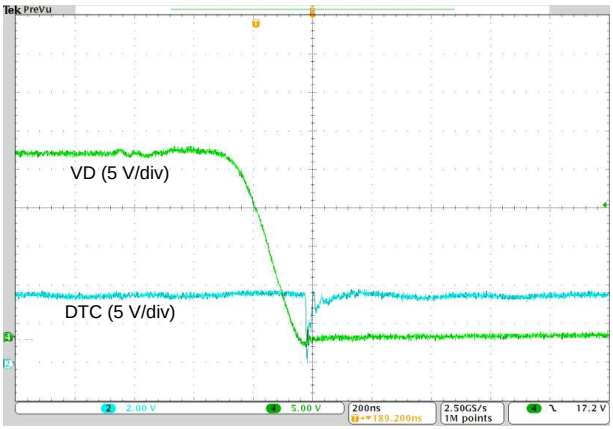
With optimization
Horizontal: 200 ns/div

Figure 41. SR Turnon Edge After Optimization



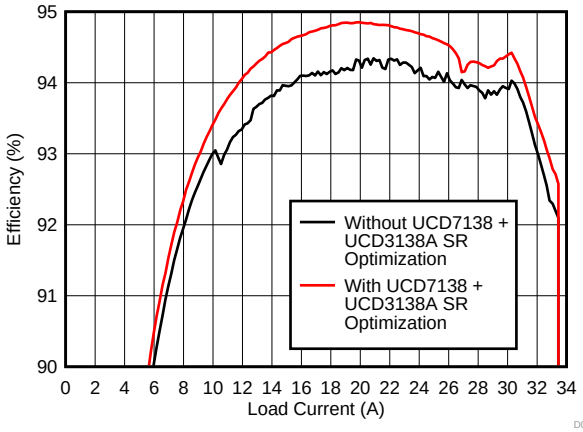
No optimization, SR turnon too early.
Horizontal: 200 ns/div

Figure 42. SR Turnon Edge Before Optimization



With optimization
Horizontal: 200 ns/div

Figure 43. SR Turnon Edge After Optimization



Efficiency increase at peak efficiency: 0.54% Peak efficiency increase (occurs at no-load): 2.62%
Average efficiency increase over constant voltage load range: 0.63%
Peak efficiency with and without SR optimization: 94.85% at 19.92 A

Figure 44. Efficiency Comparison with and without UCD7138 + UCD3138A Advanced SR Control

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10 Power Supply Recommendations

Because the driver draws current from the V_{CC} pin to bias all internal circuits, for the best high-speed circuit performance, two V_{CC} bypass capacitors are recommended to prevent noise problems. The use of surface-mount (SM) components is highly recommended. A 1µF ceramic capacitor should be placed as close as possible to the V_{CC} to ground pad of the gate driver.

11 Layout

11.1 Layout Guidelines

Proper PCB layout is extremely important in a high-current, fast-switching circuit to provide appropriate device operation and design robustness. The following circuit layout guidelines are strongly recommended.

- Place the driver device as close as possible to power and ground to minimize the length of high-current traces between the output pins and the gate of the power device.
- Place the V_{CC} bypass capacitors between the V_{CC} pin and ground as close as possible to the driver with minimal trace length to improve the noise filtering. These capacitors support the high-peak current that is drawn from the V_{CC} supply during turnon of the power MOSFET. The use of low inductance SM components such as chip resistors and chip capacitors is highly recommended.
- The turnon and turnoff current-loop paths (driver device, power MOSFET, and V_{CC} bypass capacitors) should be minimized as much as possible to keep the stray inductance to a minimum.
- Separate power traces and signal traces, such as output and input signals.
- Star-point grounding is a good way to minimize noise coupling from one current loop to another. The ground of the driver should be connected to the other circuit nodes such as the source of power switch, ground of PWM controller, and others at one single point. The connected paths should be as short as possible and as wide as possible to reduce resistance and inductance.
- Use a ground plane to provide noise shielding. Fast rise and fall times at the OUT pin can corrupt the input signals during transition. The ground plane must not be a conduction path for any current loop. Instead, the ground plane must be connected to the star-point with one single trace to establish the ground potential.
- A 1-Ω resistor may be connected between OUT pin and the gate terminal of the MOSFET to reduce gate to source voltage ringing.
- A 20-Ω resistor should be connected between VD pin and the drain terminal of the MOSFET to limit the current flowing out of VD pin when the drain terminal voltage is negative.

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11.2 Layout Example

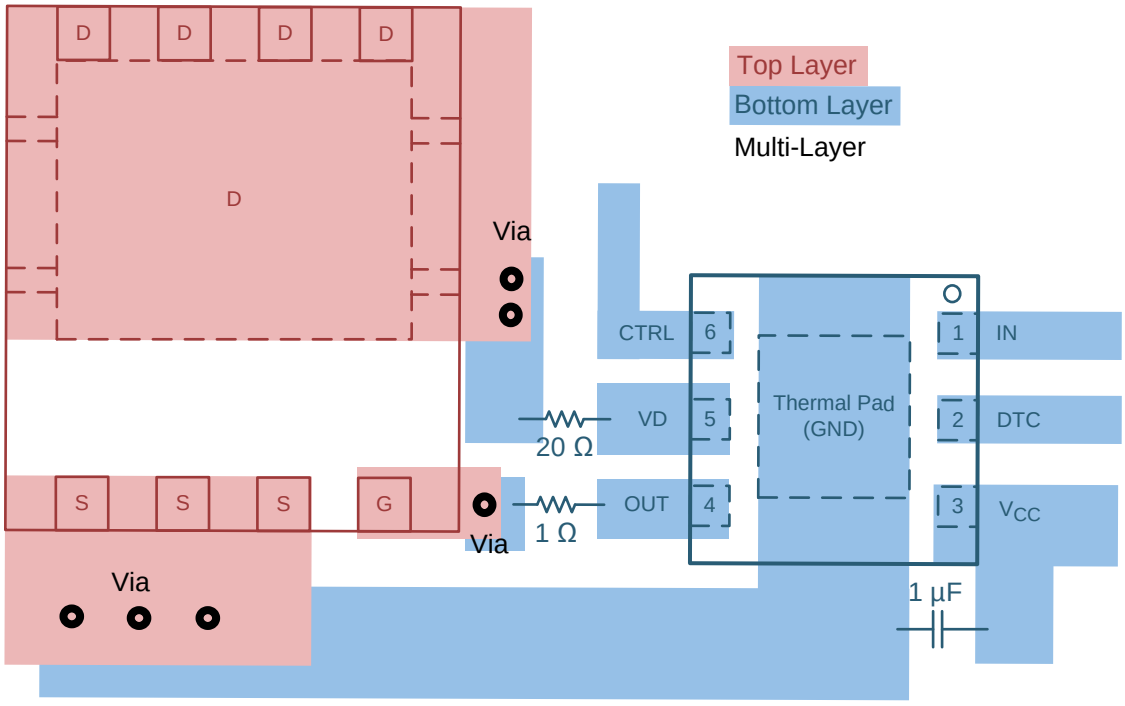

Figure 45. Layout Example With Surface-Mount MOSFET

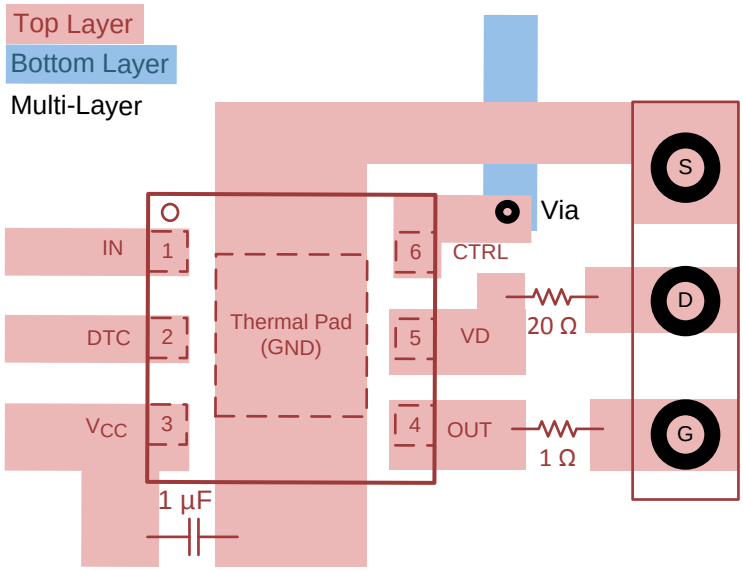

Figure 46. Layout Example With Through-Hole MOSFET

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12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation, see the following:

- *UCD3138A Highly Integrated Digital Controller for Isolated Power*, SLUSC66
- *Using UCD7138 and UCD3138A for Advanced Synchronous Rectification Control*, SLUA737
- *UCD3138 Digital Power Peripherals Programmer's Manual* , SLUU995
- *UCD3138A Migration Guide*, SLUA741

12.2 Trademarks

All trademarks are the property of their respective owners.

12.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
UCD7138DRS	PREVIEW	SON	DRS	6	250	TBD	Call TI	Call TI			
UCD7138DRSR	PREVIEW	SON	DRS	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR		UD7138	
UCD7138DRST	PREVIEW	SON	DRS	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR		UD7138	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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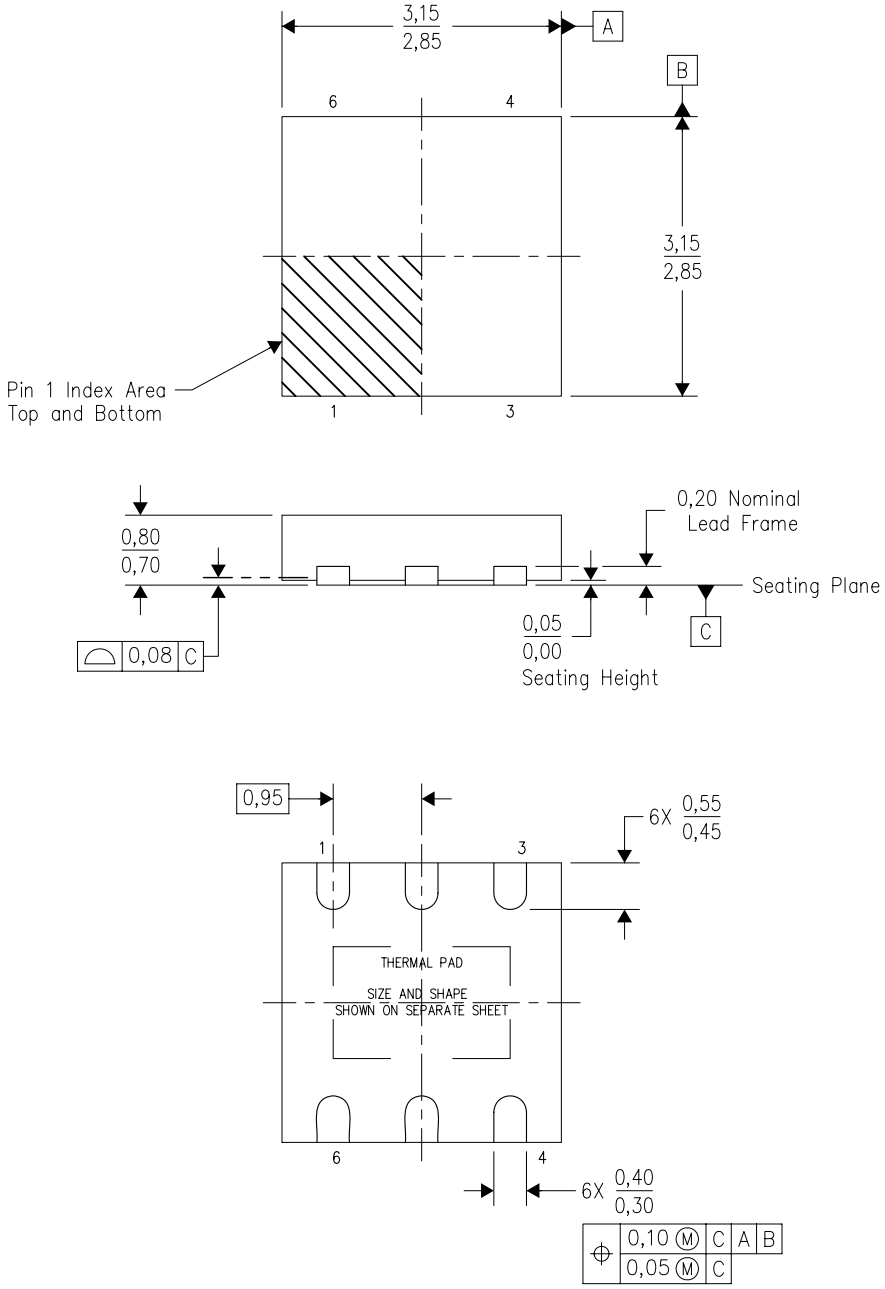
DRS (S–PWSON–N6) PLASTIC SMALL OUTLINE NO–LEAD



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NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. SON (Small Outline No–Lead) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.

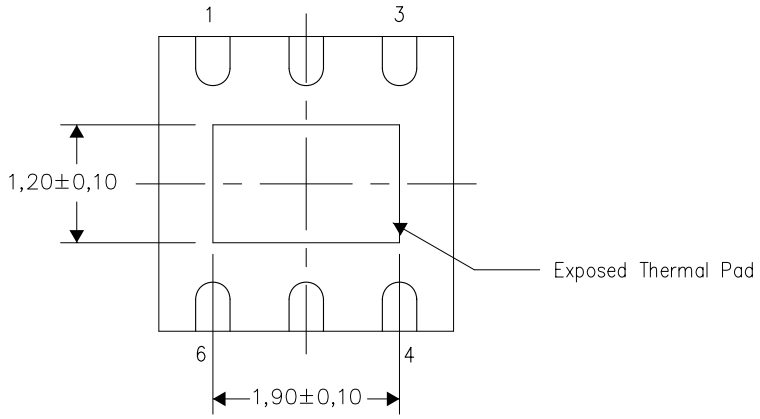
DRS (S–PWSON–N6) PLASTIC SMALL OUTLINE NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

Exposed Thermal Pad Dimensions

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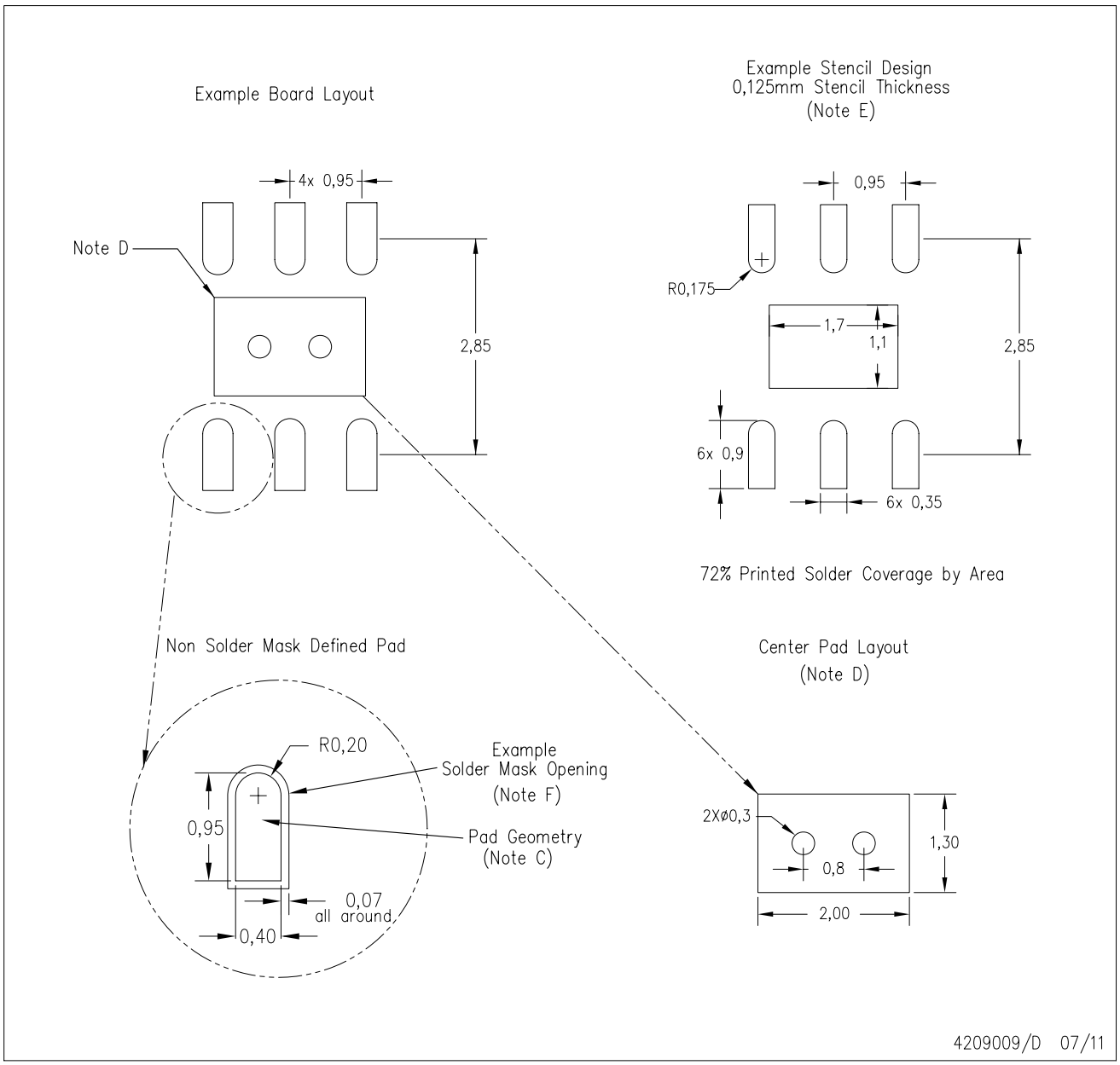
NOTE: All linear dimensions are in millimeters

DRS (S–PWSON–N6) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for solder mask tolerances.

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