

LOW-DROPOUT 0.5-A NEGATIVE LINEAR REGULATOR

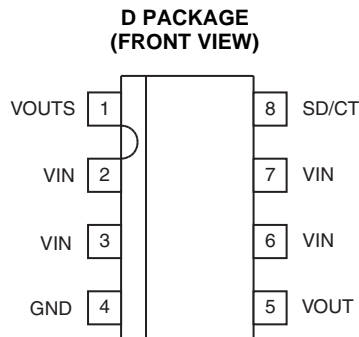
FEATURES

- Precision Negative Series Pass Voltage Regulation
- 0.2-V Dropout at 0.5 A
- Wide Input Voltage Range –3.2 V to –15 V
- Low Quiescent Current Irrespective of Load D Simple Logic Shutdown Interfacing
- –5 V, –12 V, and Adjustable Output
- 2.5% Duty Cycle Short Circuit Protection

SUPPORTS DEFENSE, AEROSPACE AND MEDICAL APPLICATIONS

- Controlled Baseline
- One Assembly/Test Site
- One Fabrication Site
- Available in S-Temp (–55°C/100°C) Temperature Range⁽¹⁾
- Extended Product Life Cycle
- Extended Product-Change Notification
- Product Traceability

(1) Additional temperature ranges are available – contact factory.



DESCRIPTION

The UCC284-x family of negative linear-series pass regulators is tailored for low-dropout applications where low-quiescent power is important. Fabricated with a BCDMOS technology ideally suited for low input-to-output differential applications, the UCC284-x passes 0.5 A while requiring only 0.2 V of input-voltage headroom. Dropout voltage decreases linearly with output current, so that dropout at 50 mA is less than 20 mV.

Quiescent current consumption for the device under normal (non-dropout) conditions is typically 200 μ A. An integrated charge pump is internally enabled only when the device is operating near dropout with low V_{IN} . This ensured that the device meets the dropout specifications even for maximum load current and a V_{IN} of –3.2 V with only a modest increase in quiescent current. Quiescent current is always less than 360 μ A, with the charge pump enabled. The quiescent current of the UCC284 does not increase with load current.

Short-circuit current is internally limited. The device responds to a sustained overcurrent condition by turning off after a t_{ON} delay. The device then stays off for a period, t_{OFF} , that is 40 times the t_{ON} delay. The device then begins pulsing on and off at the t_{ON}/t_{OFF} duty cycle of 2.5%. This drastically reduces the power dissipation during short circuit such that heat sinking, if at all required, must only accommodate normal operation. An external capacitor sets the on time. The off time is always 40 times t_{ON} .

The UCC284-x can be shutdown to 45 μ A (maximum) by pulling the SD/CT pin more positive than –0.7 V. To allow for simpler interfacing, the SD/CT pin may be pulled up to 6 V above the ground pin without turning on clamping diodes.

Internal power dissipation is further controlled with thermal-overload protection circuitry. Thermal shutdown occurs if the junction temperature exceeds 140°C. The chip remains off until the temperature has dropped 20°C ($T_J = 120^\circ\text{C}$).



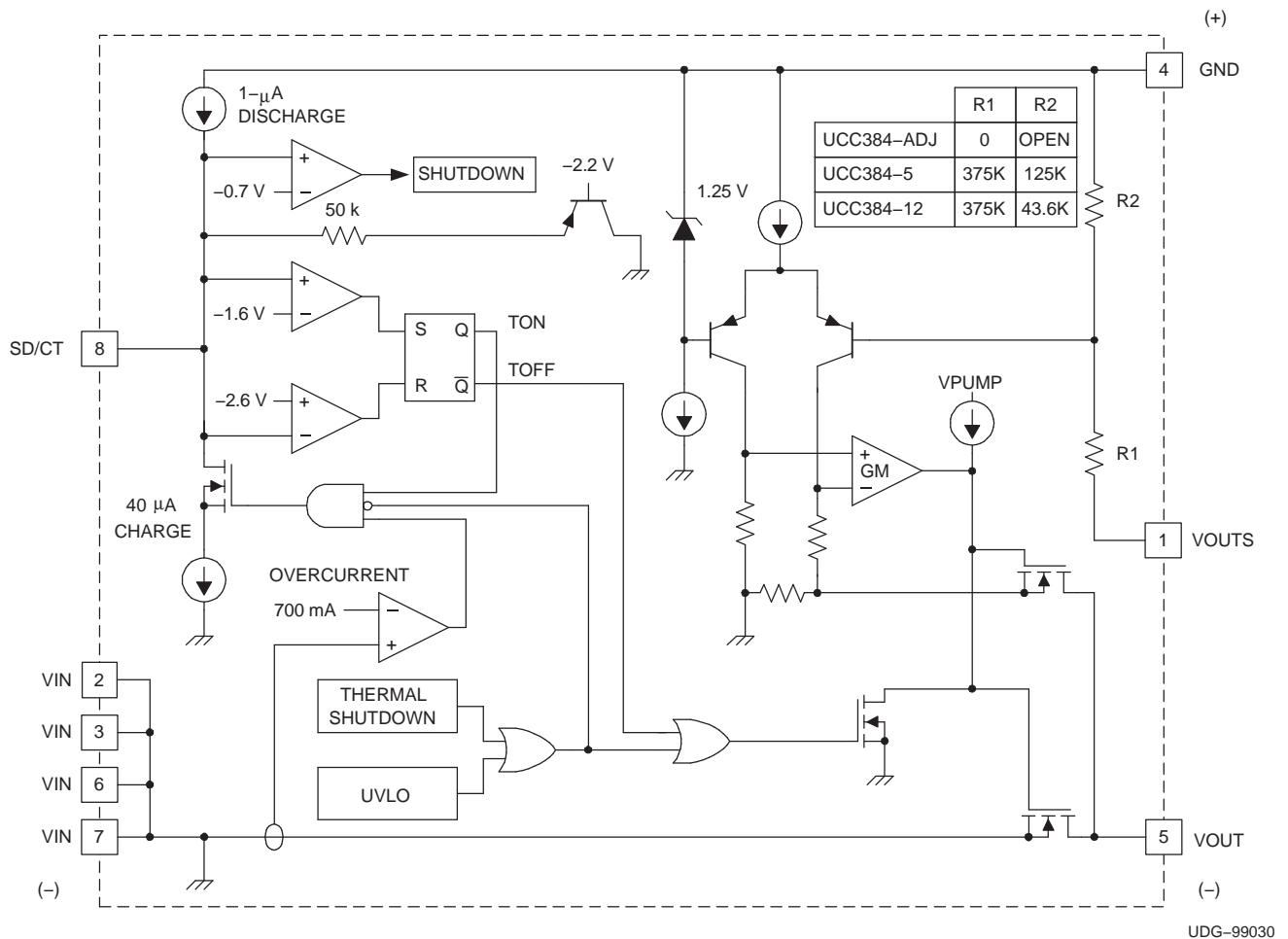
Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

ORDERING INFORMATION⁽¹⁾

T _A	OUTPUT VOLTAGE (V) TYP	PACKAGE DEVICES (SOIC) D ⁽²⁾
-55°C to 100°C	-5	UCC284SDR-5EP
-55°C to 100°C	-12	UCC284SDR-12EP ⁽³⁾
-55°C to 100°C	-5 (Adj)	UCC284SDR-ADJEP ⁽³⁾

- (1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.
- (2) Package drawings, standard packing quantities, symbolization, and PCB design guidelines are available at www.ti.com/sc/package. Thermal data can be found at http://www-s.ti.com/cgi-bin/sc/thermal_derating_curve.cgi.
- (3) Product preview only.

functional block diagram



ABSOLUTE MAXIMUM RATINGS⁽¹⁾⁽²⁾

over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
V _{IN} Input voltage range ⁽²⁾	-16		V
SD/CT Shutdown voltage range	-5	6	V
T _J Operating virtual junction temperature range	-55	150	V
T _{stg} Storage temperature range	-65	150	°C
Lead temperature (Soldering, 10 seconds)		300	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltages are with respect to ground. Currents are positive into and negative out of the specified terminals.

ELECTRICAL CHARACTERISTICS

 T_A = -55°C to 100°C for the UCC284, V_{IN} = V_{OUT} - 1.5 V, I_{OUT} = 0 mA, C_{OUT} = 4.7 μF, and CT = 0.015 μF. For UCC284-ADJ, V_{OUT} is set to -3.3 V (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
UCC284-5 Fixed -5-V 0.5-A Regulation Section					
Output voltage	T _A = 25°C	-5.075	-5	-4.925	V
	Over all temperature conditions	-5.150		-4.850	V
Line regulation	T _A = 25°C, V _{IN} = -5.2 V to -15 V		1.5	10	mV
	Over all temperature conditions			12	
Load regulation	T _A = 25°C, I _{OUT} = 0 mA to 0.5 A		0.1	0.25	%
	Over all temperature conditions		0.1	0.30	
Output noise voltage	T _A = 25°C, BW = 10 Hz to 10 kHz		200		μVRMS
Dropout voltage, V _{OUT} - V _{IN}	T _A = 25°C, I _{OUT} 0.5 A, V _{OUT} = -4.8 V		0.2	0.5	V
	Over all temperature conditions		0.2	0.55	
	T _A = 25°C, I _{OUT} 50 mA, V _{OUT} = -4.8 V		20	50	mV
	Over all temperature conditions		20	55	
UCC284-5 Fixed -5-V 0.5-A Power Supply Section					
Input voltage range		-15		-5.2	V
Quiescent current charge pump on	T _A = 25°C, V _{IN} = -4.85 V ⁽¹⁾		280	350	μA
	Over all temperature conditions			360	
Quiescent current	T _A = 25°C, V _{IN} = -15 V		200	250	μA
	Over all temperature conditions			260	
Quiescent current in shutdown	V _{IN} = -13 V, SD/CT = 0 V, T _A = 0°C to 100°C ⁽²⁾		15	45	μA
	V _{IN} = -13 V, SD/CT = 0 V, T _A = -55°C to 0°C ⁽²⁾			100	μA
Shutdown threshold	T _A = 25°C, At shutdown pin (SD/CT)	-1.0	-0.7	-0.4	V
	Over all temperature conditions	-1.2		-0.2	
Shutdown input current	T _A = 25°C, SD/CT = 0 V	5	10	25	μA
	Over all temperature conditions	3	10	30	
Output leakage in shutdown	V _{IN} = -15 V, V _{OUT} = 0 V ⁽³⁾		1	50	μA
Overtemperature shutdown			140		°C
Overtemperature hysteresis			20		°C
UCC284-5 Fixed -5-V 0.5-A Current Limit Section					

- (1) The internal charge pump is enabled only for dropout condition with low V_{IN}. Only in this condition is the charge pump required to provide additional output FET gate drive to maintain dropout specifications. For conditions where the charge pump is not required, it is disabled, which lowers overall device power consumption.
- (2) Ensured by design. Not production tested.
- (3) In the application during shutdown mode, output leakage current adds to quiescent current.

ELECTRICAL CHARACTERISTICS (continued)

$T_A = -55^{\circ}\text{C}$ to 100°C for the UCC284, $V_{IN} = V_{OUT} - 1.5\text{ V}$, $I_{OUT} = 0\text{ mA}$, $C_{OUT} = 4.7\text{ }\mu\text{F}$, and $CT = 0.015\text{ }\mu\text{F}$. For UCC284-ADJ, V_{OUT} is set to -3.3 V (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Peak current limit	$T_A = 25^{\circ}\text{C}$, $V_{OUT} = 0\text{ V}$	0.7	1.1	1.5	A
	Over all temperature conditions	0.5		1.7	
Overcurrent threshold		0.55	0.7	0.9	A
Current limit duty cycle	$V_{OUT} = 0\text{ V}$		2.5	4	%
Overcurrent time out, t_{ON}	$T_A = 25^{\circ}\text{C}$, $V_{OUT} = 0\text{ V}$	300	500	700	μs
	Over all temperature conditions	300		720	
UCC284-12 Fixed 12-V 0.5-A Regulation Section					
Output voltage	$T_A = 25^{\circ}\text{C}$	-12.18	-12	-11.82	V
	Over all conditions	-12.24		-11.64	V
Line regulation	$V_{IN} = -12.5\text{ V}$ to -15 V		5	15	mV
Load regulation	$I_{OUT} = 0\text{ mA}$ to 0.5 A		0.1	0.3	%
Output noise voltage	$T_A = 25^{\circ}\text{C}$, $BW = 10\text{ Hz}$ to 10 kHz		200		μVRMS
Dropout voltage, $V_{OUT} - V_{IN}$	$I_{OUT} = 0.5\text{ A}$, $V_{OUT} = -11.6\text{ V}$		0.15	0.5	V
	$I_{OUT} = 50\text{ mA}$, $V_{OUT} = -11.6\text{ V}$		15	50	mV
UCC284-12 Fixed -12-V 0.5-A Power Supply Section					
Input voltage range		-15		-12.5	V
Quiescent current	$V_{IN} = -15\text{ V}$		220	350	μA
Quiescent current in shutdown	$V_{IN} = -13\text{ V}$, $SD/CT = 0\text{ V}$ $T_A = 0^{\circ}\text{C}$ to 100°C (4)		15	45	μA
	$V_{IN} = -13\text{ V}$, $SD/CT = 0\text{ V}$ $T_A = -55^{\circ}\text{C}$ to 0°C (4)			100	μA

(4) Ensured by design. Not production tested.

ELECTRICAL CHARACTERISTICS

$T_A = -55^{\circ}\text{C}$ to 100°C for the UCC284, $V_{IN} = V_{OUT} - 1.5\text{ V}$, $I_{OUT} = 0\text{ mA}$, $C_{OUT} = 4.7\text{ }\mu\text{F}$, and $CT = 0.015\text{ }\mu\text{F}$. For UCC284-ADJ, V_{OUT} is set to -3.3 V (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
UCC284-12 Fixed -12 V -0.5-A Power Supply Section (continued)					
Shutdown threshold	At shutdown pin (SD/CT)	-1.0	-0.7	-0.4	V
Shutdown input current	$SD/CT = 0\text{ V}$	5	10	25	μA
Output leakage in shutdown	$V_{IN} = -15\text{ V}$, $V_{OUT} = 0\text{ V}$ (1)		1	50	μA
Overtemperature shutdown			140		$^{\circ}\text{C}$
Overtemperature hysteresis			20		$^{\circ}\text{C}$
UCC284-12 Fixed -12-V 0.5-A Current Limit Section					
Peak current limit	$V_{OUT} = 0\text{ V}$	0.7	1.1	1.5	A
Overcurrent threshold		0.55	0.7	0.9	A
Current limit duty cycle	$V_{OUT} = 0\text{ V}$		2.5	4	%
Overcurrent time out, t_{ON}	$V_{OUT} = 0\text{ V}$	300	500	700	μs
UCC284-ADJ Adjustable 0.5-A Regulation Section					
Reference voltage	$T_A = 25^{\circ}\text{C}$	-1.27	-1.25	-1.23	V
	Over temperature	-1.275		-1.215	V
Line regulation	$V_{IN} = -3.5\text{ V}$ to -15 V , $V_{OUT} = V_{OUTS}$		0.5	3	mV
Load regulation	$I_{OUT} = 0\text{ mA}$ to 0.5 A		0.1	0.18	%
Output noise voltage	$BW = 10\text{ Hz}$ to 10 kHz , $T_A = 25^{\circ}\text{C}$		200		μVRMS

(1) In the application during shutdown mode, output leakage current adds to quiescent current.

ELECTRICAL CHARACTERISTICS (continued)

$T_A = -55^\circ\text{C}$ to 100°C for the UCC284, $V_{IN} = V_{OUT} - 1.5\text{ V}$, $I_{OUT} = 0\text{ mA}$, $C_{OUT} = 4.7\text{ }\mu\text{F}$, and $CT = 0.015\text{ }\mu\text{F}$. For UCC284-ADJ, V_{OUT} is set to -3.3 V (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Dropout voltage, $V_{OUT} - V_{IN}$	$I_{OUT} = 0.5\text{ A}$, $V_{OUT} = -3.15\text{ V}$		0.25	0.5	V
	$I_{OUT} = 50\text{ mA}$, $V_{OUT} = -3.15\text{ V}$		25	50	mV
Sense pin input current			100	250	nA
UCC284-ADJ Adjustable 0.5-A Power Supply Section					
Input voltage range		-15		-3.5	V
Undervoltage lockout		-3.2	-2.95	-2.7	V
Quiescent current charge pump on	$V_{IN} = -3.15\text{ V}^{(2)}$		200	350	μA
Quiescent current	$V_{IN} = -15\text{ V}$		200	250	μA
Quiescent current in shutdown	$V_{IN} = -13\text{ V}$, $SD/CT = 0\text{ V}$		15	45	μA
	$T_A = 0^\circ\text{C}$ to $100^\circ\text{C}^{(3)}$				
	$V_{IN} = -13\text{ V}$, $SD/CT = 0\text{ V}$			100	μA
	$T_A = -55^\circ\text{C}$ to $0^\circ\text{C}^{(3)}$				
Shutdown threshold	At shutdown pin (SD/CT)	-1.0	-0.7	-0.4	V
Shutdown input current	$SD/CT = 0\text{ V}$	5	10	25	μA
Output leakage in shutdown	$V_{IN} = -15\text{ V}$, $V_{OUT} = 0\text{ V}^{(4)}$		1	50	μA
Overtemperature shutdown			140		$^\circ\text{C}$
Overtemperature hysteresis			20		$^\circ\text{C}$
UCC284-ADJ Adjustable 0.5-A Current Limit Section					
Peak current limit	$V_{OUT} = 0\text{ V}$	0.7	1.1	1.5	A
Overcurrent threshold		0.55	0.7	0.9	A
Current limit duty cycle	$V_{OUT} = 0\text{ V}$		2.5	4	%
Overcurrent time out, t_{ON}	$V_{OUT} = 0\text{ V}$	300	500	700	μs

- (2) The internal charge pump is enabled only for dropout condition with low V_{IN} . Only in this condition is the charge pump required to provide additional output FET gate drive to maintain dropout specifications. For conditions where the charge pump is not required, it is disabled, which lowers overall device power consumption.
- (3) Ensured by design. Not production tested.
- (4) In the application during shutdown mode, output leakage current adds to quiescent current.

PIN DESCRIPTION

GND: This is the low noise ground reference input. All voltages are measured with respect to the GND pin.

SD/CT: This is the shutdown pin and also the short-circuit timing pin. Pulling this pin more positive than -0.7 V puts the circuit in a low-current shutdown mode. Placing a timing capacitor between this pin and GND sets the short-circuit charging time, t_{ON} during an overcurrent condition. During an overcurrent condition, the output pulses at approximately a 2.5% duty cycle.

NOTE:

The CT capacitor must be connected between this pin and GND, not V_{IN} , to assure that the SD/CT pin is not pulled significantly negative during power-up. This pin should not be externally driven more negative than -5 V or the device will be damaged.

V_{IN} : This is the negative input supply. Bypass this pin to GND with at least $1\text{ }\mu\text{F}$ of low ESR or ESL capacitance.

V_{OUT} : Regulated negative-output voltage. A single $4.7\text{-}\mu\text{F}$ capacitor should be connected between this pin and GND. Smaller value capacitors can be used for light loads, but this degrades the load-step performance of the regulator.

VOUTS: This is the feedback pin for sensing the output of the regulator. For the UCC284-5 and UCC284-12 versions, VOUTS can be connected directly to VOUT. If the load is placed at a considerable distance from the regulator, the VOUTS lead can be used as a Kelvin connection to minimize errors due to lead resistance. Connecting VOUTS at the load moves the resistance of the VOUT wire into the control loop of the regulator, thereby effectively canceling the IR drop associated with the load path.

APPLICATION INFORMATION

overview

The UCC284–x family of negative low-dropout linear (LDO) regulators provides a regulated-output voltage for applications with up to 0.5 A of load current. The regulators feature a low-dropout voltage and short-circuit protection, making their use ideal for demanding applications requiring fault protection.

programming the output voltage on the UCC284

The UCC284–5 and UCC284–12 have output voltages that are fixed at –5 V and –12 V respectively. Connecting VOUTS to VOUT gives the proper output voltage with respect to ground.

The UCC284–ADJ can be programmed for any output voltage between –1.25 V and –15 V. This is easily accomplished with the addition of an external resistor divider connected between GND and VOUT with VOUTS connected to the center tap of the divider. For an output of –1.25 V, no resistors are needed and VOUTS is connected directly to VOUT. The regulator-input voltage cannot be more positive than the UVLO threshold, or approximately –3 V. Thus, low dropout cannot be achieved when programming the output voltage more positive than approximately –3.3 V. A typical application circuit is shown in [Figure 1](#).

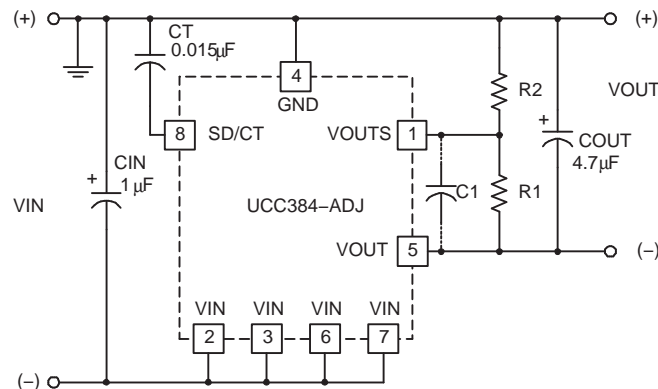


Figure 1. Typical Application Circuit

For the UCC284-ADJ, the output voltage is programmed by the following equation:

$$V_{OUT} = -1.25 \times \left(1 + \frac{R1}{R2}\right) \quad (1)$$

When R1 or R2 are selected to be greater than about 100 kΩ, a small ceramic capacitor should be placed across R1 to cancel the input pole created by R1 and the parasitic capacitance appearing on VOUTS. Values of approximately 20 pF should be adequate.

dropout performance

The UCC284 is tailored for low-dropout applications where low-quiescent power is important. Fabricated with a BCDMOS technology ideally suited for low input-to-output differential applications, the UCC284 passes 0.5 A while requiring only 0.2 V of headroom. The dropout voltage is dependent on operating conditions such as load current, input and load voltages, and temperature. The UCC284 achieves a low RDS(on) through the use of an internal charge-pump that drives the MOSFET gate.

[Figure 2](#) shows typical dropout voltages versus output voltage for the UCC284–5 V and –12 V versions as well as the UCC284-ADJ version programmed between –3.3 V and –15 V. Since the dropout voltage is also affected by output current, [Figure 3](#) shows typical dropout voltages versus load current for different values of VOUT.

Operating temperatures also affect the RDS(on) and the dropout voltage of the UCC284. [Figure 4](#) shows typical dropout voltages for the UCC284 over temperature under a full load of 0.5 A.

short-circuit protection

The UCC284 provides unique short-circuit protection circuitry that reduces power dissipation during a fault. When an overcurrent condition is detected, the device enters a pulsed mode of operation, limiting the output to a 2.5% duty cycle. This reduces the heat sink requirements during a fault. The operation of the UCC284 during an overcurrent condition is shown in [Figure 5](#).

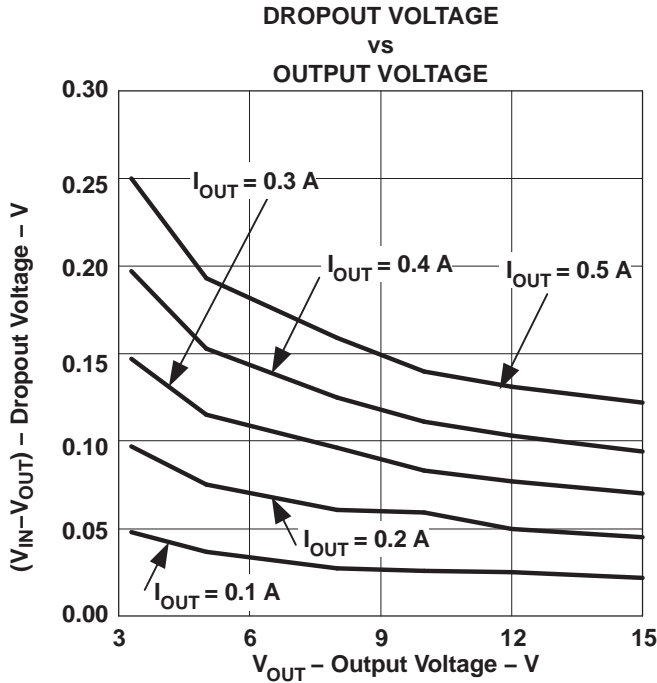


Figure 2.

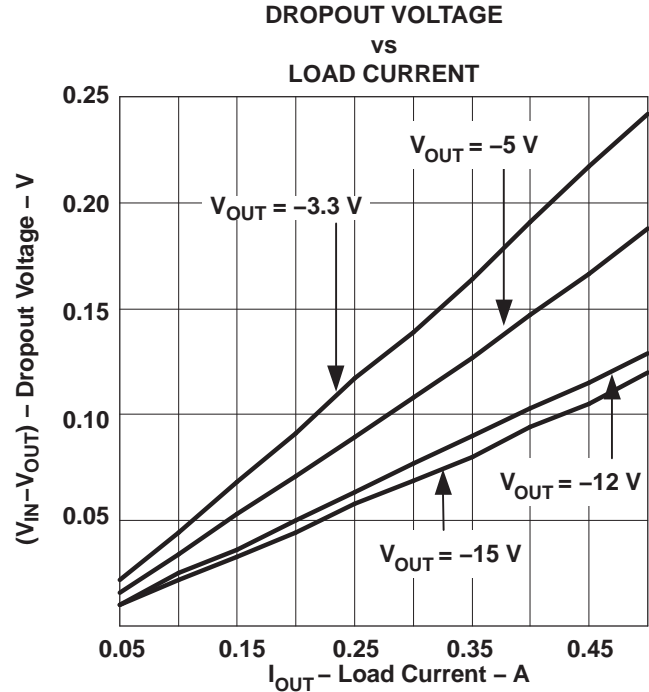


Figure 3.

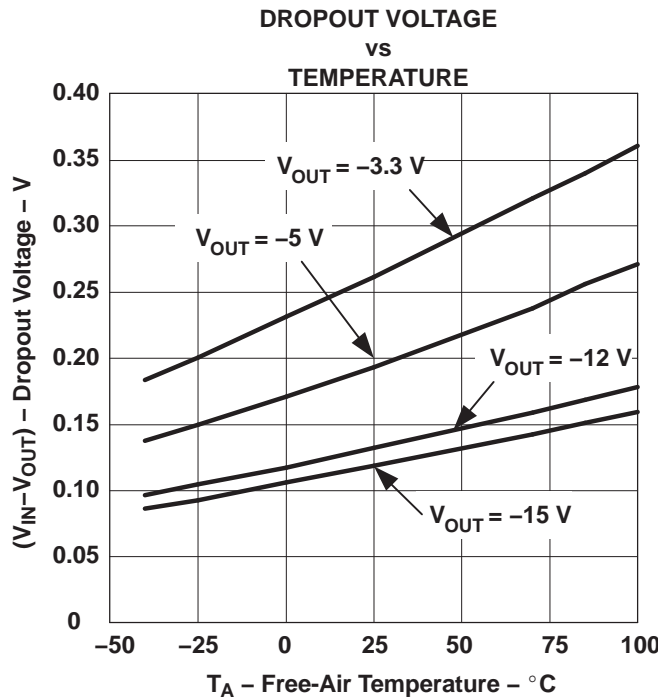
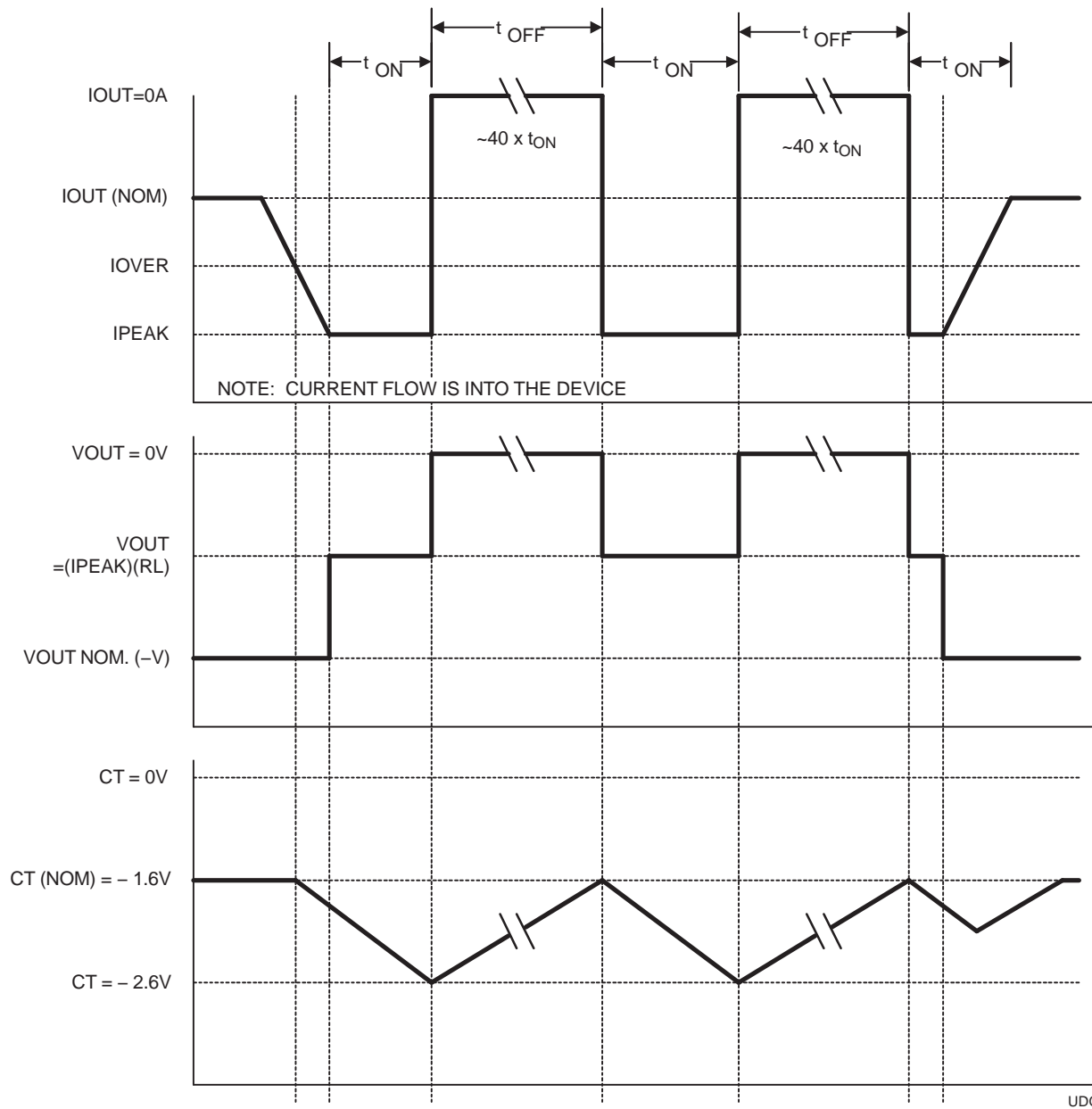


Figure 4.



UDG-99031

Figure 5. Short Circuit Timing

short-circuit timing

During normal operation the output voltage is in regulation and the SD/CT pin is held to -1.5 V via a 50-k Ω internal-source impedance. If the output-current rises above the overcurrent threshold, the CT capacitor is charged by a 40- μ A current sink. The voltage on the SD/CT pin moves in a negative direction with respect to GND.

During an overcurrent condition, the regulator actively limits the maximum output current to the peak-current limit. This limits the output voltage of the regulator to:

$$V_{OUT} = I_{PEAK} \times R_L \quad (2)$$

If the output current stays above the overcurrent threshold, the voltage on the SD/CT pin reaches -2.6 V with respect to GND and the output turns off. The CT capacitor is then discharged by a 1- μ A current source. When the voltage on the SD/CT pin reaches -1.6 V with respect to GND, the output turns back on. This process repeats until the output current falls below the overcurrent threshold.

t_{ON}, the time the output is on during an overcurrent condition is determined by the following equation:

$$t_{ON} = CT (\mu F) \times \frac{1 V}{40 \mu A} \text{seconds} \quad (3)$$

t_{OFF}, the time the output is off during an overcurrent condition is determined by the following equation:

$$t_{OFF} = CT (\mu F) \times \frac{1 V}{1 \mu A} \text{seconds} \quad (4)$$

capacitive loads

A capacitive load on the regulator's output appears as a short-circuit during start-up. If the capacitance is too large, the output voltage does not begin to regulate during the initial t_{ON} period and the UCC284 enters a pulsed mode operation. For a constant current load the maximum allowed output capacitance is calculated as follows:

$$C_{OUT(max)} = \left[I_{PEAK(A)} - I_{LOAD(A)} \right] \times \frac{t_{ON(sec)}}{V_{OUT(V)}} \text{Farads} \quad (5)$$

For worst case calculations, the minimum value for t_{ON} should be used, which is based on the value of CT capacitor selected. For a resistive load the maximum output capacitor can be estimated as follows:

$$C_{OUT(max)} = \frac{t_{ON(sec)}}{R_{LOAD} (\Omega) \times \ln \left[\frac{1}{1 - \left(\frac{V_{OUT(V)}}{I_{MAX(A)} \times R_{LOAD(\Omega)}} \right)} \right]} \text{Farads} \quad (6)$$

Figure 6 and Figure 7 are oscilloscope photos of the UCC284-ADJ operating during an overcurrent condition. Figure 6 shows operation of the circuit as the output current initially rises above the overcurrent threshold. This is shown on a 1 ms/div. scale. Figure 7 shows operation of the same circuit on a 25 ms/div. scale showing one complete cycle of operation during an overcurrent condition.

**UCC284-ADJ
OVERCURRENT CONDITION OPERATION
1 ms/div**

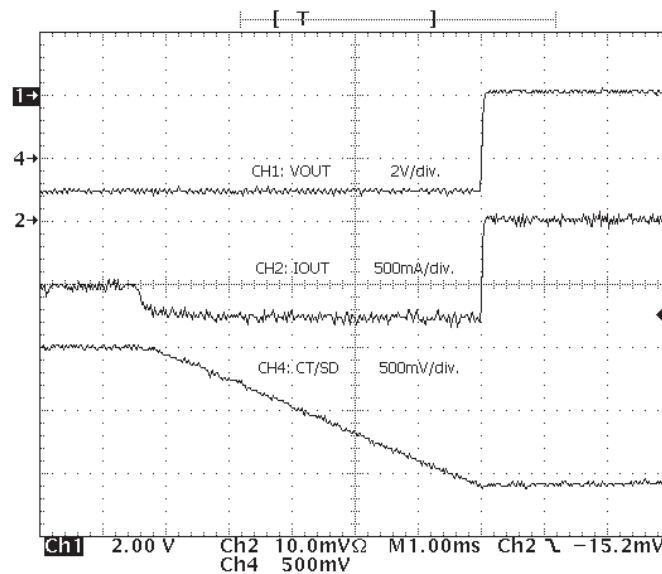


Figure 6.

**UCC284-ADJ
OVERCURRENT CONDITION OPERATION
25 ms/div**

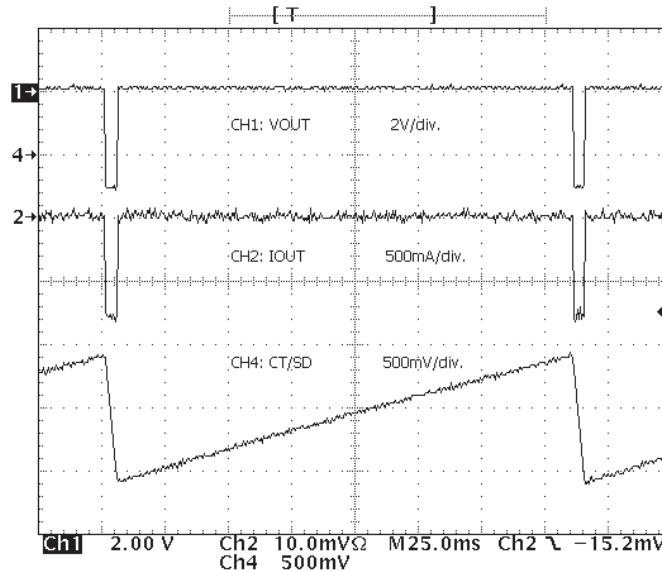


Figure 7.

shutdown feature of the UCC284

The shutdown feature of the UCC284 allows the device to be placed in a low quiescent current mode. The UCC284 is shut down by pulling the SD/CT pin more positive than -0.7 V with respect to GND. Figure 8 shows how a shutdown circuit can be configured for the UCC284 using a standard transistor-transistor logic signal to control it.

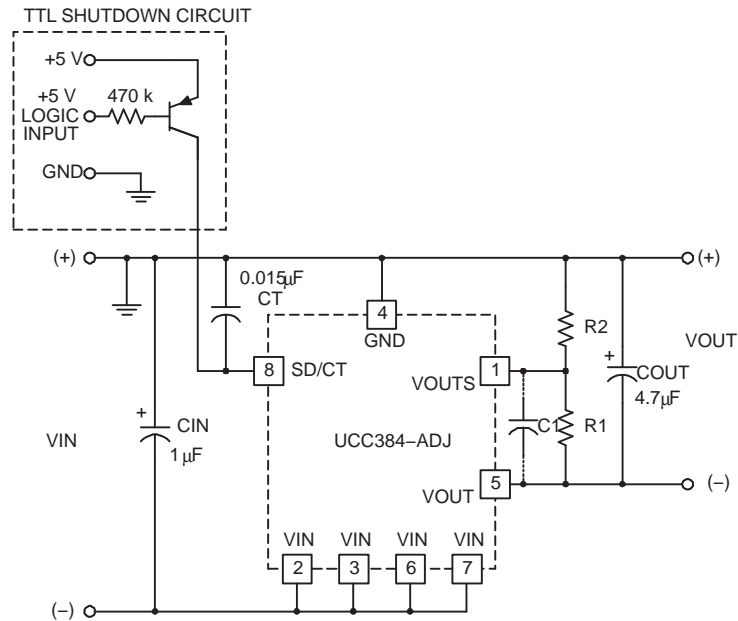


Figure 8. TTL Controlled Shutdown Circuit

controlling the SD/CT pin

Forcing the SD/CT pin to any fixed voltage affects the operation of the circuit. As mentioned before, pulling the SD/CT pin more positive than -0.7 V puts the circuit in a shutdown mode, limiting the quiescent current to less than $45\text{ }\mu\text{A}$. Pulling this pin more positive than 6 V with respect to GND damages the device.

Forcing the SD/CT pin to any fixed voltage between -0.7 V and -1.6 V with respect to GND enables the output. However, in an overcurrent condition, the output does not pulse at a 2.5% duty cycle, but the output current is still limited to the peak current limit. This circuit may be used where a fixed current limit is needed, where a 2.5% duty cycle is undesirable. The UCC284 supplies a maximum current in this configuration as long as the temperature of the device does not exceed the overtemperature shutdown. This is determined by the peak current being supplied, the input and output voltages, and the type of heat sink being used. Thermal design is discussed later on in this data sheet.

Forcing the SD/CT pin to a voltage level between approximately -1.6 V and -2.6 V with respect to GND is not recommended as the output may or may not be enabled.

Forcing the SD/CT pin to a voltage level between approximately -2.6 V and -5 V with respect to GND turns the output off completely. The output remains off as long as the voltage is applied. Pulling this pin more negative than -5 V with respect to GND damages the device (see Table 1).

Table 1. SD/CT Voltage Levels

SD/CT	STATE
6 V to -0.7 V	Output disabled and device in low quiescent shutdown mode.
-0.7 V to -1.6 V	Output enabled
-1.6 V to -2.6 V	Output enabled or disabled depending on the previous state.
-2.6 V to -5 V	Output disabled

VIN TO VOUT DELAY TIME
DURING POWER-UP WITH CT = 0.22 μF

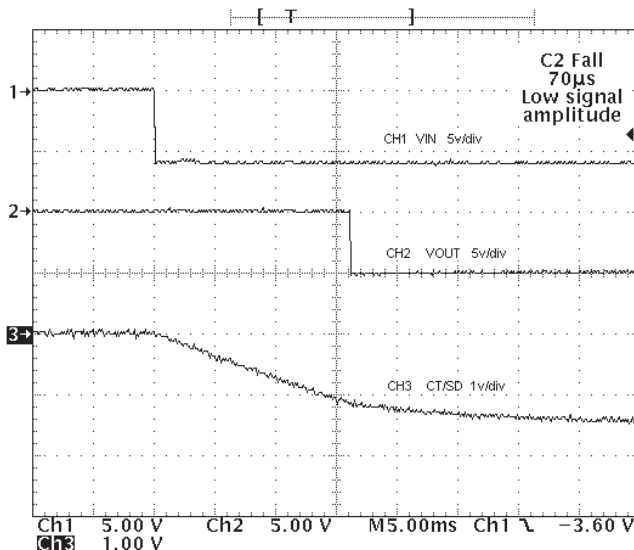


Figure 9.

VIN to VOUT Delay

During power-up there is a delay between VIN and VOUT. The majority of this delay time is due to the charging time of the CT capacitor. When VIN moves more negative than the UVLO of the device with respect to GND, the CT capacitor begins to charge. A 17-μA current sink is used only during power up to charge the CT capacitor. When the voltage on the SD/CT pin reaches approximately -1.6 V with respect to GND, the output turns on and regulates. The larger the value of the CT capacitor, the greater the delay time between VIN and VOUT. Figure 9 shows the VIN to VOUT start-up delay, approximately 16 ms for a circuit with CT = 0.22 μF.

Shorter delay times can be achieved with a smaller CT capacitor. The problem with a smaller CT capacitor is that with a very large load, the circuit may stay in overcurrent mode and never turn on. A circuit with a large capacitive load needs a large CT capacitor to operate properly.

One way to shorten the delay from VIN to VOUT during powerup is with the use of the quick start-up circuit shown in Figure 10.

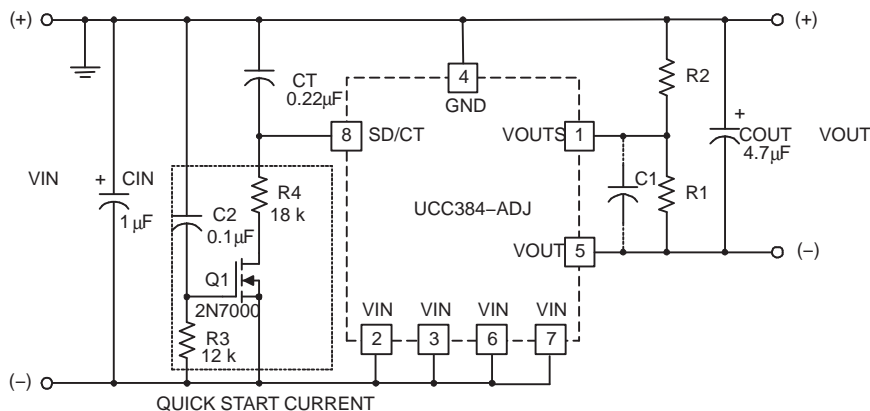


Figure 10. Quick Start-Up Circuit

With the quick start-up circuit, the delay time between VIN and VOUT during start-up can be reduced dramatically. Figure 11 shows that with the quick start-up circuit, the VIN to VOUT delay time has been reduced to approximately 1 ms.

VIN TO VOUT DELAY TIME WITH QUICK START-UP CIRCUIT

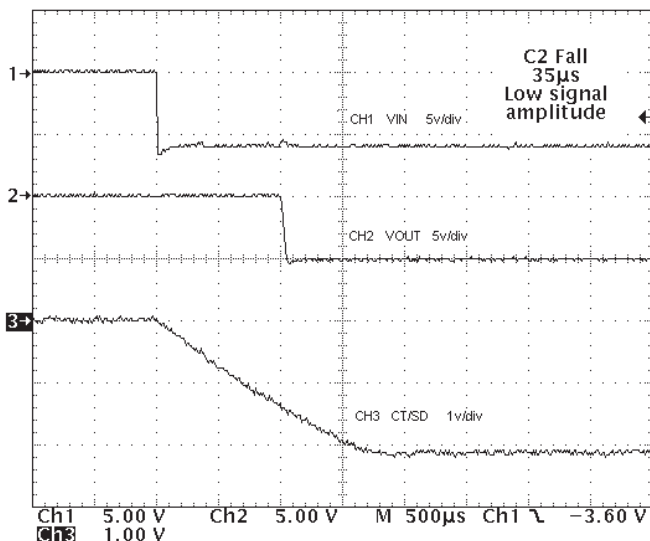


Figure 11.

VIN TO VOUT DELAY TIME WITH CT CAPACITOR REMOVED

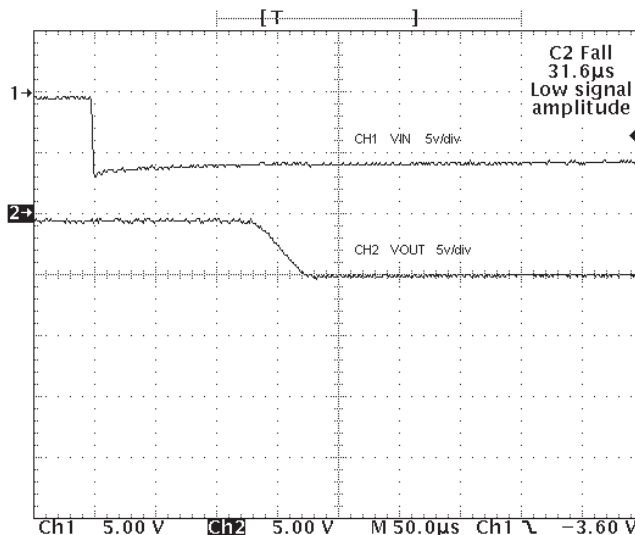


Figure 12.

operation of the quick start-up circuit

During normal start-up, the UCC284 does not turn on until the voltage on the SD/CT pin reaches approximately –1.6 V with respect to ground. It takes a certain amount of time for the CT capacitor to charge to this point. For a circuit that has a very large load, the CT capacitor needs to be large in order for the overcurrent timing to work properly. A large value of capacitance on the SD/CT pin increases the VIN to VOUT delay time.

The quick start-up circuit uses Q1 to quickly pull the SD/CT pin in a negative direction during start-up, thus decreasing the VIN-to-VOUT delay time. When VIN is applied to the circuit, Q1 turns on and starts to charge the CT capacitor. The current pulled through R4 determines the rate at which CT is charged. R4 can be calculated as follows:

$$R4 = \frac{V_{IN}(V) \times T_D \text{ seconds}}{1.6 \times CT (F)} \text{ ohms} \tag{7}$$

t_D is the approximate VIN-to-VOUT delay time desired.

Q1 needs to be turned off after a fixed time to prevent the SD/CT pin from going too far negative with respect to GND. If the SD/CT pin is allowed to go too far negative with respect to GND, the output turns off again or possibly even damages the SD/CT pin. The maximum amount of time that Q1 should be allowed to be on is referred to as t_M and can be calculated as follows:

$$t_M = \frac{2.6}{1.6} \times t_D \text{ seconds} \tag{8}$$

R3 along with C2 set the time that Q1 is allowed to be on. Since t_M is the maximum amount of time that Q1 should be allowed to stay on, an added safety margin may be to use $0.9 \times t_M$ instead. This ensures that Q1 is turned off in the proper amount of time. With a chosen value for C2, R3 can be calculated as follows:

$$R3 = \frac{0.9 \times t_M \text{ seconds}}{C2(F) \times \ln \left(1 - \frac{V_{IN}(V) - 1.6}{V_{IN}(V)} \right)} \text{ Ohms} \quad (9)$$

After the CT capacitor has charged up for a time equal to $0.9 \times t_M$, Q1 turns off and allows the SD/CT pin to be pulled back to -1.5 V with respect to GND through a $50\text{-k}\Omega$ resistor. At this point, the SD/CT pin can be used by the UCC284 overcurrent timing control.

minimum VIN to VOUT delay time

Although it may desirable to have as short a delay time as possible, a small portion of this delay time is fixed by the UCC284 and cannot be shortened. This is shown in [Figure 12](#), where the CT capacitor has been removed from the circuit completely, giving a fixed VIN to VOUT delay of approximately $150 \mu\text{s}$ for a circuit with $V_{IN} = -6 \text{ V}$ and $V_{OUT} = -5 \text{ V}$.

thermal design

The Packaging Information section of the Power Supply Control Products Data Book (literature number SLUD003) contains reference material for the thermal ratings of various packages. The section also includes an excellent article entitled Thermal Characteristics of Surface Mount Packages, which is the basis for the following discussion.

Thermal design for the UCC284 includes two modes of operation, normal and pulsed. In normal mode, the linear regulator and heat sink must dissipate power equal to the maximum forward voltage drop multiplied by the maximum load current. Assuming a constant current load, the expected heat rise at the regulator's junction can be calculated as follows:

$$t_{RISE} = P_{DISS} \times (\theta_{jc} + \theta_{ca}) \quad (10)$$

Theta (θ) is the thermal resistance and PDISS is the power dissipated. The junction-to-case thermal resistance (θ_{jc}) of the SOIC-8 D package is 22°C/W . In order to prevent the regulator from going into thermal shutdown, the case-to-ambient thermal resistance (θ_{ca}) must keep the junction temperature below 150°C . If the UCC284 is mounted on a 5 square inch pad of 1-ounce copper, for example, the thermal resistance (θ_{ja}) becomes $40\text{-}70^\circ\text{C/W}$. If a lower thermal resistance is required for the application, the device heat sinking needs to be improved.

When the UCC284 is in a pulsed mode, due to an overcurrent condition, the maximum average power dissipation is calculated as follows:

$$P_{avg} = [V_{IN}(V) - V_{OUT}(V)] \times I_{PEAK}(A) \times \left(\frac{t_{ON}(\text{seconds})}{40 \times t_{ON}(\text{seconds})} \right) \text{ Watts} \quad (11)$$

As seen in equation (10), the average power during a fault is reduced dramatically by the duty cycle, allowing the heat sink to be sized for normal operation. Although the peak power in the regulator during the t_{ON} period can be significant, the thermal mass of the package normally keeps the junction temperature from rising unless the t_{ON} period is increased to several milliseconds.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
UCC284SDR-5EP	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-55 to 100	284-5E	Samples
V62/09609-01XE	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-55 to 100	284-5E	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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TAPE AND REEL INFORMATION
REEL DIMENSIONS

TAPE DIMENSIONS


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UCC284SDR-5EP	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

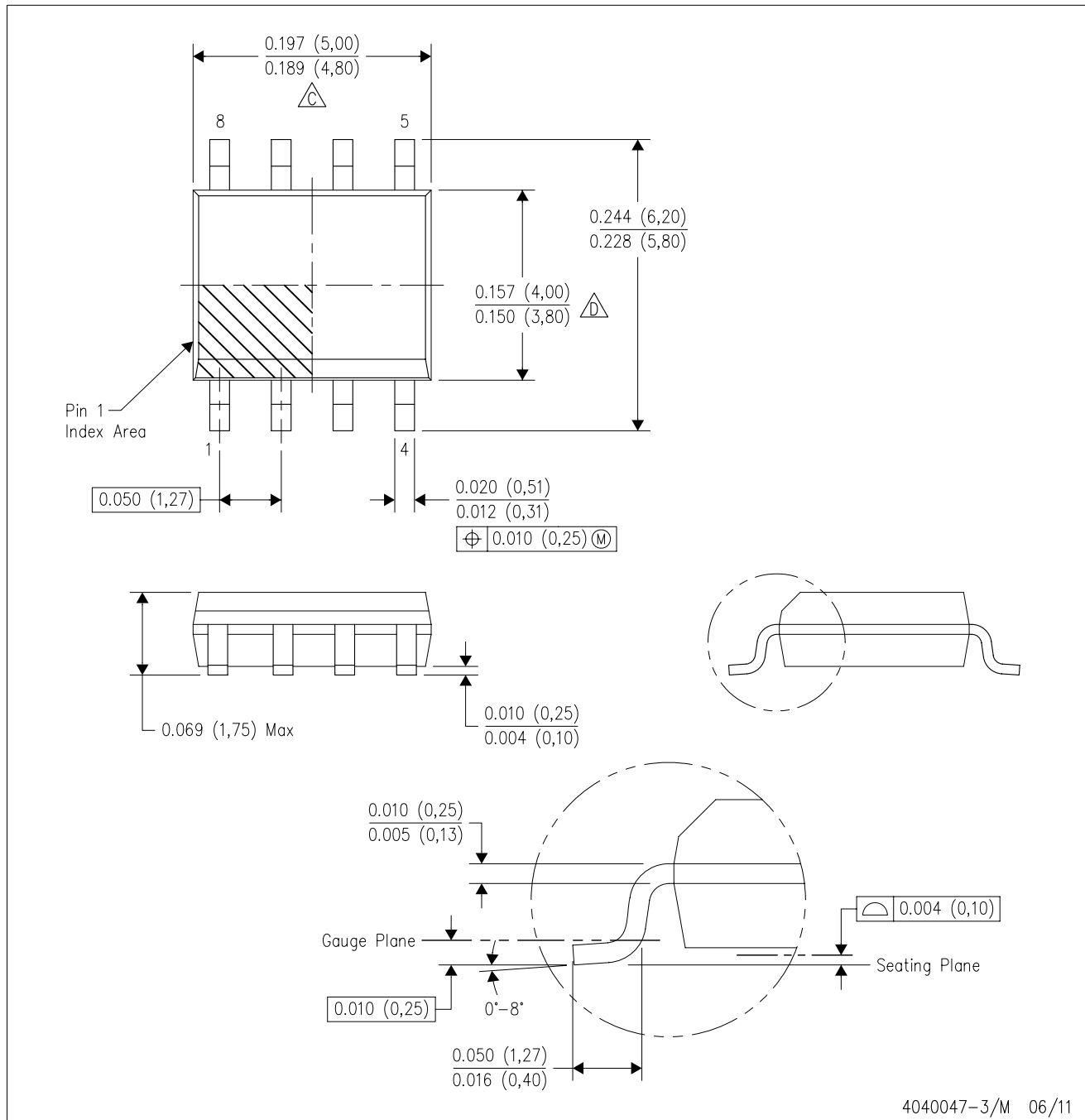
TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UCC284SDR-5EP	SOIC	D	8	2500	367.0	367.0	35.0

D (R-PDSO-G8)

PLASTIC SMALL OUTLINE

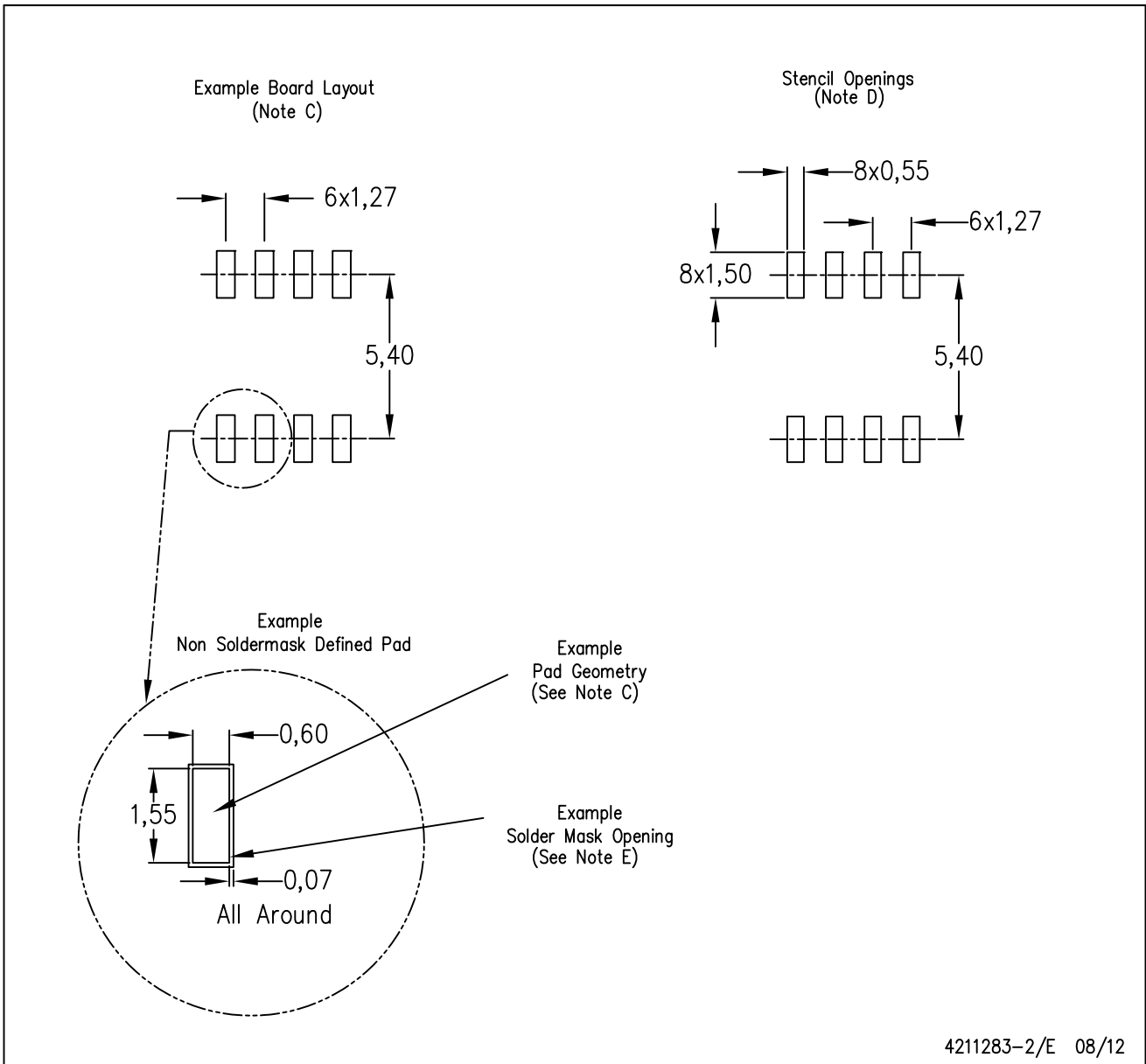


4040047-3/M 06/11

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 - Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AA.

D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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