

# UCC27528-Q1 Dual 5-A High-Speed Low-Side Gate Driver Based on CMOS Input Threshold Logic

## 1 Features

- Qualified for Automotive Applications
- AEC-Q100 Device Temperature Grade 1
- Industry-Standard Pin Out
- Two Independent Gate-Drive Channels
- 5-A Peak Source and Sink Drive Current
- CMOS Input Logic Threshold (Function of Supply Voltage on VDD Pins)
- Hysteretic Logic Thresholds for High Noise Immunity
- Independent Enable Function for Each Output
- Inputs and Enable Pin Voltage Levels Not Restricted by VDD Pin Bias Supply Voltage
- 4.5-V to 18-V Single Supply Range
- Outputs Held Low During VDD UVLO (Ensures Glitch-Free Operation at Power Up and Power Down)
- Fast Propagation Delays (17-ns Typical)
- Fast Rise and Fall Times (7-ns and 6-ns Typical)
- 1-ns Typical Delay Matching Between 2 Channels
- Outputs Held in Low When Inputs Floating
- SOIC-8 Package
- Operating Temperature Range of  $-40^{\circ}\text{C}$  to  $140^{\circ}\text{C}$
- $-5\text{-V}$  Negative Voltage Handling Capability on Input Pins

## 2 Applications

- Automotive
- Switch-Mode Power Supplies
- DC-to-DC Converters
- Motor Control, Solar Power
- Gate Drive for Emerging Wideband Gap Power Devices Such as GaN

## 3 Description

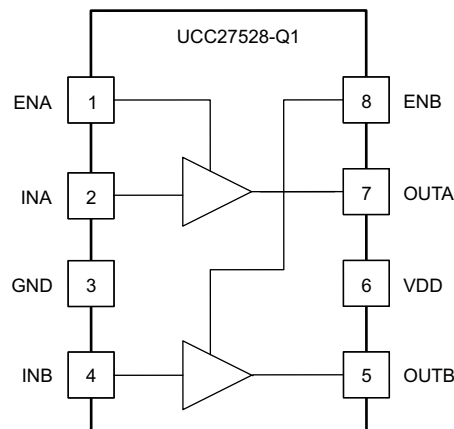
The UCC27528-Q1 device is a dual-channel, high-speed, low-side gate driver capable of effectively driving MOSFET and IGBT power switches. Using a design that inherently minimizes shoot-through current, the UCC27528-Q1 device can deliver high-peak current pulses of up to 5-A source and 5-A sink into capacitive loads along with rail-to-rail drive capability and extremely small propagation delay of 17 ns (typical). In addition, the drivers feature matched internal propagation delays between the two channels which are very well suited for applications requiring dual-gate drives with critical timing, such as synchronous rectifiers. The input pin thresholds are based on CMOS logic, which is a function of the VDD supply voltage. Wide hysteresis between the high and low thresholds offers excellent noise immunity. The enable pins are based on TTL and CMOS compatible logic, independent of the VDD supply voltage.

### Device Information<sup>(1)</sup>

PART NUMBER	PACKAGE	BODY SIZE (NOM)
UCC27528-Q1	SOIC (8)	4.90 mm x 3.91 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

### Dual Non-Inverting Inputs



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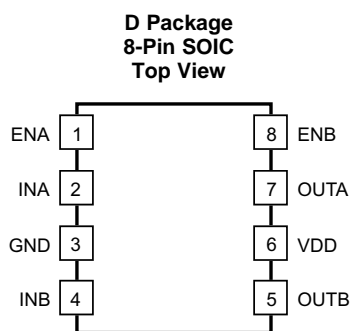
## 4 Revision History

DATE	REVISION	NOTES
December 2014	*	Initial release.

## 5 Description (continued)

The UCC27528-Q1 device is a dual noninverting driver. Internal pullup and pulldown resistors on the input pins of the UCC27528-Q1 device ensure that outputs are held low when input pins are in floating condition. The UCC27528-Q1 device features enable pins (ENA and ENB) for better control of the operation of the driver applications. The pins are internally pulled up to the VDD supply for active-high logic and can be left open for standard operation.

## 6 Pin Configuration and Functions



**Pin Functions**

PIN		I/O	DESCRIPTION
NO.	NAME		
1	ENA	I	Enable input for Channel A: ENA biased low Disables Channel A output regardless of INA state, ENA biased high or floating Enables Channel A output, ENA allowed to float.
2	INA	I	Input to Channel A: Non-Inverting Input in UCC27528-Q1, OUTA held low if INA is unbiased or floating.
3	GND	—	Ground: All signals referenced to this pin.
4	INB	I	Input to Channel B: Non-Inverting Input in UCC27528-Q1, OUTB held low if INB is unbiased or floating.
5	OUTB	O	Output of Channel B
6	VDD	I	Bias supply input
7	OUTA	O	Output of Channel A
8	ENB	I	Enable input for Channel B: ENB biased low Disables Channel B output regardless of INB state, ENB biased high or floating Enables Channel B output, ENB allowed to float.

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## 7 Specifications

### 7.1 Absolute Maximum Ratings<sup>(1)(2)</sup>

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Supply voltage range	VDD	-0.3	20	V
INA, INB, voltage <sup>(3)</sup>		-6.5	20	V
ENA, ENB voltage <sup>(3)</sup>		-0.3	20	V
OUTA, OUTB voltage	DC	-0.3	VDD + 0.3	V
	Repetitive pulse < 200 ns <sup>(4)</sup>	-2	VDD + 0.3	
Output continuous source and sink current	I <sub>OUT_DC</sub>		0.3	A
Output pulsed source and sink current (0.5 μs)	I <sub>OUT_pulsed</sub>		5	A
Operating virtual junction temperature, T <sub>J</sub>		-40	150	°C
Lead temperature	Soldering, 10 s		300	°C
	Reflow		260	
Storage temperature, T <sub>stg</sub>		-65	150	°C

- (1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltages are with respect to GND unless otherwise noted. Currents are positive into, negative out of the specified terminal. See Packaging Section of the datasheet for thermal limitations and considerations of packages.
- (3) The maximum voltage on the Input and Enable pins is not restricted by the voltage on the VDD pin.
- (4) Values are verified by characterization on bench.

### 7.2 ESD Ratings

		VALUE	UNIT
V <sub>(ESD)</sub> Electrostatic discharge	Human-body model (HBM), per AEC Q100-002 <sup>(1)</sup>	±4000	V
	Charged-device model (CDM), per AEC Q100-011	±1000	

- (1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

### 7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V <sub>DD</sub> Supply voltage		4.5	12	18	V
Input voltage	INA, INB	-5		18	V
Enable voltage	ENA and ENB	0		18	V
Operating junction temperature		-40		140	°C

### 7.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		D 8 PINS	UNIT
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	128	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	77.7	
R <sub>θJB</sub>	Junction-to-board thermal resistance	68.5	
Ψ <sub>JT</sub>	Junction-to-top characterization parameter	20.7	
Ψ <sub>JB</sub>	Junction-to-board characterization parameter	68	
R <sub>θJC(bot)</sub>	Junction-to-case (bottom) thermal resistance	n/a	

- (1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

## 7.5 Electrical Characteristics

$V_{DD} = 12\text{ V}$ ,  $T_A = T_J = -40\text{ }^\circ\text{C}$  to  $140\text{ }^\circ\text{C}$ ,  $1\text{-}\mu\text{F}$  capacitor from  $V_{DD}$  to GND. Currents are positive into, negative out of the specified terminal (unless otherwise noted.)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>BIAS CURRENTS</b>						
$I_{DD(\text{off})}$	Startup current	$V_{DD} = 3.4\text{ V}$ , $INA = V_{DD}$ , $INB = V_{DD}$	55	125	225	$\mu\text{A}$
		$V_{DD} = 3.4\text{ V}$ , $INA = \text{GND}$ , $INB = \text{GND}$	25	125	225	
<b>UNDERVOLTAGE LOCKOUT (UVLO)</b>						
$V_{ON}$	Supply start threshold	$T_J = 25\text{ }^\circ\text{C}$	3.91	4.2	4.5	V
		$T_J = -40\text{ }^\circ\text{C}$ to $140\text{ }^\circ\text{C}$	3.75	4.2	4.65	
$V_{OFF}$	Minimum operating voltage after supply start		3.6	3.9	4.4	
$V_{DD\_H}$	Supply voltage hysteresis		0.2	0.3	0.5	
<b>INPUTS (INA, INB)</b>						
$V_{IN\_H}$	Input signal high threshold	Output high for non-inverting input pins Output low for inverting input pins		55	70	$\%V_{DD}$
$V_{IN\_L}$	Input signal low threshold	Output low for non-inverting input pins Output high for inverting input pins	30	38		
$V_{IN\_HYS}$	Input hysteresis			17		
<b>ENABLE (ENA, ENB)</b>						
$V_{EN\_H}$	Enable signal high threshold	Output enabled	1.7	1.9	2.1	V
$V_{EN\_L}$	Enable signal low threshold	Output disabled	0.95	1.10	1.25	
$V_{EN\_HYS}$	Enable hysteresis		0.7	0.8	1.1	
<b>OUTPUTS (OUTA, OUTB)</b>						
$I_{SNK/SRC}$	Sink and source peak current <sup>(1)</sup>	$C_{LOAD} = 0.22\text{ }\mu\text{F}$ , $f_{SW} = 1\text{ kHz}$		$\pm 5$		A
$V_{DD}-V_{OH}$	High output voltage	$I_{OUT} = -10\text{ mA}$			0.075	V
$V_{OL}$	Low output voltage	$I_{OUT} = 10\text{ mA}$			0.01	
$R_{OH}$	Output pullup resistance <sup>(2)</sup>	$I_{OUT} = -10\text{ mA}$	2.5	5	7.5	$\Omega$
$R_{OL}$	Output pulldown resistance	$I_{OUT} = 10\text{ mA}$	0.15	0.5	1	$\Omega$

(1) Ensured by design.

(2)  $R_{OH}$  represents on-resistance of only the P-Channel MOSFET device in pullup structure of UCC27528-Q1 output stage.

## 7.6 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_R$	Rise time	$C_{LOAD} = 1.8\text{ nF}$ , $V_{DD} = 10\text{ V}$		7		ns
$t_F$	Fall time	$C_{LOAD} = 1.8\text{ nF}$ , $V_{DD} = 10\text{ V}$		6		ns
$t_M$	Delay matching between 2 channels	$INA = INB$ , $OUTA$ and $OUTB$ at 50% transition point, $V_{DD} = 10\text{ V}$		1	4	ns
$t_{PW}$	Minimum input pulse width that changes the output state	$V_{DD} = 10\text{ V}$		15		ns
$t_{D1}$ , $t_{D2}$	Input to output propagation delay, See <a href="#">Figure 2</a> .	$C_{LOAD} = 1.8\text{ nF}$ , 7-V input pulse, $V_{DD} = 10\text{ V}$	6	17	26	ns
$t_{D3}$ , $t_{D4}$	EN to output propagation delay, See <a href="#">Figure 1</a> .	$C_{LOAD} = 1.8\text{ nF}$ , 7-V enable pulse, $V_{DD} = 10\text{ V}$	6	13	23	ns

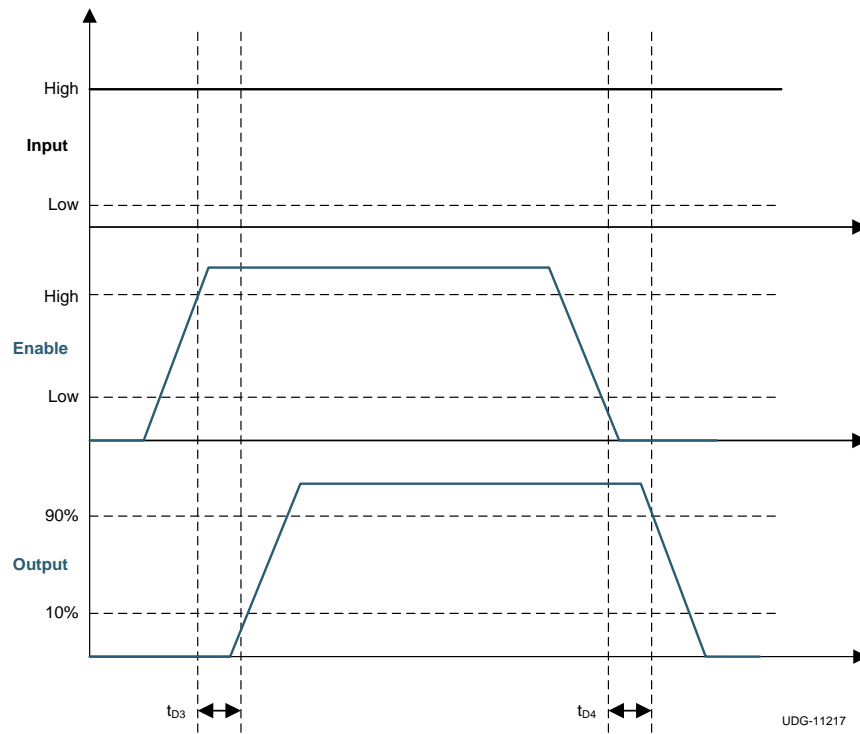


Figure 1. Enable Function (Non-Inverting Input Driver Operation)

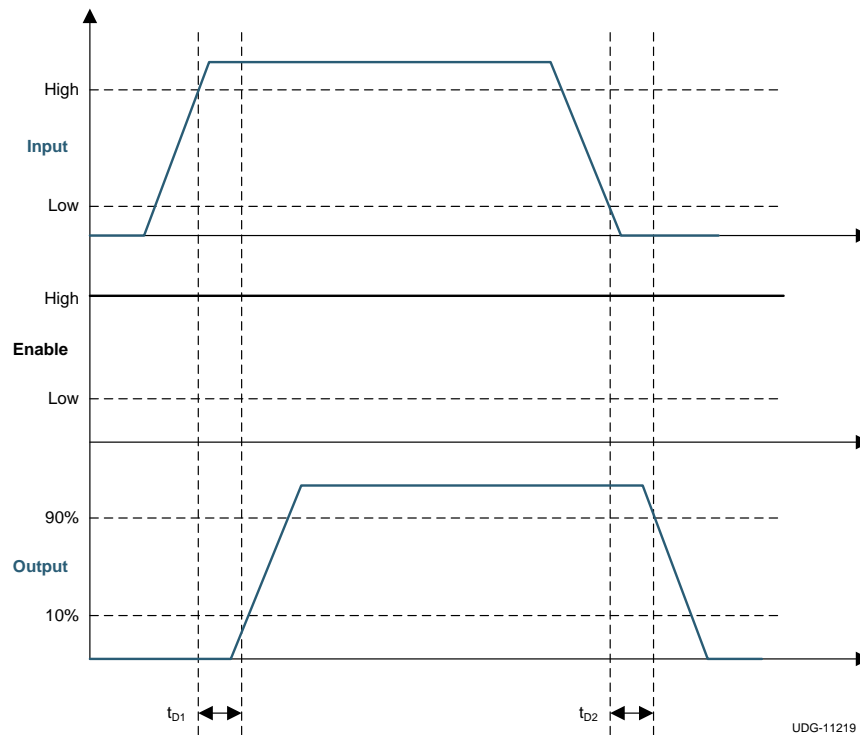
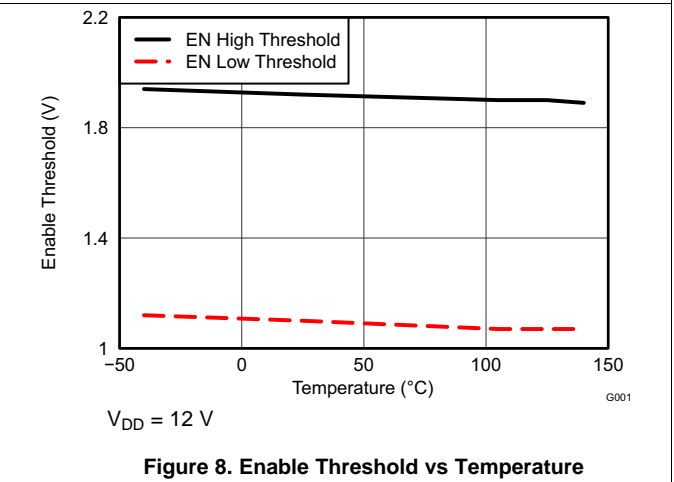
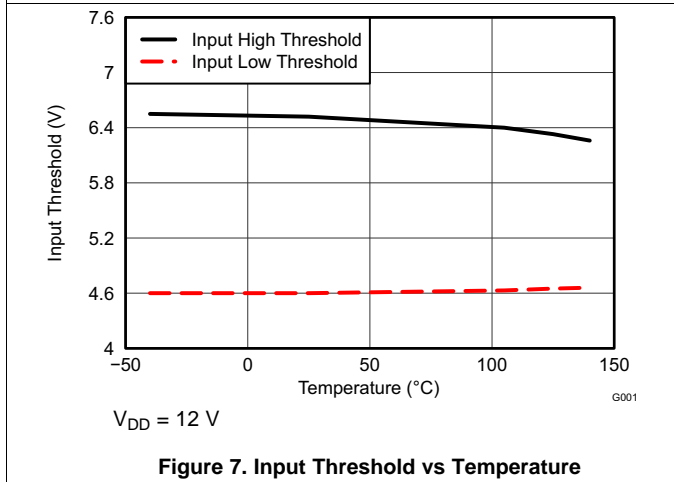
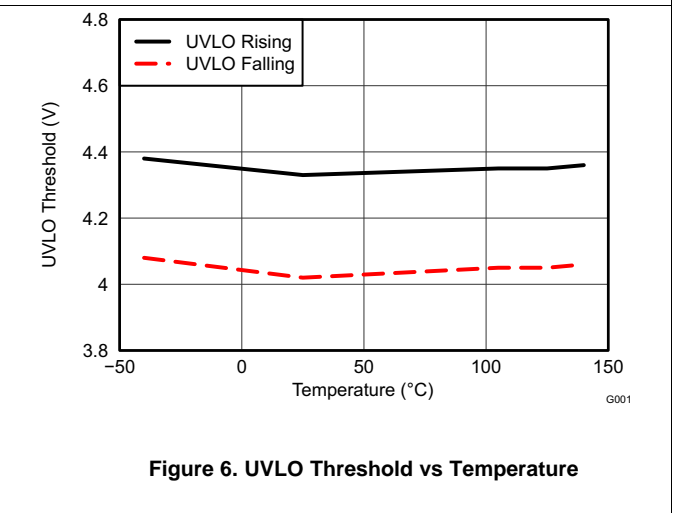
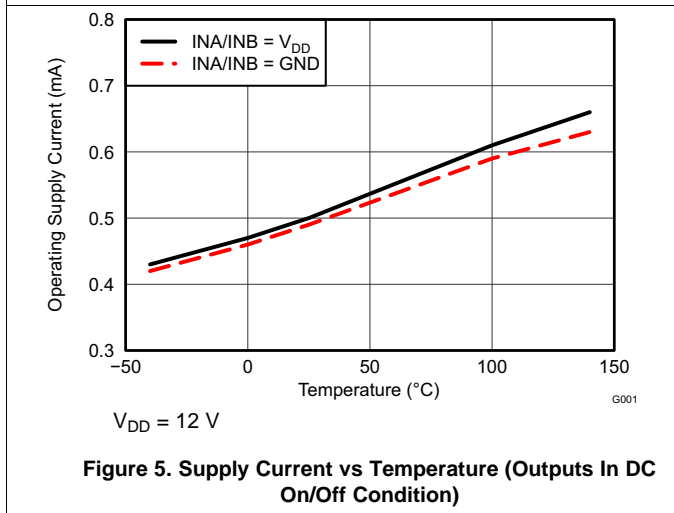
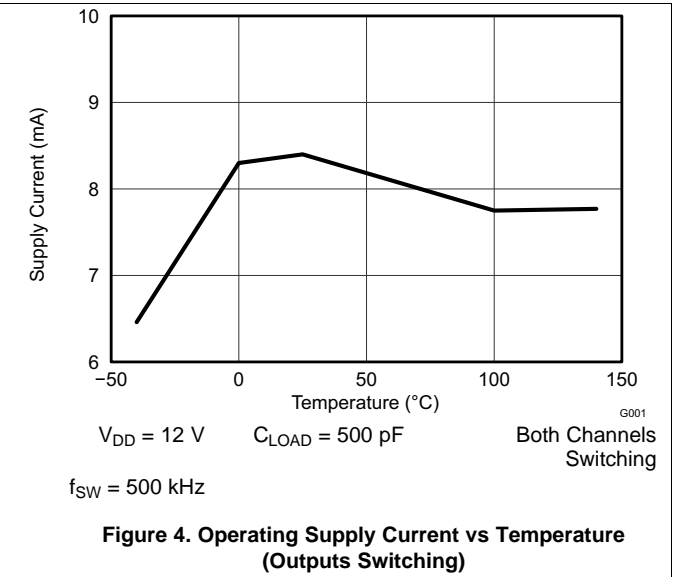
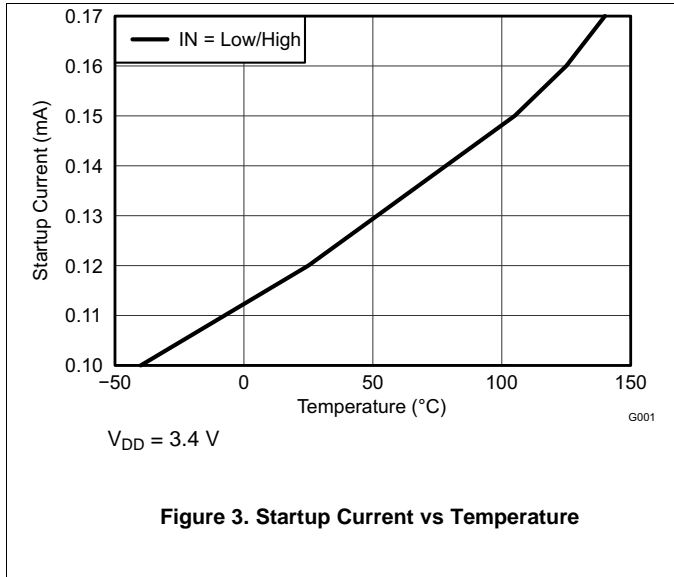


Figure 2. Non-Inverting Input Driver Operation

7.7 Typical Characteristics



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Typical Characteristics (continued)

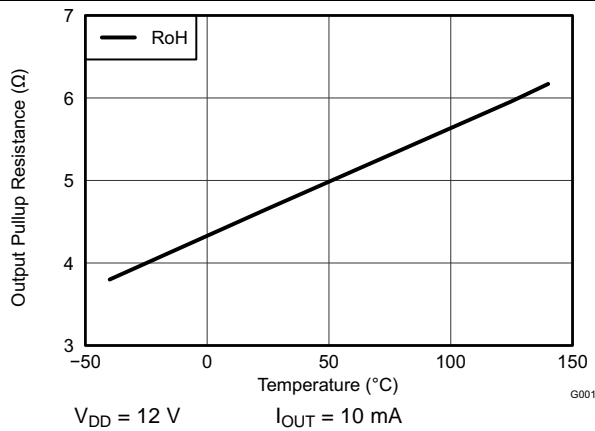


Figure 9. Output Pullup Resistance vs Temperature

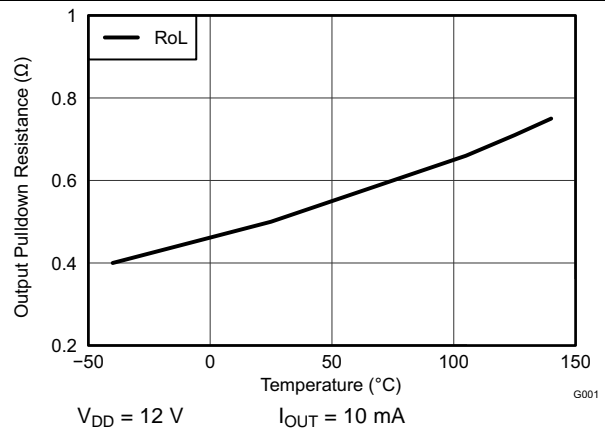


Figure 10. Output Pulldown Resistance vs Temperature

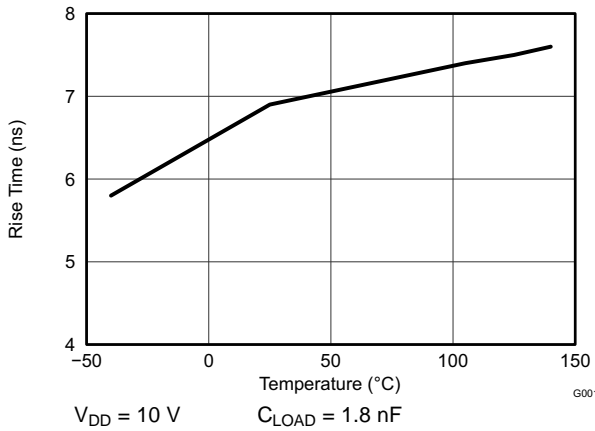


Figure 11. Rise Time vs Temperature

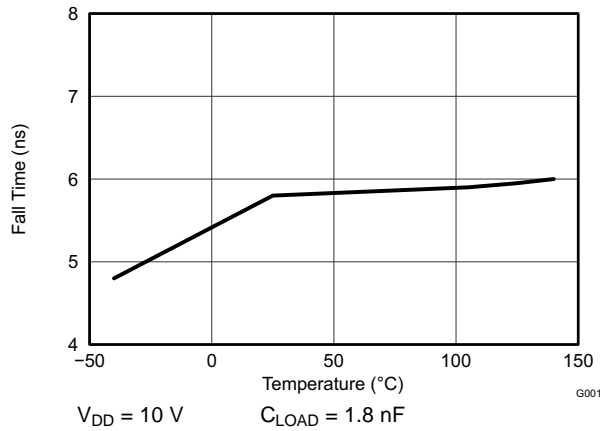


Figure 12. Fall Time vs Temperature

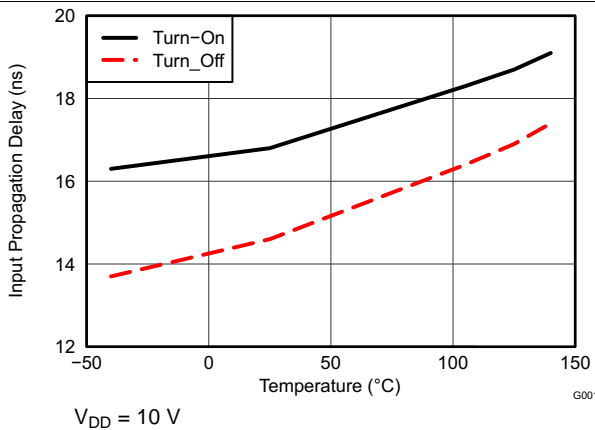


Figure 13. Input To Output Propagation Delay vs Temperature

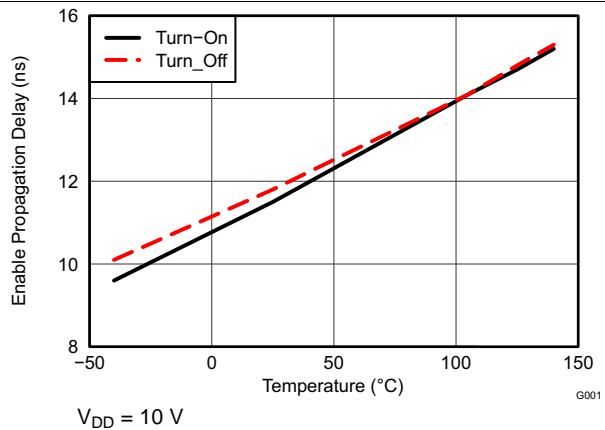


Figure 14. En To Output Propagation Delay vs Temperature

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Typical Characteristics (continued)

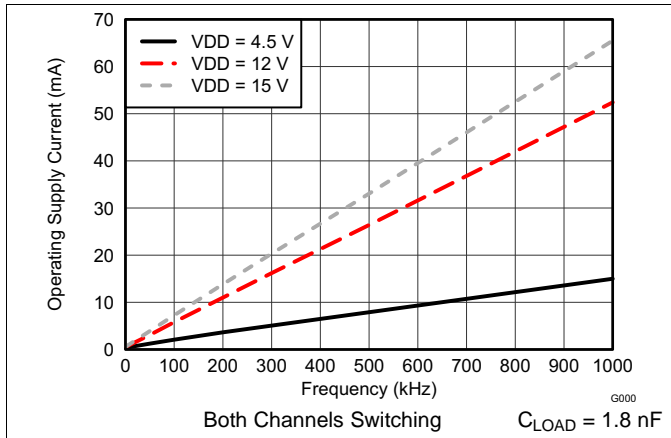


Figure 15. Operating Supply Current vs Frequency

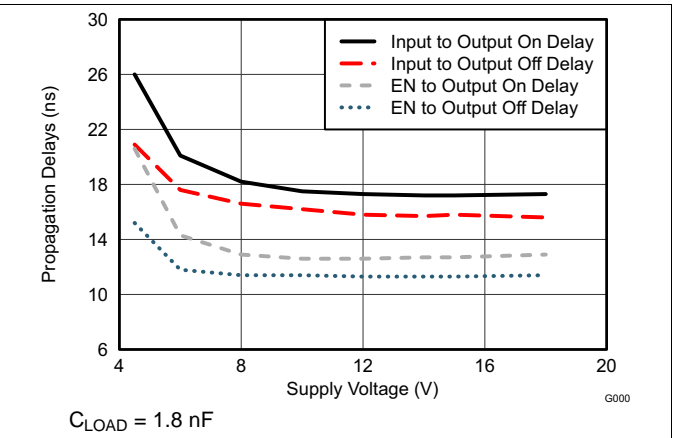


Figure 16. Propagation Delays vs Supply Voltage

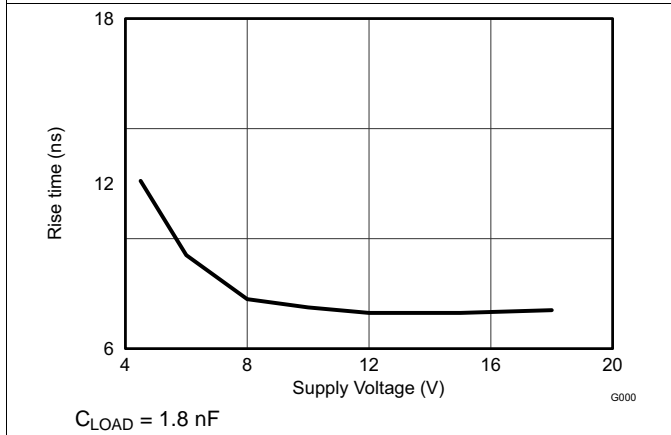


Figure 17. Rise Time vs Supply Voltage

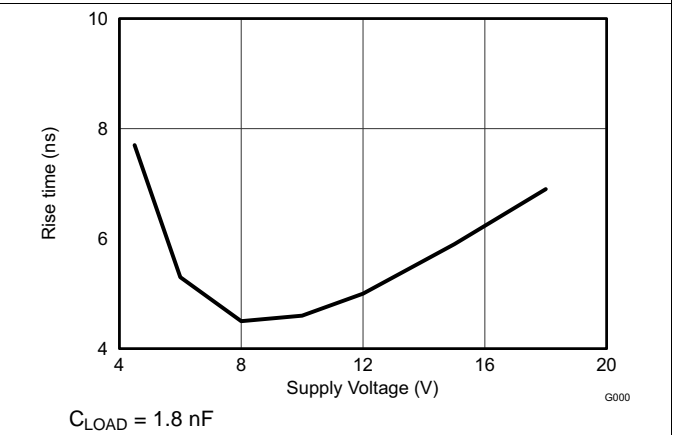


Figure 18. Fall Time vs Supply Voltage

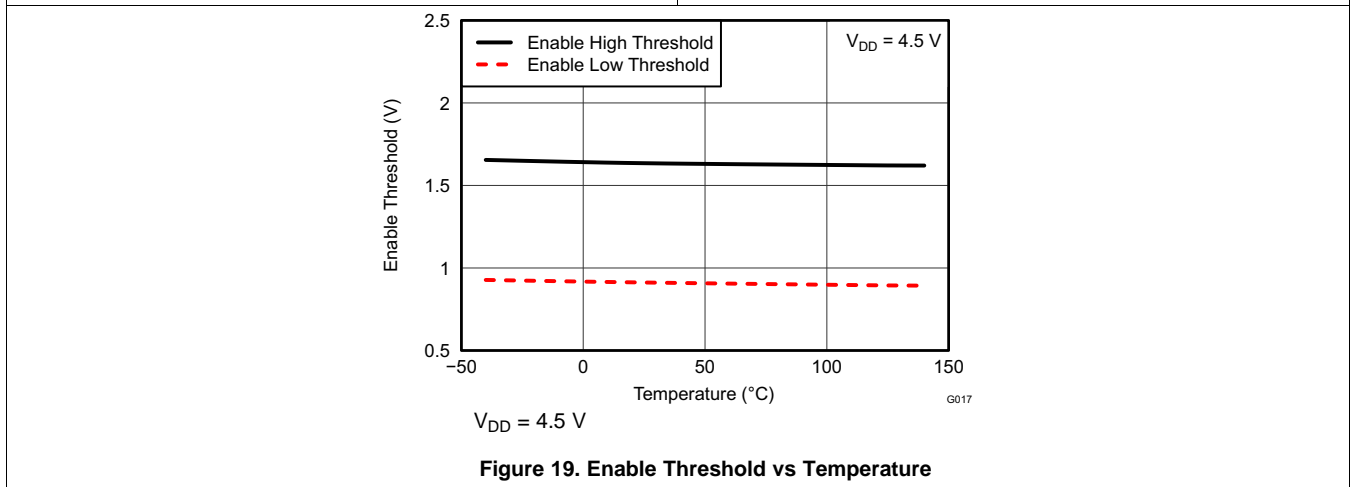


Figure 19. Enable Threshold vs Temperature

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## 8 Detailed Description

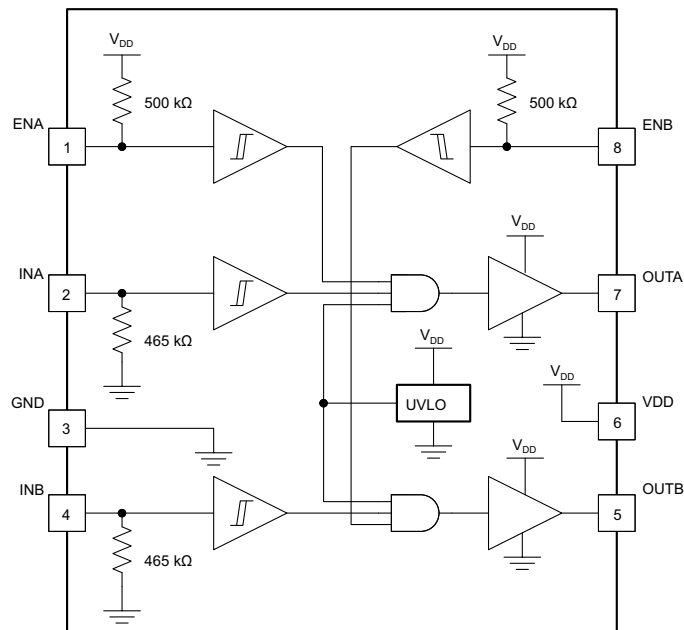
### 8.1 Overview

The UCC27528-Q1 device represents Texas Instruments' latest generation of dual-channel, low-side high-speed gate driver devices featuring 5-A source- and sink current capability, industry best-in-class switching characteristics, and many other features listed in [Table 1](#) all of which combine to provide efficient, robust, and reliable operation in high-frequency switching power circuits.

**Table 1. UCC27528-Q1 Features and Benefits**

FEATURE	BENEFIT
Best-in-class 13-ns (typical) propagation delay	Extremely low pulse-transmission distortion
1-ns (typical) delay matching between channels	Ease of paralleling outputs for higher (2x) current capability, ease of driving parallel power switches
Expanded VDD operating range of 4.5 V to 18 V	Flexibility in system design
Expanded operating temperature range of -40 °C to 140 °C (See the <a href="#">Electrical Characteristics</a> table)	
VDD UVLO protection	Outputs are held low in UVLO condition, which ensures predictable, glitch-free operation at power up and power down
Outputs held low when the input pins (INx) are in floating condition	Feature which is specifically useful in passing abnormal condition tests during certification
Outputs enabled when the enable pins (ENx) are in floating condition	Pin-to-pin compatibility with the UCC2732x family of device from TI, in designs where pin 1 and pin 8 are in the floating condition
CMOS input threshold logic	Enhanced noise immunity, higher threshold level and wider hysteresis which is a function of the VDD supply voltage and ability to employ RCD delay circuits on input pins.
The input and enable pins are able to handle voltage levels not restricted by VDD pin bias voltage	System simplification, specifically related to auxiliary bias supply architecture

### 8.2 Functional Block Diagram



## 8.3 Feature Description

### 8.3.1 $V_{DD}$ and Undervoltage Lockout

The UCC27528-Q1 device has internal undervoltage-lockout (UVLO) protection feature on the VDD pin supply-circuit blocks. When the VDD supply is rising and the level is still below UVLO threshold, the circuit (as shown in the [Functional Block Diagram](#)) holds the output low, regardless of the status of the inputs. The UVLO threshold is 4.25 V (typical) with 350-mV hysteresis (typical). This hysteresis helps prevent chatter when low VDD supply voltages have noise from the power supply and also when droops in the VDD bias voltage occur when the system commences switching and a sudden increase in the  $I_{DD}$  current occurs. The ability to operate at low-voltage levels, such as below 5 V, along with best-in-class switching characteristics, is well suited for driving emerging GaN-power semiconductor devices.

For example, at power-up, the UCC27528-Q1 driver device output remains low until the  $V_{DD}$  voltage reaches the UVLO threshold if the enable pin is active or floating. The magnitude of the OUT signal rises with  $V_{DD}$  until steady-state  $V_{DD}$  is reached. The non-inverting operation in [Figure 20](#) shows that the output remains low until the UVLO threshold is reached. The output is then in-phase with the input.

Because the device draws current from the VDD pin to bias all internal circuits, for the best high-speed circuit performance, two VDD bypass capacitors are recommended to prevent noise problems. The use of surface-mount components is highly recommended. A 0.1- $\mu$ F ceramic capacitor should be located as close as possible to the VDD to GND pins of the gate-driver device. In addition, to help deliver the high-current peaks required by the load, a larger capacitor (such as a 1- $\mu$ F capacitor) with relatively low ESR should be connected in parallel and close proximity. The parallel combination of capacitors should present a low impedance characteristic for the expected current levels and switching frequencies in the application.

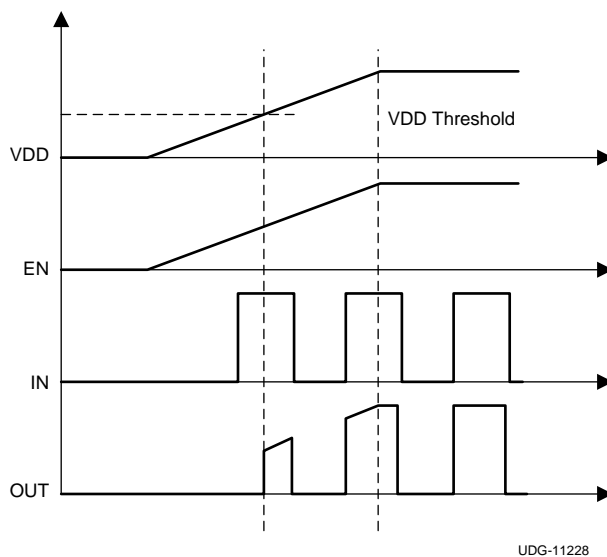


Figure 20. Power-Up Non-Inverting Driver

### 8.3.2 Operating Supply Current

The UCC27528-Q1 device features very low quiescent  $I_{DD}$  currents. [Figure 3](#), [Figure 4](#), and [Figure 5](#) list the typical operating supply current in the UVLO state and fully-on state (under static and switching conditions). The  $I_{DD}$  current that is present when the device is fully on and the outputs are in a static state (DC high or DC low, see [Figure 4](#)) represents lowest quiescent  $I_{DD}$  current when all the internal logic circuits of the device are fully operational. The total supply current is the sum of the quiescent  $I_{DD}$  current, the average  $I_{OUT}$  current from switching, and any current related to pullup resistors on the enable pins and inverting input pins.

[Figure 15](#) shows a complete characterization of the  $I_{DD}$  current as a function of switching frequency at different  $V_{DD}$  bias voltages under 1.8-nF switching load in both channels. The strikingly linear variation and close correlation with the theoretical value of the average  $I_{OUT}$  indicates negligible shoot-through inside the gate-driver device attesting to the high-speed characteristics.

### 8.3.3 Input Stage

The input pins of UCC27528-Q1 gate driver device are based on CMOS input threshold logic. In CMOS input threshold logic the threshold voltage level is a function of the bias voltage on the VDD pin of the device. The typical high threshold is 55% of the VDD supply voltage and the typical low threshold is 38% of the VDD supply voltage. Built-in hysteresis is available which is typically 17% of the VDD supply voltage.

In most applications, the absolute value of the threshold voltage offered by the CMOS logic is higher (for example,  $V_{IN\_H} = 5.5\text{ V}$  if  $V_{DD} = 10\text{ V}$ ) than what is offered by the more common TTL and CMOS-compatible input threshold logic where  $V_{IN\_H}$  is typically less than 3 V. The same is true of the input-threshold hysteresis parameter as well. This feature offers the following benefits:

- Better noise immunity which is desirable in high power systems.
- Ability to accept slow dV/dt input signals, which allows designers to use RCD circuits on the input pin to program propagation delays in the application, as shown in [Figure 21](#).

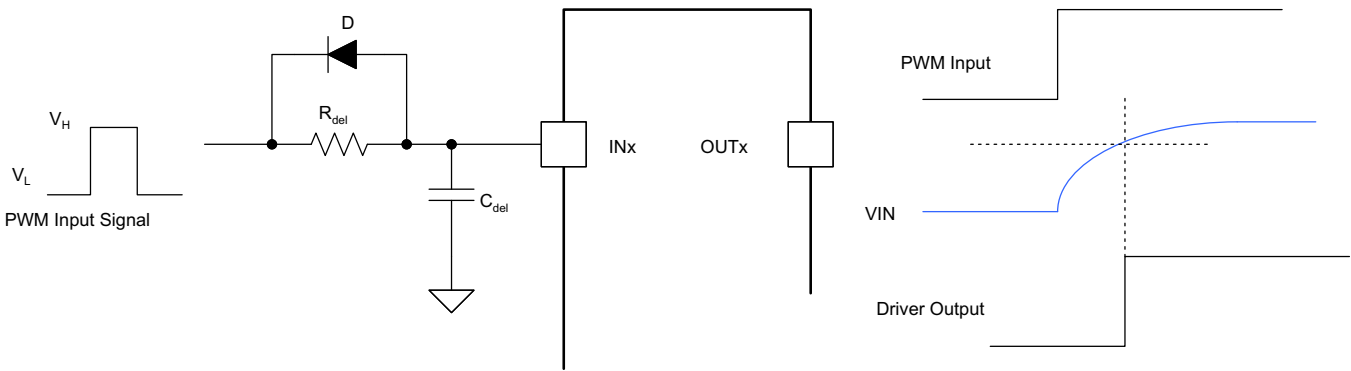


Figure 21. Using RCD Circuits

$$t_{del} = -R_{del}C_{del} \times \ln\left(\frac{V_L - V_{IN\_H}}{V_H - V_L} + 1\right) \tag{1}$$

The UCC27528-Q1 device features an important feature, whenever any of the input pins is in a floating condition, the output of the respective channel is held in the low state. Holding the respective channel in the low state is achieved by using GND pulldown resistors on all the non-inverting input pins (INA, INB), as shown in the [Functional Block Diagram](#).

- To drive channel x ( $x = A$  or  $B$ ) in a non-inverting configuration, apply the PWM control input signal to one of the IN pins. In this case, the unused IN pin must be biased low (for example, tied to GND) to enable the output of this channel.
  - Alternately, the unused IN pin can be used to implement the enable and disable function using an external logic signal. The output pin is disabled when the unused IN pin is biased high and the OUT pin is enabled when the unused IN pin is biased low.

See [Table 2](#) and [Figure 24](#) for additional clarification.

### 8.3.4 Enable Function

The enable function is an extremely beneficial feature in gate driver devices, especially for certain applications such as synchronous rectification where the driver outputs can be disabled in light-load conditions to prevent negative current circulation and to improve light-load efficiency.

The UCC27528-Q1 device has independent enable pins, ENx, for exclusive control of the operation of each driver channel. The enable pins are based on a non-inverting configuration (active-high operation). Therefore, when the ENx pins are driven high the drivers are enabled and when ENx pins are driven low and the drivers are disabled. Similar to the input pins, the enable pins are also based on a TTL and CMOS-compatible input threshold logic that is independent of the supply voltage and can be effectively controlled using logic signals from 3.3-V and 5-V microcontrollers. The UCC27528-Q1 device also features tight control of the enable-function threshold voltage levels which eases system design considerations and ensures stable operation across temperature (see [Figure 8](#)). The ENx pins are internally pulled up to the VDD supply using pullup resistors as a result of which the outputs of the device are enabled in the default state. Therefore, the ENx pins can be left

floating or not connected (NC) for standard operation in which case the enable feature is not needed. This ability allows the UCC27528-Q1 device to be pin-to-pin compatible with TI's previous-generation drivers, the UCC27323, UCC273234, and UCC273235 device, where pin 1 and pin 8 are NC pins. If the Channel A and Channel B inputs and outputs are connected in parallel to increase the driver current capacity, the ENA and ENB pins should be connected and driven together.

### 8.3.5 Output Stage

The UCC27528-Q1 output stage features a unique architecture on the pullup structure which delivers the highest-peak source current when it is most needed during the Miller plateau region of the power-switch turn-on transition (when the power switch drain and collector voltage experiences  $dV/dt$ ). The output-stage pullup structure features a P-Channel MOSFET and an additional N-Channel MOSFET in parallel. The N-Channel MOSFET provides a brief boost in the peak sourcing current which enables fast turn-on. This boost is accomplished by briefly turning on the N-Channel MOSFET during a short time frame when the output is changing state from low to high.

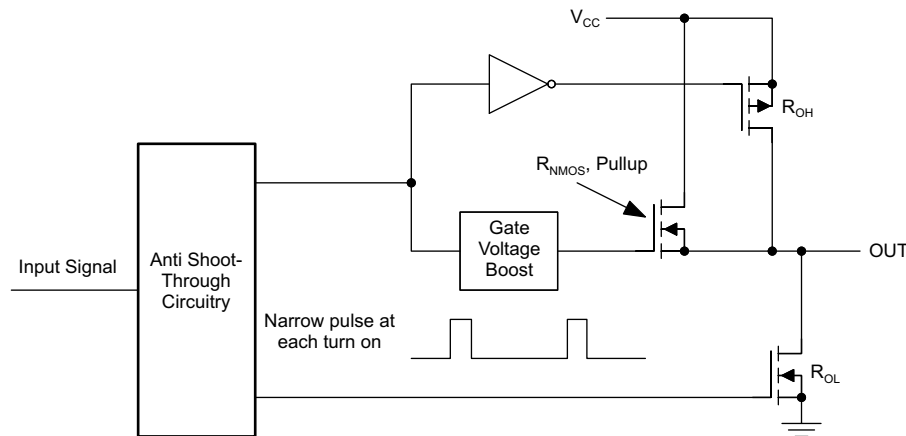


Figure 22. UCC27528-Q1 Gate Driver Output Structure

The  $R_{OH}$  parameter (see the [Electrical Characteristics](#) table) is a DC measurement and is representative of the on-resistance of the P-Channel device only because the N-Channel device is held in the off state in DC condition and is turned on only for a short time frame when the output changes state from low to high. Therefore, the effective resistance of UCC27528-Q1 pullup stage during turn-on instant is much lower than what is represented by  $R_{OH}$  parameter.

The pulldown structure in the UCC27528-Q1 device is simply composed of a N-Channel MOSFET. The  $R_{OL}$  parameter (see the [Electrical Characteristics](#) table), which is also a DC measurement, is representative of the impedance of the pulldown stage in the device. In the UCC27528-Q1 device, the effective resistance of the hybrid pullup structure during turnon is estimated on design considerations as approximately  $1.5 \times R_{OL}$ .

Each output stage in the UCC27528-Q1 device is capable of supplying 5-A peak source and 5-A peak sink current pulses. The output voltage swings between VDD and GND, providing rail-to-rail operation because of the MOS output stage which delivers very-low dropout. The presence of the MOSFET body diodes also offers low impedance to switching overshoots and undershoots which means that in many cases, external Schottky diode clamps can be eliminated. The outputs of these drivers are designed to withstand 500-mA reverse current without either damage to the device or logic malfunction.

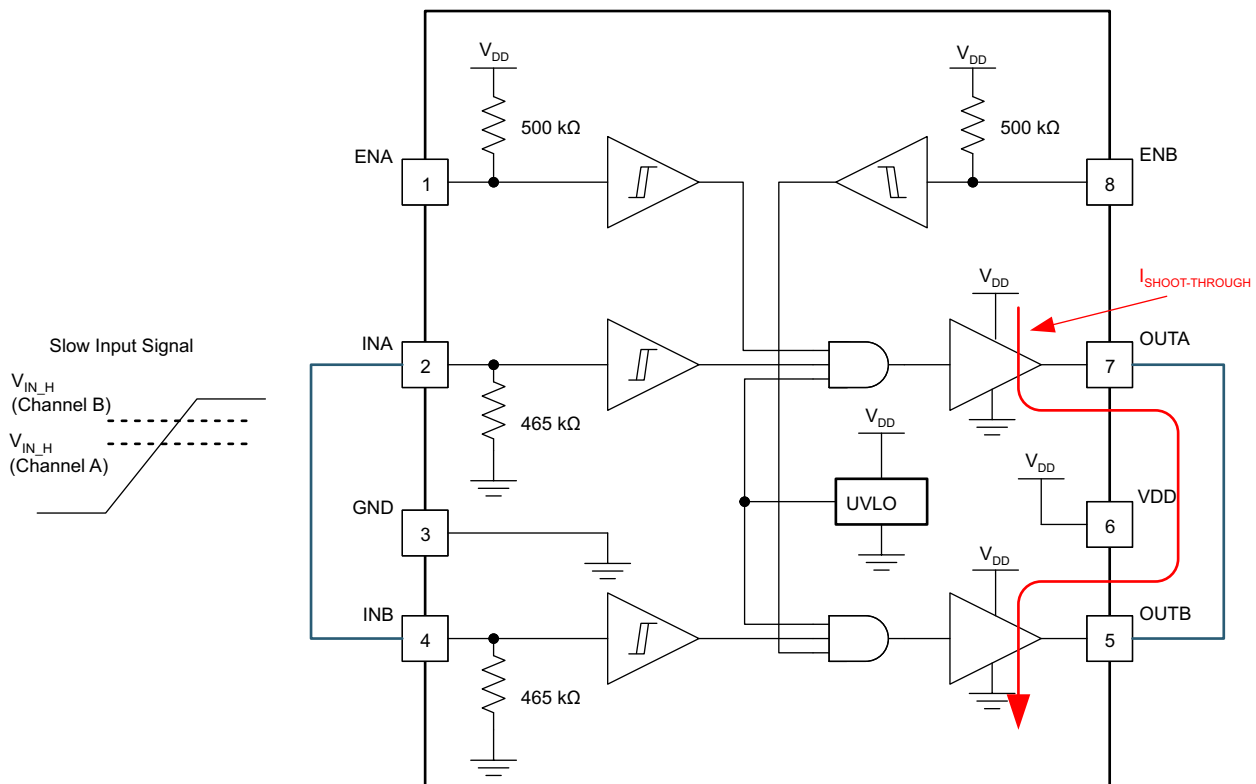
The UCC27528-Q1 device is particularly suited for dual-polarity, symmetrical drive-gate transformer applications where the primary winding of transformer driven by the OUTA and OUTB pins, with the inputs INA and INB driven complementary to each other. The device is well suited for these applications because of the extremely low dropout offered by the MOS output stage of the device, both during high ( $V_{OH}$ ) and low ( $V_{OL}$ ) states along with the low impedance of the driver output stage, all of which allow alleviate concerns regarding transformer demagnetization and flux imbalance. The low propagation delays also ensure accurate reset for high-frequency applications.

For applications that have zero voltage switching during power MOSFET turn-on or turn-off interval, the driver supplies high-peak current for fast switching even though the miller plateau is not present. This situation often occurs in synchronous rectifier applications because the body diode is generally conducting before power MOSFET is switched on.

### 8.3.6 Low Propagation Delays and Tightly Matched Outputs

The UCC27528-Q1 driver devices offer a very low propagation delay of 17-ns (typical) between input and output which offers lowest level of pulse transmission distortion available in the industry for high-frequency switching applications. For example in synchronous rectifier applications, the SR MOSFETs can be driven with very low distortion when a single driver device is used to drive both the SR MOSFETs. Further, the driver devices also feature an extremely accurate, 1-ns (typ) matched internal propagation delays between the two channels which is beneficial for applications requiring dual gate drives with critical timing. For example in a PFC application, a pair of paralleled MOSFETs may be driven independently using each output channel, which the inputs of both channels are driven by a common control signal from the PFC controller device. In this case the 1-ns delay matching ensures that the paralleled MOSFETs are driven in a simultaneous fashion with the minimum of turn-on delay difference.

Since the CMOS input threshold of UCC27528-Q1 allows the use of slow dV/dt input signals, when paralleling outputs for obtaining higher peak output current capability, it is recommended to connect external gate resistors directly to the output pins to avoid shoot-through current conduction between the 2 channels, as shown in Figure 23. While the two channels are inherently very well matched (4-ns Max propagation delay), it should be noted that there may be differences in the input threshold voltage level between the two channels or differences in the input signals which can cause the delay between the two outputs.



**Figure 23. Slow Input Signal May Cause Shoot-Through Between Channels During Paralleling**

## 8.4 Device Functional Modes

The device operates in normal mode and UVLO mode. See the *V<sub>DD</sub> and Undervoltage Lockout* section for information on the UVLO operation mode. In the normal mode the output state is dependent on the state of the IN pins. [Table 2](#) lists the output states for different input-pin combinations.

**Table 2. Device Logic Table**

ENA	ENB	INA	INB	OUTA	OUTB
H	H	L	L	L	L
H	H	L	H	L	H
H	H	H	L	H	L
H	H	H	H	H	H
L	L	Any	Any	L	L
Any	Any	x <sup>(1)</sup>	x <sup>(1)</sup>	L	L
x <sup>(1)</sup>	x <sup>(1)</sup>	L	L	L	L
x <sup>(1)</sup>	x <sup>(1)</sup>	L	H	L	H
x <sup>(1)</sup>	x <sup>(1)</sup>	H	L	H	L
x <sup>(1)</sup>	x <sup>(1)</sup>	H	H	H	H

(1) Floating condition

## 9 Application and Implementation

### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

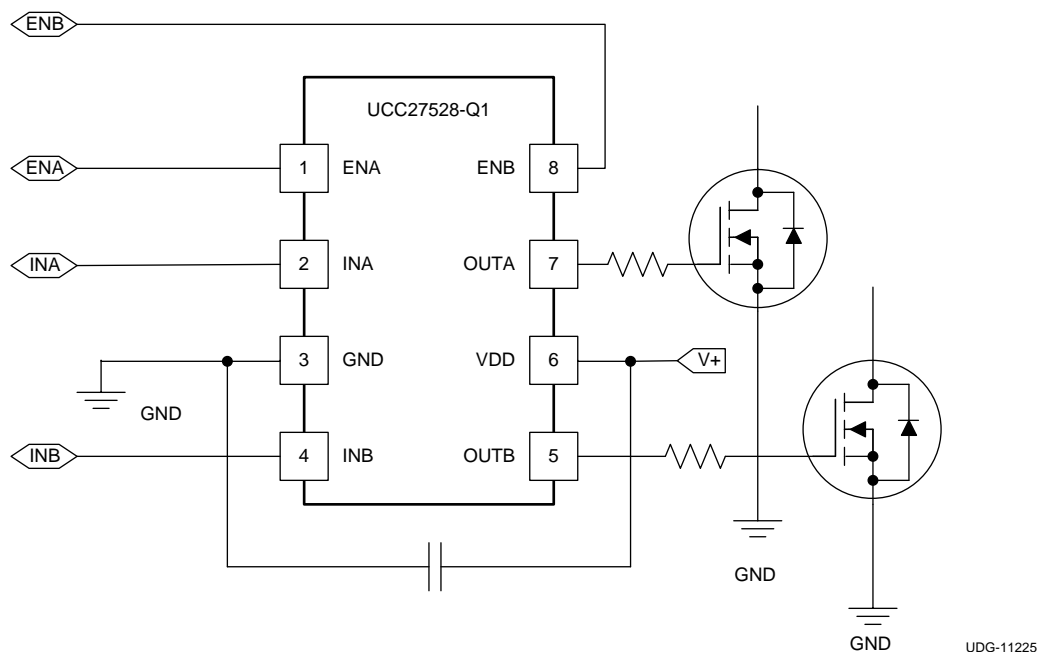
### 9.1 Application Information

High-current gate-driver devices are required in switching power applications for a variety of reasons. To implement fast switching in power devices and reduce associated switching power losses, a powerful gate-driver device can be employed between the PWM output of control devices and the gates of the power semiconductor devices.

Furthermore, gate driver devices are indispensable when having the PWM-controller device directly drive the gates of the switching devices is not feasible. With the advent of digital power, this situation is often encountered because the PWM signal from the digital controller is typically a 3.3-V logic signal which is not capable of effectively turning on a power switch. A level shifting circuitry is required to boost the 3.3-V signal to the gate-drive voltage (such as 12 V) to fully turn on the power device and minimize conduction losses. Traditional buffer drive circuits based on NPN and PNP bipolar transistors in totem-pole arrangement are emitter follower configurations. These circuits prove inadequate with digital power because they lack level-shifting capability.

Gate driver devices effectively combine both the level-shifting and buffer drive functions. Gate driver devices also satisfy other needs such as minimizing the effect of high-frequency switching noise by locating the high-current driver physically close to the power switch, driving gate drive transformers and controlling floating power device gates which reduces power dissipation and thermal stress in controller devices by moving gate charge power losses into itself. In summary Gate-driver devices are an extremely important component in switching power combining benefits of high performance, low cost, component count, board-space reduction, and simplified system design.

### 9.2 Typical Application



**Figure 24. UCC27528-Q1 Typical Application Diagram**

## Typical Application (continued)

### 9.2.1 Design Requirements

When selecting the proper gate driver device for an end application, some design considerations must be evaluated first to make the most appropriate selection. Among these considerations are input-to-output Logic, enable and disable function, supply voltage (VDD), propagation delay, and power dissipation.

The design requirements include the following:

- Supply voltage ( $V_{DD}$ )
- Type of input threshold (CMOS or TTL)
- Propagation delay
- Delay matching
- Peak drive current
- Enable function (whether or not it exists)
- Operating temperature range

### 9.2.2 Detailed Design Procedure

#### 9.2.2.1 Input-to-Output Logic

The design should specify which type of input-to-output configuration should be used. The UCC27528-Q1 device can only provide dual non-inverting input-to-output with enable control.

#### 9.2.2.2 Enable and Disable Function

Certain applications demand independent control of the output state of the driver. The UCC27528-Q1 device offers two independent enable pins ENx pins for exclusive control of each driver channels as listed in [Table 2](#). The ENA, ENB pins in the UCC27528-Q1 device can be in the floating condition during standard operation with the outputs enabled.

#### 9.2.2.3 VDD Bias Supply Voltage

The bias supply voltage to be applied to the VDD pin of the device should never exceed the values listed in the [Recommended Operating Conditions](#) table. However, different power switches demand different voltage levels to be applied at the gate terminals for effective turnon and turnoff. With certain power switches, a positive gate voltage may be required for turnon and a negative gate voltage may be required for turnoff, in which case the VDD bias supply equals the voltage differential. With a wide operating range from 4.5 V to 18 V, the UCC27528-Q1 device can be used to drive a variety of power switches, such as Si MOSFETs (for example,  $V_{GS} = 4.5\text{ V}$ , 10V, 12 V), IGBTs ( $V_{GE} = 15\text{ V}$ , 18 V), and wide-bandgap power semiconductors (such as GaN, certain types of which allow no higher than 6 V to be applied to the gate pins).

#### 9.2.2.4 Propagation Delay

The acceptable propagation delay from the gate driver is dependent on the switching frequency at which it is used and the acceptable level of pulse distortion to the system. The UCC27528-Q1 device features fast 17-ns (typical) propagation delays which ensures very-little pulse distortion and allows operation at very high-frequencies. See the [Switching Characteristics](#) table for the propagation and switching characteristics of the UCC27528-Q1 device. For certain application that require programmable propagation delay, The UCC27528-Q1 device can accept slow  $dv/dt$  input signals which allows designers to use RCD circuits on the input pin to program propagation as shown in [Figure 21](#).

## Typical Application (continued)

### 9.2.2.5 Drive Current and Power Dissipation

The UCC27528-Q1 driver device is capable of delivering 5 A of current to a MOSFET gate for a period of several hundred nanoseconds at  $V_{DD} = 12$  V. High peak current is required to quickly turn on the device. Then, to turn off the device, the driver is required to sink a similar amount of current to ground. This process repeats at the operating frequency of the power device. The power dissipated in the gate-driver device package depends on the following factors:

- The gate charge required of the power MOSFET (usually a function of the drive voltage  $V_{GS}$ , which is very close to input bias supply voltage  $V_{DD}$  because of low  $V_{OH}$  drop-out)
- Switching frequency
- Use of external gate resistors

Because the UCC27528-Q1 device features very-low quiescent currents and internal logic to eliminate any shoot-through in the output driver stage, the effect on the power dissipation within the gate driver can be safely assumed to be negligible.

When a driver device is tested with a discrete, capacitive load, calculating the power that is required from the bias supply fairly simple. Use [Equation 2](#) to calculate the energy that must be transferred from the bias supply to charge the capacitor.

$$E_G = \frac{1}{2} C_{LOAD} V_{DD}^2$$

where

- $C_{LOAD}$  is load capacitor
  - $V_{DD}$  is bias voltage feeding the driver
- (2)

An equal amount of energy is dissipated when the capacitor is charged which leads to a total power loss given by [Equation 3](#).

$$P_G = C_{LOAD} V_{DD}^2 f_{SW}$$

where

- $f_{SW}$  is the switching frequency
- (3)

With  $V_{DD} = 12$  V,  $C_{LOAD} = 10$  nF, and  $f_{SW} = 300$  kHz, use [Equation 4](#) to calculate the power loss.

$$P_G = 10 \text{ nF} \times 12 \text{ V}^2 \times 300 \text{ kHz} = 0.432 \text{ W}$$
(4)

The switching load presented by a power MOSFET can be converted to an equivalent capacitance by examining the gate charge required to switch the device. This gate charge includes the effects of the input capacitance plus the added charge required to swing the drain voltage of the power device as it switches between the ON and OFF states. Most manufacturers provide specifications that provide the typical and maximum gate charge, in nC, to switch the device under specified conditions. Use the gate charge  $Q_g$  to determine the power that must be dissipated when charging a capacitor by using the equivalence  $Q_g = C_{LOAD} V_{DD}$  to provide [Equation 5](#) for power.

$$P_G = C_{LOAD} V_{DD}^2 f_{SW} = Q_g V_{DD} f_{SW}$$
(5)

Assuming that the UCC27528-Q1 device is driving power MOSFET with 60 nC of gate charge ( $Q_g = 60$  nC at  $V_{DD} = 12$  V) on each output, use [Equation 6](#) to calculate the gate-charge related power loss.

$$P_G = 2 \times 60 \text{ nC} \times 12 \text{ V} \times 300 \text{ kHz} = 0.432 \text{ W}$$
(6)

This power,  $P_G$ , is dissipated in the resistive elements of the circuit when the MOSFET is turned on or off. Half of the total power is dissipated when the load capacitor is charged during turn-on, and the other half is dissipated when the load capacitor is discharged during turn-off. When no external gate resistor is employed between the driver and MOSFET or IGBT, this power is completely dissipated inside the driver package. With the use of external gate drive resistors, the power dissipation is shared between the internal resistance of driver and external gate resistor in accordance to the ratio of the resistances (more power dissipated in the higher resistance component). Based on this simplified analysis, use [Equation 7](#) to calculate the driver power dissipation during switching.

Typical Application (continued)

$$P_{SW} = 0.5 \times Q_G \times V_{DD} \times f_{SW} \times \left( \frac{R_{OFF}}{R_{OFF} + R_{GATE}} + \frac{R_{ON}}{R_{ON} + R_{GATE}} \right)$$

where

- $R_{OFF} = R_{OL}$
- $R_{ON}$  (effective resistance of pullup structure) =  $1.5 \times R_{OL}$

In addition to the previously calculated gate-charge related power dissipation, additional dissipation in the driver is related to the power associated with the quiescent bias current consumed by the device to bias all internal circuits, such as input stage (with pullup and pulldown resistors), enable, and UVLO sections. Referring to Figure 4, the quiescent current is less than 0.6 mA even in the highest case. Use Equation 8 to calculate the quiescent power dissipation.

$$P_Q = I_{DD} V_{DD}$$

Assuming,  $I_{DD} = 6$  mA, use Equation 9 to calculate the power loss.

$$P_Q = 0.6 \text{ mA} \times 12 \text{ V} = 7.2 \text{ mW}$$

Clearly, this power loss is insignificant compared to gate-charge related power dissipation that was calculated previously.

With a 12-V supply, the bias current can be estimated as shown in Equation 10, with an additional 0.6-mA overhead for the quiescent consumption:

$$I_{DD} \sim \frac{P_G}{V_{DD}} = \frac{0.432 \text{ W}}{12 \text{ V}} = 0.036 \text{ A}$$

9.2.3 Application Curves

$V_{DD} = 5$  V, Load = 2 RJK0453DPB (power FET)

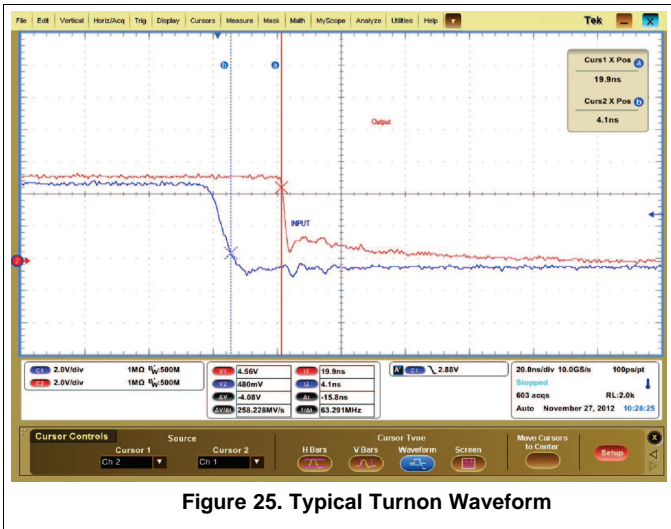


Figure 25. Typical Turnon Waveform

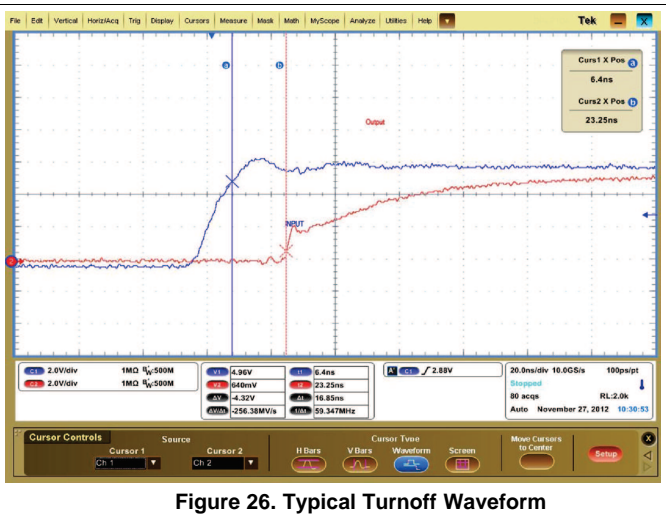


Figure 26. Typical Turnoff Waveform

10 Power Supply Recommendations

The bias supply voltage range for which the UCC27528-Q1 device is rated to operate is from 4.5 V to 18 V. The lower end of this range is governed by the internal undervoltage-lockout (UVLO) protection feature on the VDD pin supply circuit blocks. Whenever the driver is in UVLO condition when the VDD pin voltage is below the  $V_{ON}$  supply start threshold, this feature holds the output low, regardless of the status of the inputs. The upper end of this range is driven by the 20-V absolute-maximum voltage rating of the VDD pin of the device (which is a stress rating). Maintaining a 2-V margin to allow for transient voltage spikes, the maximum recommended voltage for the VDD pin is 18 V.

PRODUCT PREVIEW

The UVLO protection feature also involves a hysteresis function. This hysteresis function means that when the VDD pin bias voltage exceeds the threshold voltage and device begins to operate, and if the voltage drops, then the device continues to deliver normal functionality unless the voltage drop exceeds the hysteresis specification, VDD\_H. Therefore, ensuring that, while operating at or near the 4.2-V range, the voltage ripple on the auxiliary power supply output is smaller than the hysteresis specification of the device is important to avoid triggering device shutdown. During system shutdown, the device operation continues until the VDD pin voltage has dropped below the V<sub>OFF</sub> threshold which must be accounted for while evaluating system shutdown timing design requirements. Likewise, at system startup, the device does not begin operation until the VDD pin voltage has exceeded above the V<sub>ON</sub> threshold.

The quiescent current consumed by the internal circuit blocks of the device is supplied through the VDD pin. Although this fact is well known, recognizing that the charge for source current pulses delivered by the OUTA or OUTB pin is also supplied through the same VDD pin is important. As a result, every time a current is sourced out of the output pins, a corresponding current pulse is delivered into the device through the VDD pin. Thus ensuring that local bypass capacitors are provided between the VDD and GND pins and located as close to the device as possible for the purpose of decoupling is important. A low-ESR, ceramic surface-mount capacitor is a must. TI recommends having 2 capacitors; a 100-nF ceramic surface-mount capacitor which can be nudged very close to the pins of the device and another surface-mount capacitor of few microfarads added in parallel.

## 11 Layout

### 11.1 Layout Guidelines

Proper PCB layout is extremely important in a high-current, fast-switching circuit to provide appropriate device operation and design robustness. The UCC27528-Q1 gate driver incorporates short propagation delays and powerful output stages capable of delivering large current peaks with very-fast rise and fall times at the gate of the power MOSFET to facilitate voltage transitions very quickly. At higher VDD voltages, the peak current capability is even higher (5-A peak current is at V<sub>DD</sub> = 12 V). Very high di/dt can cause unacceptable ringing if the trace lengths and impedances are not well controlled. The following circuit layout guidelines are strongly recommended when designing with these high-speed drivers:

- Locate the driver device as close as possible to power device to minimize the length of high-current traces between the output pins and the gate of the power device.
- Locate the VDD bypass capacitors between the VDD and GND pins as close as possible to the driver with minimal trace length to improve the noise filtering. These capacitors support the high peak current that is drawn from the VDD pin during turn-on of power MOSFET. The use of low inductance SMD components, such as chip resistors and chip capacitors, is highly recommended.
- The turn-on and turn-off current-loop paths (driver device, power MOSFET, and VDD bypass capacitor) should be minimized as much as possible to keep the stray inductance to a minimum. High di/dt is established in these loops at two instances: during turn-on transients and turn-off transients, which will induce significant voltage transients on the output pin of the driver device and gate of the power MOSFET.
- Wherever possible parallel the source and return traces, taking advantage of flux cancellation.
- Separate power traces and signal traces, such as output and input signals.
- Star-point grounding is a good way to minimize noise coupling from one current loop to another. The GND of the driver should be connected to the other circuit nodes such as the source of power MOSFET, the ground of PWM controller, and other sources at one, single point. The connected paths should be as short as possible to reduce inductance and be as wide as possible to reduce resistance.
- Use a ground plane to provide noise shielding. Fast rise and fall times at the OUTx pin may corrupt the input signals during transition. The ground plane must not be a conduction path for any current loop. Instead the ground plane must be connected to the star-point with one single trace to establish the ground potential. In addition to noise shielding, the ground plane can help in power dissipation.

## 11.2 Layout Example

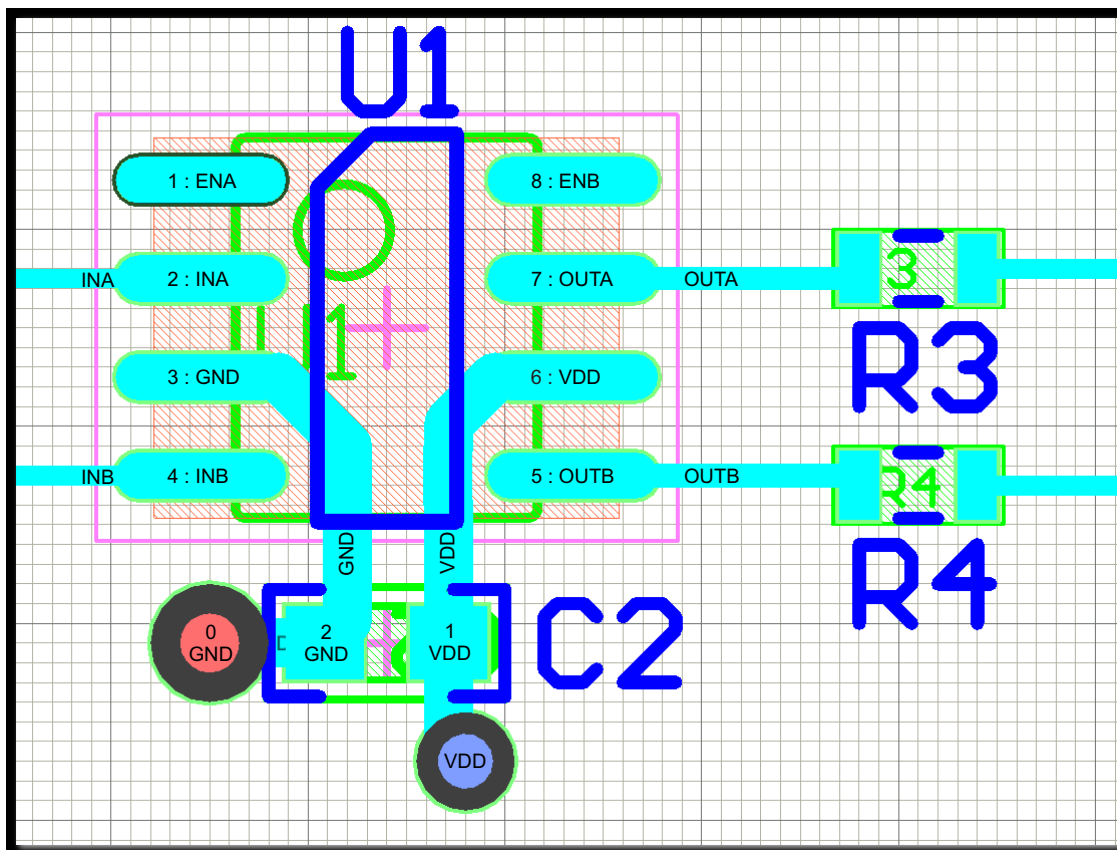


Figure 27. Layout Example for UCC27528-Q1

## 11.3 Thermal Considerations

The useful range of a driver is greatly affected by the drive power requirements of the load and the thermal characteristics of the device package. In order for a gate driver device to be useful over a particular temperature range the package must allow for the efficient removal of the heat produced while keeping the junction temperature within rated limits.

## 12 Device and Documentation Support

### 12.1 Trademarks

All trademarks are the property of their respective owners.

### 12.2 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### 12.3 Glossary

SLYZ022 — TI Glossary.

This glossary lists and explains terms, acronyms, and definitions.

### 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
UCC27528QDRQ1	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	27528Q	Samples

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF UCC27528-Q1 :**

- Catalog: [UCC27528](#)

## NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

## TAPE AND REEL INFORMATION



### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UCC27528QDRQ1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



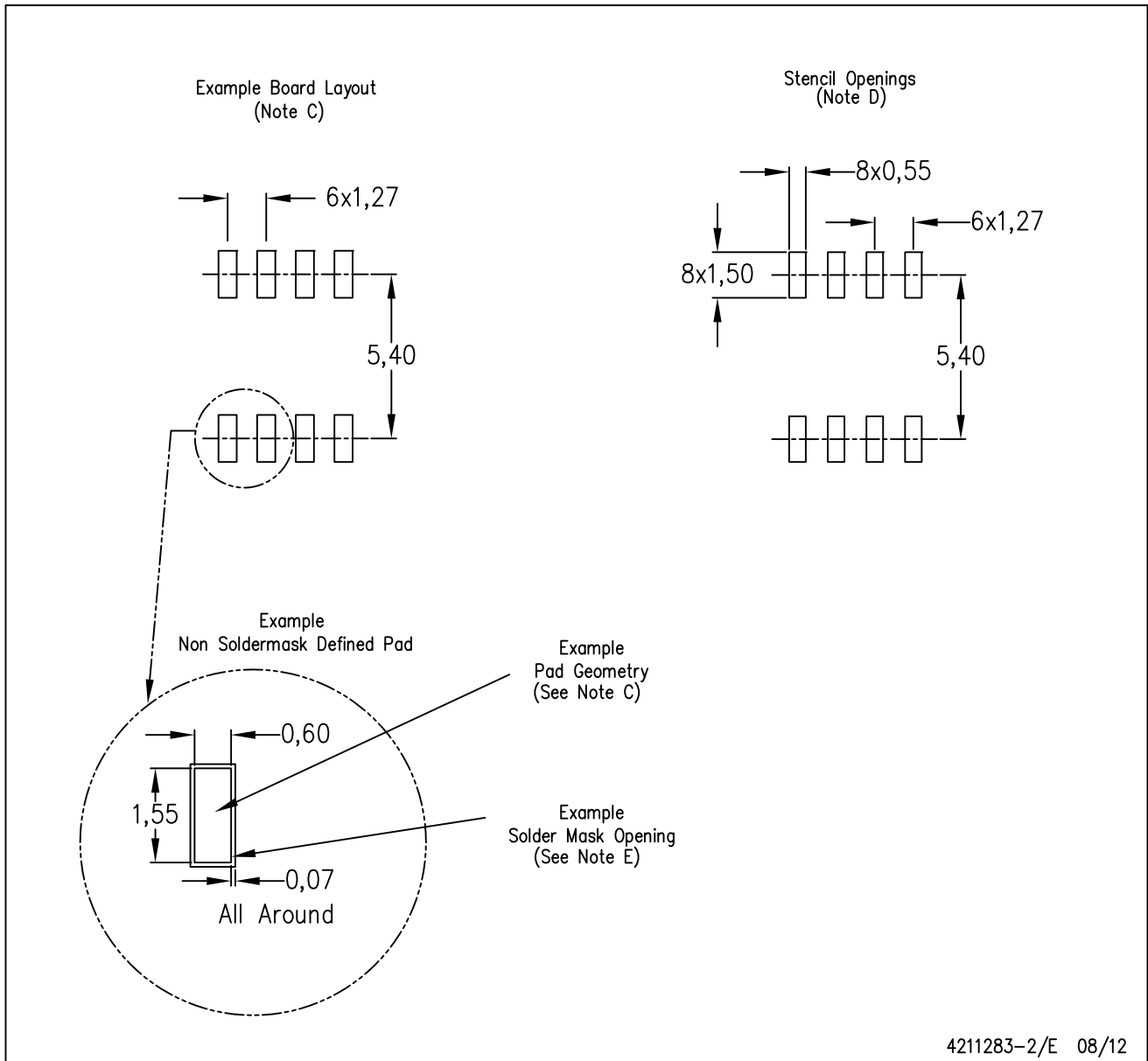
\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UCC27528QDRQ1	SOIC	D	8	2500	367.0	367.0	35.0



D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



4211283-2/E 08/12

- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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