UCC2752x Dual 5-A High-Speed Low-Side Gate Driver Based on CMOS Input Threshold Logic

1 Features

- Industry-Standard Pin Out
- Two Independent Gate-Drive Channels
- 5-A Peak Source and Sink Drive Current
- CMOS Input Logic Threshold (Function of Supply Voltage on VDD Pins)
- Hysteretic Logic Thresholds for High Noise Immunity
- Independent Enable Function for Each Output
- Inputs and Enable Pin Voltage Levels Not Restricted by VDD Pin Bias Supply Voltage
- 4.5-V to 18-V Single Supply Range
- Outputs Held Low During VDD UVLO (Ensures Glitch-Free Operation at Power Up and Power Down)
- Fast Propagation Delays (17-ns Typical)
- Fast Rise and Fall Times (7-ns and 6-ns Typical)
- 1-ns Typical Delay Matching Between 2 Channels
- Outputs Held in Low When Inputs Floating
- SOIC-8, and 3-mm x 3-mm WSON-8 Package Options
- Operating Temperature Range of –40°C to 140°C
- –5-V Negative Voltage Handling Capability on Input Pins

2 Applications

- Switch-Mode Power Supplies
- DC-to-DC Converters
- Motor Control, Solar Power
- Gate Drive for Emerging Wideband Gap Power Devices Such as GaN

3 Description

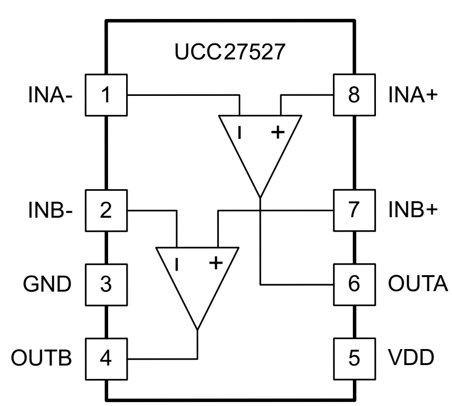
The UCC2752x family of devices are dual-channel, high-speed, low-side gate driver devices capable of effectively driving MOSFET and IGBT power switches. Using a design that inherently minimizes shoot-through current, UCC2752x can deliver high-peak current pulses of up to 5-A source and 5-A sink into capacitive loads along with rail-to-rail drive capability and extremely small propagation delay typically 17 ns. In addition, the drivers feature matched internal propagation delays between the two channels which are very well suited for applications requiring dual-gate drives with critical timing, such as synchronous rectifiers. The input pin thresholds are based on CMOS logic, which is a function of the VDD supply voltage. Wide hysteresis between the high and low thresholds offers excellent noise immunity. The Enable pins are based on TTL and CMOS compatible logic, independent of VDD supply voltage.

Device Information(1)

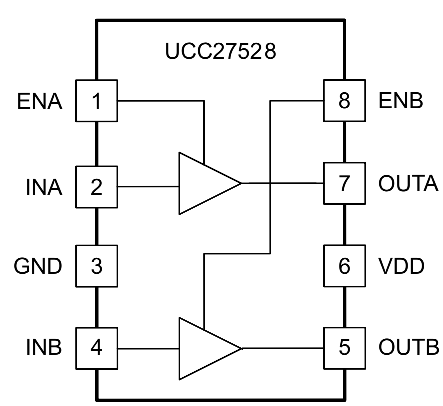
PART NUMBER	PACKAGE	BODY SIZE (NOM)
UCC27527	WSON (8)	3.00 mm x 3.00 mm
	SOIC (8)	4.90 mm x 3.91 mm
UCC27528	WSON (8)	3.00 mm x 3.00 mm
	SOIC (8)	4.90 mm x 3.91 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Dual Input Configuration



Dual Non-Inverting Inputs



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4 Revision History

Changes from Revision D (July 2013) to Revision E	Page
• Added *Handling Rating* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section	1

Changes from Revision C (June 2013) to Revision D	Page
• Added OUTA, OUTB voltage field and values.	5
• Changed table note from "Values are verified by characterization and are not production tested." to "Values are verified by characterization on bench."	5
• Changed Bias Current TYP values from 170 µA to 180 µA.	6

Changes from Revision B (January 2013) to Revision C	Page
• Changed UCC27527 packaging options	4
• Added UCC27527 Bias Current specifications.	6
• Added an updated Output Stage section.	15
• Added UCC2752X Gate Driver Output Structure image	15
• Added updated Drive Current and Power Dissipation section.	20
• Added a PSW... equation.	21

Changes from Revision A (December 2012) to Revision B	Page
• Changed Feature bullet from "-5-V Negative Voltage Handling Capability on Input and Enable Pins" to -5-V Negative Voltage Handling Capability on Input Pins"	1

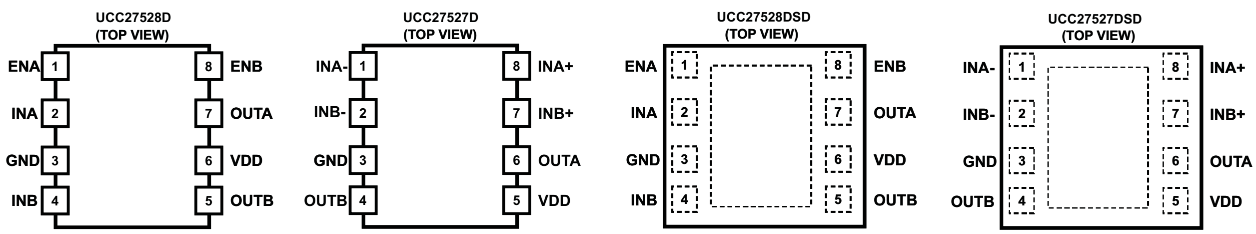
Changes from Original (December 2012) to Revision A **Page**

5 Description (continued)

The UCC27528 is a dual noninverting driver. UCC27527 features a dual input design which offers flexibility of both inverting (IN– pin) and non-inverting (IN+ pin) configuration for each channel. Either IN+ or IN– pin can be used to control the state of the driver output. The unused input pin can be used for enable and disable functions. For safety purpose, internal pullup and pulldown resistors on the input pins of all the devices in UCC2752x family to ensure that outputs are held low when input pins are in floating condition. UCC27528 features Enable pins (ENA and ENB) to have better control of the operation of the driver applications. The pins are internally pulled up to VDD for active high logic and can be left open for standard operation.

6 Pin Configuration and Functions

8-Pin WSON and SOIC
DSD and D Package
Top View



Pin Functions (UCC27527)

PIN		I/O	DESCRIPTION
NUMBER	NAME		
1	INA-	I	Inverting Input to Channel A: when Channel A is used in Non-Inverting configuration connect INA- to GND in order to Enable Channel A output, OUTA held low if INA- is unbiased or floating.
2	INB-	I	Inverting Input to Channel B: when Channel B is used in Non-Inverting configuration connect INB- to GND in order to Enable Channel B output, OUTB held low if INB- is unbiased or floating.
3	GND	–	Ground: All signals referenced to this pin.
4	OUTB	I	Output of Channel B
5	VDD	O	Bias Supply Input
6	OUTA	I	Output of Channel A
7	INB+	O	Non-Inverting Input to Channel B: When Channel B is used in Inverting configuration connect INB+ to VDD in order to Enable Channel B output, OUTB held low if INB+ is unbiased or floating.
8	INA+	I	Non-Inverting Input to Channel A: When Channel A is used in Inverting configuration connect INA+ to VDD in order to Enable Channel A output, OUTA held low if INA+ is unbiased or floating.

Pin Functions (UCC27528)

PIN		I/O	DESCRIPTION
NUMBER	NAME		
1	ENA	I	Enable input for Channel A: ENA biased low Disables Channel A output regardless of INA state, ENA biased high or floating Enables Channel A output, ENA allowed to float.
2	INA	I	Input to Channel A: Non-Inverting Input in UCC27528, OUTA held low if INA is unbiased or floating.
3	GND	–	Ground: All signals referenced to this pin.
4	INB	I	Input to Channel B: Non-Inverting Input in UCC27528, OUTB held low if INB is unbiased or floating.
5	OUTB	O	Output of Channel B
6	VDD	I	Bias supply input

Pin Functions (UCC27528) (continued)

PIN		I/O	DESCRIPTION
NUMBER	NAME		
7	OUTA	O	Output of Channel A
8	ENB	I	Enable input for Channel B: ENB biased low Disables Channel B output regardless of INB state, ENB biased high or floating Enables Channel B output, ENB allowed to float.

7 Specifications

7.1 Absolute Maximum Ratings(1)(2)

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Supply voltage range	VDD	–0.3	20.0	V
OUTA, OUTB voltage	DC	–0.3	VDD + 0.3	
	Repetitive pulse < 200 ns(3)	–2.0	VDD + 0.3	
Output continuous source/sink current	I_{OUT_DC}		0.3	A
Output pulsed source/sink current (0.5 µs)	I_{OUT_pulsed}		5	
INA, INB, INA+, INA-, INB+, INB- voltage(4)		–6.5	20	V
ENA, ENB voltage(4)		–0.3	20	
Operating virtual junction temperature, T_J range		–40	150	°C
Lead temperature	Soldering, 10 s		300	
	Reflow		260	

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to GND unless otherwise noted. Currents are positive into, negative out of the specified terminal. See Packaging Section of the datasheet for thermal limitations and considerations of packages.
(3) Values are verified by characterization on bench.
(4) The maximum voltage on the Input and Enable pins is not restricted by the voltage on the VDD pin.

7.2 Handling Ratings

			MIN	MAX	UNIT
T_{stg}	Storage temperature range		–65	150	°C
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	–4000	4000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	–1000	1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	TYP	MAX	UNIT
Supply voltage range, VDD	4.5	12	18	V
Operating junction temperature range	–40		140	°C
Input voltage, INA, INB, INA+, INA-, INB+, INB-	–5		18	V
Enable voltage, ENA and ENB	0		18	

7.4 Thermal Information

THERMAL METRIC(1)		UCC27527, UCC27528 D 8 PINS	UCC27527, UCC27528 DSD 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	128	46.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	77.7	50.7	
$R_{\theta JB}$	Junction-to-board thermal resistance	68.5	21.8	
ψ_{JT}	Junction-to-top characterization parameter	20.7	1.1	
ψ_{JB}	Junction-to-board characterization parameter	68.0	22.0	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	9.0	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

7.5 Electrical Characteristics

V_{DD} = 12 V, T_A = T_J = –40 °C to 140 °C, 1-µF capacitor from V_{DD} to GND. Currents are positive into, negative out of the specified terminal (unless otherwise noted,)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
BIAS CURRENTS							
$I_{DD(off)}$	Startup current	VDD = 3.4 V, INA=VDD, INB=VDD	UCC27528	55	125	225	µA
			UCC27527	55	180	270	
		VDD = 3.4 V, INA=GND, INB=GND	UCC27528	25	125	225	
			UCC27527	25	180	270	
UNDERVOLTAGE LOCKOUT (UVLO)							
V_{ON}	Supply start threshold	T_J = 25°C		3.91	4.20	4.50	V
		T_J = -40°C to 140°C		3.75	4.20	4.65	
V_{OFF}	Minimum operating voltage after supply start			3.60	3.90	4.40	
VDD_H	Supply voltage hysteresis			0.20	0.30	0.50	
INPUTS (INA, INB, INA+, INA-, INB+, INB-), UCC2752X (D, DSD)							
V_{IN_H}	Input signal high threshold	Output high for non-inverting input pins Output low for inverting input pins			55	70	$\%V_{DD}$
V_{IN_L}	Input signal low threshold	Output low for non-inverting input pins Output high for inverting input pins		30	38		
V_{IN_HYS}	Input hysteresis				17		
ENABLE (ENA, ENB) UCC2752X (D, DSD)							
V_{EN_H}	Enable signal high threshold	Output enabled		1.7	1.9	2.1	V
V_{EN_L}	Enable signal low threshold	Output disabled		0.95	1.10	1.25	
V_{EN_HYS}	Enable hysteresis			0.70	0.80	1.10	
OUTPUTS (OUTA, OUTB)							
$I_{SNK/SRC}$	Sink/source peak current(1)	C_{LOAD} = 0.22 µF, F_{SW} = 1 kHz			±5		A
V_{DD}-V_{OH}	High output voltage	I_{OUT} = -10 mA				0.075	V
V_{OL}	Low output voltage	I_{OUT} = 10 mA				0.01	
R_{OH}	Output pull-up resistance(2)	I_{OUT} = -10 mA		2.5	5	7.5	Ω
R_{OL}	Output pull-down resistance	I_{OUT} = 10 mA		0.15	0.5	1	Ω

(1) Ensured by design.
(2) R_{OH} represents on-resistance of only the P-Channel MOSFET device in pull-up structure of UCC2752X output stage.

7.6 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_R	Rise time (1)	C_{LOAD} = 1.8 nF, V_{DD} = 10 V		7		ns
t_F	Fall time (1)	C_{LOAD} = 1.8 nF, V_{DD} = 10 V		6		
t_M	Delay matching between 2 channels	INA = INB, OUTA and OUTB at 50% transition point, V_{DD} = 10 V		1	4	
t_{PW}	Minimum input pulse width that changes the output state (1)	V_{DD} = 10 V		15		
t_{D1}, t_{D2}	Input to output propagation delay (1)	C_{LOAD} = 1.8 nF, 7-V input pulse, V_{DD} = 10 V	6	17	26	
t_{D3}, t_{D4}	EN to output propagation delay (1)	C_{LOAD} = 1.8 nF, 7-V enable pulse, V_{DD} = 10 V	6	13	23	

(1) See timing diagrams in Figure 1, Figure 2, Figure 3, and Figure 4

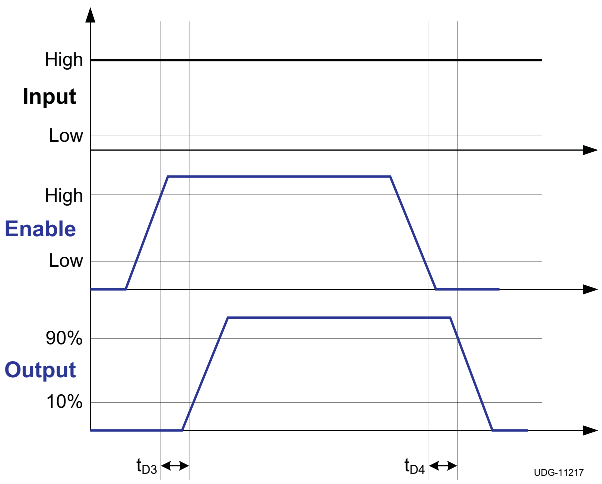


Figure 1. Enable Function (For Non-Inverting Input Driver Operation)

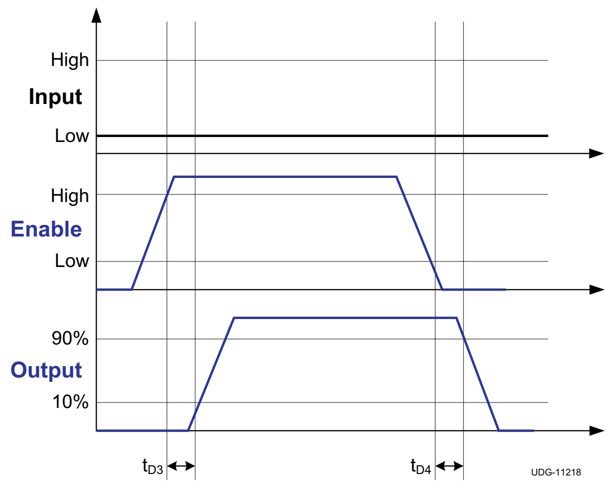


Figure 2. Enable Function (For Inverting Input Driver Operation)

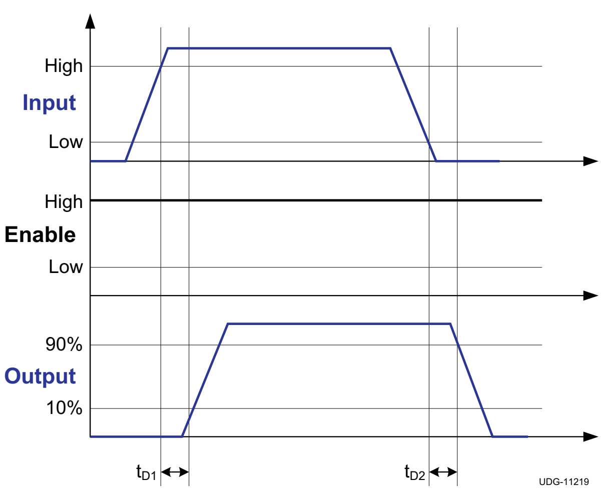


Figure 3. Non-Inverting Input Driver Operation

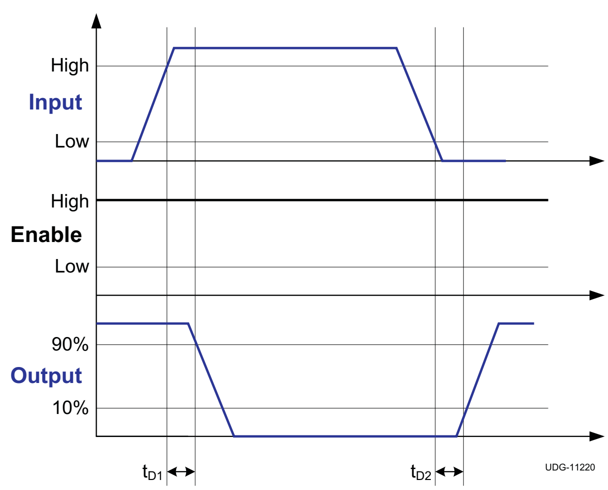
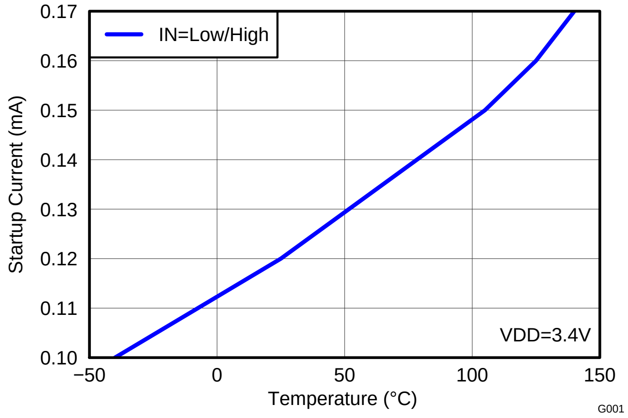


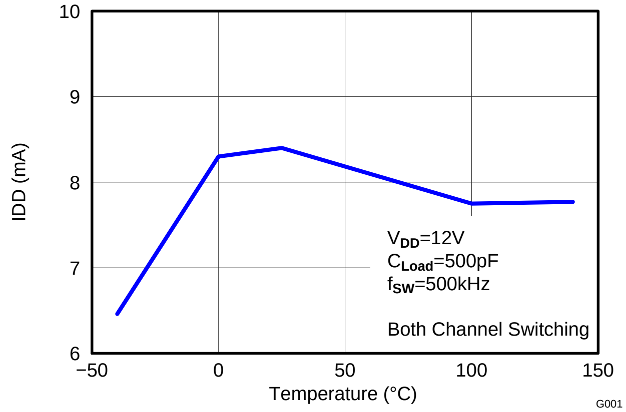
Figure 4. Inverting Input Driver Operation

7.7 Typical Characteristics



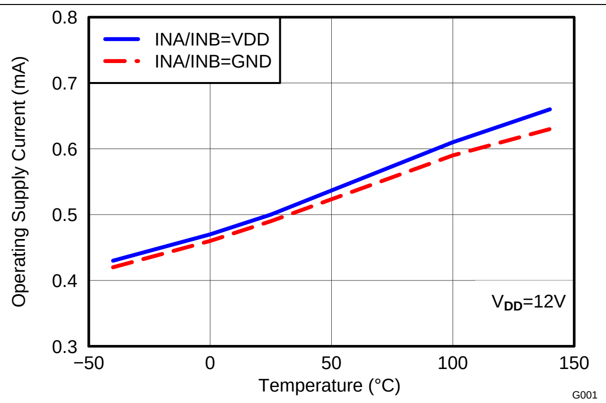
V_{DD} = 3.4 V

Figure 5. Start-Up Current vs Temperature



V_{DD} = 12 V C_{LOAD} = 500 pF
f_{SW} = 500 kHz Both Channel Switching

Figure 6. Operating Supply Current vs Temperature (Outputs Switching)



V_{DD} = 12 V

Figure 7. Supply Current vs Temperature (Outputs In DC On/Off Condition)

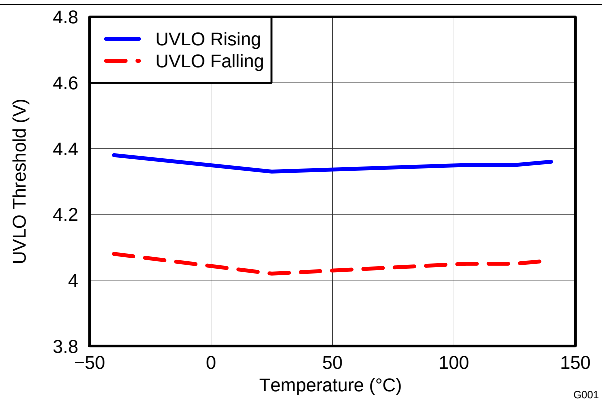
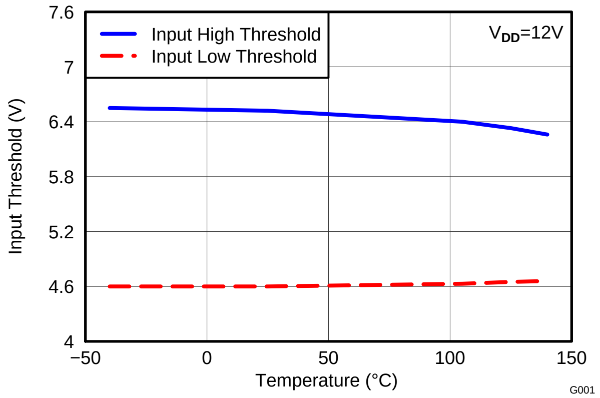
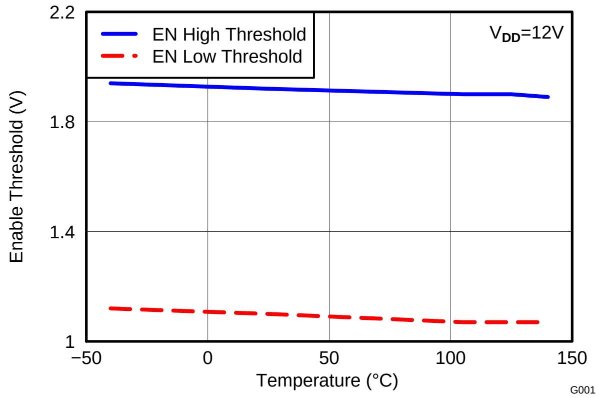


Figure 8. UVLO Threshold vs Temperature



V_{DD} = 12 V

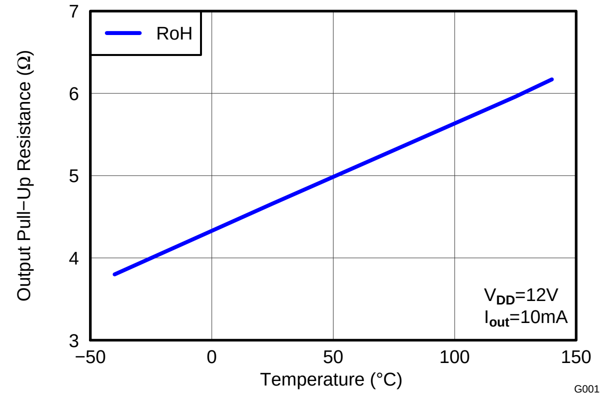
Figure 9. Input Threshold vs Temperature



V_{DD} = 12 V

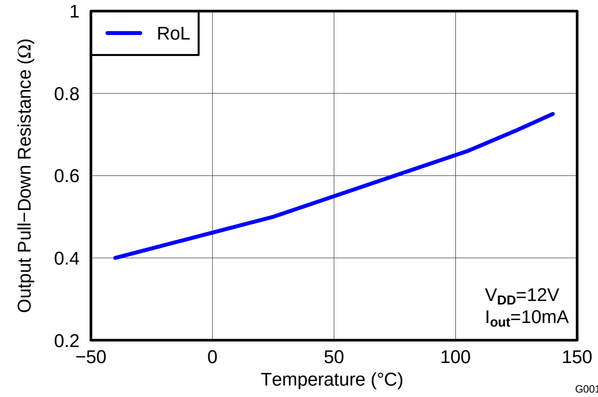
Figure 10. Enable Threshold vs Temperature

Typical Characteristics (continued)



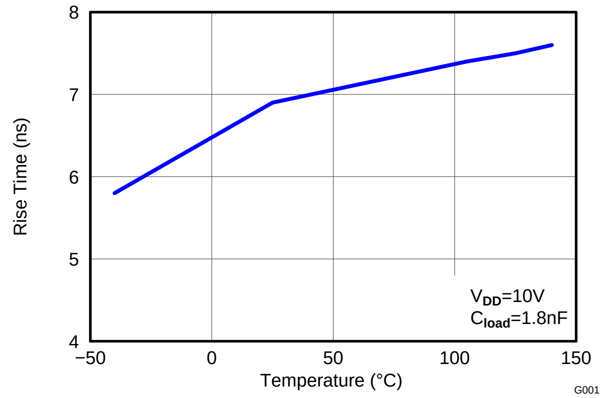
V_{DD} = 12 V I_{OUT} = 10 mA

Figure 11. Output Pullup Resistance vs Temperature



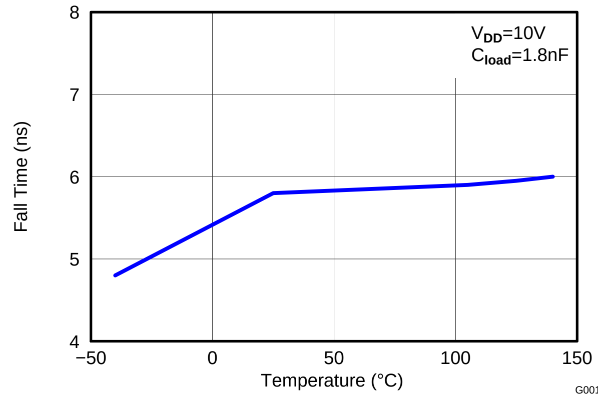
V_{DD} = 12 V I_{OUT} = 10 mA

Figure 12. Output Pulldown Resistance vs Temperature



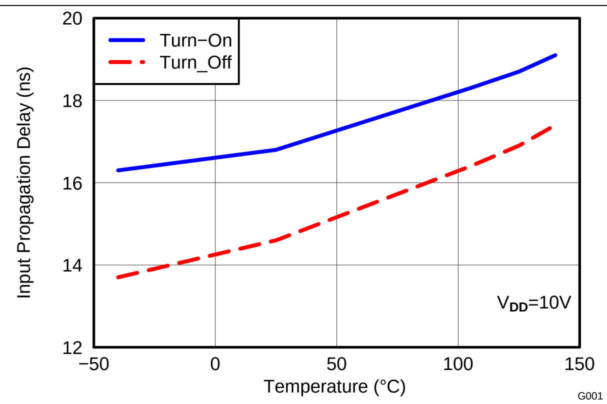
V_{DD} = 10 V C_{LOAD} = 1.8 nF

Figure 13. Rise Time vs Temperature



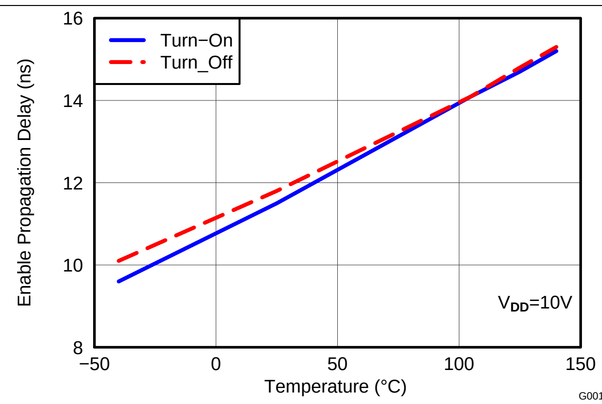
V_{DD} = 10 V C_{LOAD} = 1.8 nF

Figure 14. Fall Time vs Temperature



V_{DD} = 10 V

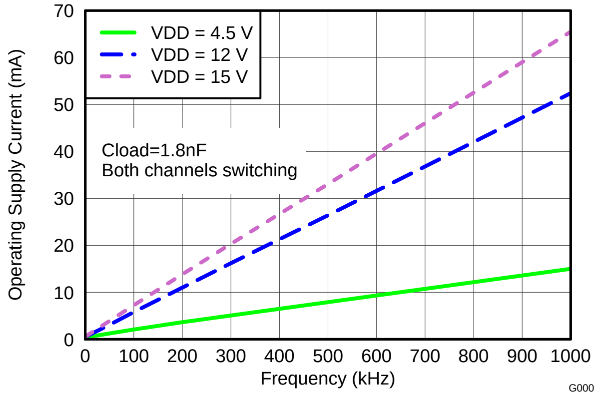
Figure 15. Input To Output Propagation Delay vs Temperature



V_{DD} = 10 V

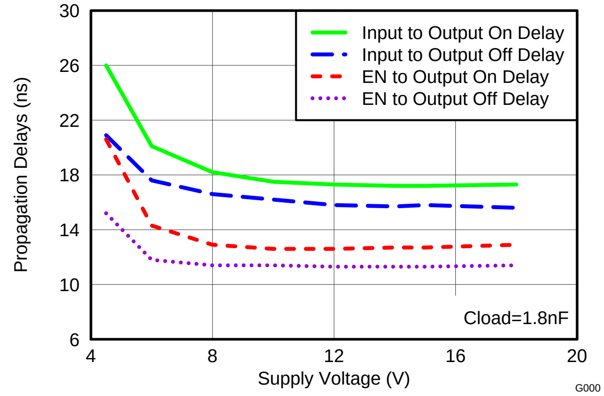
Figure 16. En To Output Propagation Delay vs Temperature

Typical Characteristics (continued)



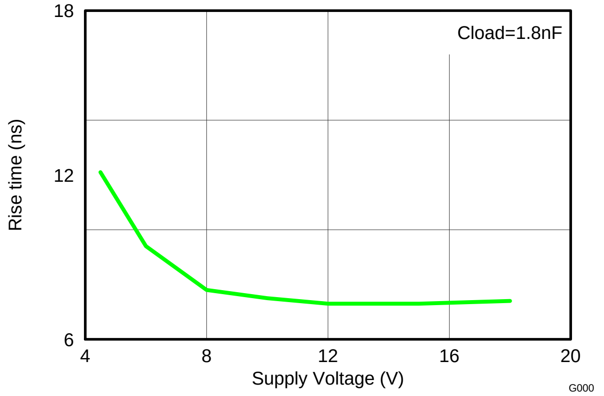
Both Channels Switching C_{LOAD} = 1.8 nF

Figure 17. Operating Supply Current vs Frequency



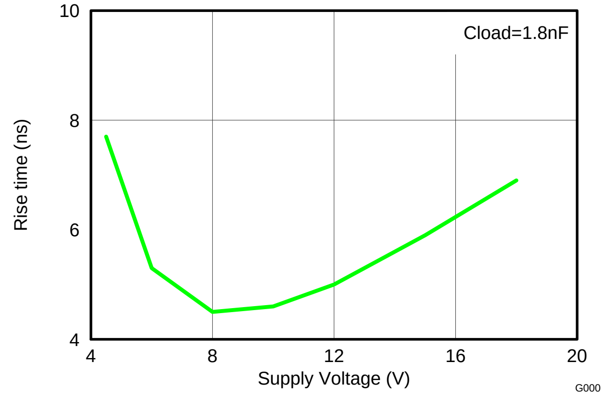
C_{LOAD} = 1.8 nF

Figure 18. Propagation Delays vs Supply Voltage



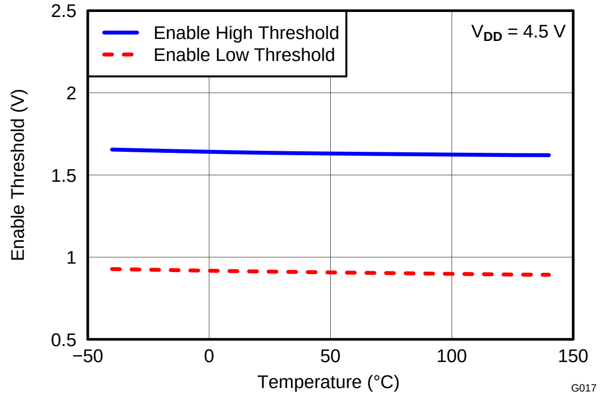
C_{LOAD} = 1.8 nF

Figure 19. Rise Time vs Supply Voltage



C_{LOAD} = 1.8 nF

Figure 20. Fall Time vs Supply Voltage



V_{DD} = 4.5 V

Figure 21. Enable Threshold vs Temperature

8 Detailed Description

8.1 Overview

The UCC2752x family of products represent Texas Instruments' latest generation of dual-channel, low-side high-speed gate driver devices featuring 5-A source/sink current capability, industry best-in-class switching characteristics and a host of other features listed in table below all of which combine to provide efficient, robust, and reliable operation in high-frequency switching power circuits.

Table 1. UCC27527 and UCC27528 Features and Benefits

FEATURE	BENEFIT
Best-in-class 13-ns (typ) propagation delay	Extremely low pulse transmission distortion
1-ns (typ) delay matching between channels	Ease of paralleling outputs for higher (2x) current capability, ease of driving parallel power switches
Expanded VDD Operating range of 4.5 V to 18 V	Flexibility in system design
Expanded operating temperature range of -40 °C to 140 °C (See *Electrical Characteristics* table)	
VDD UVLO Protection	Outputs are held Low in UVLO condition, which ensures predictable, glitch-free operation at power-up and power-down
Outputs held Low when input pins (INx) in floating condition	Safety feature, especially useful in passing abnormal condition tests during safety certification
Outputs enabled when enable pins (ENx) in floating condition	Pin-to-pin compatibility with UCC2732X family of products from TI, in designs where pin #1, 8 are in floating condition
CMOS input threshold logic	Enhanced noise immunity, higher threshold level and wider hysteresis which is a function of VDD supply voltage and ability to employ RCD delay circuits on input pins.
Ability of input and enable pins to handle voltage levels not restricted by VDD pin bias voltage	System simplification, especially related to auxiliary bias supply architecture

8.2 Functional Block Diagram

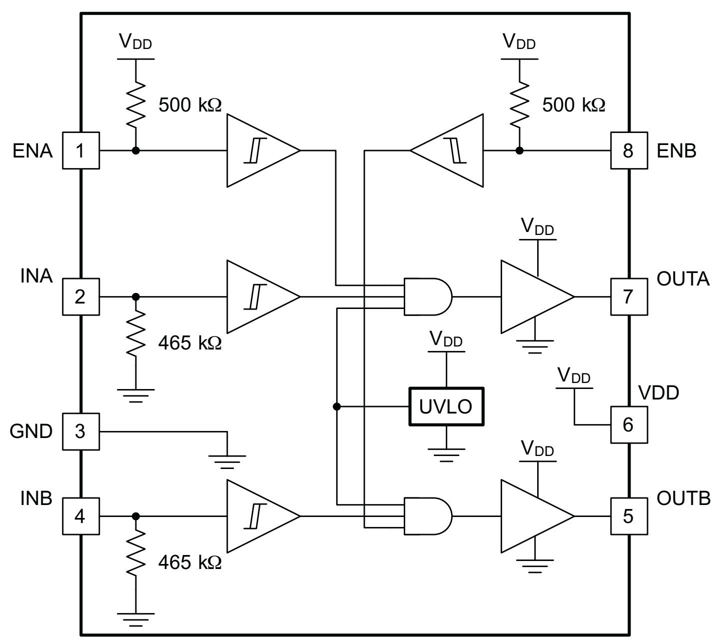


Figure 22. UCC27528 Block Diagram

Functional Block Diagram (continued)

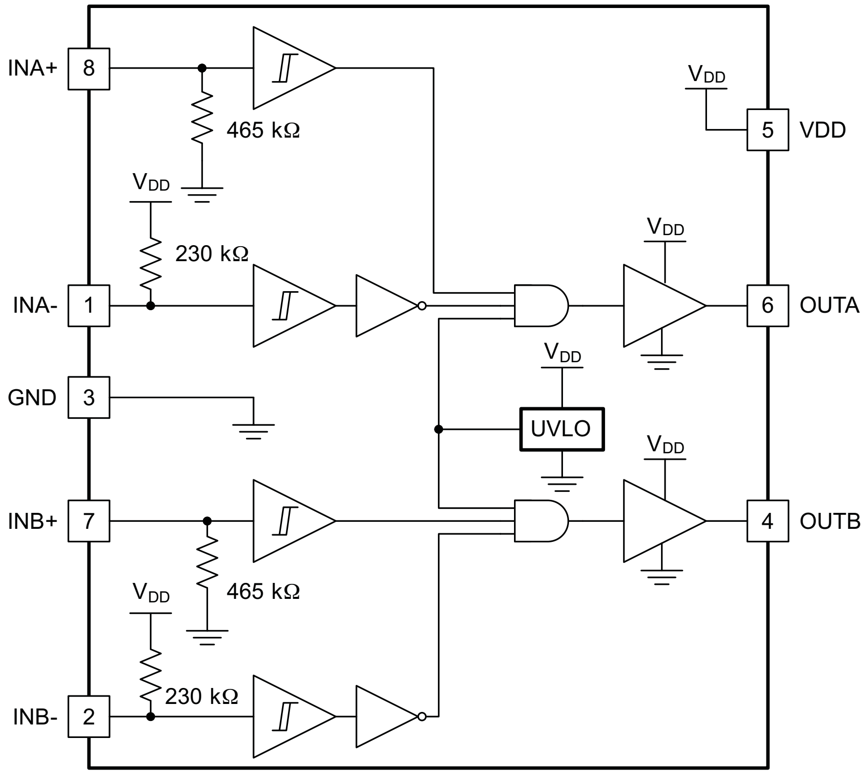


Figure 23. UCC27527 Block Diagram

8.3 Feature Description

8.3.1 V_{DD} and Undervoltage Lockout

The UCC2752x devices have internal under voltage lockout (UVLO) protection feature on the VDD pin supply circuit blocks. When VDD is rising and the level is still below UVLO threshold, this circuit holds the output low, regardless of the status of the inputs. The UVLO is typically 4.25 V with 350-mV typical hysteresis. This hysteresis helps prevent chatter when low VDD supply voltages have noise from the power supply and also when there are droops in the VDD bias voltage when the system commences switching and there is a sudden increase in I_{DD}. The capability to operate at low voltage levels such as below 5 V, along with best in class switching characteristics, is especially suited for driving emerging GaN power semiconductor devices.

For example, at power-up, the UCC2752x driver-device output remains low until the V_{DD} voltage reaches the UVLO threshold if Enable pin is active or floating. The magnitude of the OUT signal rises with V_{DD} until steady-state V_{DD} is reached. The non-inverting operation in Figure 24 shows that the output remains low until the UVLO threshold is reached, and then the output is in-phase with the input. The inverting operation in Figure 25 shows that the output remains low until the UVLO threshold is reached, and then the output is out-phase with the input. With UCC27527 the output turns to high state only if INX+ is high and INX- is low after the UVLO threshold is reached.

Because the device draws current from the VDD pin to bias all internal circuits, for the best high-speed circuit performance, two VDD bypass capacitors are recommended to prevent noise problems. The use of surface mount components is highly recommended. A 0.1-µF ceramic capacitor should be located as close as possible to the VDD to GND pins of the gate-driver device. In addition, a larger capacitor (such as 1-µF) with relatively low ESR should be connected in parallel and close proximity, in order to help deliver the high-current peaks required by the load. The parallel combination of capacitors should present a low impedance characteristic for the expected current levels and switching frequencies in the application.

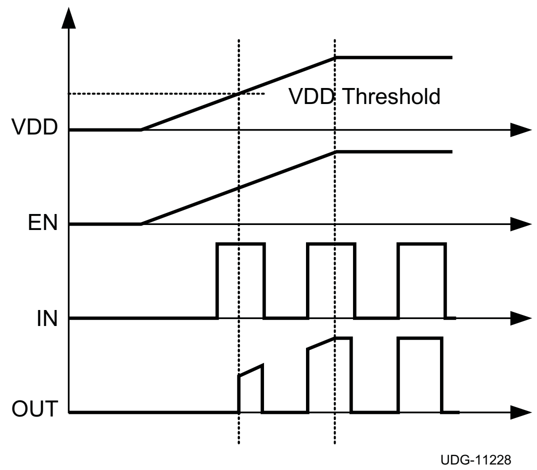


Figure 24. Power-Up Non-Inverting Driver

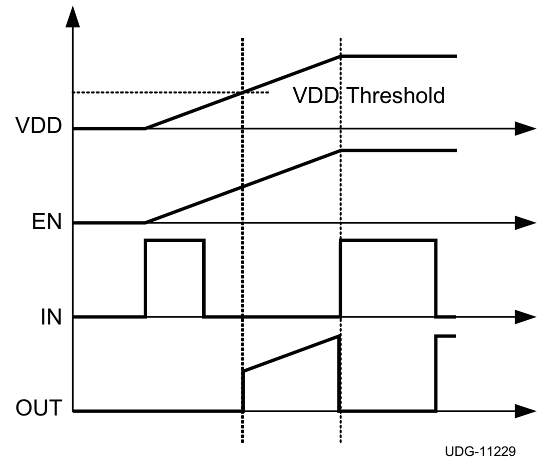


Figure 25. Power-Up Inverting Driver

8.3.2 Operating Supply Current

The UCC2752x products feature very low quiescent I_{DD} currents. The typical operating supply current in Under Voltage Lock-Out (UVLO) state and fully-on state (under static and switching conditions) are summarized in Figure 5, Figure 6 and Figure 7. The I_{DD} current when the device is fully on and outputs are in a static state (DC high or DC low, refer Figure 6) represents lowest quiescent I_{DD} current when all the internal logic circuits of the device are fully operational. The total supply current is the sum of the quiescent I_{DD} current, the average I_{OUT} current due to switching and finally any current related to pull-up resistors on the enable pins and inverting input pins. For example when the inverting Input pins are pulled low additional current is drawn from VDD supply through the pull-up resistors (refer to Figure 22 though Figure 23). Knowing the operating frequency (f_{SW}) and the MOSFET gate (Q_G) charge at the drive voltage being used, the average I_{OUT} current can be calculated as product of Q_G and f_{SW}.

A complete characterization of the I_{DD} current as a function of switching frequency at different V_{DD} bias voltages under 1.8-nF switching load in both channels is provided in Figure 17. The strikingly linear variation and close correlation with theoretical value of average I_{OUT} indicates negligible shoot-through inside the gate-driver device attesting to its high-speed characteristics.

8.3.3 Input Stage

The Input pins of UCC2752X gate driver devices are based on what is known as CMOS input threshold logic. In CMOS input threshold logic the threshold voltage level is a function of the bias voltage on the VDD pin of the device. The typical high threshold is 55% of VDD supply voltage and the typical low threshold is 38% of VDD supply voltage. There is built in hysteresis which is typically 17% of VDD supply voltage.

In most applications, the absolute value of the threshold voltage offered by the CMOS logic will be higher (eg. VINH = 5.5 V if VDD = 10 V) than what is offered by the more common TTL and CMOS compatible input threshold logic where VINH is typically less than 3 V). The same is true of the input threshold hysteresis parameter as well. This offers the following benefits:

- Better noise immunity which is desirable in high power systems.
- Ability to accept slow dV/dt input signals, which allows designers to use RCD circuits on the input pin to program propagation delays in the application, as shown below:

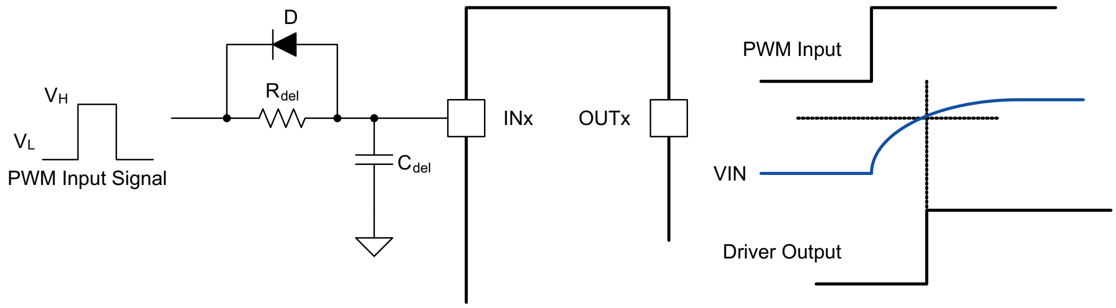


Figure 26. Using RCD Circuits

$$t_{del} = -R_{del}C_{del} \times \ln\left(\frac{V_L - V_{IN\_H}}{V_H - V_L} + 1\right) \tag{1}$$

The UCC2752x devices feature an important safety feature, whenever any of the input pins is in a floating condition, the output of the respective channel is held in the low state. This is achieved using VDD pull-up resistors on all the inverting inputs (INA-, INB- in UCC27527) or GND pull-down resistors on all the non-inverting input pins (INA, INB in UCC27528 and INA+, INB+ in UCC27527), as shown in the device's block diagrams.

While UCC27528 features one input pin per channel, the UCC27527 features a dual input configuration with two input pins available to control the output state of each channel. With the UCC27527 device the user has the flexibility to drive each channel using either a non-inverting input pin (INx+) or an inverting input pin (INx-). The state of the output pin is dependent on the bias on both the INx+ and INx- pins (where x = A, B). Once an input pin has been chosen to drive a channel, the other input pin of that channel (the *unused* Input pin) must be properly biased in order to enable the output of the channel. The *unused* input pin cannot remain in a floating condition because, as mentioned earlier, whenever any input pin is left in a floating condition, the output of that channel is disabled using the internal pull-up and down resistors for safety purposes. Alternatively, the *unused* input pin can effectively be used to implement an enable and disable function, as explained below.

- In order to drive the channel "x" (x = A or B) in a non-inverting configuration, apply the PWM control input signal to INx+ pin. In this case, the *unused* input pin, INx-, must be biased low (eg. tied to GND) in order to enable the output of this channel.
  - Alternately, the INx- pin can be used to implement the enable and disable function using an external logic signal. OUTx is disabled when INx- is biased high and OUTx is enabled when INX- is biased low.
- In order to drive the channel "X" (X = A or B) in an inverting configuration, apply the PWM control input signal to INX- pin. In this case, the *unused* input pin, INX+, must be biased high (eg. tied to VDD) in order to enable the output of the channel.
  - Alternately, the INX+ pin can be used to implement the enable and disable function using an external logic signal. OUTX is disabled when INX+ is biased low and OUTX is enabled when INX+ is biased high.
- Finally, it is worth noting that the UCC27527 output pin can be driven into high state ONLY when INx+ pin is biased high AND INx- input is biased low.

Refer to the input and output logic truth table and typical application diagram for additional clarification.

8.3.4 Enable Function

The enable function is an extremely beneficial feature in gate driver devices especially for certain applications such as synchronous rectification where the driver outputs can be disabled in light-load conditions to prevent negative current circulation and to improve light-load efficiency.

UCC27528 device is provided with independent enable pins ENx for exclusive control of each driver channel operation. The enable pins are based on a non-inverting configuration (active high operation). Thus when ENx pins are driven high the drivers are enabled and when ENx pins are driven low the drivers are disabled. Like the input pins, the enable pins are also based on a TTL/CMOS compatible input threshold logic that is independent of the supply voltage and can be effectively controlled using logic signals from 3.3-V and 5-V microcontrollers. The UCC2752X devices also feature tight control of the Enable function threshold voltage levels which eases system design considerations and ensures stable operation across temperature (refer to Figure 10). The ENx pins are internally pulled up to VDD using pull-up resistors as a result of which the outputs of the device are enabled in the default state. Hence the ENx pins can be left floating or Not Connected (N/C) for standard operation, where the enable feature is not needed. Essentially, this allows the UCC27528 device to be pin-to-pin compatible with TI's previous generation drivers UCC27323/4/5 respectively, where pins 1, 8 are N/C pins. If the channel A and Channel B inputs and outputs are connected in parallel to increase the driver current capacity, ENA and ENB should be connected and driven together.

The UCC27527 device does not feature dedicated enable pins. However, as mentioned earlier, an enable/disable function can be easily implemented in UCC27527 using the unused input pin. When INx+ is pulled-down to GND or INx- is pulled-down to VDD, the output is disabled. Thus INx+ pin can be used like an enable pin that is based on active high logic, while INx- can be used like an enable pin that is based on active low logic. It is important to note that while the ENA, ENB pins in the UCC27528 are allowed to be in floating condition during standard operation and the outputs will be enabled, the INx+, INx- pins in UCC27527 are not allowed to be floating since this will disable the outputs.

8.3.5 Output Stage

The UCC2752x device output stage features a unique architecture on the pull-up structure which delivers the highest peak Source current when it is most needed during the Miller plateau region of the power switch turn-on transition (when the power switch drain/collector voltage experiences dV/dt). The output stage pull-up structure features a P-Channel MOSFET and an additional N-Channel MOSFET in parallel. The function of the N-Channel MOSFET is to provide a brief boost in the peak sourcing current enabling fast turn-on. This is accomplished by briefly turning-on on the N-Channel MOSFET during a narrow instant when the output is changing state from Low to High.

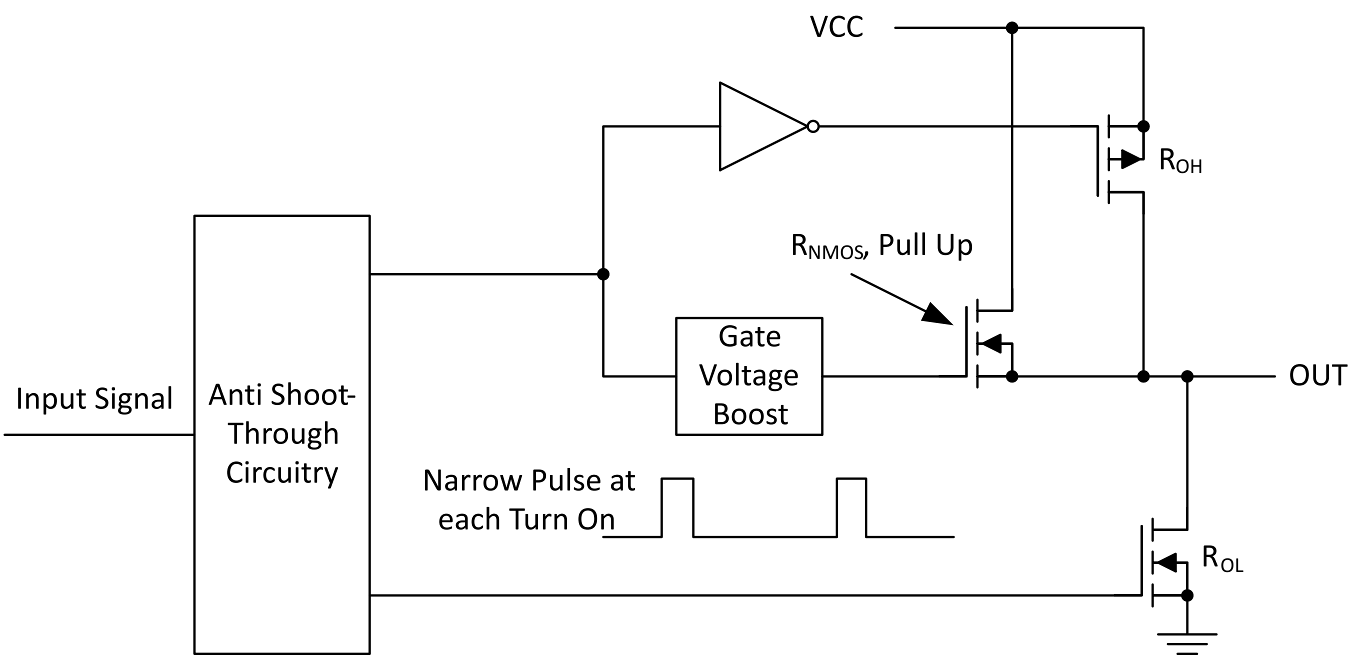


Figure 27. UCC2752x Gate Driver Output Structure

The R_{OH} parameter (see *Electrical Characteristics*) is a DC measurement and it is representative of the on-resistance of the P-Channel device only. This is because the N-Channel device is held in the off state in DC condition and is turned-on only for a narrow instant when output changes state from low to high. Thus it should be noted that effective resistance of UCC2752x pull-up stage during turn-on instant is much lower than what is represented by R_{OH} parameter.

The pull-down structure in UCC2752x is simply composed of a N-Channel MOSFET. The R_{OL} parameter (see *Electrical Characteristics*), which is also a DC measurement, is representative of the impedance of the pull-down stage in the device. In UCC2752x, the effective resistance of the hybrid pull-up structure during turn-on is estimated to be approximately 1.5 x R_{OL}, estimated based on design considerations.

Each output stage in UCC2752x is capable of supplying 5-A peak source and 5-A peak sink current pulses. The output voltage swings between VDD and GND providing rail-to-rail operation, thanks to the MOS output stage which delivers very low drop-out. The presence of the MOSFET body diodes also offers low impedance to switching overshoots and undershoots. This means that in many cases, external Schottky diode clamps may be eliminated. The outputs of these drivers are designed to withstand 500-mA reverse current without either damage to the device or logic malfunction.

The UCC2752x devices are particularly suited for dual-polarity, symmetrical drive gate transformer applications where the primary winding of transformer driven by OUTA and OUTB, with inputs INA and INB being driven complementary to each other. This is due to the extremely low drop-out offered by the MOS output stage of these devices, both during high (V_{OH}) and low (V_{OL}) states along with the low impedance of the driver output stage, all of which allow alleviate concerns regarding transformer demagnetization and flux imbalance. The low propagation delays also ensure accurate reset for high-frequency applications.

For applications that have zero voltage switching during power MOSFET turn-on or turn-off interval, the driver supplies high-peak current for fast switching even though the miller plateau is not present. This situation often occurs in synchronous rectifier applications because the body diode is generally conducting before power MOSFET is switched on.

8.3.6 Low Propagation Delays and Tightly Matched Outputs

The UCC2752x driver devices offer a very low propagation delay of 17-ns (typical) between input and output which offers lowest level of pulse transmission distortion available in the industry for high-frequency switching applications. For example in synchronous rectifier applications, the SR MOSFETs can be driven with very low distortion when a single driver device is used to drive both the SR MOSFETs. Further, the driver devices also feature an extremely accurate, 1-ns (typ) matched internal propagation delays between the two channels which is beneficial for applications requiring dual gate drives with critical timing. For example in a PFC application, a pair of paralleled MOSFETs may be driven independently using each output channel, which the inputs of both channels are driven by a common control signal from the PFC controller device. In this case the 1-ns delay matching ensures that the paralleled MOSFETs are driven in a simultaneous fashion with the minimum of turn-on delay difference.

Since the CMOS input threshold of UCC27528 allows the use of slow dV/dt input signals, when paralleling outputs for obtaining higher peak output current capability, it is recommended to connect external gate resistors directly to the output pins to avoid shoot-through current conduction between the 2 channels, as shown in Figure 28. While the two channels are inherently very well matched (4-ns Max propagation delay), it should be noted that there may be differences in the input threshold voltage level between the two channels or differences in the input signals which can cause the delay between the two outputs.

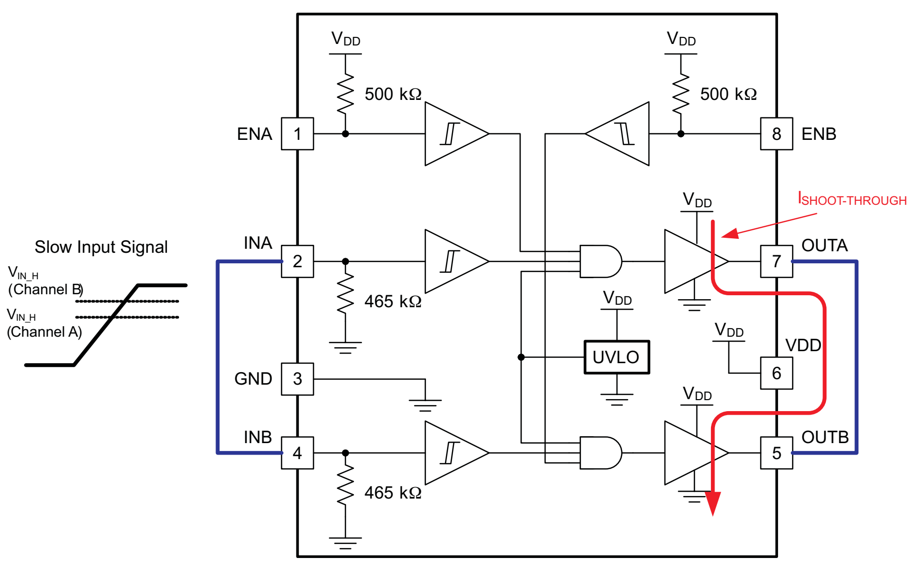


Figure 28. Slow Input Signal May Cause Shoot-Through Between Channels During Paralleling

8.4 Device Functional Modes

The device operates in normal mode and UVLO mode. See the *V_{DD} and Undervoltage Lockout* section for information on UVLO operation mode. In the normal mode the output state is dependent on states of the IN+ and IN– pins. Table 2 and Table 3 lists the output states for different input pin combinations.

Table 2. Device Logic Table (UCC27528)

				UCC27528	
ENA	**ENB**	**INA**	**INB**	**OUTA**	**OUTB**
H	H	L	L	L	L
H	H	L	H	L	H
H	H	H	L	H	L
H	H	H	H	H	H
L	L	Any	Any	L	L
Any	Any	x (1)	x (1)	L	L
x (1)	x (1)	L	L	L	L
x (1)	x (1)	L	H	L	H
x (1)	x (1)	H	L	H	L
x (1)	x (1)	H	H	H	H

(1) Floating condition

Table 3. Device Logic Table (UCC27527)

INx+ (x = A or B)	INx- (x = A or B)	OUTx+ (x = A or B)
L	L	L
L	H	L
H	L	H
H	H	L
x (1)	Any	L
Any	x (1)	L

(1) Floating condition

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

High-current gate-driver devices are required in switching power applications for a variety of reasons. In order to effect fast switching of power devices and reduce associated switching power losses, a powerful gate driver device can be employed between the PWM output of control devices and the gates of the power semiconductor devices. Further, gate driver devices are indispensable when sometimes it is just not feasible to have the PWM controller device directly drive the gates of the switching devices. With advent of digital power, this situation will be often encountered since the PWM signal from the digital controller is often a 3.3-V logic signal which is not capable of effectively turning on a power switch. A level shifting circuitry is needed to boost the 3.3-V signal to the gate-drive voltage (such as 12 V) in order to fully turn on the power device and minimize conduction losses. Traditional buffer drive circuits based on NPN/PNP bipolar transistors in totem-pole arrangement, being emitter follower configurations, prove inadequate with digital power since they lack level-shifting capability. Gate driver devices effectively combine both the level-shifting and buffer drive functions. Gate driver devices also find other needs such as minimizing the effect of high-frequency switching noise by locating the high-current driver physically close to the power switch, driving gate drive transformers and controlling floating power device gates, reducing power dissipation and thermal stress in controller devices by moving gate charge power losses into itself. In summary Gate-driver devices are an extremely important component in switching power combining benefits of high performance, low cost, component count, board-space reduction and simplified system design.

9.2 Typical Application

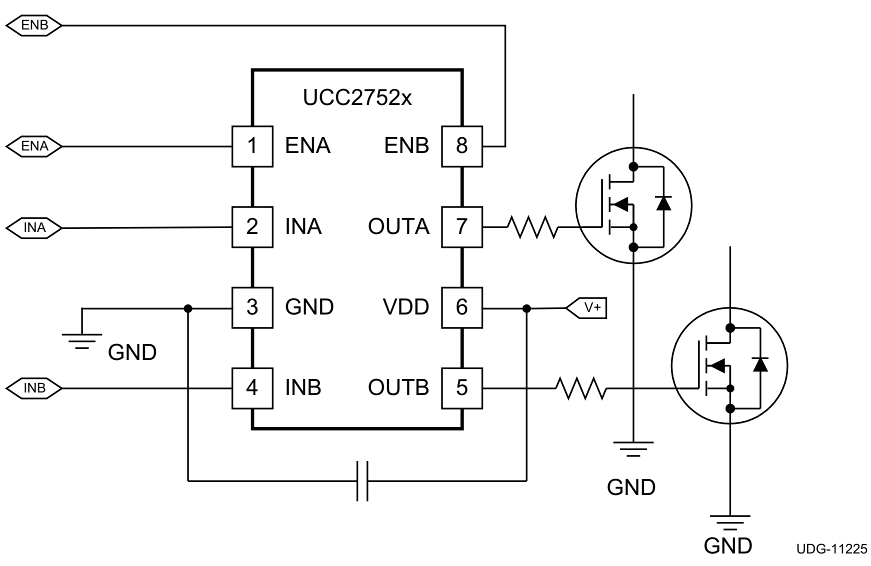


Figure 29. UCC2752x Typical Application Diagram (X = 8)

Typical Application (continued)

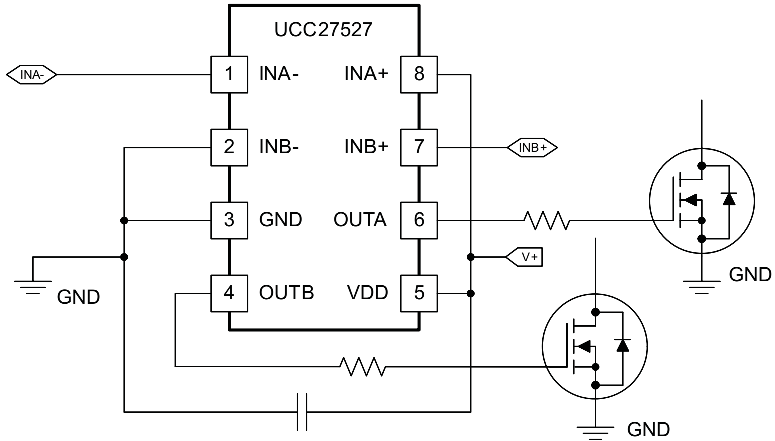


Figure 30. UCC27527 Typical Application Diagram
Channel A in Inverting and Channel B in Non-Inverting Configuration,
(Enable Function Not Used)

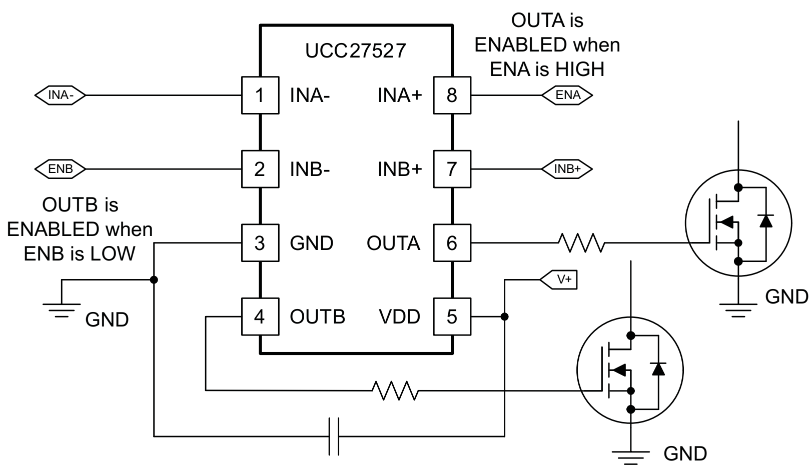


Figure 31. UCC27527 Typical Application Diagram
Channel A In Inverting And Channel B In Non-Inverting Configuration,
(Enable Function Implemented)

9.2.1 Design Requirements

When selecting the proper gate driver device for an end application, some design considerations must be evaluated first in order to make the most appropriate selection. Among these considerations are Input-to-Output Logic, Enable and Disable function, VDD, Propagation delay, and power dissipation.

Typical Application (continued)

9.2.2 Detailed Design Procedure

9.2.2.1 Input-to-Output Logic

The design should specify which type of input-to-output configuration should be used. UCC27528 can only provide dual non-inverting input-to-output with enable control. If turning on the power MOSFET or IGBT when the input signal is in high state is preferred, then the non-inverting configuration must be selected. If turning off the power MOSFET or IGBT when the input signal is in high state is preferred, the inverting configuration must be chosen. UCC27527 has dual configuration channel. Each Channel of UCC27527 device can be configured in either an inverting or non-inverting input-to-output configuration using the INx– or INx+ pins respectively like in Figure 30 and Figure 31. To configure the channel for use in inverting mode, tie the INx+ pin to VDD and apply the input signal to the INx– pin. For the non-inverting configuration, tie the INx– pin to GND and apply the input signal to the INx+ pin.

9.2.2.2 Enable and Disable Function

Certain applications demand independent control of the output state of the driver. UCC278525 device offers two independent enable pins ENx for exclusive control of each driver channels as listed in Table 2. The UCC27527 device does not feature dedicated enable pins. However, as mentioned earlier, an enable/disable function can be easily implemented in UCC27527 using the unused input pin. When INx+ is pulled-down to GND or INx- is pulled-down to VDD, the output is disabled. Thus INx+ pin can be used like an enable pin that is based on active high logic, while INx- can be used like an enable pin that is based on active low logic. It is important to note that while the ENA, ENB pins in the UCC27528 are allowed to be in floating condition during standard operation and the outputs will be enabled, the INx+, INx- pins in UCC27527 are not allowed to be floating since this will disable the outputs.

9.2.2.3 VDD Bias Supply Voltage

The bias supply voltage to be applied to the VDD pin of the device should never exceed the values listed in the *Recommended Operating Conditions* table. However, different power switches demand different voltage levels to be applied at the gate terminals for effective turnon and turnoff. With certain power switches, a positive gate voltage may be required for turnon and a negative gate voltage may be required for turnoff, in which case the VDD bias supply equals the voltage differential. With a wide operating range from 4.5 V to 18 V, the UCC2752X device can be used to drive a variety of power switches, such as Si MOSFETs (for example, VGS = 4.5 V, 10V, 12 V), IGBTs (VGE = 15 V, 18 V), and wide-bandgap power semiconductors (such as GaN, certain types of which allow no higher than 6 V to be applied to the gate pins).

9.2.2.4 Propagation Delay

The acceptable propagation delay from the gate driver is dependent on the switching frequency at which it is used and the acceptable level of pulse distortion to the system. The UCC2752X device features fast 17-ns (typical) propagation delays which ensures very little pulse distortion and allows operation at very high-frequencies. See the *Switching Characteristics* table for the propagation and switching characteristics of the UCC2752X device. For certain application which needed programmable propagation delay, The UCC2752X device can accept slow dv/dt input signals which allows designers to use RCD circuits on the input pin to program propagation as in Figure 26.

9.2.2.5 Drive Current and Power Dissipation

The UCC27527 and UCC27528 family of drivers are capable of delivering 5-A of current to a MOSFET gate for a period of several hundred nanoseconds at VDD = 12 V. High peak current is required to turn the device ON quickly. Then, to turn the device OFF, the driver is required to sink a similar amount of current to ground. This repeats at the operating frequency of the power device. The power dissipated in the gate driver device package depends on the following factors:

- Gate charge required of the power MOSFET (usually a function of the drive voltage V_{GS}, which is very close to input bias supply voltage V_{DD} due to low V_{OH} drop-out)
- Switching frequency
- Use of external gate resistors

Typical Application (continued)

Since UCC2752x features very low quiescent currents and internal logic to eliminate any shoot-through in the output driver stage, their effect on the power dissipation within the gate driver can be safely assumed to be negligible.

When a driver device is tested with a discrete, capacitive load it is a fairly simple matter to calculate the power that is required from the bias supply. The energy that must be transferred from the bias supply to charge the capacitor is given by:

$$E_G = \frac{1}{2} C_{LOAD} V_{DD}^2$$

where

- C_{LOAD} is load capacitor
- V_{DD} is bias voltage feeding the driver (2)

There is an equal amount of energy dissipated when the capacitor is charged. This leads to a total power loss given by the following:

$$P_G = C_{LOAD} V_{DD}^2 f_{SW}$$

where

- f_{SW} is the switching frequency (3)

With V_{DD} = 12 V, C_{LOAD} = 10 nF and f_{SW} = 300 kHz the power loss can be calculated as:

$$P_G = 10\,nF \times 12\,V^2 \times 300\,kHz = 0.432\,W \tag{4}$$

The switching load presented by a power MOSFET can be converted to an equivalent capacitance by examining the gate charge required to switch the device. This gate charge includes the effects of the input capacitance plus the added charge needed to swing the drain voltage of the power device as it switches between the ON and OFF states. Most manufacturers provide specifications that provide the typical and maximum gate charge, in nC, to switch the device under specified conditions. Using the gate charge Q_g, one can determine the power that must be dissipated when charging a capacitor. This is done by using the equivalence $Q_g = C_{LOAD}V_{DD}$ to provide the following equation for power:

$$P_G = C_{LOAD} V_{DD}^2 f_{SW} = Q_g V_{DD} f_{SW} \tag{5}$$

Assuming that UCC2752x is driving power MOSFET with 60 nC of gate charge (Q_g = 60 nC at V_{DD} = 12 V) on each output, the gate charge related power loss can be calculated as:

$$P_G = 2\,x\,60\,nC \times 12\,V \times 300\,kHz = 0.432\,W \tag{6}$$

This power PG is dissipated in the resistive elements of the circuit when the MOSFET is being turned-on or off. Half of the total power is dissipated when the load capacitor is charged during turn-on, and the other half is dissipated when the load capacitor is discharged during turn-off. When no external gate resistor is employed between the driver and MOSFET/IGBT, this power is completely dissipated inside the driver package. With the use of external gate drive resistors, the power dissipation is shared between the internal resistance of driver and external gate resistor in accordance to the ratio of the resistances (more power dissipated in the higher resistance component). Based on this simplified analysis, the driver power dissipation during switching is calculated as follows:

$$P_{SW} = 0.5 \times Q_G \times VDD \times f_{SW} \times \left(\frac{R_{OFF}}{R_{OFF} + R_{GATE}} + \frac{R_{ON}}{R_{ON} + R_{GATE}} \right)$$

where

- $R_{OFF} = R_{OL}$
- R_{ON} (effective resistance of pull-up structure) = 1.5 x R_{OL} (7)

In addition to the above gate charge related power dissipation, additional dissipation in the driver is related to the power associated with the quiescent bias current consumed by the device to bias all internal circuits such as input stage (with pull-up and pull-down resistors), enable, and UVLO sections. Referring to the Figure 6 it can be seen that the quiescent current is less than 0.6 mA even in the highest case. The quiescent power dissipation can be simply calculated as:

Typical Application (continued)

$$P_Q = I_{DD} V_{DD} \quad (8)$$

Assuming , I_{DD} = 6 mA, the power loss is:

$$P_Q = 0.6 \text{ mA} \times 12\text{ V} = 7.2\text{ mW} \quad (9)$$

Clearly, this is insignificant compared to gate charge related power dissipation calculated earlier.

With a 12-V supply, the bias current can be estimated as follows, with an additional 0.6-mA overhead for the quiescent consumption:

$$I_{DD} \sim \frac{P_G}{V_{DD}} = \frac{0.432 \text{ W}}{12 \text{ V}} = 0.036 \text{ A} \quad (10)$$

9.2.3 Application Curves

VDD = 5 V, Load = 2 RJK0453DPB

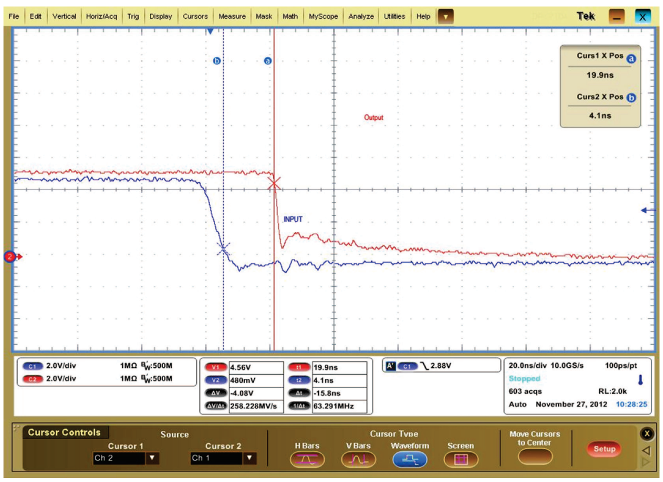


Figure 32. Typical Turnon Waveform

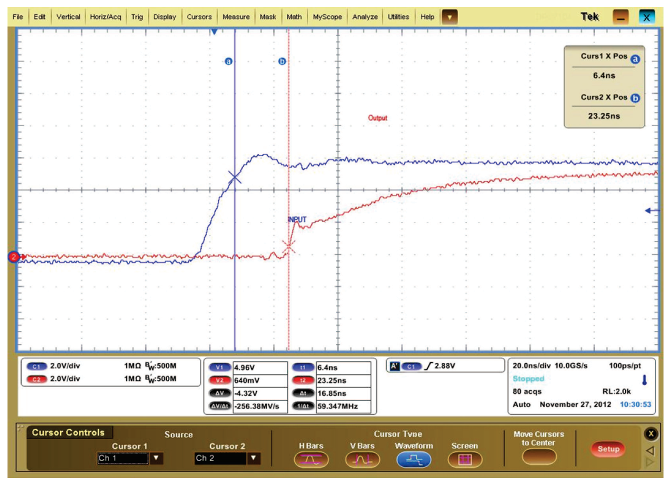


Figure 33. Typical Turnoff Waveform

10 Power Supply Recommendations

The bias supply voltage range for which the UCC2752X device is rated to operate is from 4.5 V to 18 V. The lower end of this range is governed by the internal undervoltage-lockout (UVLO) protection feature on the VDD pin supply circuit blocks. Whenever the driver is in UVLO condition when the VDD pin voltage is below the VON supply start threshold, this feature holds the output low, regardless of the status of the inputs. The upper end of this range is driven by the 20-V absolute maximum voltage rating of the VDD pin of the device (which is a stress rating). Keeping a 2-V margin to allow for transient voltage spikes, the maximum recommended voltage for the VDD pin is 18 V.

The UVLO protection feature also involves a hysteresis function. This means that when the VDD pin bias voltage has exceeded the threshold voltage and device begins to operate, and if the voltage drops, then the device continues to deliver normal functionality unless the voltage drop exceeds the hysteresis specification VDD_H. Therefore, ensuring that, while operating at or near the 4.2V range, the voltage ripple on the auxiliary power supply output is smaller than the hysteresis specification of the device is important to avoid triggering device shutdown. During system shutdown, the device operation continues until the VDD pin voltage has dropped below the VOFF threshold which must be accounted for while evaluating system shutdown timing design requirements. Likewise, at system startup, the device does not begin operation until the VDD pin voltage has exceeded above the VON threshold. The quiescent current consumed by the internal circuit blocks of the device is supplied through the VDD pin. Although this fact is well known, recognizing that the charge for source current pulses delivered by the OUTA/B pin is also supplied through the same VDD pin is important. As a result, every time a current is sourced out of the output pins, a corresponding current pulse is delivered into the device through the VDD pin. Thus ensuring that local bypass capacitors are provided between the VDD and GND pins and located as close to the device as possible for the purpose of decoupling is important. A low ESR, ceramic surface mount capacitor is a must. TI recommends having 2 capacitors; a 100-nF ceramic surface-mount capacitor which can be nudged very close to the pins of the device and another surface-mount capacitor of few microfarads added in parallel.

11 Layout

11.1 Layout Guidelines

Proper PCB layout is extremely important in a high current, fast switching circuit to provide appropriate device operation and design robustness. The UCC27527 and UCC27528 family of gate drivers incorporates short propagation delays and powerful output stages capable of delivering large current peaks with very fast rise and fall times at the gate of power MOSFET to facilitate voltage transitions very quickly. At higher VDD voltages, the peak current capability is even higher (5-A peak current is at VDD = 12 V). Very high di/dt can cause unacceptable ringing if the trace lengths and impedances are not well controlled. The following circuit layout guidelines are strongly recommended when designing with these high-speed drivers.

- Locate the driver device as close as possible to power device in order to minimize the length of high-current traces between the Output pins and the Gate of the power device.
- Locate the VDD bypass capacitors between VDD and GND as close as possible to the driver with minimal trace length to improve the noise filtering. These capacitors support high peak current being drawn from VDD during turn-on of power MOSFET. The use of low inductance SMD components such as chip resistors and chip capacitors is highly recommended.
- The turn-on and turn-off current loop paths (driver device, power MOSFET and VDD bypass capacitor) should be minimized as much as possible in order to keep the stray inductance to a minimum. High dI/dt is established in these loops at 2 instances – during turn-on and turn-off transients, which will induce significant voltage transients on the output pin of the driver device and Gate of the power MOSFET.
- Wherever possible parallel the source and return traces, taking advantage of flux cancellation
- Separate power traces and signal traces, such as output and input signals.
- Star-point grounding is a good way to minimize noise coupling from one current loop to another. The GND of the driver should be connected to the other circuit nodes such as source of power MOSFET, ground of PWM controller etc at one, single point. The connected paths should be as short as possible to reduce inductance and be as wide as possible to reduce resistance.
- Use a ground plane to provide noise shielding. Fast rise and fall times at OUT may corrupt the input signals during transition. The ground plane must not be a conduction path for any current loop. Instead the ground plane must be connected to the star-point with one single trace to establish the ground potential. In addition

Layout Guidelines (continued)

to noise shielding, the ground plane can help in power dissipation as well

- In noisy environments, it may be necessary to tie inputs of an unused channel of UCC27527 to VDD (in case of INx+) or GND (in case of INX-) using short traces in order to ensure that the output is enabled and to prevent noise from causing malfunction in the output.

11.2 Layout Example

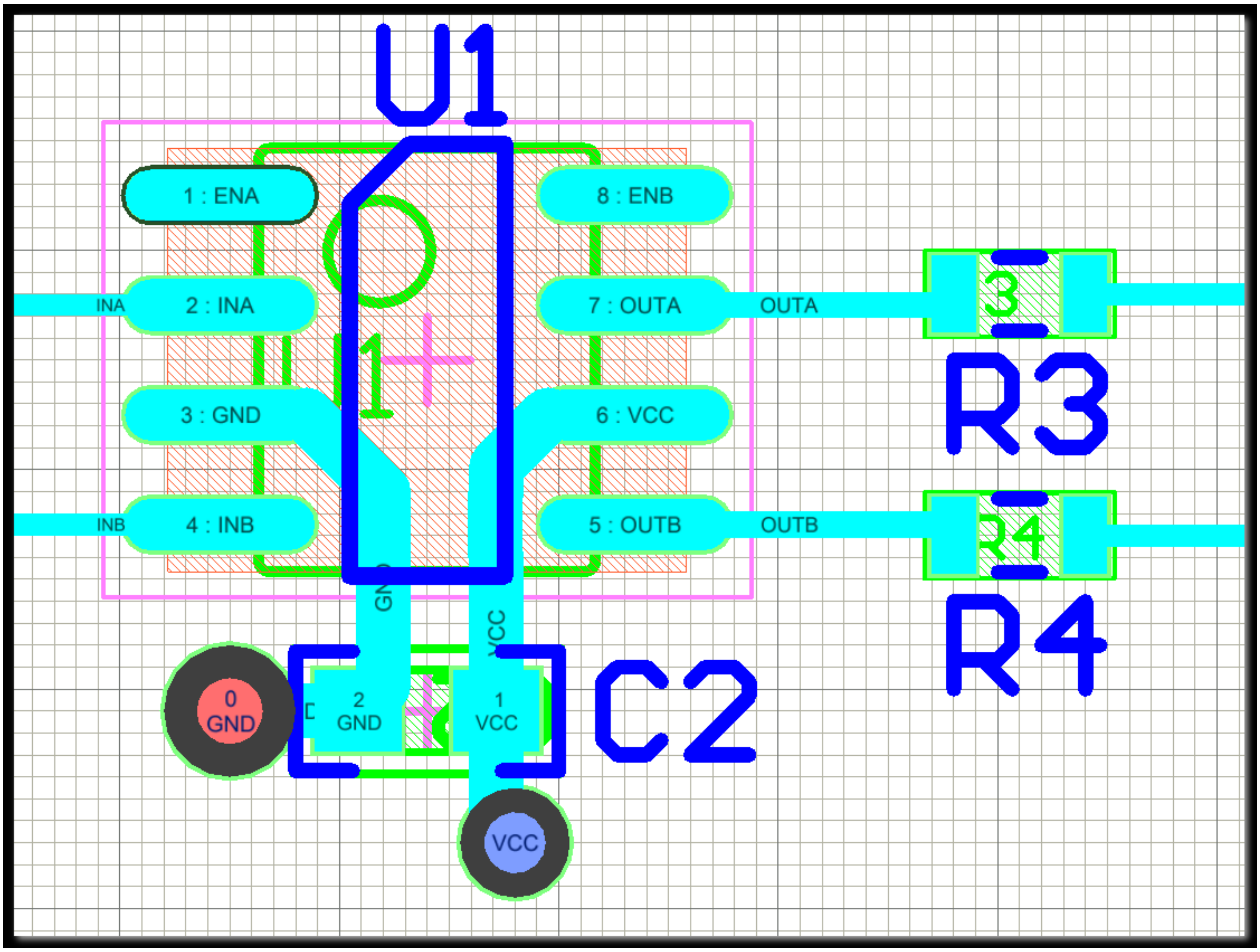


Figure 34. Layout Example for UCC27528

Layout Example (continued)

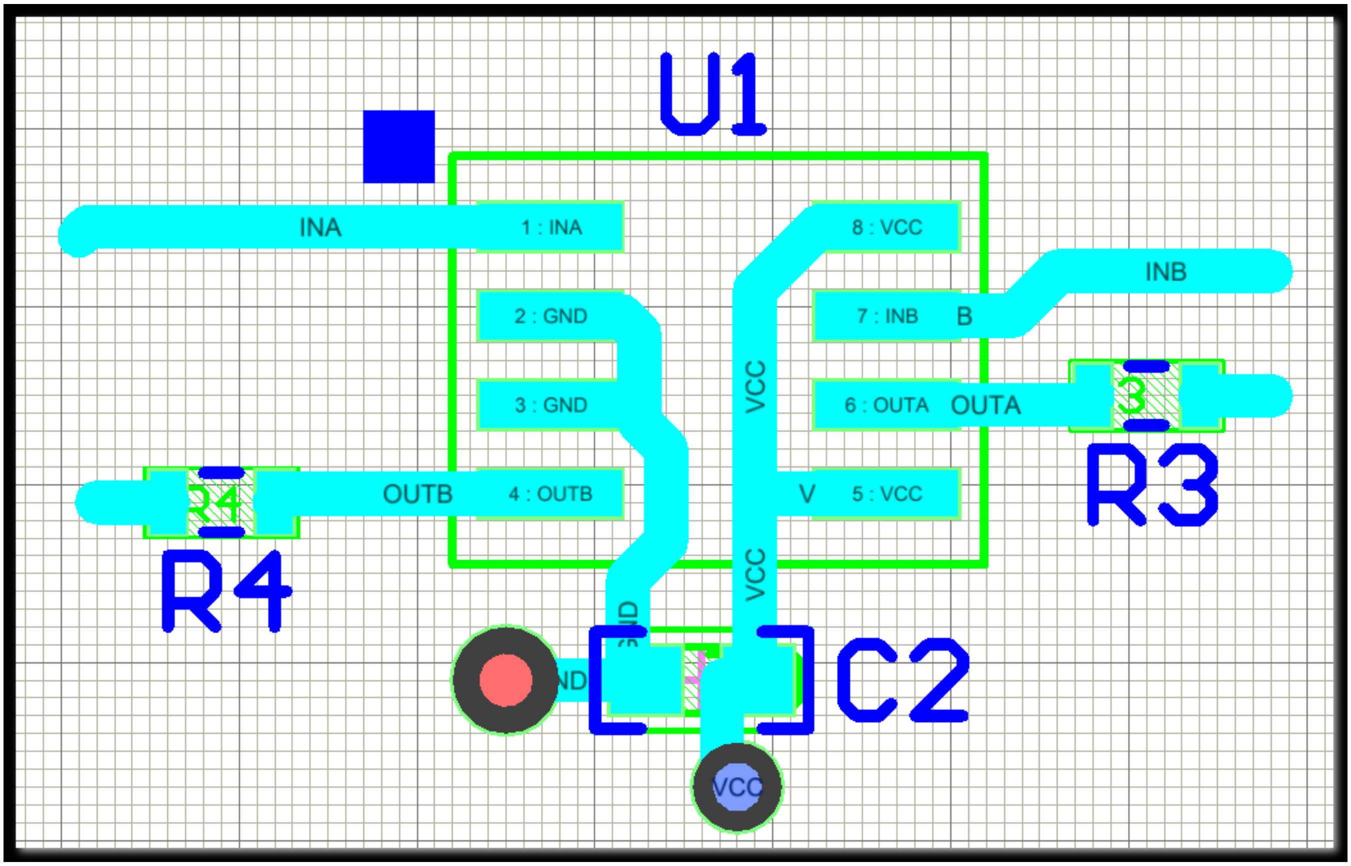


Figure 35. Layout Example for UCC27527 (Channel A in Inverting and Channel B in Non-Inverting Configuration)

11.3 Thermal Considerations

The useful range of a driver is greatly affected by the drive power requirements of the load and the thermal characteristics of the device package. In order for a gate driver device to be useful over a particular temperature range the package must allow for the efficient removal of the heat produced while keeping the junction temperature within rated limits. The UCC27527 and UCC27528 family of drivers is available in two different packages to cover a range of application requirements. The thermal metrics for each of these packages are summarized in the Thermal Information section of the datasheet. For detailed information regarding the thermal information table, please refer to Application Note from Texas Instruments entitled *IC Package Thermal Metrics*, SPRA953).

Among the different package options available in the UCC2752x family, of particular mention is the DSD package when it comes to power dissipation capability. The 3-mm x 3-mm WSON (DSD) package offer a means of removing the heat from the semiconductor junction through the exposed thermal pad at the base of the package. This pad is soldered to the copper on the printed circuit board directly underneath the device package, reducing the thermal resistance to a very low value. This allows a significant improvement in heat-sinking over that available in the D package. The printed circuit board must be designed with thermal lands and thermal vias to complete the heat removal subsystem. Note that the exposed pads in the WSON-8 package is not directly connected to any leads of the package. However, it is electrically and thermally connected to the substrate of the device which is the ground of the device. It is recommended to externally connect the exposed pads to GND in PCB layout for better EMI immunity.

12 Device and Documentation Support

12.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 4. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
UCC27527	Click here	Click here	Click here	Click here	Click here
UCC27528	Click here	Click here	Click here	Click here	Click here

12.2 Trademarks

All trademarks are the property of their respective owners.

12.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
UCC27527DSDR	ACTIVE	SON	DSD	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 140	27527	Samples
UCC27527DSDT	ACTIVE	SON	DSD	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 140	27527	Samples
UCC27528D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 140	27528	Samples
UCC27528DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 140	27528	Samples
UCC27528DSDR	ACTIVE	SON	DSD	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 140	27528	Samples
UCC27528DSDT	ACTIVE	SON	DSD	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 140	27528	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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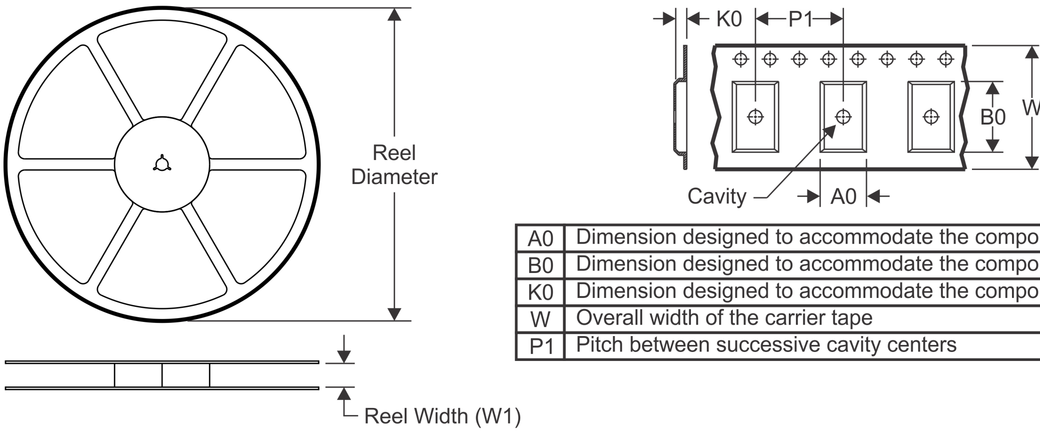
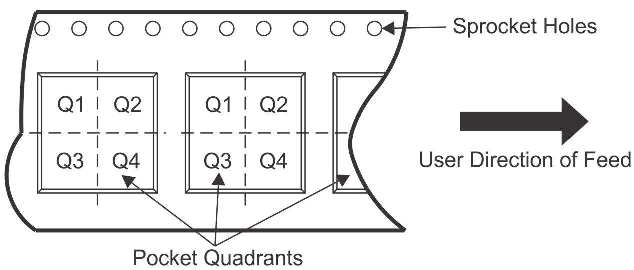
TAPE AND REEL INFORMATION



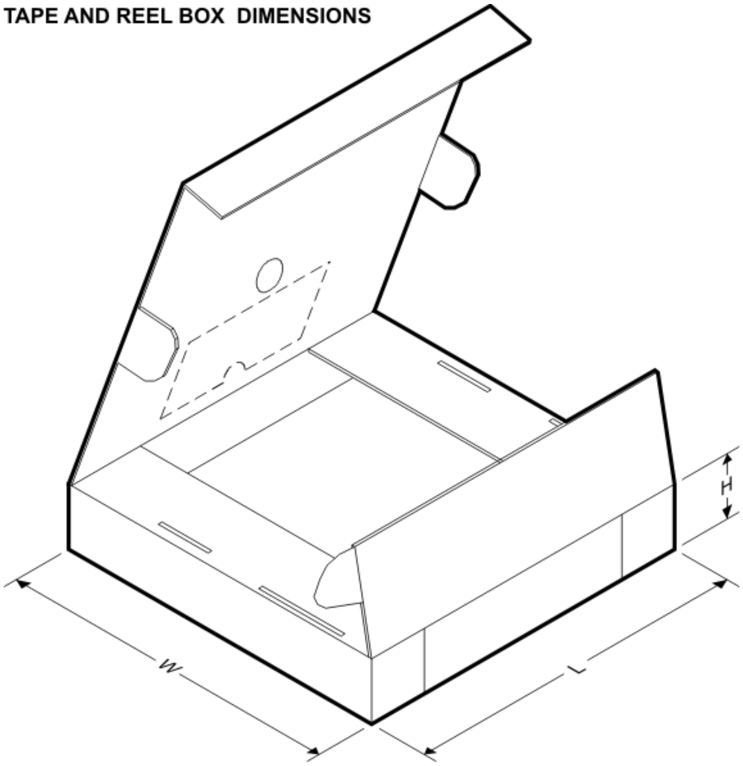
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UCC27527DSDR	SON	DSD	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
UCC27527DSDT	SON	DSD	8	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
UCC27528DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UCC27528DSDR	SON	DSD	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
UCC27528DSDT	SON	DSD	8	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

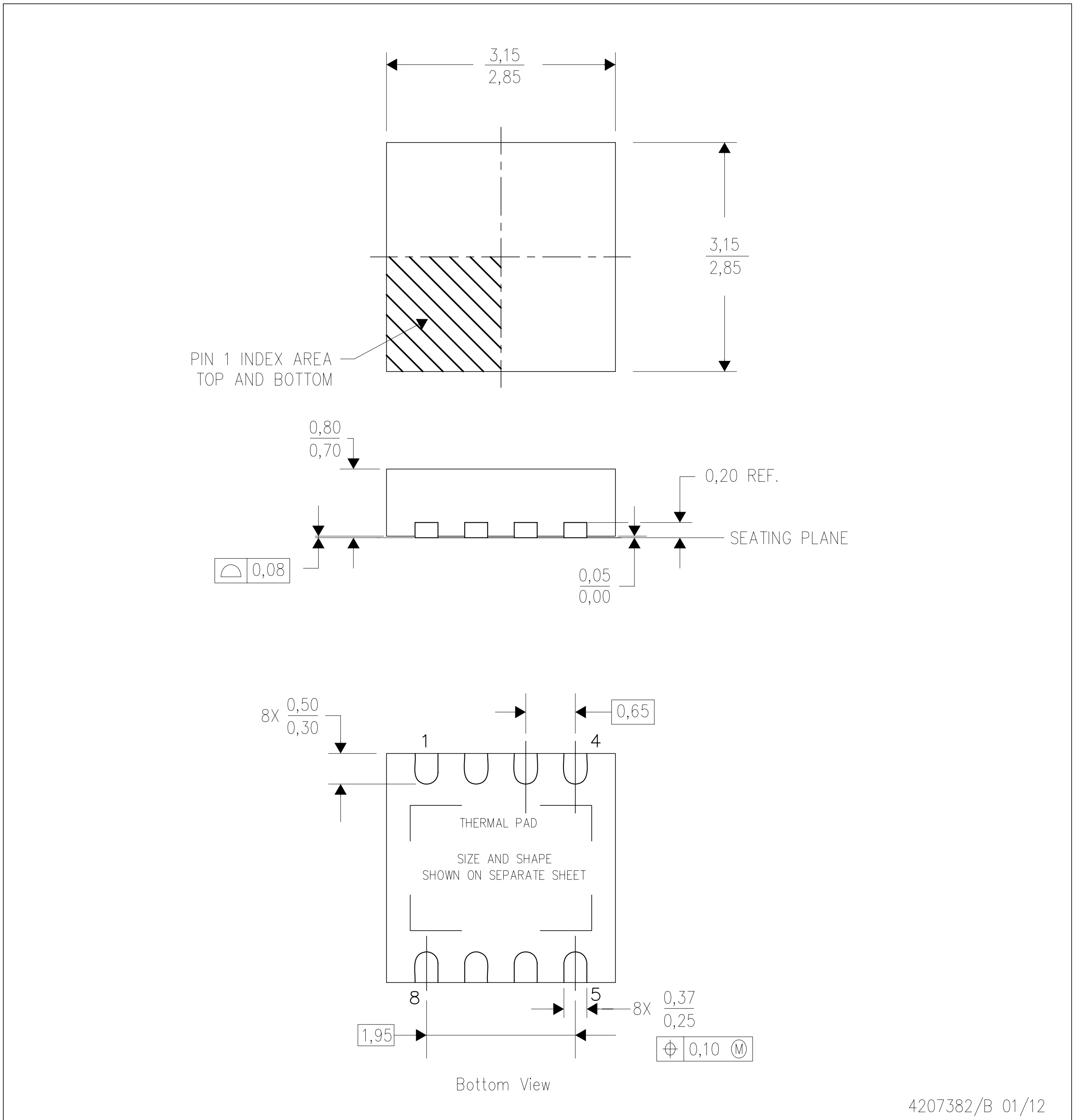
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UCC27527DSDR	SON	DSD	8	3000	367.0	367.0	35.0
UCC27527DSDT	SON	DSD	8	250	552.0	185.0	36.0
UCC27528DR	SOIC	D	8	2500	367.0	367.0	35.0
UCC27528DSDR	SON	DSD	8	3000	367.0	367.0	35.0
UCC27528DSDT	SON	DSD	8	250	210.0	185.0	35.0

DSD (S-PWSON-N8) PLASTIC SMALL OUTLINE NO-LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.
C. Small Outline No-Lead (SON) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.

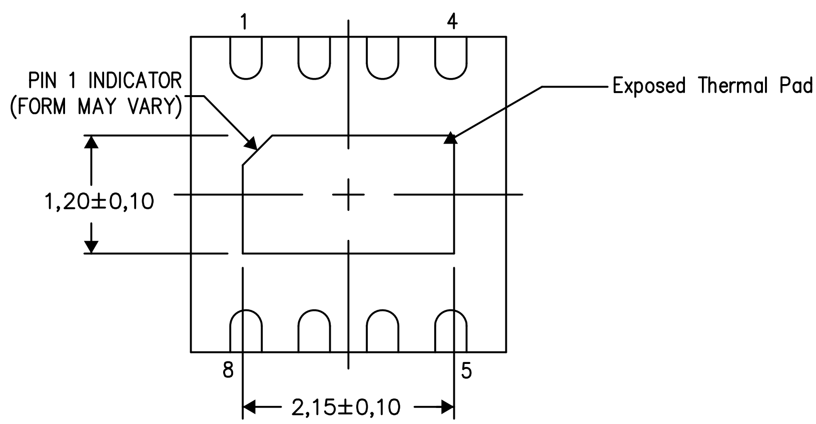
DSD (S-PWSON-N8) PLASTIC SMALL OUTLINE NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



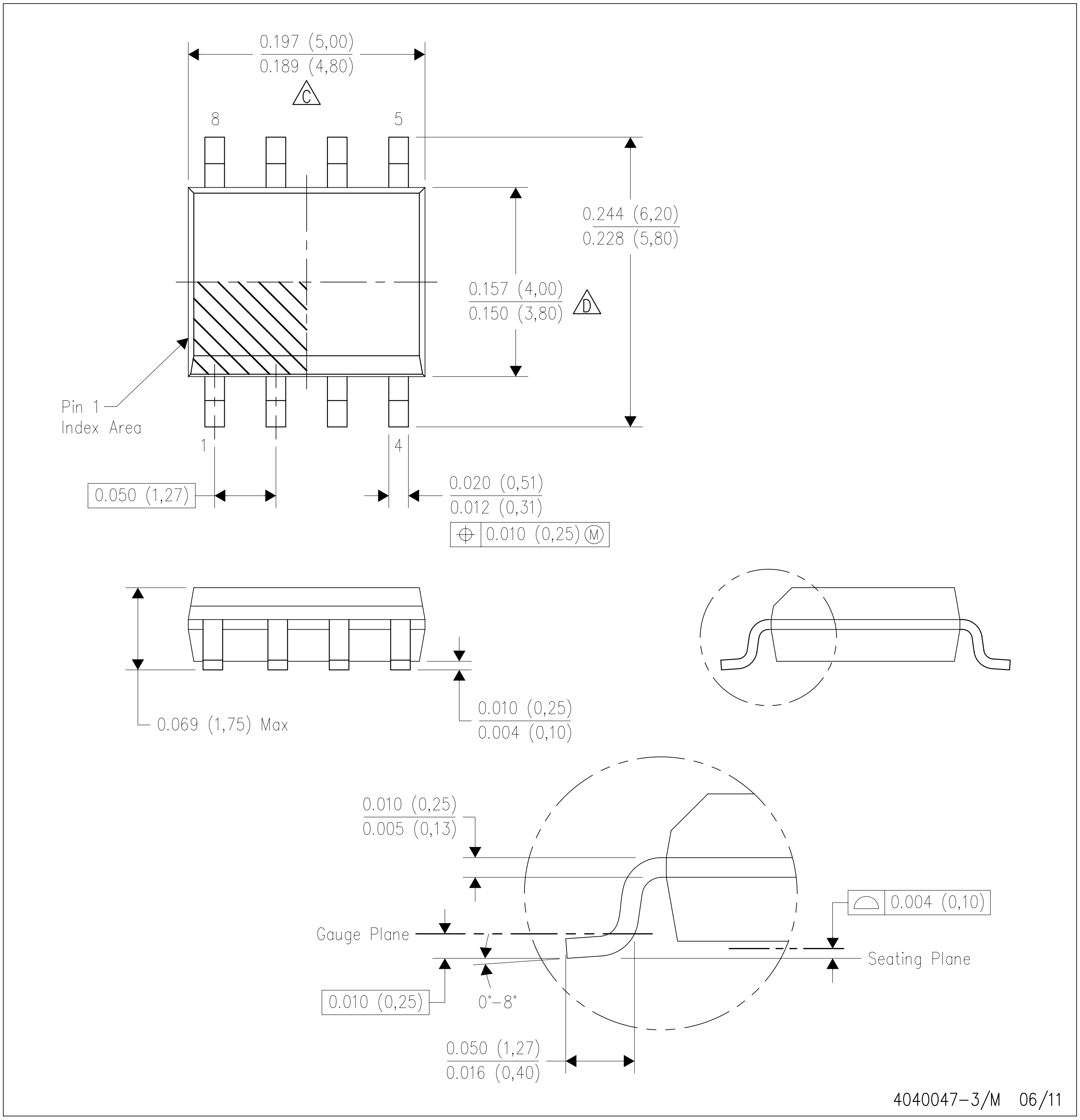
Bottom View

Exposed Thermal Pad Dimensions

4211722-5/B 02/14

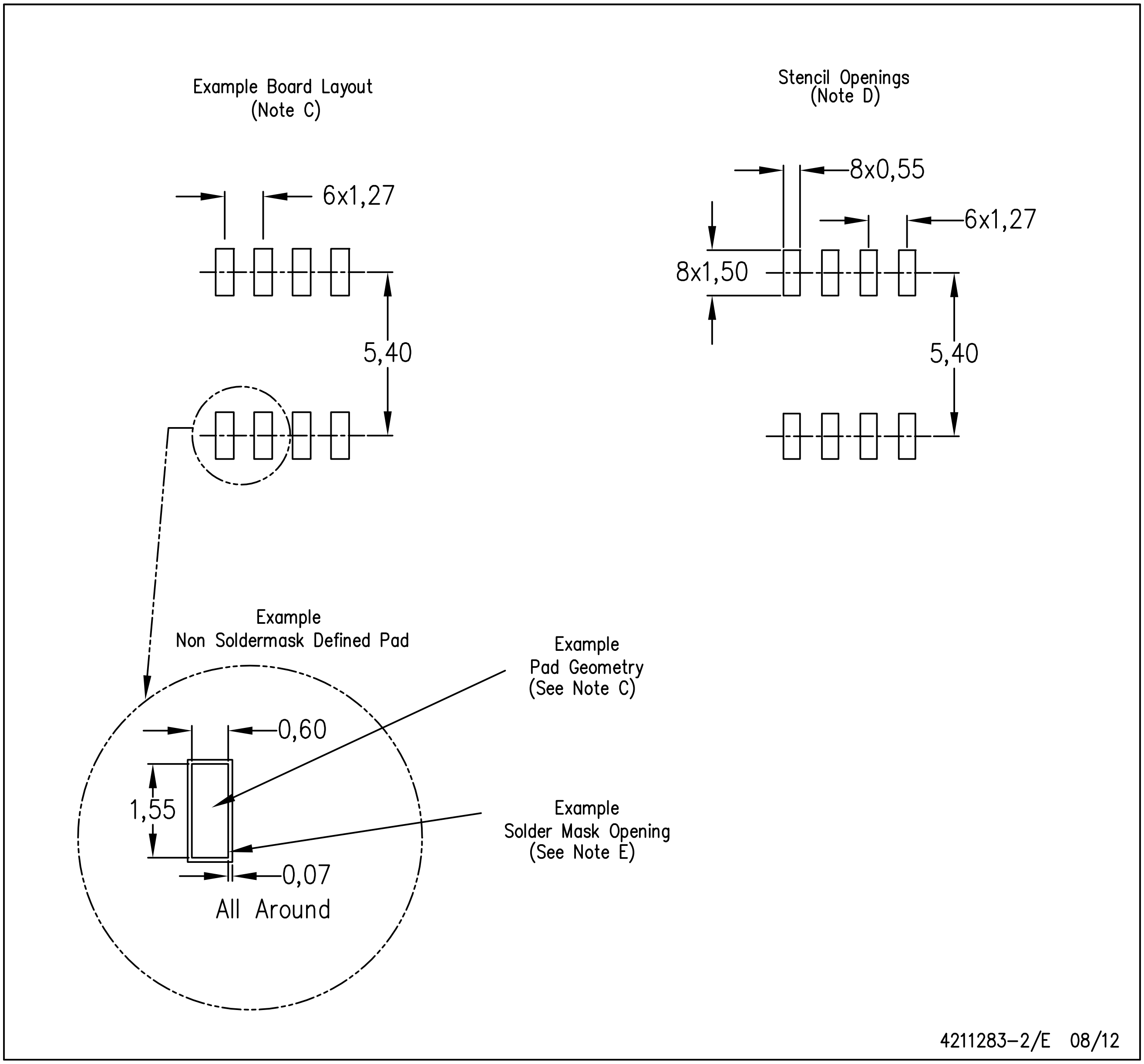
NOTE: A. All linear dimensions are in millimeters

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AA.

D (R-PDSO-G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC-7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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