

## 120-V Boot, 3-A Peak, High Frequency, High-Side/Low-Side Driver

### FEATURES

- Specified from -40 °C to 140 °C
- Drives Two N-Channel MOSFETs in High-Side/Low-Side Configuration
- Maximum Boot Voltage 120 V
- Maximum VDD Voltage 20 V
- On-Chip 0.65-V VF, 0.6-Ω RD Bootstrap Diode
- Greater than 1 MHz of Operation
- 20-ns Propagation Delay Times
- 3-A Sink, 3-A Source Output Currents
- 8-ns Rise/7-ns Fall Time with 1000-pF Load
- 1-ns Delay Matching
- Under Voltage Lockout for High-Side and Low-Side Driver

### APPLICATIONS

- Power Supplies for Telecom, Datacom, and Merchant Markets
- Half-Bridge Applications and Full-Bridge Converters
- Isolated Bus Architecture
- Two-Switch Forward Converters
- Active-Clamp Forward Converters
- High Voltage Synchronous-Buck Converters
- Class-D Audio Amplifiers

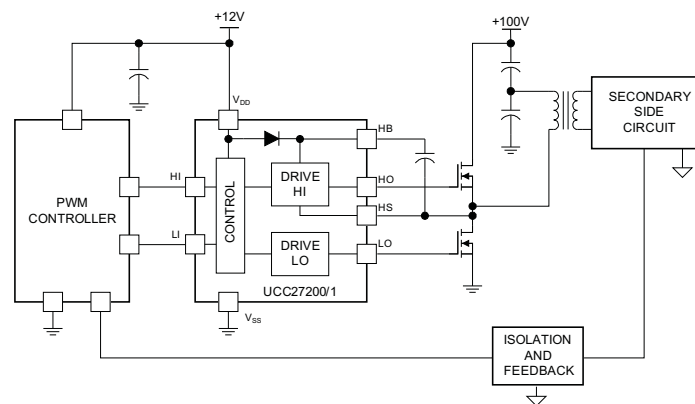
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### DESCRIPTION

The UCC27200/1 family of high frequency N-Channel MOSFET drivers include a 120-V bootstrap diode and high-side/low-side driver with independent inputs for maximum control flexibility. This allows for N-Channel MOSFET control in half-bridge, full-bridge, two-switch forward and active clamp forward converters. The low-side and the high-side gate drivers are independently controlled and matched to 1-ns between the turn-on and turn-off of each other.

### Simplified Application Diagram



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## DESCRIPTION (CONT.)

An on-chip bootstrap diode eliminates the external discrete diodes. Under-voltage lockout is provided for both the high-side and the low-side drivers forcing the outputs low if the drive voltage is below the specified threshold.

Two versions of the UCC27200 are offered. The UCC27200 has high noise immune CMOS input thresholds while the UCC27201 has TTL compatible thresholds.

Both devices are offered in 8-pin SOIC (D), PowerPad™ SOIC-8 (DDA) and SON-8 (DRM) packages.

## ORDERING INFORMATION

PACKAGED DEVICES <sup>(1)</sup>				
TEMPERATURE RANGE $T_A = T_J$	INPUT COMPATIBILITY	SOIC-8 (D) <sup>(2)</sup>	PowerPad™ SOIC-8 (DDA) <sup>(2)</sup>	SON-8 (DRM) <sup>(3)</sup>
-40°C to +140°C	CMOS	UCC27200D	UCC27200DDA	UCC27200DRMT
	TTL	UCC27201D	UCC27201DDA	UCC27201DRMT

- (1) These products are packaged in Lead (Pb)-Free and green lead finish of PdNiAu which is compatible with MSL level 1 at 255-260°C peak reflow temperature to be compatible with either lead free or Sn/Pb soldering operations.
- (2) D (SOIC-8) and DDA (Power Pad™ SOIC-8) packages are available taped and reeled. Add R suffix to device type (e.g. UCC27200DR) to order quantities of 2,500 devices per reel.
- (3) DRM (SON-8) package comes either in a small reel of 250 pieces as part number UCC27200DRMT, or larger reels of 3000 pieces as part number UCC27200 DRMR.

## DEVICE RATINGS

### ABSOLUTE MAXIMUM RATINGS

Over operating free-air temperature, unless noted, all voltages are with respect to  $V_{SS}$ <sup>(1)</sup>

PARAMETER	VALUE	UNIT	
Supply voltage range, <sup>(2)</sup> $V_{DD}$	-0.3 to 20	V	
Input voltages on LI and HI, $V_{LI}$ , $V_{HI}$	-0.3 to 20		
Output voltage on LO, $V_{LO}$	DC		-0.3 to $V_{DD} + 0.3$ ,
	Repetitive pulse <100 ns		-2 to $V_{DD} + 0.3$
Output voltage on HO, $V_{HO}$	DC		$V_{HS} - 0.3$ to $V_{HB} + 0.3$
	Repetitive pulse <100 ns		$V_{HS} - 2$ to $V_{HB} + 0.3$ , ( $V_{HB} - V_{HS} < 20$ )
Voltage on HS, $V_{HS}$	DC		-1 to 120
	Repetitive pulse <100 ns		-5 to 120
Voltage on HB, $V_{HB}$	-0.3 to 120		
Voltage On HB-HS	-0.3 to 20		
Operating virtual junction temperature range, $T_J$	-40 to +150	°C	
Storage temperature, $T_{STG}$	-65 to +150		
Lead temperature (soldering, 10 sec.)	+300		
Power dissipation at $T_A = 25^\circ\text{C}$ (D package) <sup>(3)</sup>	1.3	W	
Power dissipation at $T_A = 25^\circ\text{C}$ (DDA package) <sup>(3)</sup>	2.7		
Power dissipation at $T_A = 25^\circ\text{C}$ (DRM package) <sup>(3)</sup>	3.3		

- (1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltages are with respect to  $V_{SS}$ . Currents are positive into, negative out of the specified terminal.
- (3) This data was taken using the JEDEC proposed high-K test PCB. See THERMAL CHARACTERISTICS section for details.

## RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

PARAMETER		MIN	NOM	MAX	UNIT
V <sub>DD</sub>	Supply voltage range	8	12	17	V
V <sub>HS</sub>	Voltage on HS	-1		105	
	Voltage on HS, (repetitive pulse <100 ns)	-5		110	
V <sub>HB</sub>	Voltage on HB	V <sub>HS</sub> + 8, V <sub>DD</sub> -1		V <sub>HS</sub> + 17, 115	
	Voltage slew rate on HS			50	V / ns
T <sub>J</sub>	Operating junction temperature range	-40		+140	°C

## ELECTROSTATIC DISCHARGE (ESD) PROTECTION

METHOD	MIN	UNIT
Human body model	2000	V
CDM	1000	

## THERMAL CHARACTERISTICS

over operating free-air temperature range, maximum power dissipation at ambient temperature:  $P_{DISS} = (150 - T_A) / \theta_{JA}$ , (unless otherwise noted)

PACKAGE	$\theta_{JA}$ (°C/W)(Junction to Ambient)	$\theta_{JC}$ (°C/W)( Junction to Case)	$\theta_{JP}$ (°C/W) ( Junction to PowerPad™)
D	95	71	NA
DDA <sup>(1)</sup>	46	71	4.8
DRM <sup>(2)</sup>	38	56	4.1

- (1) Test board conditions:
- 3in x 3in, four4 layers, thickness: 0.062 in.
  - 2-oz copper traces located on the top and bottom of the PCB.
  - 2-oz copper ground planes on the internal 2 layers.
  - Six thermal vias in the PowerPad™ area under the device package.
- (2) Test board conditions:
- 3in x 3in, 4 layers, thickness: 0.062 in.
  - 2-oz copper traces located on the top and bottom of the PCB.
  - 2-oz copper ground planes on the internal 2 layers.
  - Four thermal vias in the PowerPad™ area under the device package.

### ELECTRICAL CHARACTERISTICS

over operating free-air temperature range,  $V_{DD} = V_{HB} = 12\text{ V}$ ,  $V_{HS} = V_{SS} = 0\text{ V}$ , No load on LO or HO,  $T_A = T_J = -40^\circ\text{C}$  to  $+140^\circ\text{C}$ , (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>Supply Currents</b>						
$I_{DD}$	VDD quiescent current	$V_{LI} = V_{HI} = 0$		0.4	0.8	mA
$I_{DDO}$	VDD operating current	UCC27200		2.5	4	
		UCC27201		3.8	5.5	
$I_{HB}$	Boot voltage quiescent current	$V_{LI} = V_{HI} = 0\text{ V}$		0.4	0.8	
$I_{HBO}$	Boot voltage operating current	$f = 500\text{ kHz}$ , $C_{LOAD} = 0$		2.5	4	
$I_{HBS}$	HB to $V_{SS}$ quiescent current	$V_{HS} = V_{HB} = 110\text{ V}$		0.0005	1	
$I_{HBSO}$	HB to $V_{SS}$ operating current	$f = 500\text{ kHz}$ , $C_{LOAD} = 0$		0.1		mA
<b>Input</b>						
$V_{HIT}$	Input rising threshold	UCC27200		5.8	8	V
$V_{LIT}$	Input falling threshold		3	5.4		
$V_{IHYS}$	Input voltage hysteresis			0.4		
$V_{HIT}$	Input voltage threshold	UCC27201		1.7	2.5	mV
$V_{LIT}$	Input voltage threshold		0.8	1.6		
$V_{IHYS}$	Input voltage Hysteresis			100		
$R_{IN}$	Input pulldown resistance		100	200	350	k $\Omega$
<b>Undervoltage Protection (UVLO)</b>						
	VDD rising threshold		6.2	7.1	7.8	V
	VDD threshold hysteresis			0.5		
	VHB rising threshold		5.8	6.7	7.2	
	VHB threshold hysteresis			0.4		
<b>Bootstrap Diode</b>						
$V_F$	Low-current forward voltage	$I_{VDD} - HB = 100\ \mu\text{A}$		0.65	0.85	V
$V_{FI}$	High-current forward voltage	$I_{VDD} - HB = 100\text{ mA}$		0.85	1.1	
$R_D$	Dynamic resistance, $\Delta V/\Delta I$	$I_{VDD} - HB = 100\text{ mA}$ and 80 mA		0.6	1.0	$\Omega$
<b>LO Gate Driver</b>						
$V_{LOL}$	Low level output voltage	$I_{LO} = 100\text{ mA}$		0.18	0.4	V
$V_{LOH}$	High level output voltage	$T_J = -40$ to $125^\circ\text{C}$	$I_{LO} = -100\text{ mA}$ , $V_{LOH} = V_{DD} - V_{LO}$	0.25	0.4	
		$T_J = -40$ to $140^\circ\text{C}$	$I_{LO} = -100\text{ mA}$ , $V_{LOH} = V_{DD} - V_{LO}$	0.25	0.42	
	Peak pull-up current	$V_{LO} = 0\text{ V}$		3		A
	Peak pull-down current	$V_{LO} = 12\text{ V}$		3		
<b>HO Gate Driver</b>						
$V_{HOL}$	Low level output voltage	$I_{HO} = 100\text{ mA}$		0.18	0.4	V
$V_{HOH}$	High level output voltage	$T_J = -40$ to $125^\circ\text{C}$	$I_{HO} = -100\text{ mA}$ , $V_{HOH} = V_{HB} - V_{HO}$	0.25	0.4	
		$T_J = -40$ to $140^\circ\text{C}$	$I_{HO} = -100\text{ mA}$ , $V_{HOH} = V_{HB} - V_{HO}$	0.25	0.42	
	Peak pull-up current	$V_{HO} = 0\text{ V}$		3		A
	Peak pull-down current	$V_{HO} = 12\text{ V}$		3		
<b>Propagation Delays</b>						

**ELECTRICAL CHARACTERISTICS (continued)**

over operating free-air temperature range,  $V_{DD} = V_{HB} = 12\text{ V}$ ,  $V_{HS} = V_{SS} = 0\text{ V}$ , No load on LO or HO,  $T_A = T_J = -40^\circ\text{C}$  to  $+140^\circ\text{C}$ , (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT	
$T_{DLFF}$	$V_{LI}$ falling to $V_{LO}$ falling	$T_J = -40$ to $125^\circ\text{C}$	$C_{LOAD} = 0$		20	45	ns	
		$T_J = -40$ to $140^\circ\text{C}$	$C_{LOAD} = 0$		20	50		
$T_{DHFF}$	$V_{HI}$ falling to $V_{HO}$ falling	$T_J = -40$ to $125^\circ\text{C}$	$C_{LOAD} = 0$		20	45		
		$T_J = -40$ to $140^\circ\text{C}$	$C_{LOAD} = 0$		20	50		
$T_{DLRR}$	$V_{LI}$ rising to $V_{LO}$ rising	$T_J = -40$ to $125^\circ\text{C}$	$C_{LOAD} = 0$		20	45		
		$T_J = -40$ to $140^\circ\text{C}$	$C_{LOAD} = 0$		20	50		
$T_{DHRR}$	$V_{HI}$ rising to $V_{HO}$ rising	$T_J = -40$ to $125^\circ\text{C}$	$C_{LOAD} = 0$		20	45		
		$T_J = -40$ to $140^\circ\text{C}$	$C_{LOAD} = 0$		20	50		
<b>Delay Matching</b>								
$T_{MON}$	LI ON, HI OFF				1	7		ns
$T_{MOFF}$	LI OFF, HI ON				1	7		
<b>Output Rise and Fall Time</b>								
$t_R$	LO, HO		$C_{LOAD} = 1000\text{ pF}$		8		ns	
$t_F$	LO, HO		$C_{LOAD} = 1000\text{ pF}$		7			
$t_R$	LO, HO (3 V to 9 V)		$C_{LOAD} = 0.1\text{ }\mu\text{F}$		0.35	0.6	us	
$t_F$	LO, HO (3 V to 9 V)		$C_{LOAD} = 0.1\text{ }\mu\text{F}$		0.3	0.6		
<b>Miscellaneous</b>								
	Minimum input pulse width that changes the output					50	ns	
	Bootstrap diode turn-off time		$I_F = 20\text{ mA}$ , $I_{REV} = 0.5\text{ A}^{(1)(2)}$		20			

(1) Typical values for  $T_A = 25^\circ\text{C}$

(2)  $I_F$ : Forward current applied to bootstrap diode,  $I_{REV}$ : Reverse current applied to bootstrap diode.

**TYPICAL CHARACTERISTICS**

**UCC27200 IDD OPERATING CURRENT  
VS  
FREQUENCY**

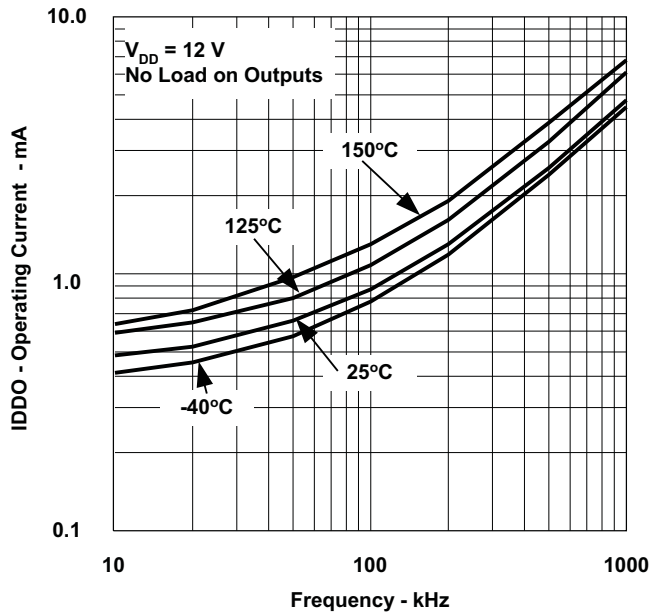


Figure 1.

**UCC27201 IDD OPERATING CURRENT  
VS  
FREQUENCY**

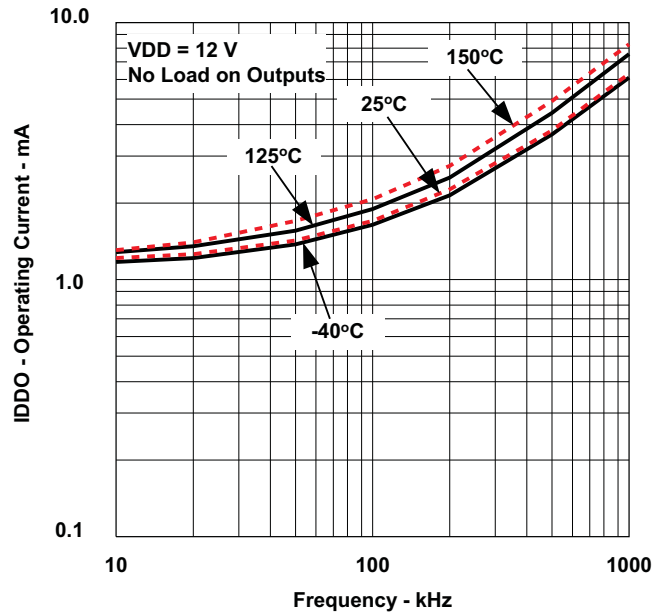


Figure 2.

**BOOT VOLTAGE OPERATING CURRENT  
VS  
FREQUENCY**

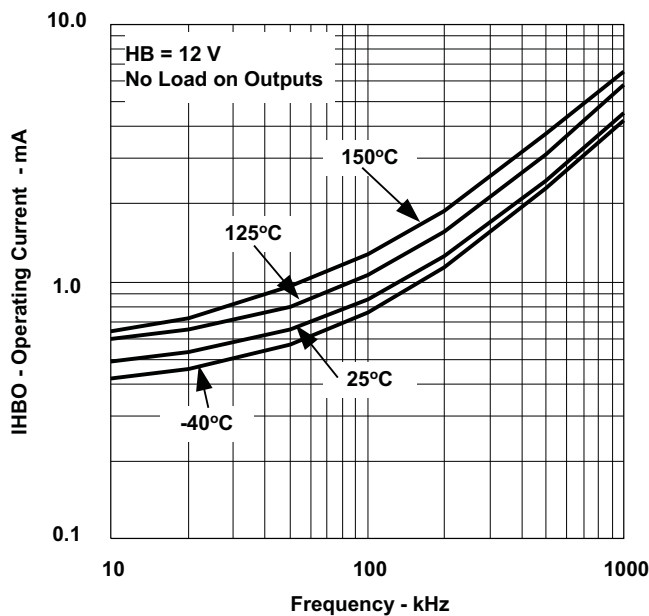


Figure 3.

**HB TO VSS OPERATING CURRENT  
VS  
FREQUENCY**

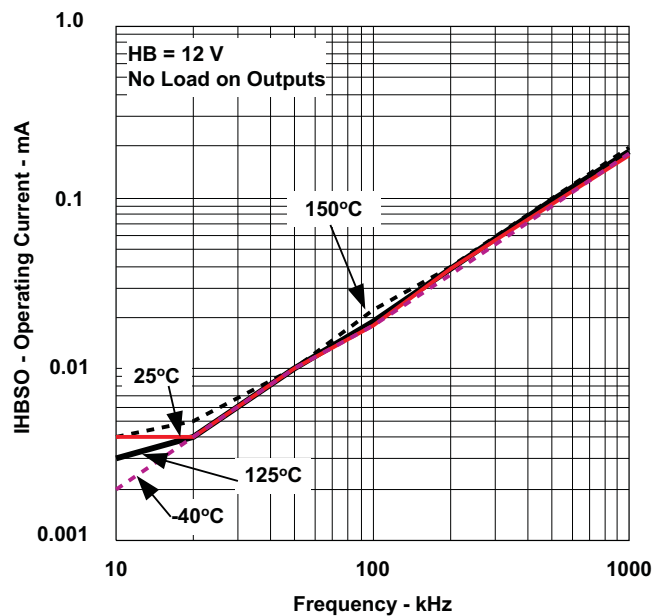


Figure 4.

TYPICAL CHARACTERISTICS (continued)

UCC27200 INPUT THRESHOLD  
vs  
SUPPLY VOLTAGE

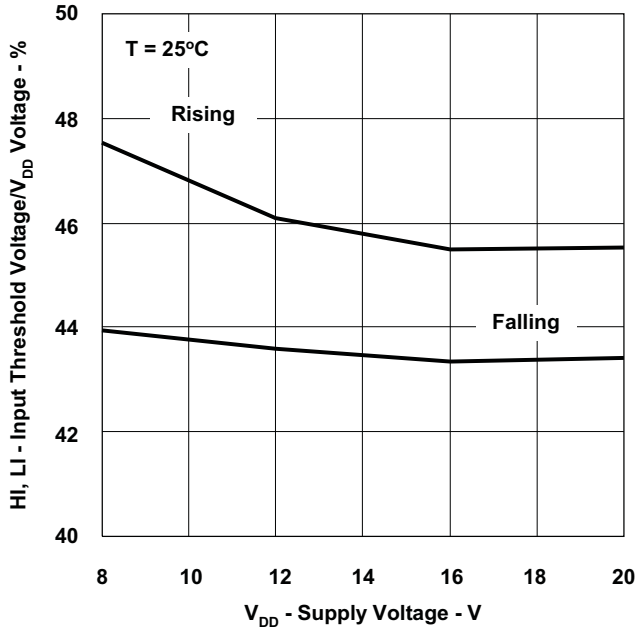


Figure 5.

UCC27201 INPUT THRESHOLD  
vs  
SUPPLY VOLTAGE

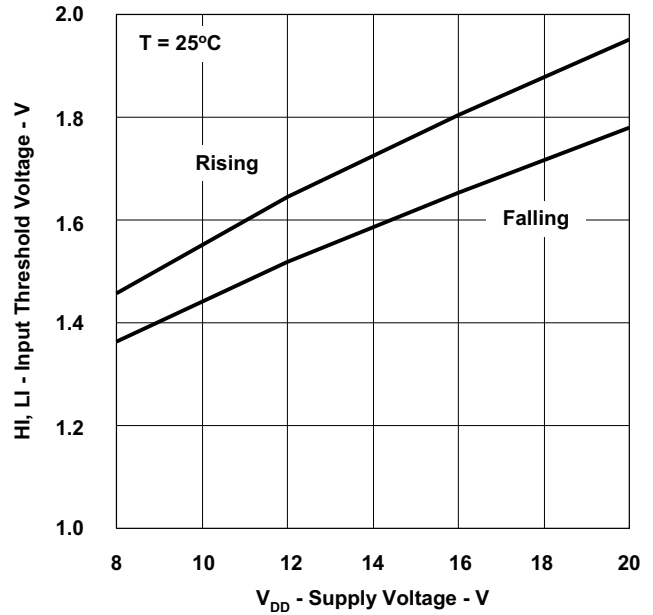


Figure 6.

UCC27200 INPUT THRESHOLD  
vs  
TEMPERATURE

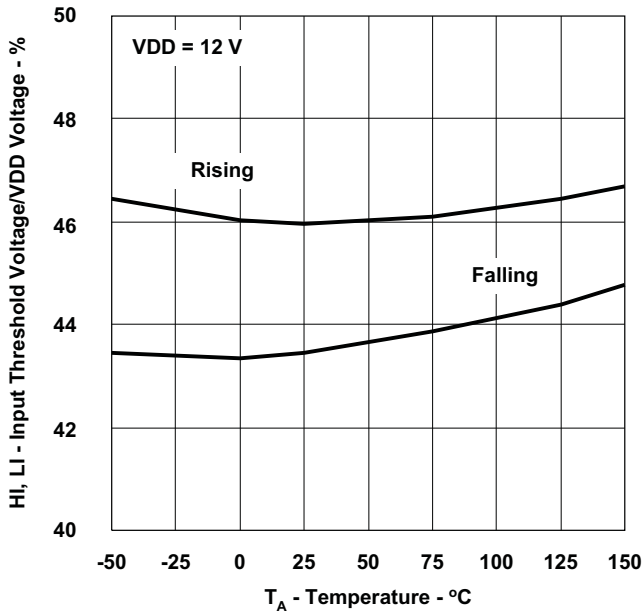


Figure 7.

UCC27201 INPUT THRESHOLD  
vs  
TEMPERATURE

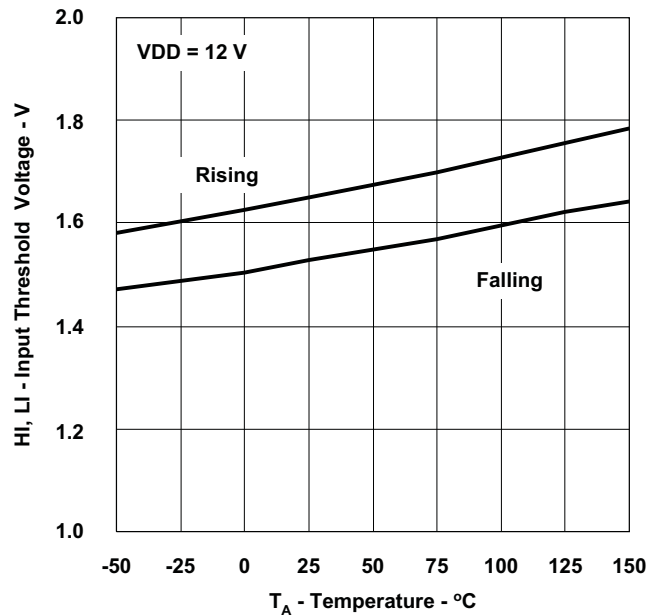
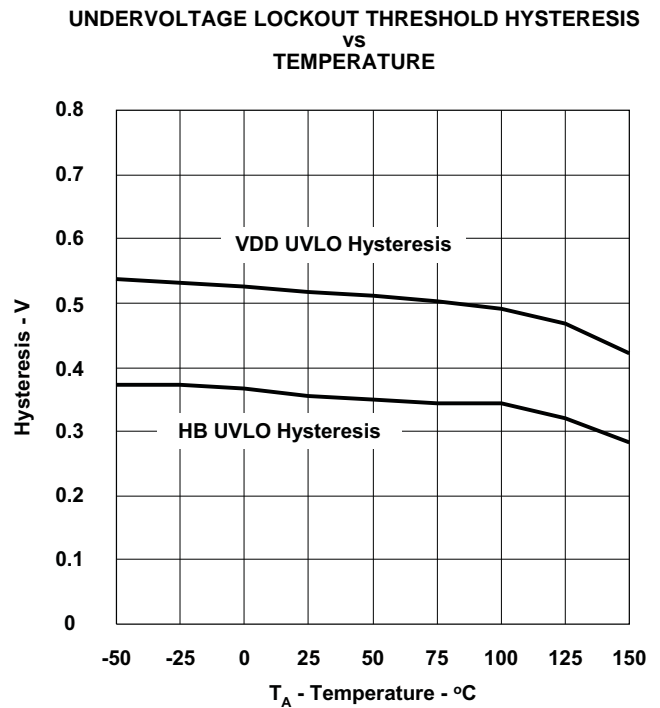
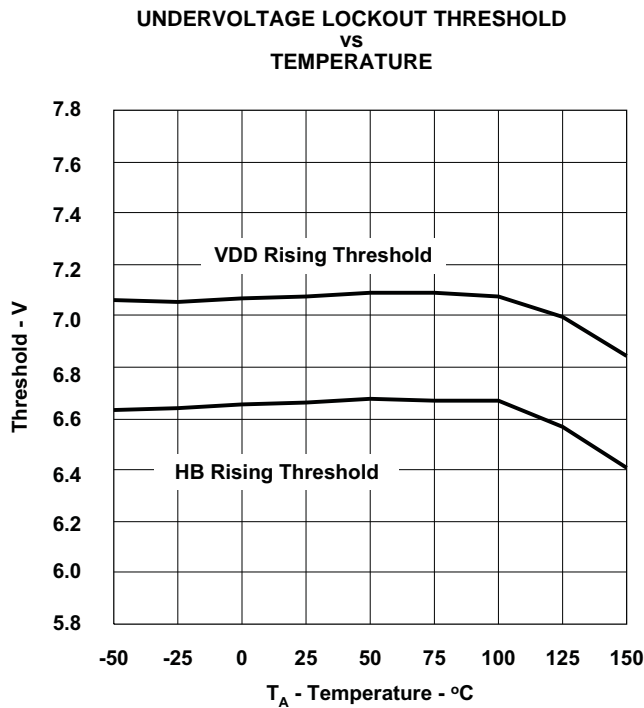
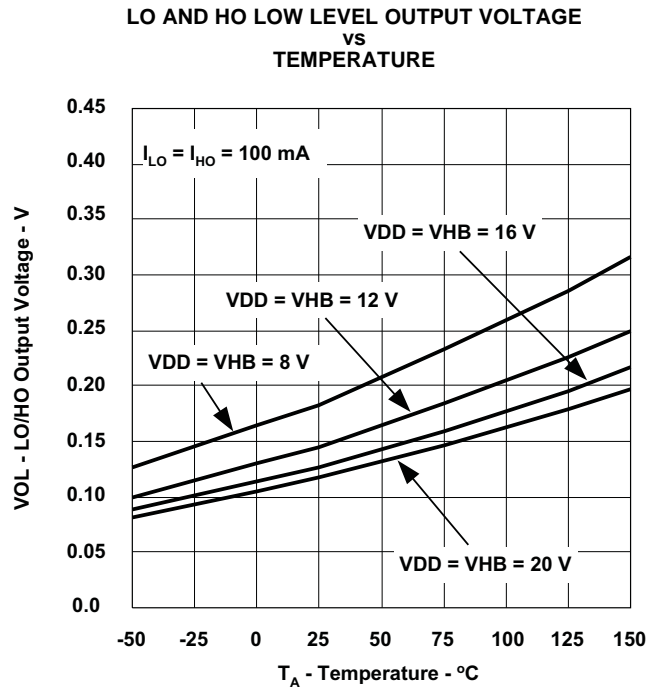
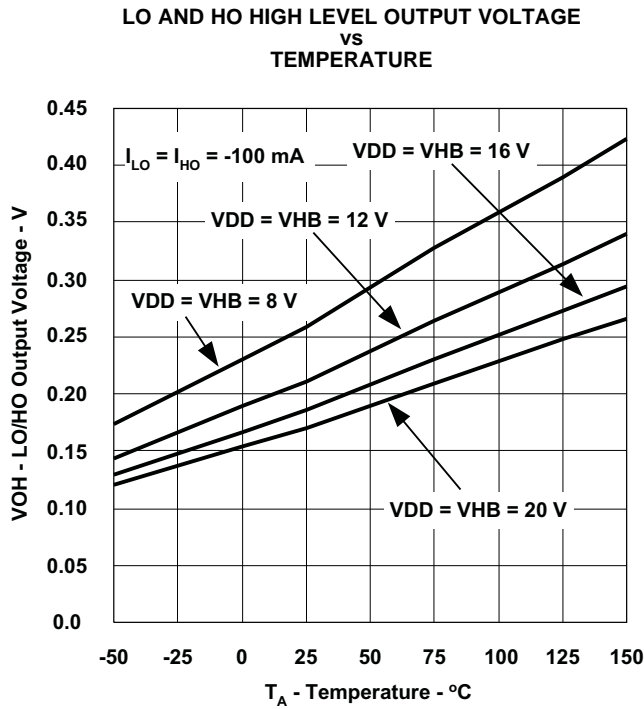


Figure 8.

TYPICAL CHARACTERISTICS (continued)



TYPICAL CHARACTERISTICS (continued)

UCC27200 PROPAGATION DELAYS  
vs  
TEMPERATURE

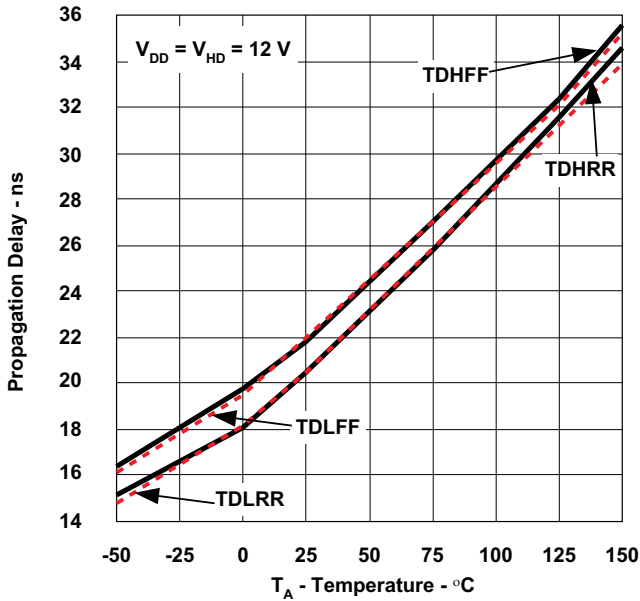


Figure 13.

UCC27201 PROPAGATION DELAYS  
vs  
TEMPERATURE

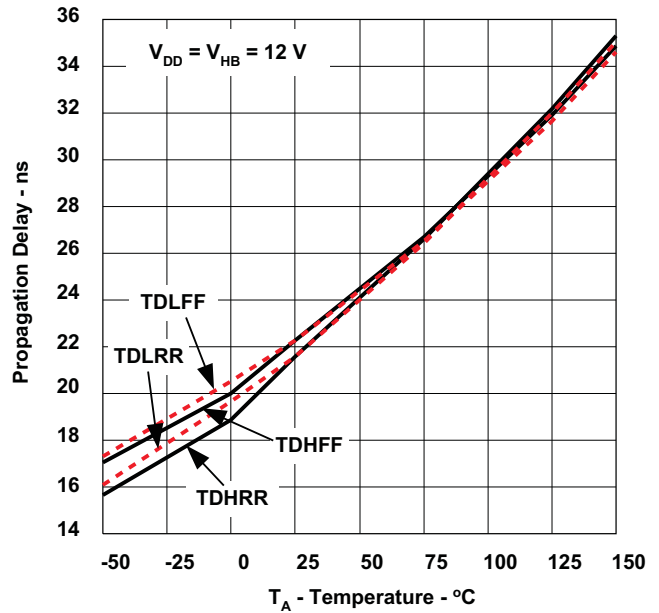


Figure 14.

UCC27200 PROPAGATION DELAY  
vs  
SUPPLY VOLTAGE

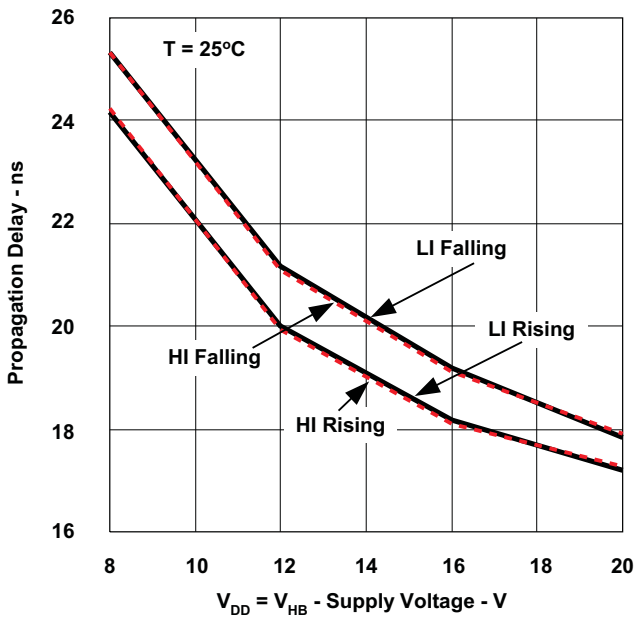


Figure 15.

UCC27201 PROPAGATION DELAY  
vs  
SUPPLY VOLTAGE

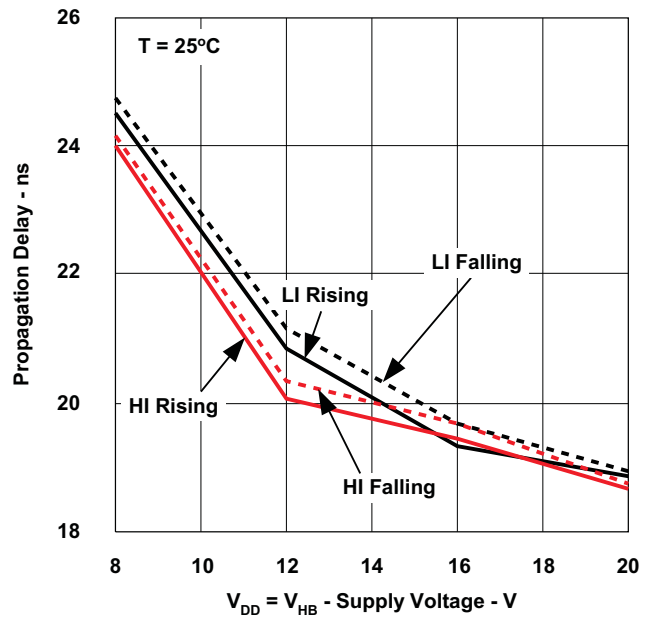


Figure 16.

TYPICAL CHARACTERISTICS (continued)

DELAY MATCHING  
VS  
TEMPERATURE

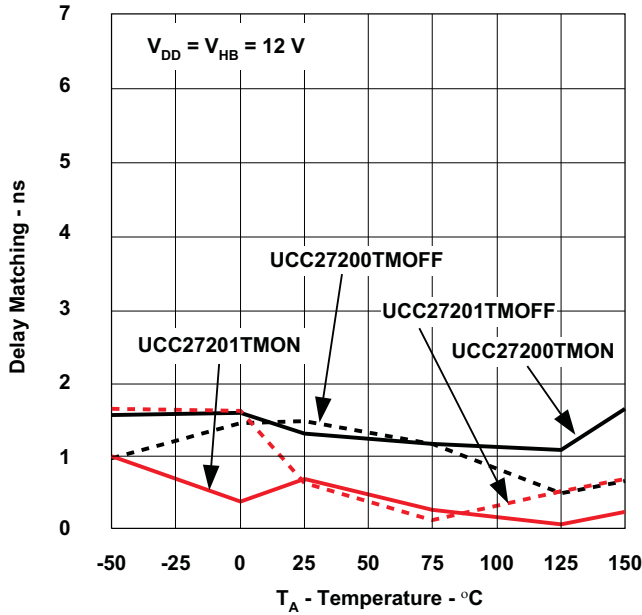


Figure 17.

OUTPUT CURRENT  
VS  
OUTPUT VOLTAGE

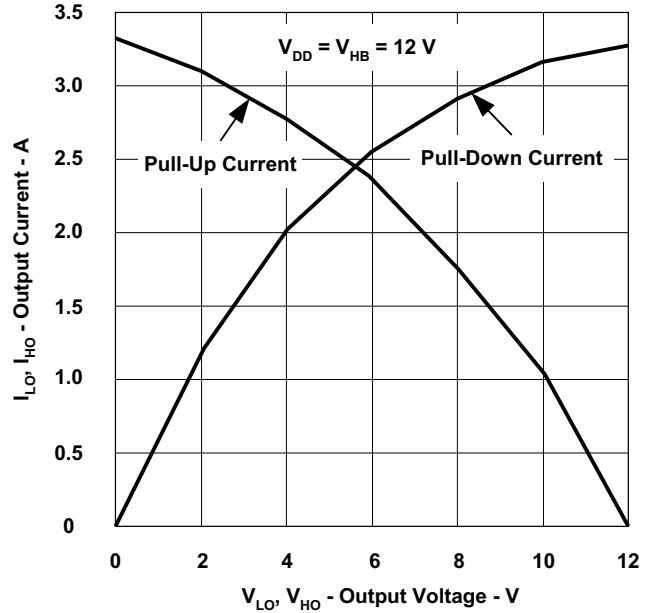


Figure 18.

DIODE CURRENT  
VS  
DIODE VOLTAGE

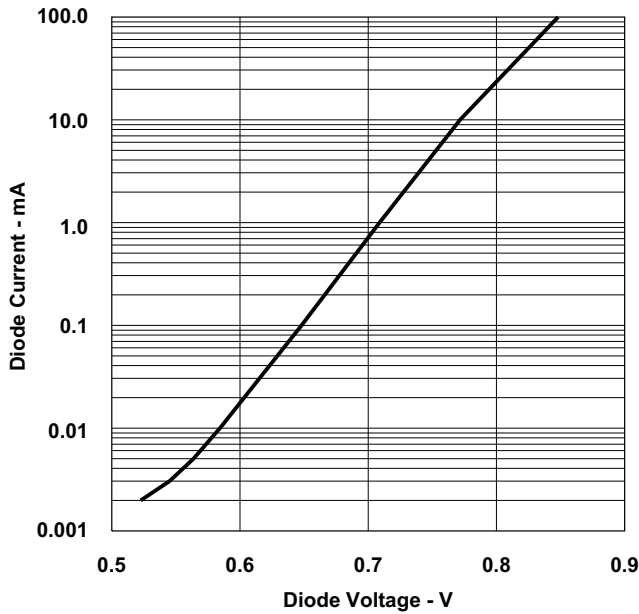


Figure 19.

QUIESCENT CURRENT  
VS  
SUPPLY VOLTAGE

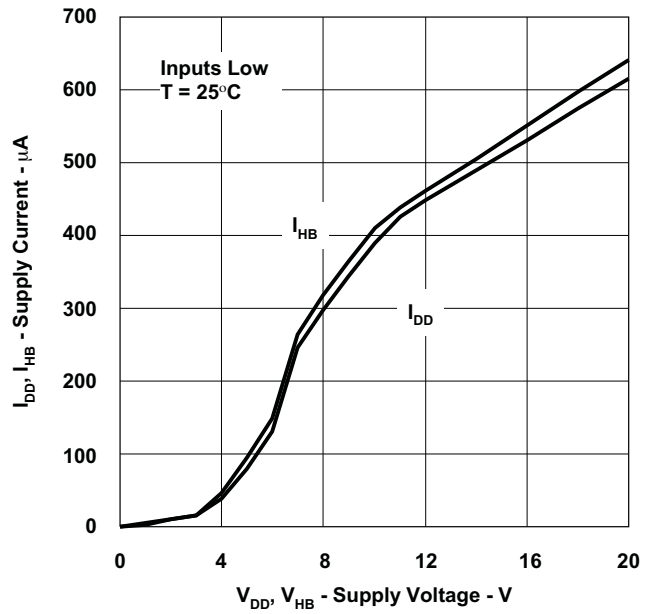
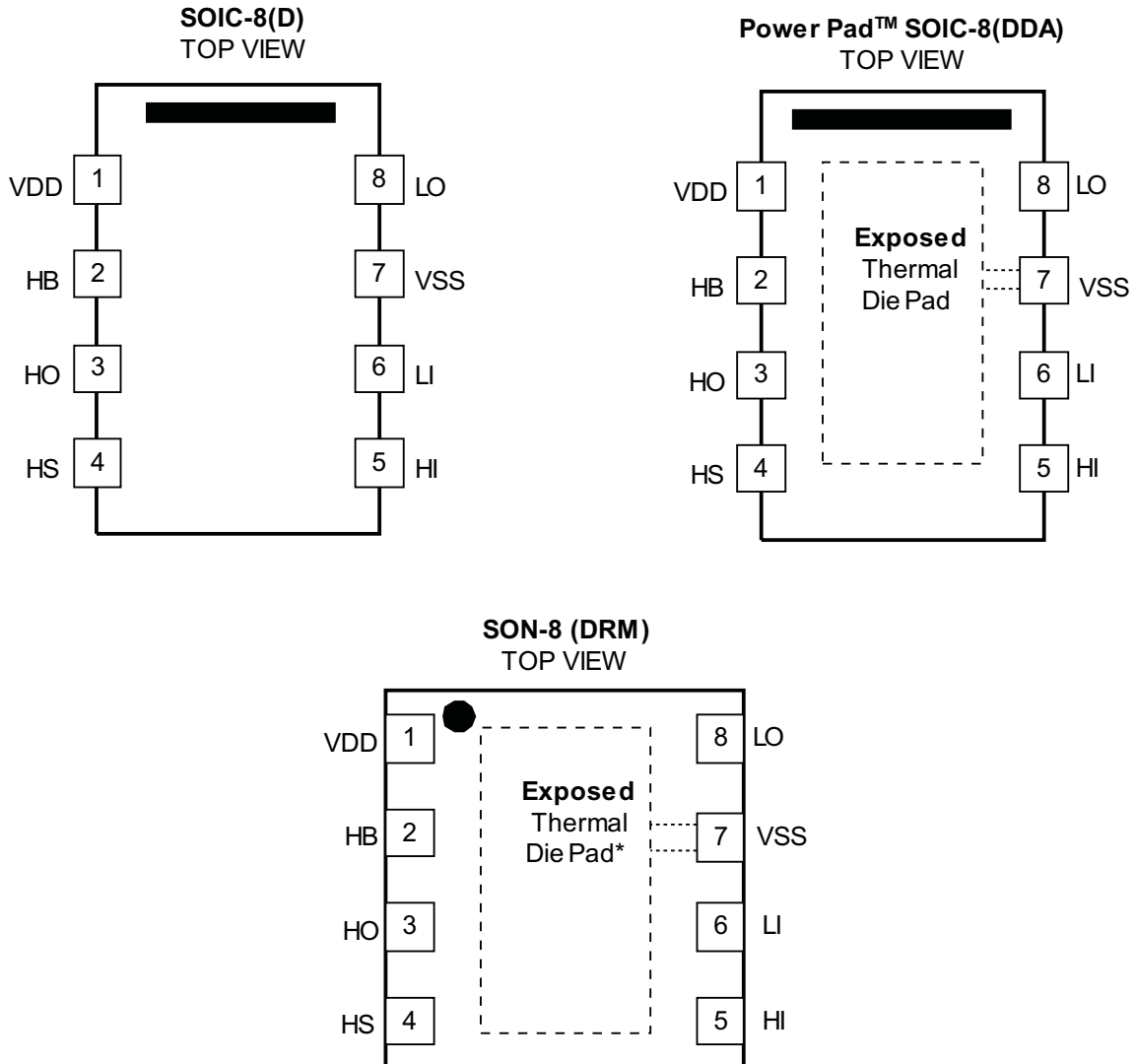


Figure 20.

DEVICE INFORMATION



NOTE:

Pin VSS and the exposed thermal die pad are internally connected.

**TERMINAL FUNCTIONS**

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
VDD	1	I	Positive supply to the lower gate driver. De-couple this pin to VSS (GND). Typical decoupling capacitor range is 0.22 $\mu$ F to 1.0 $\mu$ F.
HB	2	I	High-side bootstrap supply. The bootstrap diode is on-chip but the external bootstrap capacitor is required. Connect positive side of the bootstrap capacitor to this pin. Typical range of HB bypass capacitor is 0.022 $\mu$ F to 0.1 $\mu$ F, the value is dependant on the gate charge of the high-side MOSFET however.
HO	3	O	High-side output. Connect to the gate of the high-side power MOSFET.
HS	4	I	High-side source connection. Connect to source of high-side power MOSFET. Connect negative side of bootstrap capacitor to this pin.
HI	5	I	High-side input.
LI	6	I	Low-side input.
VSS	7	O	Negative supply terminal for the device which is generally grounded.
LO	8	O	Low-side output. Connect to the gate of the low-side power MOSFET.
PowerPAD™	PAD	-	Utilized on the DDA and DRM packages only. Electrically referenced to VSS (GND). Connect to a large thermal mass trace or GND plane to dramatically improve thermal performance.

FUNCTIONAL BLOCK DIAGRAM

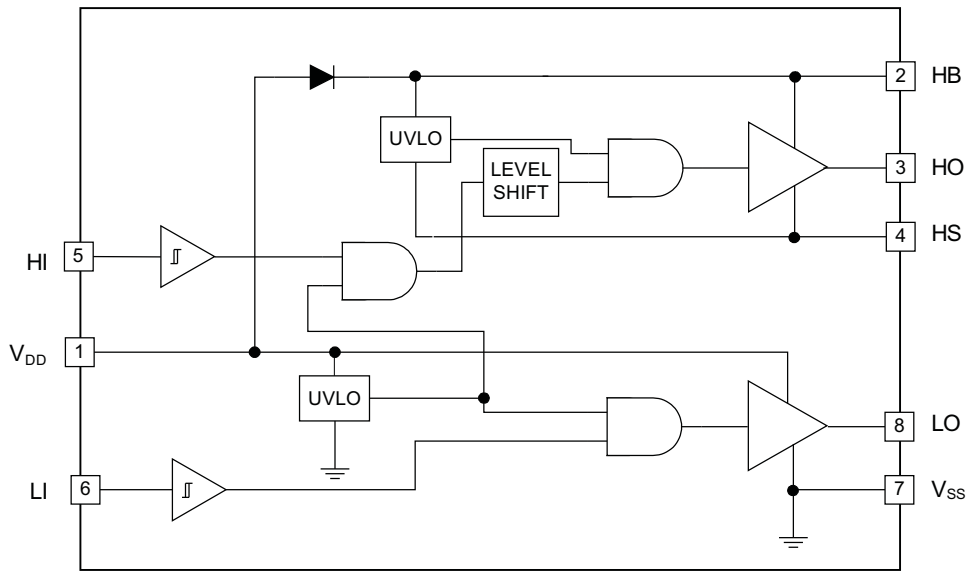


Figure 21.

TIMING DIAGRAMS

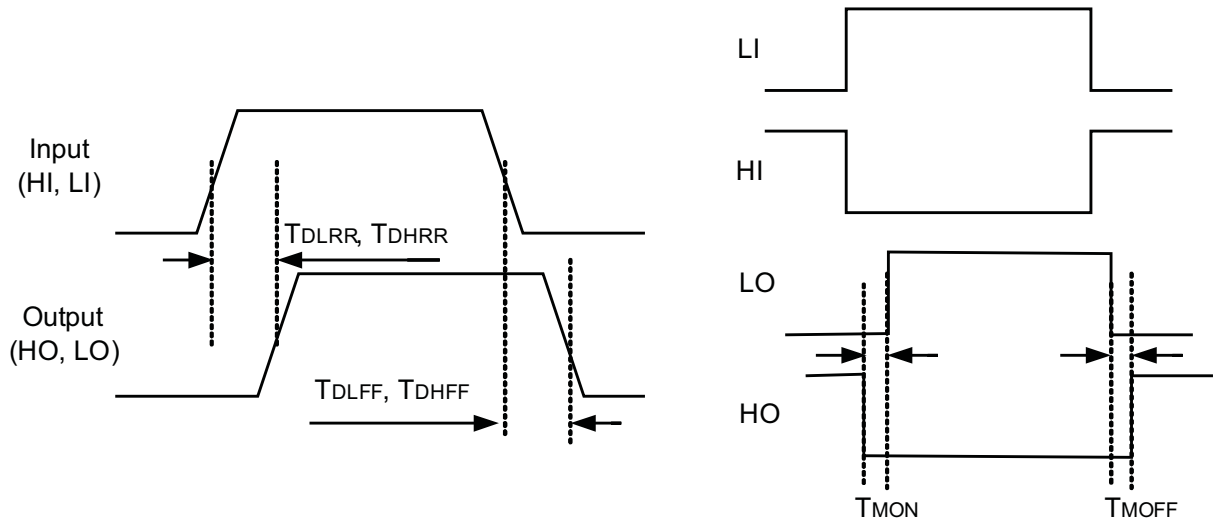


Figure 22.

## APPLICATION INFORMATION

### Functional Description

The UCC27200 and UCC27201 are high-side/low-side drivers. The high-side and low-side each have independent inputs which allow maximum flexibility of input control signals in the application. The boot diode for the high-side driver bias supply is internal to the UCC27200 and UCC27201. The UCC27200 is the CMOS compatible input version and the UCC27201 is the TTL or logic compatible version. The high-side driver is referenced to the switch node (HS) which is typically the source pin of the high side MOSFET and drain pin of the low-side MOSFET. The low-side driver is referenced to VSS which is typically ground. The functions contained are the input stages, UVLO protection, level shift, boot diode, and output driver stages.

#### NOTE:

The term “UCC2720x” applies to both the UCC27200 and UCC27201.

### Input Stages

The input stages provide the interface to the PWM output signals. The input impedance of the UCC27200 is 200 k $\Omega$  nominal and input capacitance is approximately 2 pF. The 200 k $\Omega$  is a pull-down resistance to Vss (ground). The CMOS compatible input of the UCC27200 provides a rising threshold of 48% of VDD and falling threshold of 45% of VDD. The inputs of the UCC27200 are intended to be driven from 0 to VDD levels.

The input stages of the UCC27201 incorporate an open drain configuration to provide the lower input thresholds. The input impedance is 200 k $\Omega$  nominal and input capacitance is approximately 4 pF. The 200 k $\Omega$  is a pull-down resistance to VSS (ground). The logic level compatible input provides a rising threshold of 1.7 V and a falling threshold of 1.6 V.

### UVLO (Under Voltage Lockout)

The bias supplies for the high-side and low-side drivers have UVLO protection. VDD as well as VHB to VHS differential voltages are monitored. The VDD UVLO disables both drivers when VDD is below the specified threshold. The rising VDD threshold is 7.1 V with 0.5-V hysteresis. The VHB UVLO disables only the high-side driver when the VHB to VHS differential voltage is below the specified threshold. The VHB UVLO rising threshold is 6.7 V with 0.4-V hysteresis.

### Level Shift

The level shift circuit is the interface from the high-side input to the high-side driver stage which is referenced to the switch node (HS). The level shift allows control of the HO output referenced to the HS pin and provides excellent delay matching with the low-side driver.

### Boot Diode

The boot diode necessary to generate the high-side bias is included in the UCC2720x family of drivers. The diode anode is connected to VDD and cathode connected to VHB. With the VHB capacitor connected to HB and the HS pins, the VHB capacitor charge is refreshed every switching cycle when HS transitions to ground. The boot diode provides fast recovery times, low diode resistance, and voltage rating margin to allow for efficient and reliable operation.

### Output Stages

The output stages are the interface to the power MOSFETs in the power train. High slew rate, low resistance and high peak current capability of both output drivers allow for efficient switching of the power MOSFETs. The low-side output stage is referenced from VDD to VSS and the high-side is referenced from VHB to VHS.

## Design Tips

### Switching the MOSFETs

Achieving optimum drive performance at high frequency efficiently requires special attention to layout and minimizing parasitic inductances. Care must be taken at the driver die and package level as well as the PCB layout to reduce parasitic inductances as much as possible. Figure 23 shows the main parasitic inductance elements and current flow paths during the turn ON and OFF of the MOSFET by charging and discharging its CGS capacitance.

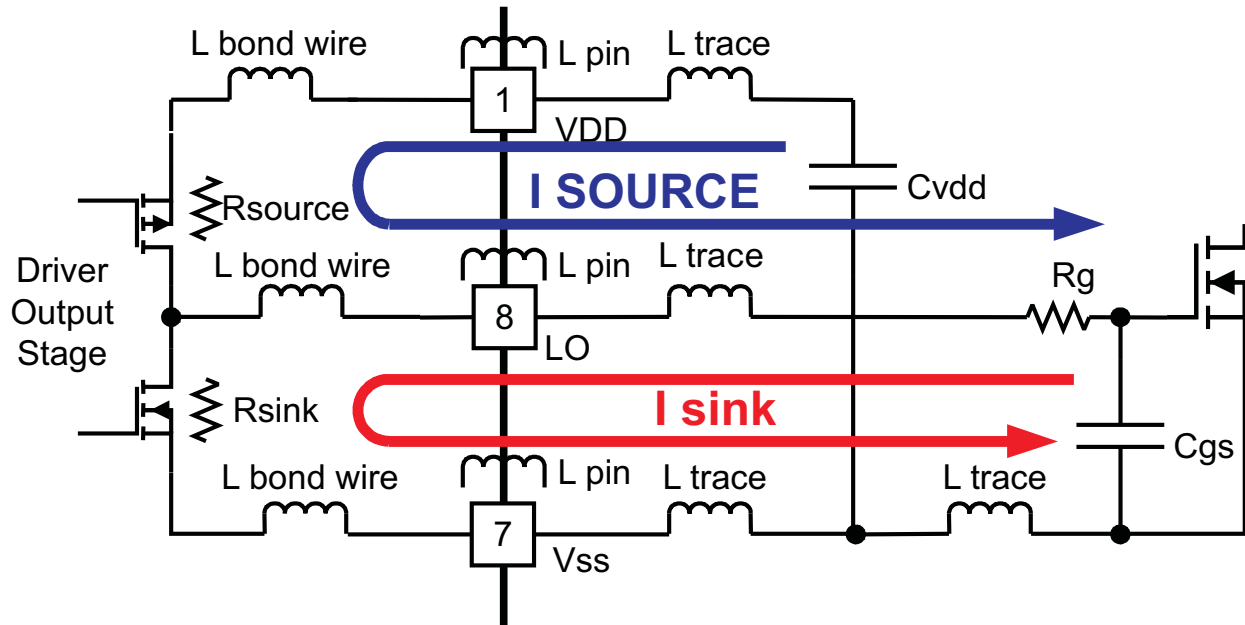


Figure 23. MOSFET Drive Paths and Circuit Parasitics

The  $I_{SOURCE}$  current charges the  $C_{GS}$  gate capacitor and the  $I_{SINK}$  current discharges it. The rise and fall time of the voltage across the gate to source defines how quickly the MOSFET can be switched. Based on actual measurements, the analytical curves in Figure 24 and Figure 25 indicate the output voltage and current of the drivers during the discharge of the load capacitor. Figure 24 shows voltage and current as a function of time. Figure 25 indicates the relationship of voltage and current during fast switching. These figures demonstrate the actual switching process and limitations due to parasitic inductances.

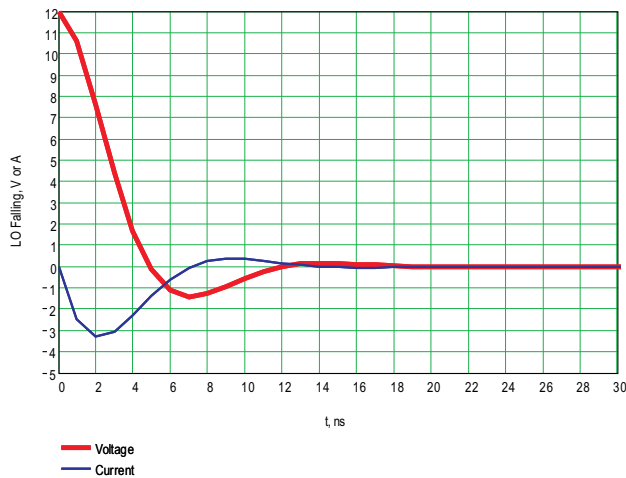


Figure 24. Turn-Off Voltage and Current vs Time

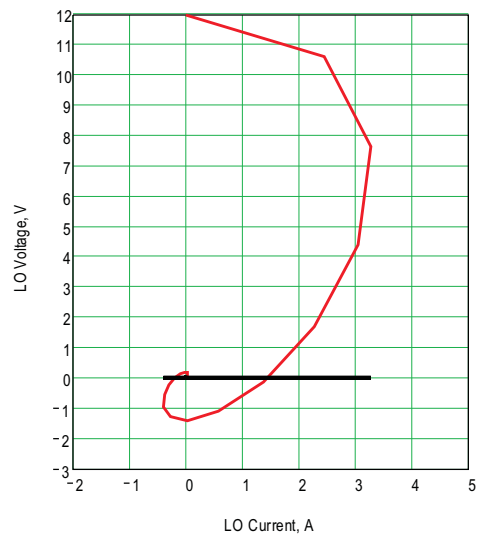


Figure 25. Turn-Off Voltage and Current Switching Diagram

Turning off the MOSFET needs to be achieved as fast as possible to minimize switching losses. For this reason the UCC2720x drivers are designed for high peak currents and low output resistance. The sink capability is specified as 0.18 V at 100-mA dc current implying 1.8-Ω  $R_{DS(on)}$ . With 12-V drive voltage, no parasitic inductance and a linear resistance, one would expect initial sink current amplitude of 6.7 A for both high-side and low-side drivers. Assuming a pure R-C discharge circuit of the gate capacitor, one would expect the voltage and current waveforms to be exponential. Due to the parasitic inductances and non-linear resistance of the driver MOSFET'S, the actual waveforms have some ringing and the peak-sink current of the drivers is approximately 3.3 A as shown in Figure 18. The overall parasitic inductance of the drive circuit is estimated at 4 nH. The internal parasitic inductance of the SOIC-8 package is estimated to be 2 nH including bond wires and leads. The SON-8 package reduces the internal parasitic inductances by more than 50%.

Actual measured waveforms are shown in Figure 26 and Figure 27. As shown, the typical rise time of 8 ns and fall time of 7 ns is conservatively rated.

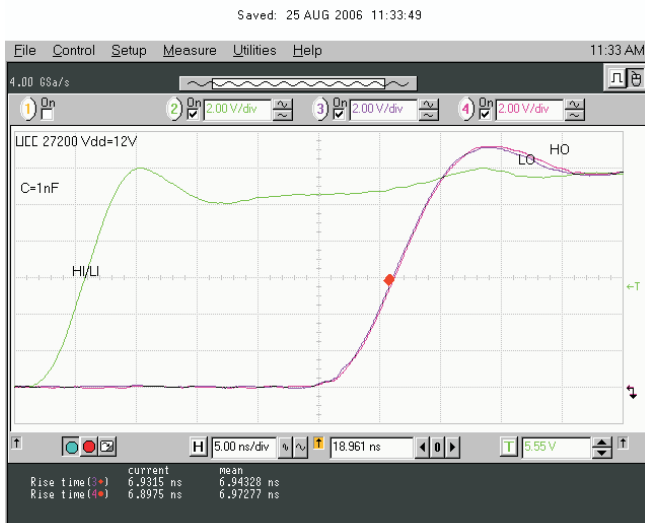


Figure 26.  $V_{LO}$  and  $V_{HO}$  Rise Time, 1-nF Load, 5 ns/Div



Figure 27.  $V_{LO}$  and  $V_{HO}$  Fall Time, 1-nF Load, 5-ns/Div

### Dynamic Switching of the MOSFETs

The true behavior of MOSFETs presents a dynamic capacitive load primarily at the gate to source threshold voltage. Using the turn off case as the example, when the gate to source threshold voltage is reached the drain voltage starts rising, the drain to gate parasitic capacitance charge into the gate resulting in the turn off plateau. The relatively low threshold voltages of many MOSFETs and the increased charge that has to be removed (Miller charge) makes good driver performance necessary for efficient switching. An open loop half bridge power converter was utilized to evaluate performance in actual applications. The schematic of the half-bridge converter is shown in [Figure 30](#). The turn off waveforms of the UCC27200 driving two MOSFETs in parallel is shown in [Figure 28](#) and [Figure 29](#).

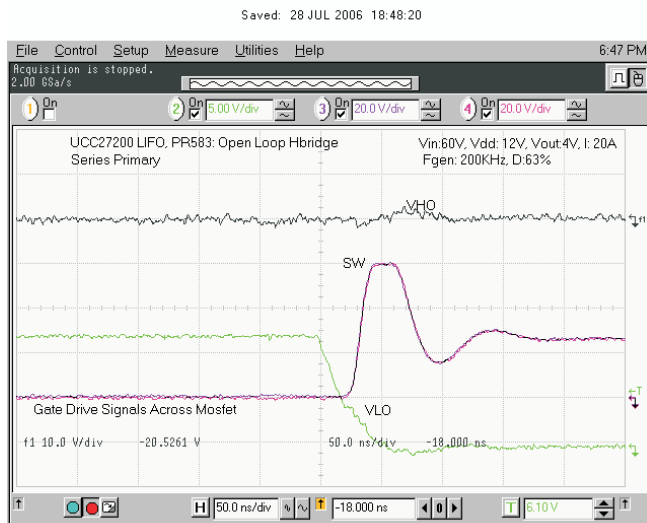


Figure 28. V<sub>LO</sub> Fall Time in Half-Bridge Converter

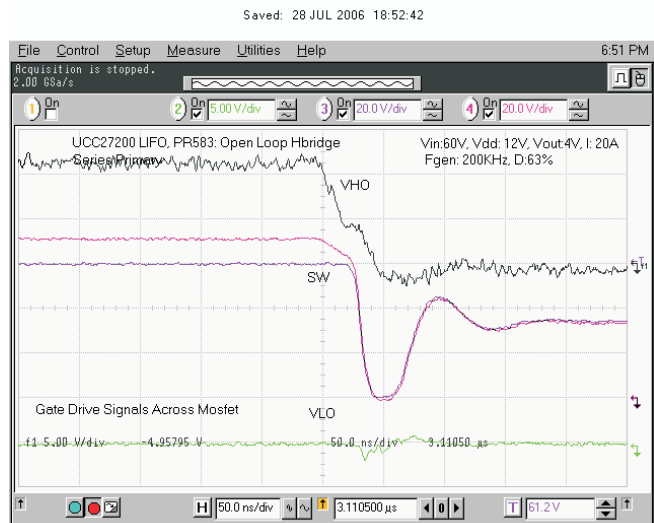


Figure 29. V<sub>HO</sub> Fall Time in Half-Bridge Converter

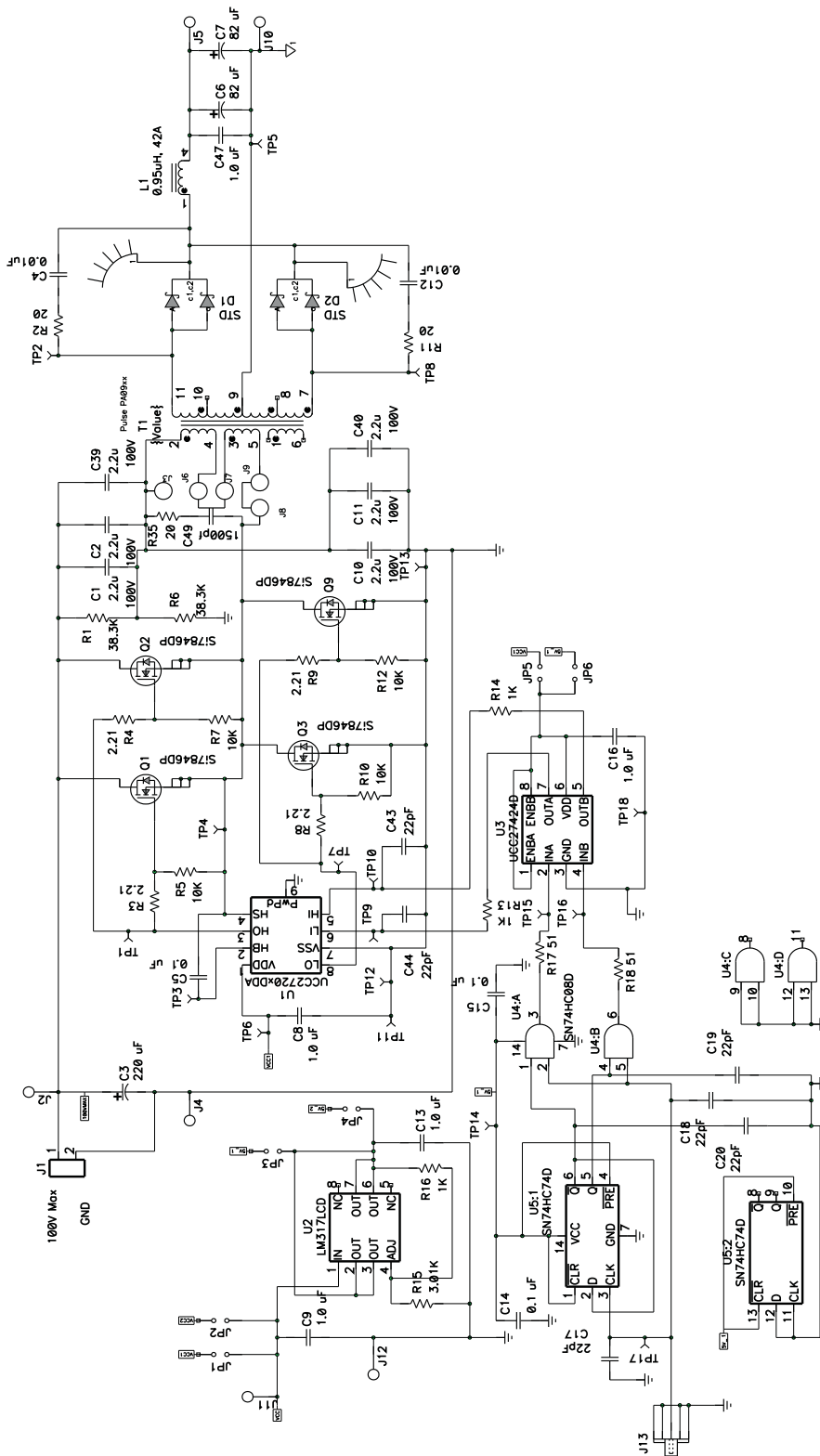


Figure 30. Open Loop Half-Bridge Converter

### Delay Matching and Narrow Pulse Widths

The total delays encountered in the PWM, driver and power stage need to be considered for a number of reasons, primarily delay in current limit response. Also to be considered are differences in delays between the drivers which can lead to various concerns depending on the topology. The sync-buck topology switching requires careful selection of dead-time between the high- and low-side switches to avoid 1) cross conduction and 2) excessive body diode conduction. Bridge topologies can be affected by a resulting volt-sec imbalance on the transformer if there is imbalance in the high and low side pulse widths in a steady state condition.

Narrow pulse width performance is an important consideration when transient and short circuit conditions are encountered. Although there may be relatively long steady state PWM output-driver-MOSFET signals, very narrow pulses may be encountered in 1) soft start, 2) large load transients, and 3) short circuit conditions.

The UCC2720x driver family offers excellent performance regarding high and low-side driver delay matching and narrow pulse width performance. The delay matching waveforms are shown in [Figure 31](#) and [Figure 32](#). The UCC2720x driver narrow pulse performance is shown in [Figure 33](#) and [Figure 34](#).

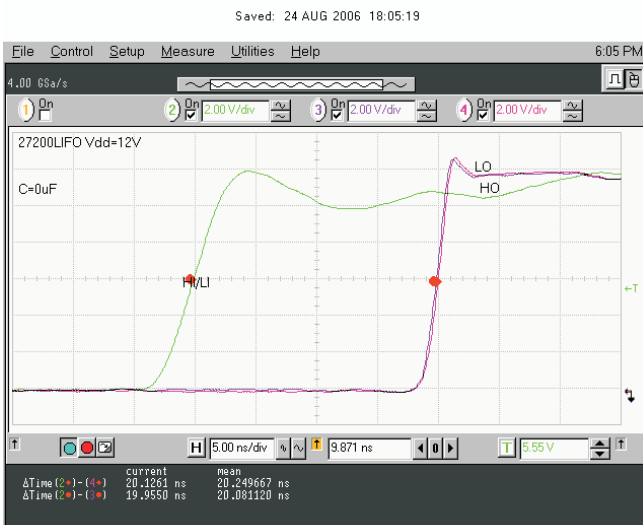


Figure 31.  $V_{LO}$  and  $V_{HO}$  Rising Edge Delay Matching

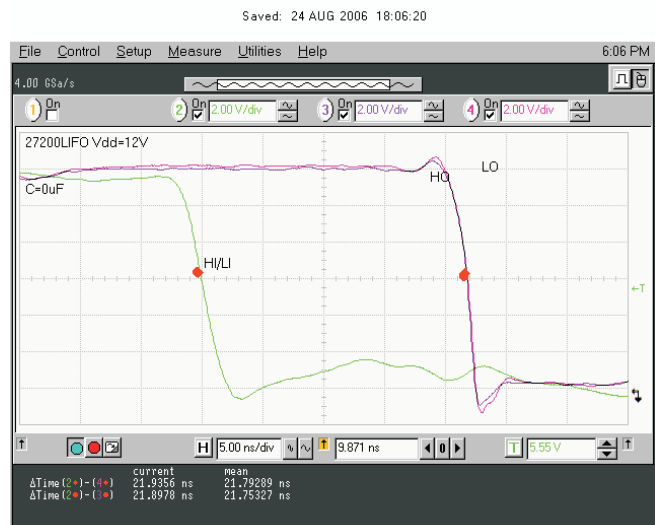


Figure 32.  $V_{LO}$  and  $V_{HO}$  Falling Edge Delay Matching

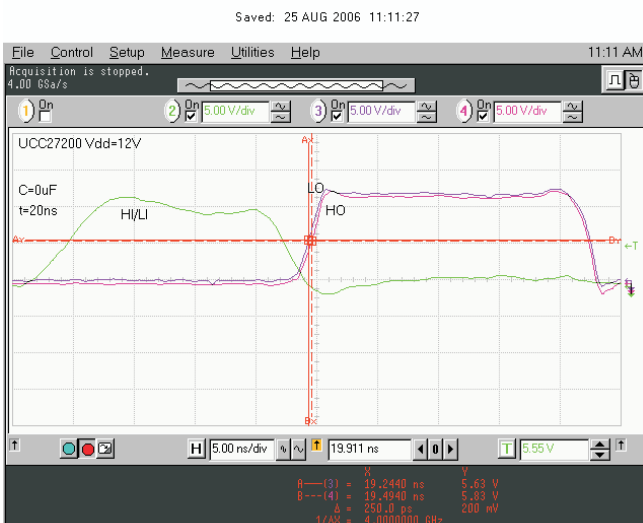


Figure 33. 20-ns Input Pulse Delay Matching



Figure 34. 10-ns Input Pulse Delay Matching

## Boot Diode Performance

The UCC2720x family of drivers incorporates the bootstrap diode necessary to generate the high side bias internally. The characteristics of this diode are important to achieve efficient, reliable operation. The dc characteristics to consider are  $V_F$  and dynamic resistance. A low  $V_F$  and high dynamic resistance results in a high forward voltage during charging of the bootstrap capacitor. The UCC2720x has a boot diode rated at 0.65-V  $V_F$  and dynamic resistance of 0.6  $\Omega$  for reliable charge transfer to the bootstrap capacitor. The dynamic characteristics to consider are diode recovery time and stored charge. Diode recovery times that are specified with no conditions can be misleading. Diode recovery times at no forward current ( $I_F$ ) can be noticeably less than with forward current applied. The UCC2720x boot diode recovery is specified at 20ns at  $I_F = 20$  mA,  $I_{REV} = 0.5$  A. At 0 mA  $I_F$  the reverse recovery time is 15 ns.

Another less obvious consideration is how the stored charge of the diode is affected by applied voltage. On every switching transition when the HS node transitions from low to high, charge is removed from the boot capacitor to charge the capacitance of the reverse biased diode. This is a portion of the driver power losses and reduces the voltage on the HB capacitor. At higher applied voltages, the stored charge of the UCC2720x PN diode is often less than a comparable Schottky diode.

## Layout Recommendations

To improve the switching characteristics and efficiency of a design, the following layout rules should be followed.

- Locate the driver as close as possible to the MOSFETs.
- Locate the  $V_{DD}$  and  $V_{HB}$  (bootstrap) capacitors as close as possible to the driver.
- Pay close attention to the GND trace. Use the thermal pad of the DDA and DRM package as GND by connecting it to the VSS pin (GND). *Note: The GND trace from the driver goes directly to the source of the MOSFET but should not be in the high current path of the MOSFET(S) drain or source current.*
- Use similar rules for the HS node as for GND for the high side driver.
- Use wide traces for LO and HO closely following the associated GND or HS traces. 60 mil to 100 mil width is preferable where possible.
- Use as least two or more vias if the driver outputs or SW node needs to be routed from one layer to another. For GND the number of vias needs to be a consideration of the thermal pad requirements as well as parasitic inductance.
- Avoid  $L_I$  and  $H_I$  (driver input) going close to the HS node or any other high dV/dT traces that can induce significant noise into the relatively high impedance leads.
- Keep in mind that a poor layout can cause a significant drop in efficiency versus a good PCB layout and can even lead to decreased reliability of the whole system.

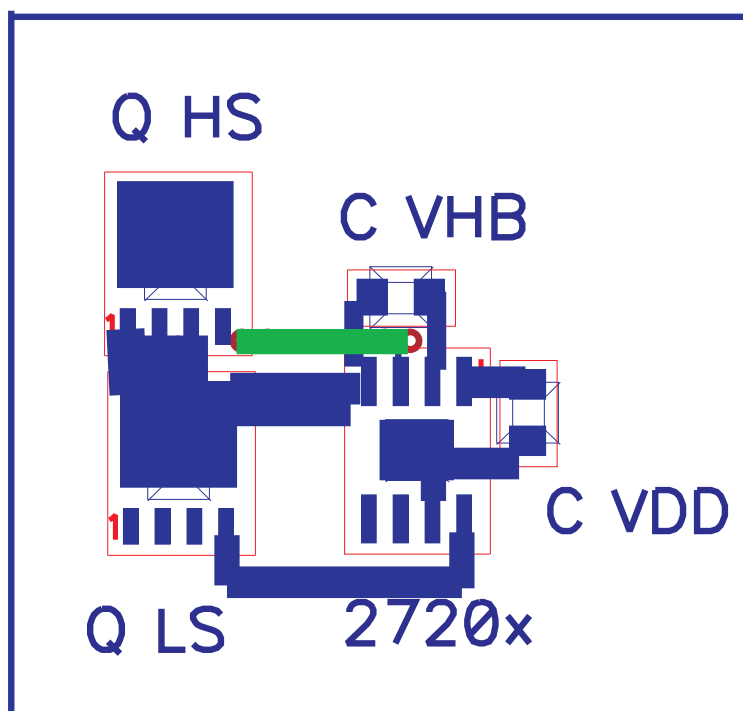


Figure 35. Example Component Placement

### Additional References

These references and links to additional information may be found at [www.ti.com](http://www.ti.com).

1. Additional layout guidelines for PCB land patterns may be found in Application Brief SLUA271
2. Additional thermal performance guidelines may be found in Application Reports SLMA002A and SLMA004

## TAPE AND REEL INFORMATION



### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UCC27200DDAR	SO Power PAD	DDA	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UCC27200DDAR	SO Power PAD	DDA	8	2500	330.0	12.8	6.4	5.2	2.1	8.0	12.0	Q1
UCC27200DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UCC27200DRMR	VSON	DRM	8	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
UCC27200DRMT	VSON	DRM	8	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
UCC27201DDAR	SO Power PAD	DDA	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UCC27201DDAR	SO Power PAD	DDA	8	2500	330.0	12.8	6.4	5.2	2.1	8.0	12.0	Q1
UCC27201DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UCC27201DRMR	VSON	DRM	8	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
UCC27201DRMT	VSON	DRM	8	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

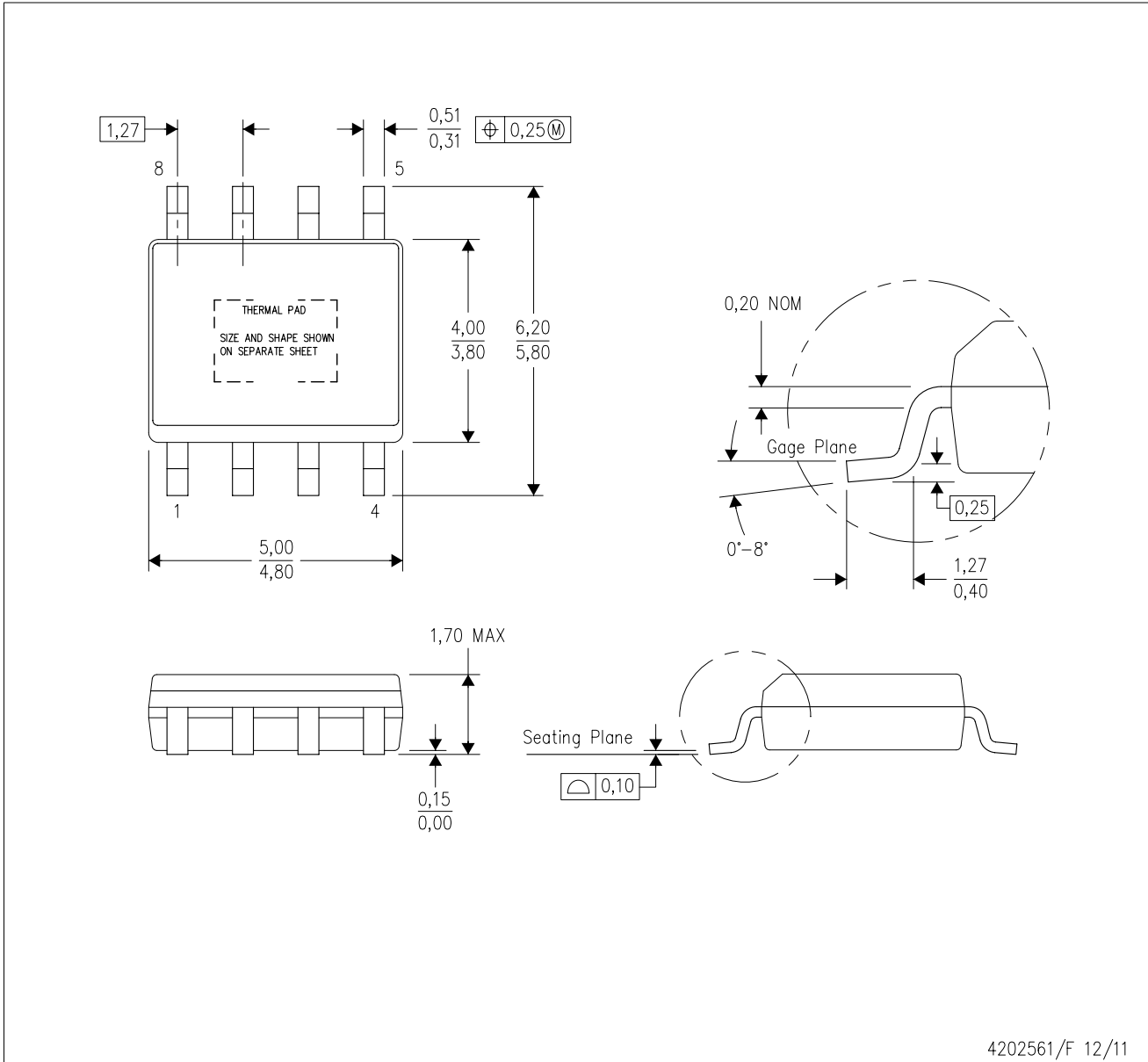
**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UCC27200DDAR	SO PowerPAD	DDA	8	2500	367.0	367.0	35.0
UCC27200DDAR	SO PowerPAD	DDA	8	2500	364.0	364.0	27.0
UCC27200DR	SOIC	D	8	2500	340.5	338.1	20.6
UCC27200DRMR	VSON	DRM	8	3000	367.0	367.0	35.0
UCC27200DRMT	VSON	DRM	8	250	210.0	185.0	35.0
UCC27201DDAR	SO PowerPAD	DDA	8	2500	367.0	367.0	35.0
UCC27201DDAR	SO PowerPAD	DDA	8	2500	364.0	364.0	27.0
UCC27201DR	SOIC	D	8	2500	340.5	338.1	20.6
UCC27201DRMR	VSON	DRM	8	3000	367.0	367.0	35.0
UCC27201DRMT	VSON	DRM	8	250	210.0	185.0	35.0

DDA (R-PDSO-G8)

PowerPAD™ PLASTIC SMALL-OUTLINE



4202561/F 12/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5-1994.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
  - D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>.
  - E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
  - F. This package complies to JEDEC MS-012 variation BA

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DDA (R-PDSO-G8)

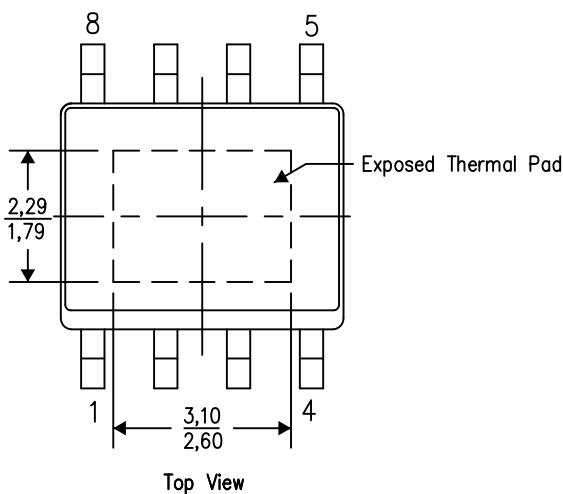
PowerPAD™ PLASTIC SMALL OUTLINE

## THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at [www.ti.com](http://www.ti.com).

The exposed thermal pad dimensions for this package are shown in the following illustration.



Exposed Thermal Pad Dimensions

4206322-8/L 05/12

NOTE: A. All linear dimensions are in millimeters

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DDA (R-PDSO-G8)

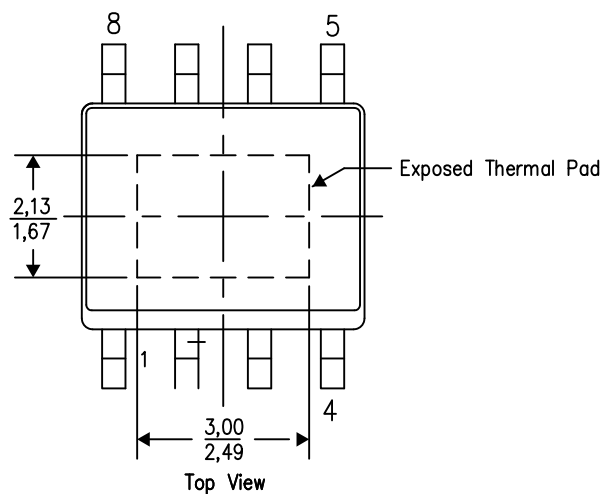
PowerPAD™ PLASTIC SMALL OUTLINE

## THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at [www.ti.com](http://www.ti.com).

The exposed thermal pad dimensions for this package are shown in the following illustration.

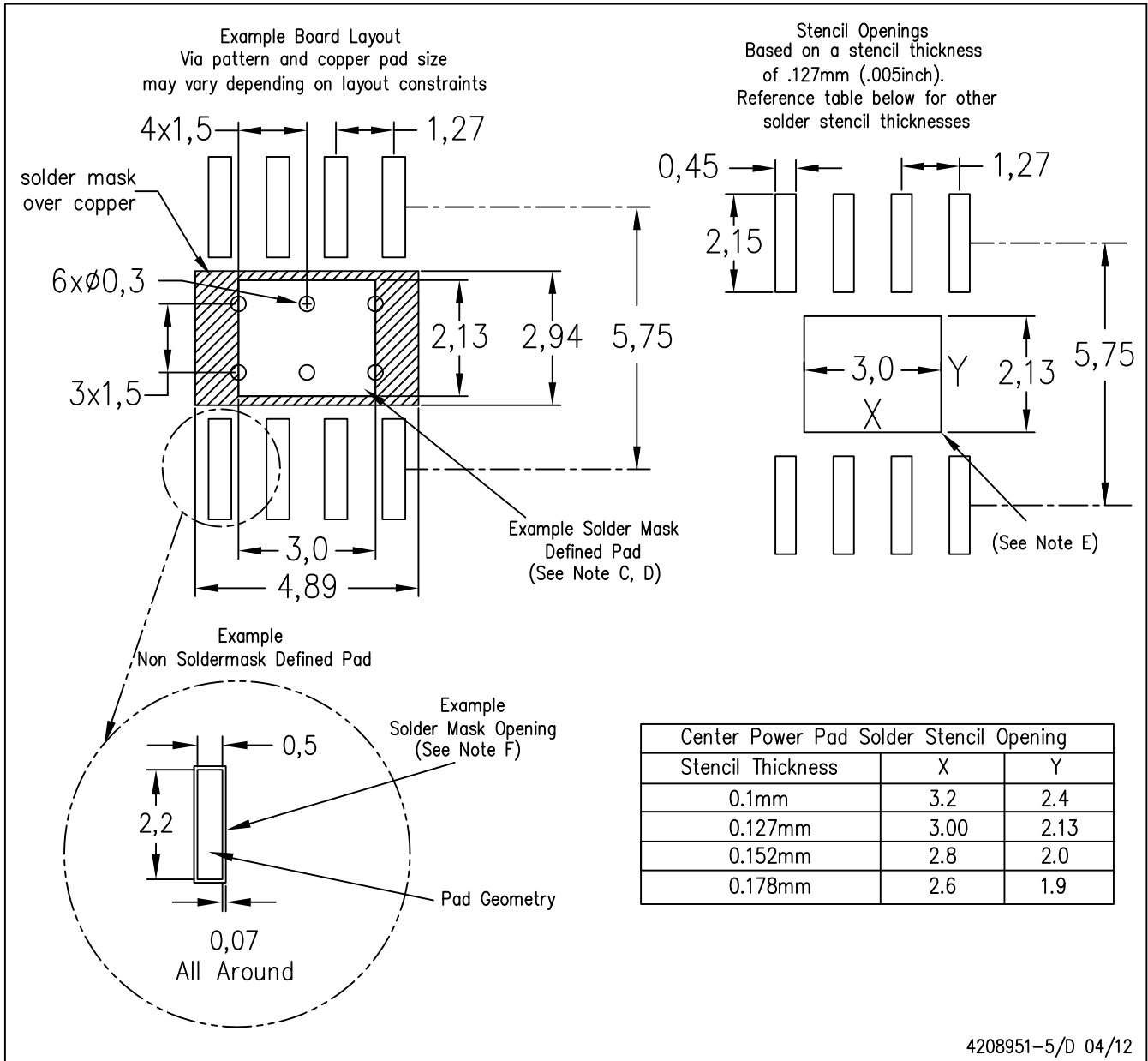


Exposed Thermal Pad Dimensions

4206322-5/L 05/12

NOTE: A. All linear dimensions are in millimeters

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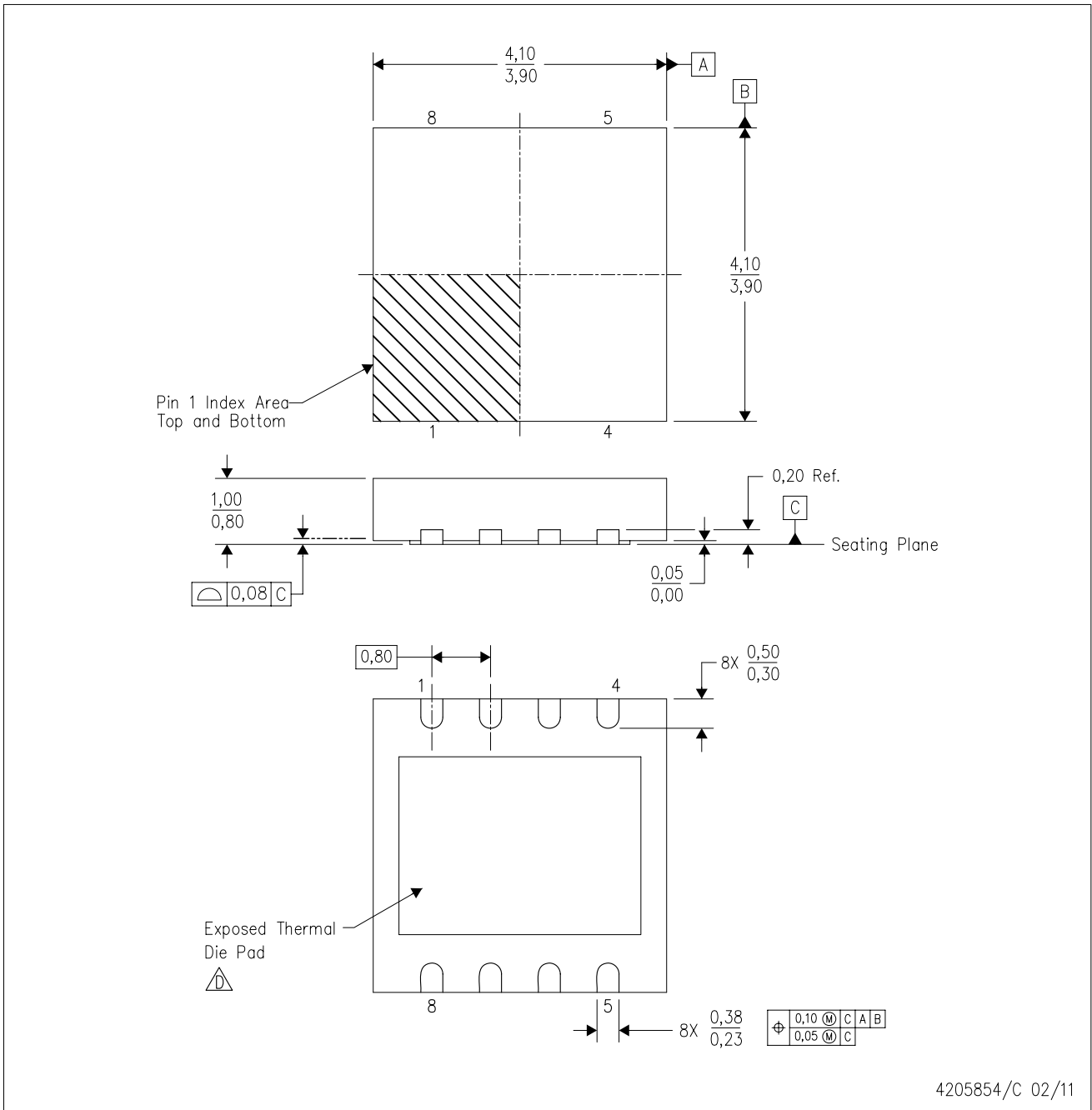


- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
  - D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>. Publication IPC-7351 is recommended for alternate designs.
  - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.
  - F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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DRM (S-PVSON-N8)

PLASTIC SMALL OUTLINE NO-LEAD



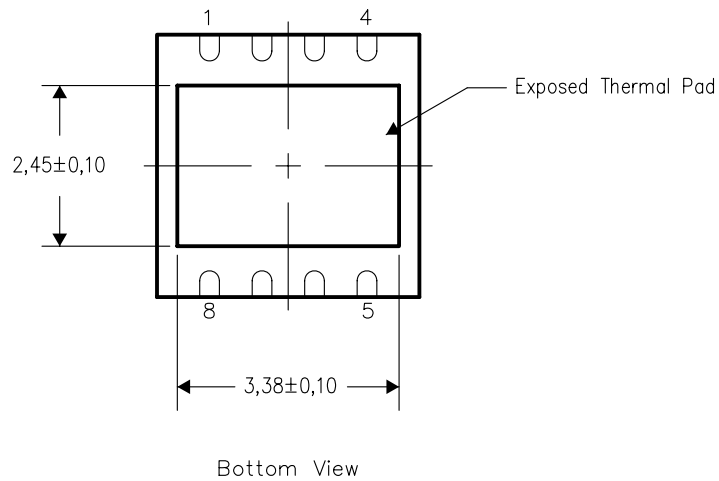
- NOTES:
- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - This drawing is subject to change without notice.
  - SON (Small Outline No-Lead) package configuration.
- The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.

### THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, Quad Flatpack No-Lead Logic Packages, Texas Instruments Literature No. SCBA017. This document is available at [www.ti.com](http://www.ti.com).

The exposed thermal pad dimensions for this package are shown in the following illustration.



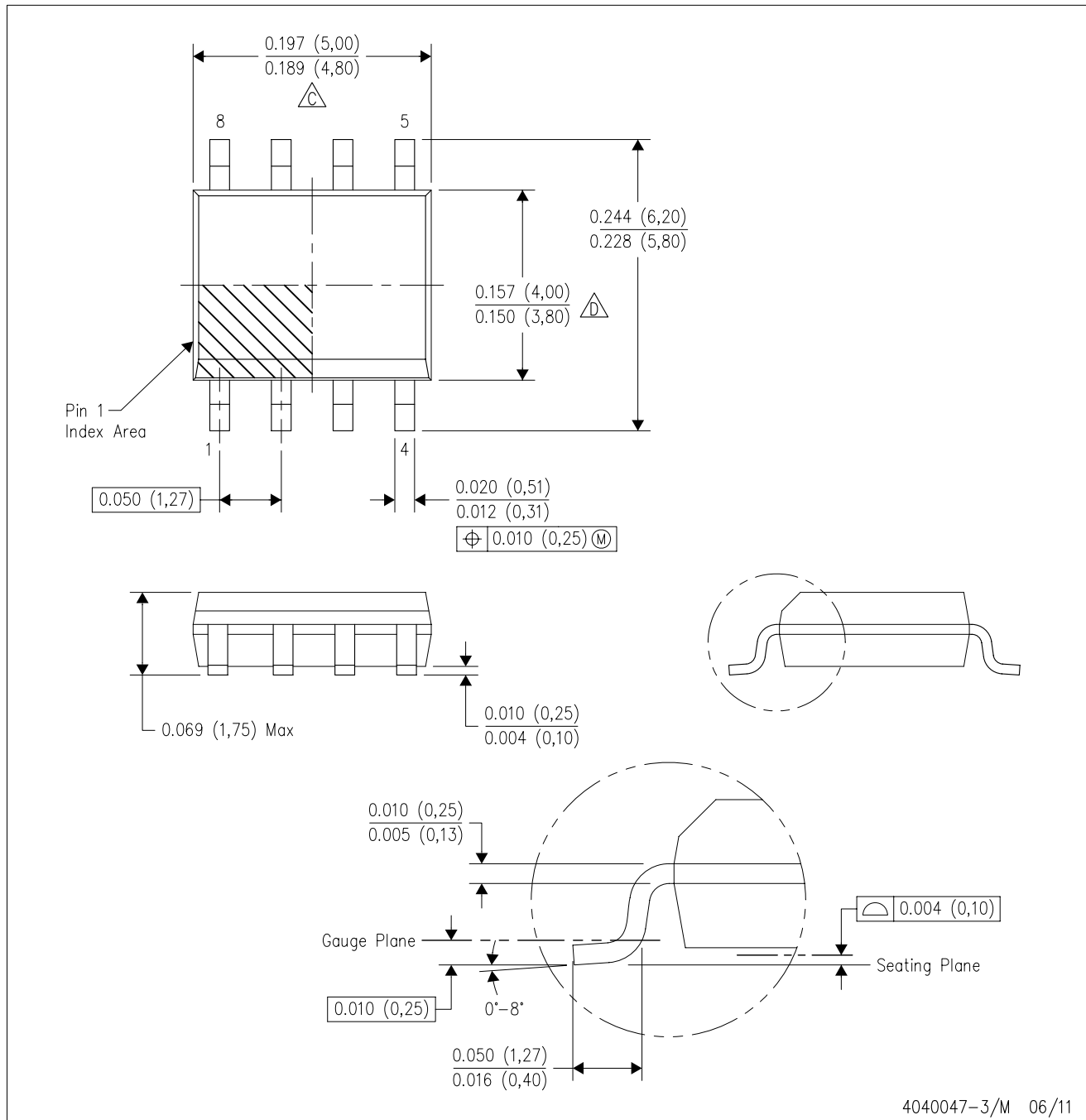
NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions



D (R-PDSO-G8)

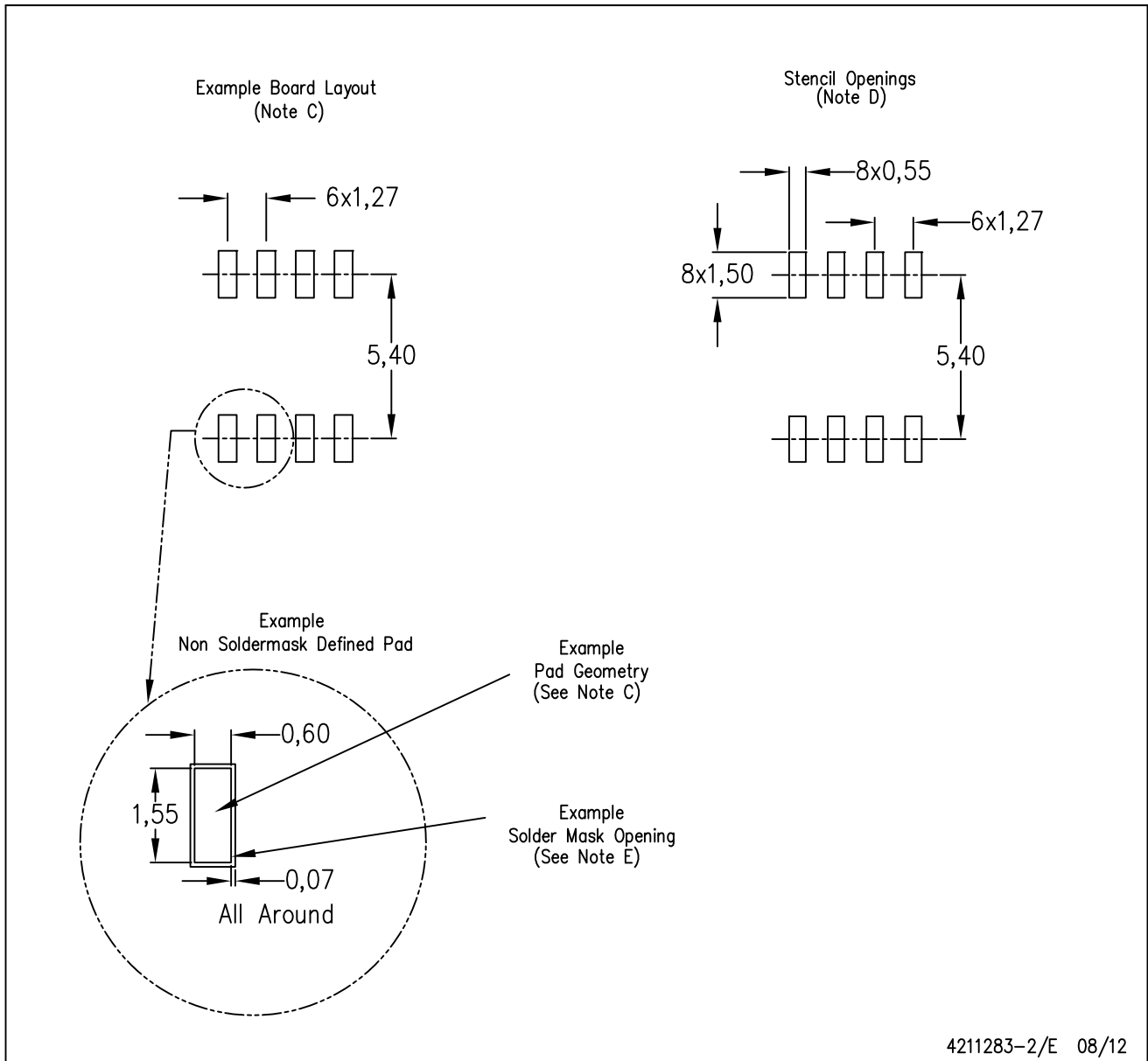
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AA.

D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



4211283-2/E 08/12

- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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