Envoy™-8FE Device

Octal Fast Ethernet Controller

TXC-06840

DATA SHEET

FEATURES

- 8 Independent SMII ports operating at 10/100 Mbit/s mixed mode
- 8 Media Access Controllers (MACs) each connected to an SMII port
- POS-PHY Level 2 interface operating at 50 MHz
- OIF SPI-3 interface operating at 100 MHz
- Full-Duplex and Half-Duplex (CSMA/CD) operation per MAC
- Support for VLAN tagged frames
- Automatic PAUSE Frame Generation and Termination
- Ingress and Egress FIFOs on a per MAC basis guarantee loss-less transmission
- Programmable High and Low FIFO watermarks for space and frame availability signal generation
- Programmable frame length
- Programmable Inter-Packet Gap (IPG) between Ethernet Frames
- Frame integrity verification (FCS and length checks)
- Statistics and performance monitoring support for RMON
- Far end switch side loopback for diagnostics
- 32-bit Motorola host interface, operating at 33/50 MHz
- IEEE 1149.1 JTAG support
- 1.8V core and 3.3V I/O power supplies, 5V tolerant I/O leads
- Industrial Temperature Range (-40 °C to +85 °C)
- 376-lead plastic ball grid array (PBGA) package, 23 mm x 23 mm

DESCRIPTION

The Envoy™-8FE is an Octal Fast Ethernet to POS-PHY Level 2/SPI-3 controller. Each SMII port is connected to a Media Access Controller (MAC), operating at 10/100 Mbits/s mixed mode. The MAC is programmable to provide Full-Duplex or Half-Duplex operation. The Envoy-8FE bridges the gap between POS-PHY Level 2 and OIF SPI-3 standard technology used in telecom to cost effective standards based Ethernet technologies. Additionally, the Envoy-8FE is a cost-effective single chip solution for backplane switching and physical layer applications, such as Ethernet uplinks, Ethernet over VDSL and Ethernet over SONET (EoS), utilizing state of the art congestion control management and flow control mechanisms to provide carrier class reliability.

The Envoy-8FE is designed to interface directly with POS-PHY Level 2/SPI-3 compliant devices, including standard off the shelf network processors. On the Ethernet side, the Envoy-8FE interfaces directly with standard Fast Ethernet PHY devices via the Serial Media Independent Interface (SMII) at 125 MHz. The Envoy-8FE has on-chip buffering and provides backpressure support in both the ingress and egress directions.

APPLICATIONS

- 3G Wireless Radio Network Controllers (RNCs)
- 3G Wireless Base Stations
- Multi-service Switches
- IP DSLAMs
- Edge Routers
- Interconnect for Fast Ethernet Backplanes

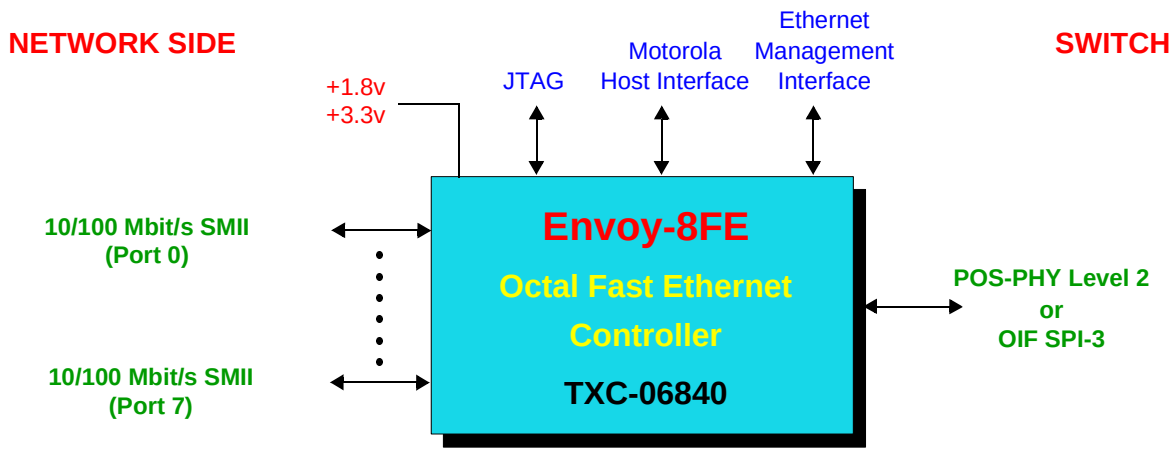

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TABLE OF CONTENTS

Section **Page**

Please note that TranSwitch provides documentation for all of its products. Current editions of many documents are available from the Products page of the TranSwitch Web site at www.transwitch.com. Customers who are using a TranSwitch Product, or planning to do so, should register with the TranSwitch Marketing Department to receive relevant updated and supplemental documentation as it is issued. They should also contact the Applications Engineering Department to ensure that they are provided with the latest available information about the product, especially before undertaking development of new designs incorporating the product.

LIST OF FIGURES

Figure **Page**

FEATURES

10/100 MBIT/S MEDIA ACCESS CONTROLLER (MAC) BLOCK

The main features supported by the MAC block are:

- Compliant to IEEE 802.3, 802.3i, 802.3u, 802.3x
- Mixed 10/100 Mbit/s mode
- Full Duplex and Half Duplex (CSMA/CD) operation per MAC
- Connection to standard 10/100 Mbit/s Fast Ethernet PHY devices via SMII interface
- Frame Integrity Verification (FCS and length checks)
- Errored Frames can be configured to be filtered
- Programmable Inter-Packet Gap (IPG) between Ethernet frames
- Programmable frame length
    - Minimum frame size = 64 bytes
    - Maximum frame size = 1550 bytes
- Support for VLAN tagged frames
- Programmable High and Low FIFO watermarks for space and frame availability generation
- MAC control sublayer provides support for control frames including PAUSE frames
- Automatic PAUSE Frame Generation and Termination
- 7.7 x 1550 byte ingress FIFO per MAC
- 2.4 x 1550 byte egress FIFO per MAC
- Far end switch side loopback for diagnostic capability
- Statistics and performance monitoring support for Remote Network Monitoring (RMON)

SERIAL MEDIA INDEPENDENT INTERFACE (SMII)

Envoy-8FE provides 8 independent SMII interfaces with an IEEE 802.3 compliant MAC connected to each interface/port. Data received at the SMII interface is first qualified by a MAC and then passed onto a 7.7 x 1550 Byte FIFO. The MAC is configured to operate in either Full-Duplex or Half-Duplex Mode. Once the MAC has processed the frame, it updates statistics which are stored in the Envoy-8FE status registers. These registers are used to provide performance monitoring. PAUSE frames received are used to backpressure the POS-PHY Level 2/OIF SPI-3 interface for that specific port. When the Ingress FIFO reaches a watermark, PAUSE frames are generated and transmitted over the SMII interface to the MII PHY (if enabled). Once the Egress FIFO has a complete frame to send, the SMII transmit interface attempts to transmit the frame over its SMII interface. In Half-Duplex mode, CSMA/CD is used to determine selection. In Full-Duplex mode, CSMA/CD is not used per IEEE 802.3.

The Envoy-8FE provides the following Ethernet Port features:

- 8 independent SMII ports operating at 10/100 Mbit/s mixed mode
- Each SMII port is comprised of:
    - Two serial data signals (TX and RX) per port
    - Global 125 MHz reference clock signal for all eight ports
    - Global synchronization signal for all eight ports
    - All signals are synchronous to the clock

A single Ethernet Management interface is provided on the Envoy-8FE to connect to an external Ethernet PHY in order to configure and control its operation. This interface is comprised of an output Management Data clock signal and a bi-directional Management Data signal that allows serial data to be clocked in and out of the external PHY device. All data transfers are synchronous to the clock signal and provide support for up to 31 PHYs (PHY Address = 0 is reserved).

POS-PHY LEVEL 2/SPI-3 INTERFACE

The Envoy-8FE POS-PHY Level 2/SPI-3 interface is a slave (PHY) interface operating at rates up to 50/100 MHz. The flow control is frame-based for POS-PHY Level 2, and both byte and frame based for SPI-3. In the POS-PHY Level 2/SPI-3 Receive direction (Envoy-8FE Ingress i.e., SMII to POS-PHY Level 2/SPI-3), when a port has a complete frame to send or a pre-configured number of bytes, the port indicates availability of data for transfer. A port is then selected for transferring data based on selection by the Link Layer POS-PHY Level 2/SPI-3 device. In the Transmit direction (Envoy-8FE Egress i.e., POS-PHY Level 2/SPI-3 to SMII), FIFO space availability is indicated to the Link Layer POS-PHY Level 2/SPI-3 device when a specific watermark is reached.

MICROPROCESSOR INTERFACE

A Motorola Microprocessor compliant interface (32-bit wide data bus) is used to configure the part and retrieve status from Envoy-8FE. It is compatible with the PowerQUICC family of microprocessors from Motorola including the MPC860, operating at 33/50 MHz.

JTAG INTERFACE

This interface provides a five signal Boundary Scan capability that conforms to the IEEE 1149.1 standard. This standard provides external boundary scan functions to read and write the external I/O pins from the Test Access Port (TAP) for board and component test. In addition to the TAP, a lead is provided to place the output buffers in a high impedance state for systems that do not support the IEEE 1149.1 standard.

BLOCK DIAGRAM

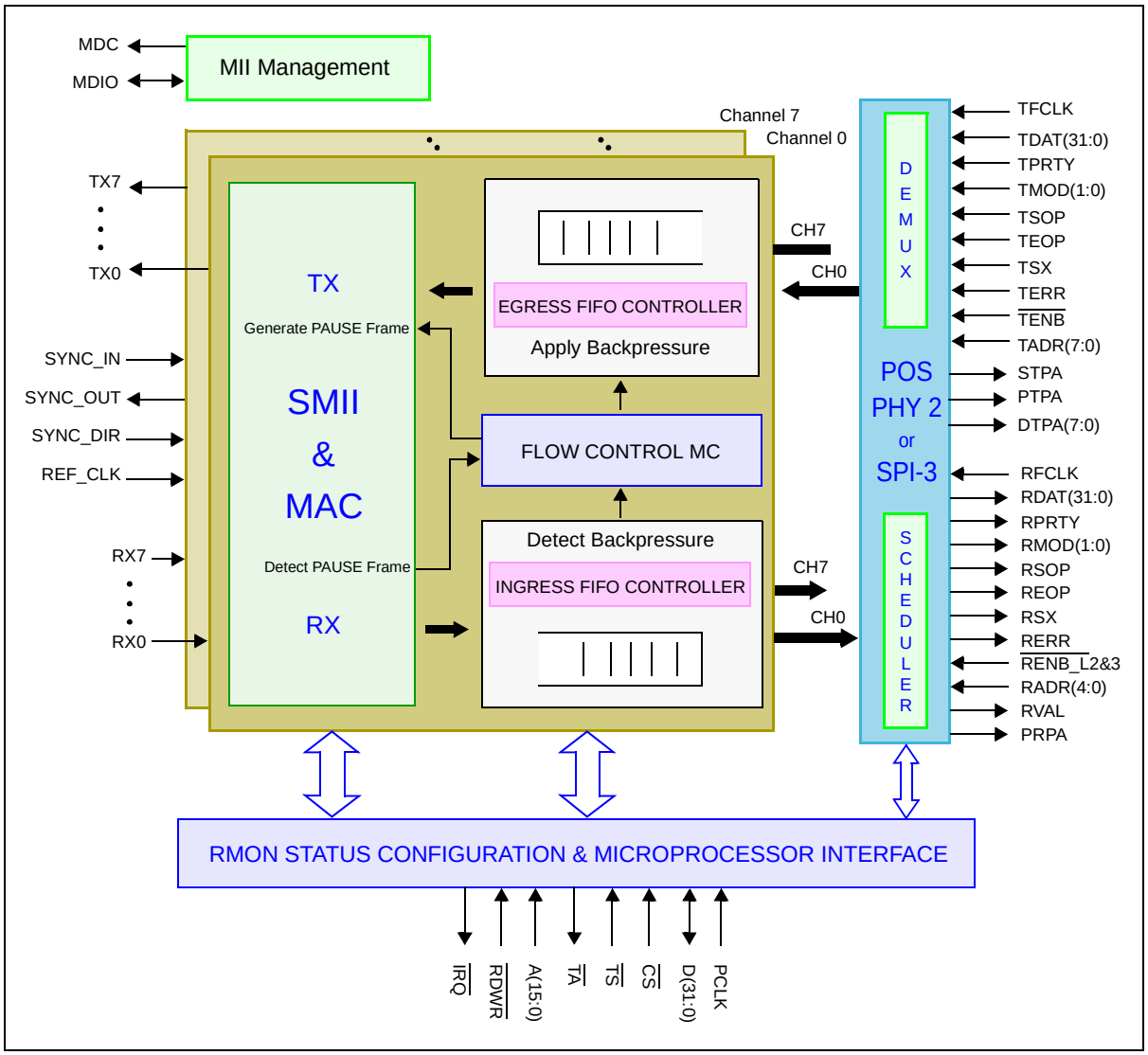


Figure 1. Functional Block Diagram of the Envoy-8FE

BLOCK DIAGRAM DESCRIPTION

Envoy-8FE INTERFACES

Media Independent Interface (MII) Management Port

The Envoy-8FE provides a MII management port, for configuration of Ethernet PHY's connected to Envoy-8FE. Envoy-8FE can retrieve status from the PHY's using the MII port. Multiple (up to 31) PHY devices are programmable via this interface. The Envoy-8FE MII management interface is compliant to the Management interface outlined in IEEE 802.3u. The device can be configured for preamble suppression at the MII interface. The frequency of the output clock of the MII management port (MDC) is programmable to PCLK/n (n = 8, 10, 14, 20 or 28).

Two additional functions performed by the interface are the Scan function and the Automatic PHY address Increment function. In Scan only mode, multiple back to back reads can be done from a particular PHY. When Scan mode and Auto PHY address increment is enabled, back to back reads can be performed with the PHY address being incremented after each read. Therefore, the PHYs are scanned. Note: When using Scan mode and Auto PHY address increment is enabled, the range of addresses scanned will be between "PHY Address" (register 0x100A, bits (12:8)) and PHY number 31. To use the auto increment scan read on the MII interface, the host must use a timer to set up the interval between consecutive reads. Following is the procedure:

a) Setup in Scan-mode, Auto-phy-inc_mode and Phy_regAddress

b) Issue Read Command

c) Wait for 70 MDC clocks periods (MII clock) if preamble suppression is disabled and 39 MDC clocks if preamble suppression is enabled

d) Sample first data

e) Wait for 67 MDC clock periods if pre-amble suppression is disabled and 35 MDC clock periods is preamble suppression is enabled

f) Sample next data

g) Repeat from step e) for consecutive reads

Note: Envoy's MII interface is in Master mode. The MII management port configuration registers are located in the SMII port 0 memory map location and not in the memory map locations for SMII port 1 to 7.

MII Configurations Bits

MII Clock Select: Address 1008 Bits 2 to 0; Divide by 8, 10, 14, 20 & 28.

Enable MII Preamble Suppression: Address 1008 Bit 4; '1' = Enable, '0' = Disable.

Enable PHY Address Increment: Address 1008 Bit 5; '1' = Enable, '0' = Disable.

Enable MII Read: Address 1009 Bit 0; '1' = Enable, '0' = Disable.

Enable MII Scan: Address 1009 Bit 1; '1' = Enable, '0' = Disable.

PHY Register Address: Address 100A Bits 4 to 0; 5 Bit PHY register address.

PHY Address: Address 100A Bits 12 to 8; 5 Bit address of the PHY for Read or Writes.

Enable MII Write Control: Address 100A Bits 15 to 0; Writing to this register initiates a write of the data in this register to the PHY whose address is in PHY Address.

Note: Please refer to "Memory Maps and Bit Descriptions" starting on page 47 for complete list of configuration bits.

Packet Over SONET (POS-PHY) Level 2 / System Packet Interface (SPI) Level 3

Envoy-8FE is a PHY (slave) device as specified in the POS-PHY Level 2/SPI-3 compatibility specification. For a complete operational specification of the POS-PHY Level 2/SPI-3 interface, please refer to the POS-PHY Level 2 and OIF SPI-3 compatibility specification.

Envoy-8FE is configurable for either POS-PHY Level 2 or OIF SPI-3 mode of operation.

POS-PHY Level 2

When configured in POS-PHY Level 2 Mode, Envoy-8FE is compliant with the POS-PHY Level 2 protocol. The data bus width is 16 bits (TDAT(15-0) and RDAT(15-0)) and the clock (TFCLK and RFCLK) rates supported from 25 MHz to 50 MHz. The Port address for channel 0 is programmable and the Port address for channel 1 will be a unit increment of the port address of channel 0. The port address of consecutive ports, starting from port 0, increment in unit increments. The Port address range is from 0 to 30 and the programmable address range (Port 0 address) is 0 to 23. Envoy-8FE provides packet-level transfer control. In the POS-PHY Level 2 Transmit interface, space availability is indicated by PTPA/DTPA signals. PTPA/DTPA is de-asserted when the number of bytes available for storage in the Egress FIFO is equal to or less than “Egress FIFO Near Full Threshold” and PTPA/DTPA is asserted when the number of bytes available for storage in the Egress FIFO is greater than “Egress FIFO Near Full Threshold”. Egress FIFO Near Full Threshold is programmable to the following values: 0 to 63 (Threshold = 0-63) and 64 (Threshold = 256). In the Receive direction (Envoy-8FE POS-PHY outlet) a channel will be selected for frame transfer, by the Link layer device, based on frame availability for each channel and the Link layer devices space availability. Frame availability (PRPA/DTPA) for a channel is indicated when either a complete frame has been stored (indicated by reception of end of frame) or when a programmable threshold of 256, 512, 768 or 1550 bytes has been stored in the channel’s Ingress FIFO.

OIF SPI-3

Envoy-8FE OIF SPI-3 operates using a 32 bit wide data bus (TDAT(31-0) and RDAT(31-0)). The minimum clock (TFCLK and RFCLK) rate in this mode is 50 MHz and the maximum clock rate is 100 MHz. The Port address for channel 0 is programmable and the Port address for channel 1 will be a unit increment of the port address of channel 0. The port address of consecutive ports, starting from port 0, increment in unit increments. The Port address range is from 0 to 255 and the programmable address range (Port 0 address) is 0 to 247. In the Transmit direction, the transfer flow-control is configurable to either byte level or frame level flow control. In the SPI3 Transmit interface, space availability is indicated by STPA/PTPA/DTPA signals. STPA/PTPA/DTPA is de-asserted when the number of bytes available for storage in the Egress FIFO is equal to or less than “Egress FIFO Near Full Threshold” and STPA/PTPA/DTPA is asserted when the number of bytes available for storage in the Egress FIFO is greater than “Egress FIFO Near Full Threshold”. Egress FIFO Near Full Threshold is programmable to the following values: 0 to 63 (Threshold = 0-63) and 64 (Threshold = 256). In the Receive direction (Envoy-8FE SPI-3 outlet) one of the channels will be selected for frame transfer, based on a round robin algorithm. Envoy-8FE will round robin to the next channel once the selected channel transfers an end of Frame or when the selected channel transfers a programmable number of bytes. This programmable number of bytes is referred to as SPI-3 Receive Forced Reselection Transfer size and is enabled by SPI-3 Receive Forced Reselection Enable. This is done to avoid latency issues due to a particular port monopolizing the interface bandwidth. In the Receive direction, frame availability for a channel is recorded internally when either a complete frame has been stored (indicated by reception of and end of frame) or when a selectable threshold of 256, 512, 768 or 1550 bytes have been stored in the channel’s Ingress FIFO. In the receive direction (Envoy-8FE SPI-3 outlet) the time between consecutive transfers (pause) is programmable between 0 or 2 cycles.

POS-PHY Level 2/SPI-3 Interface Configuration Bits (Note: n = 0 . . . 7 for ports 0 . . . 7)

Interface Selection: Addr 2008 Bit 0; '1' = OIF SPI-3, '0' = POS-PHY Level 2

SPI-3 Flow Control Mode: Addr 2008 Bit 4; '1' = Byte Level Flow Control, '0' = frame Level Flow control

Level 2 Parity Mode: Addr 2008 Bits 7-5; "00" = Odd parity over Data only. "01" = Odd parity over data and control. "10" = Even parity over data only. "11" = Even parity over data and control.

SPI-3 Parity Mode: Addr 2008 Bit 8; '1' = Even Parity. '0' = Odd parity.

SPI-3 Transmit Interface Address offset: Addr 2008 Bits 17-10

SPI-3 Receive Interface Address offset: Addr 2008 Bits 25-18

SPI-3 Transmit Interface PHY Enable: Addr (2000 + n) Bit 0; '1' = enable, 0 = disable.

SPI-3 Receive Interface PHY Enable: Addr (2000 + n) Bit 1; '1' = enable, 0 = disable.

SPI-3 Receive Forced Reselection Enable: Addr 2008 Bit 26; '1' = enable, 0 = disable.

SPI-3 Receive Forced Reselection Transfer size: Addr 2008 Bits 28 to 27; "00" = 256 bytes, "01" = 512 bytes, "10" = 768 bytes, "11" = 1550 bytes.

Level 2 Transmit Interface Address offset: Addr 2009 Bits 10-6

Level 2 Receive Interface Address offset: Addr 2009 Bits 15-11

Level 2 Transmit Interface PHY Enable: Addr 2009 Bits 17-10; '1' = enable, 0 = disable

Level 2 Receive Interface PHY Enable: Addr 2009 Bits 25-18; '1' = enable, 0 = disable

Level 2 Transmit Interface Online: Addr 2009 Bit 2; '1' = Online, '0' = Offline

Level 2 Receive Interface Online: Addr 2009 Bit 3; '1' = Online, '0' = Offline

Note: *n* = 0 . . . 7 for channels 0 . . . 7

Per Channel Transmit Near Full Indicator Threshold: Addr (2001 + n) Bits 10 to 4; These 7 bits define the number of bytes before the Egress FIFO becomes full, that the Frame Available signal to the Link device needs to be de-asserted. This Threshold value needs to be programmed the same value as the Egress FIFO Near Full Threshold (Egress FIFO Section - Addr (4001 + n) Bits 9 to 3) for proper operation. The valid values are 0 to 63 (Threshold = 0-63) and 64 (Threshold = 256).

Note: Please refer to the "Memory Maps and Bit Descriptions" starting on page 47 for complete list of configurations.

Microprocessor Interface

Envoy-8FE configuration, status and device management is performed via its microprocessor interface. The device's microprocessor interface has a 32 bit wide data bus D(31-0) and a 16 bit wide address bus A(15-0). The interface is compatible with standard Motorola micro-controllers like the MPC860. The Envoy-8FE will interface to the MPC860 seamlessly. The interface operates at a minimum clock (PCLK) frequency of 33 MHz and a maximum clock frequency of 50 MHz. The control pins are an input read/write pin RDWR, Transfer start TS, Transfer acknowledge TA, chip select CS and an interrupt pin IRQ. Single read, single write transfers can be performed and are paced with the TA signal.

Status counters can be cleared globally using a global clear or cleared on read or cleared on write based on the mode programmed. All status counters are rollover counters. The microprocessor interface is used for Remote Monitoring of the SMII MAC. Any micro controller read taking more than 15 processor clock cycles, will time out and interrupt the host indicating the internal timeout condition.

Envoy-8FE has a word (4 bytes) addressable Address bus. Below is the address and data bus mapping between the Envoy-8FE and the Motorola MPC860 (which is byte addressable).

Envoy-8FE - Motorola MPC860 Address Bus Mapping

Envoy-8FE Address Pins	MPC860 Address Pins
A0 (MSB)	A14 (MSB)
. . . .	. . . .
A15 (LSB)	A29 (LSB)

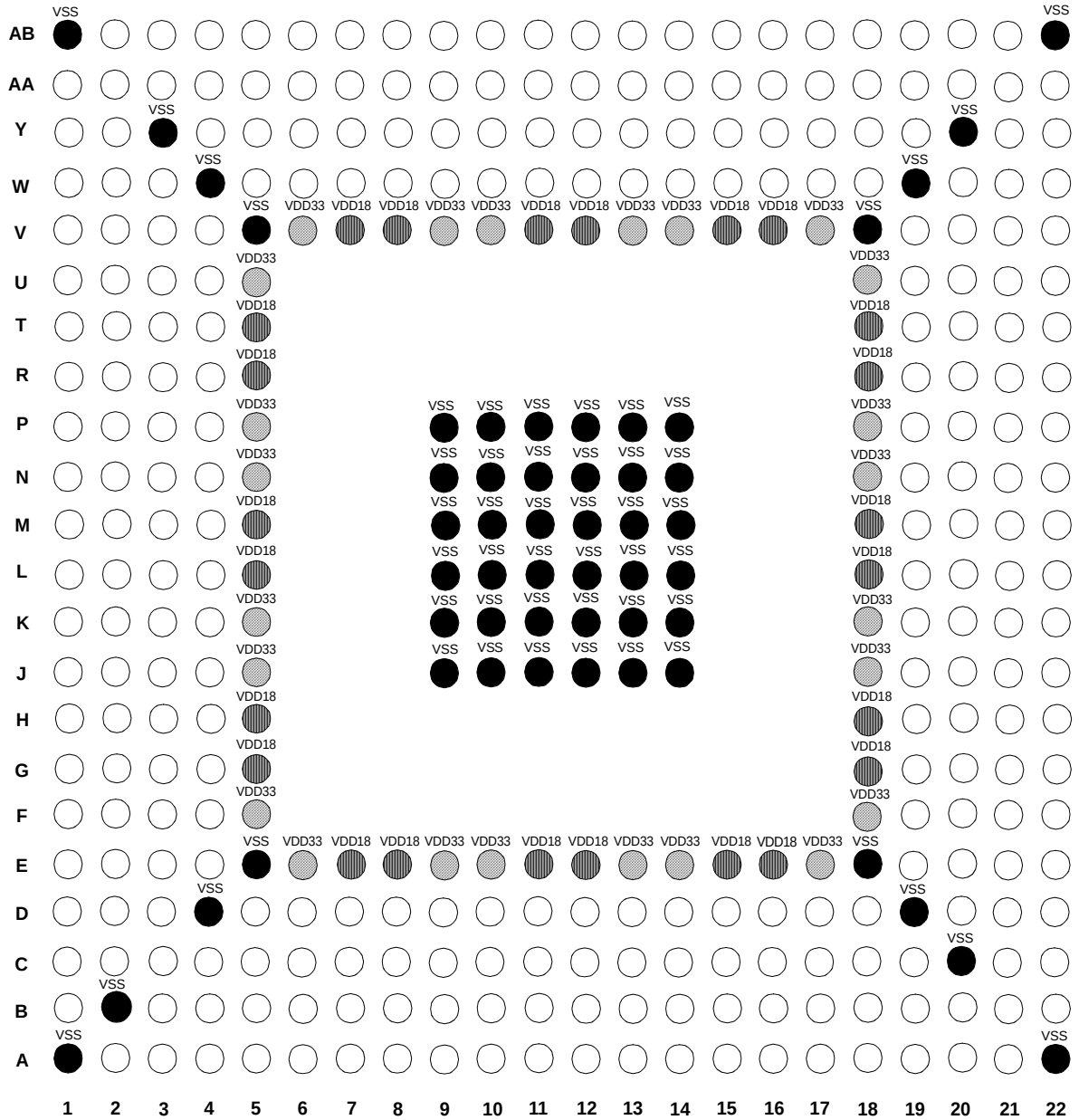
Envoy-8FE - Motorola MPC860 Data Bus Mapping

Envoy-8FE Data Pins	MPC860 Data Pins
D0 (MSB)	D0 (MSB)
. . . .	. . . .
D31 (LSB)	D31 (LSB)

JTAG Interface

The JTAG interface includes a five pin Test Access Port (TAP) interface, as the boundary scan ports that will conform to the IEEE 1149.1 standard. This standard provides external boundary scan functions to read and write the external I/O pins from the TAP, for board and component test. In addition to the TAP, a pin is provided ($\overline{\text{DEVHIZ}}$) to place the output buffers in a high impedance state for systems that do not support the IEEE 1149.1 standard. The standard IEEE 1149.1 interface comprises of 5 pins, Data In (TDI), Data Out (TDO), Clock (TCK), mode select (TMS) and reset (TRST).

LEAD DIAGRAM



Note: This is the bottom view. The leads are solder balls. See Figure 14 for package information.

Figure 2. Envoy-8FE TXC-06840 376-Lead Plastic Ball Grid Array Package Lead Diagram

LEAD DESCRIPTIONS

POWER SUPPLY, GROUND AND NO CONNECTS

Symbol	Lead No.	I/O/P *	Name/Function
VDD18	E7, E8, E11, E12, E15, E16, G5, G18, H5, H18, L5, L18, M5, M18, R5, R18, T5, T18, V7, V8, V11, V12, V15, V16	P	**V_{DD18}:** +1.8 volt ±5% CMOS core supply voltage.
VDD33	E6, E9, E10, E13, E14, E17, F5, F18, J5, J18, K5, K18, N5, N18, P5, P18, U5, U18, V6, V9, V10, V13, V14, V17	P	**V_{DD33}:** +3.3 volt ±5% CMOS input/output pad supply voltage.

Note: VDD18 and VDD33 Power Up Sequence Because of the multi-power ESD structure used for CMOS I/O cells, there is a parasitic forward diode path from core power rail (V_{DD18}) to I/O power rail (V_{DD33}). So, if V_{DD18} is powered up earlier than V_{DD33}, there will be current flowing through the parasitic diode that may trigger latch-up. To avoid this problem, users can take either one of the approaches below:

(1) Power Up VDD33 First Turning on V_{DD33} first prevents the parasitic diode turning on. For example, power up V_{DD33} first and then V_{DD18}. Note that TXC does not recommend to power up V_{DD33} much earlier than V_{DD18} for reliability reasons. That is because the un-powered V_{DD18} may result in short circuit current (crowbar current) on the CMOS IO cell's post-driver for unknown state. Bus conflict may also occur when only V_{DD33} is powered on. The maximum interval that V_{DD18} must be powered up after V_{DD33} depends on the slew rate of power ramp-up in customer's application.

(2) Place a Schottky Diode Between VDD18 and VDD33 If we can ensure that the parasitic diode does not turn on, we can even power up lower voltage first. This can be done by inserting an external diode between V_{DD18} and V_{DD33} on the board. By connecting the Schottky diode with anode to lower voltage rail (V_{DD18}) and cathode to higher voltage rail (V_{DD33}), we can force the latter to ramp up with the former with the voltage drop (Schottky diode Vt=150mV~200mV) less than the threshold voltage of the parasitic diode (parasitic diode Vt=500mV~600mV). This prevents from turning on the parasitic diode between power rails, hence avoiding latch up. The external diode will be turned off when V_{DD33} is powered up to its normal voltage.

VSS	A1, A22, AB1, AB22, B2, C20, D4, D19, E5, E18, J9 - J14, K9 - K14, L9 - L14, M9 -M14, N9 - N14, P9 - P14, V5, V18, W4, W19, Y3, Y20	P	**VSS:** Ground 0 volt reference.

*Note: I = Input; O = Output; P = Power; T = Tristate

Symbol	Lead No.	I/O/P *	Name/Function
NC	A2, A11, A12, A21, AA4, AA12, AA19, AA20, AA21, AA22, AB3, AB11, AB12, AB20, AB21, B3, B11, B12, B20, C4, C19, C22, D5, D18, E22, F21, F22, G20, G21, G22, H19, H20, H21, J19, L1, M1, M21, M22, U19, V19, V20, W6, W17, W18, W20, W21, W22, Y18, Y19, Y21		**No Connect:** NC leads are not to be connected, not even to another NC lead, but must be left floating. Connection of NC leads may impair performance or cause damage to the device. Some NC leads may be assigned functions in future upgrades of the device. Backwards compatibility of the upgraded device in existing applications may rely upon these leads having been left floating.
Reserved _Low	AA18, AB19, B19, B21, B22, C18, C21, D20, D21, D22, E19, E20, E21, F19, F20, G19, P19, R19, R20, R21, T19, T20, T21, T22, U20, U21, U22, V21, V22, W16, Y17, Y22		**Reserved_Low:** These input signals **must** be connected to V_{SS} for proper device operation.

RESET AND TEST LEADS (INCLUDING TEST ACCESS PORT FOR BOUNDARY SCAN)

Symbol	Lead No.	I/O	Type	Name/Function
TDO	AA15	O(T)	CMOS 8 mA	**Test Data Output:** Boundary scan output for data and test instructions from internal test registers.
$\overline{\text{TRST}}$	AB16	I	LVTTLpu	**Test Mode Reset:** A 1 microsecond (minimum) low on this lead resets the boundary scan; recommended for use after power-up initialization as well. 4.7k Ω pull-up recommended.
TMS	W14	I	LVTTLpu	**Test Mode Select:** Boundary scan test mode select. This signal must be pulled high. 4.7k Ω pull-up recommended.
TDI	Y15	I	LVTTLpu	**Test Data Input:** Boundary scan input for data and test instructions. 4.7k Ω pull-up recommended.
TCK	AA16	I	LVTTLpu	**Test Clock:** Boundary scan clock. Input signals are clocked in on its rising edge.
$\overline{\text{RESET}}$	AB17	I	LVTLL	**Hardware Reset:** An active low pulse with minimum width of 1 ms which must be applied after power is applied to reset all registers, counters, and FIFOs. The reset is asynchronous going into the reset state, but requires all external clocks to be active and stable during the reset state.
$\overline{\text{TESTMODE}}$	Y16	I	LVTTL	**Test Mode:** Active low to enable device test. Tie to V_{DD33}.
SCAN	W15	I	LVTTL	**SCAN Test:** Active high to enable device internal scan test. Tie to V_{SS}.
IDDTEST	AA17	I	LVTTL	**IDD Test:** Active high to enable device internal IDD test. Tie to V_{SS}.
$\overline{\text{DEVHIZ}}$	AB18	I	LVTTL	**Device High Impedance:** Active low to set all outputs (except TDO) to high impedance state. Tie to V_{DD33}.

MOTOROLA HOST INTERFACE

Symbol	Lead No.	I/O/P*	Type	Name/Function
PCLK	D17	I	LVTTL	**Processor Clock:** Clock output from MPC860. Maximum frequency of 50 MHz, minimum frequency of 33 MHz.
$\overline{\text{CS}}$	A20	I	LVTTL	**Chip Select:** Chip select lead from MPC860. Active low assertion.

Symbol	Lead No.	I/O/P*	Type	Name/Function
$\overline{TS}$	B18	I	LVTTL	**Transfer Start:** Asserted by MPC860 to indicate the start of a bus cycle that transfers data to/from a slave device. Connected to MPC860 $\overline{TS}$ signal. The transfer start signal (signal $\overline{TS}$) indicates the beginning of a transaction on the bus addressing a slave device. $\overline{TS}$ is asserted only for the first cycle of the transaction and is negated in the successive clock cycles until the end of the transaction. An external pull-up resistor should be connected to $\overline{TS}$.
$\overline{TA}$	C17	O	CMOS 8 mA	**Transfer Acknowledge:** Active low signal indicating normal completion of the bus transfer. This output requires an external pull-up resistor. Note: device asserts this high before tri-stating to improve acknowledge timing.
A(15-0)	A18, B17, C16, D15, A17, B16, C15, D14, A16, B15, A15, C14, D13, B14, A14, C13	I	LVTTL	**Address Bus:** 16-bit address bus from MPC860. A0 is MSB.
D(31-0)	B13, D12, A13, C12, C11, A10, D11, B10, A9, C10, B9, D10, C9, A8, B8, A7, D9, C8, B7, A6, D8, C7, B6, A5, A4, D7, C6, B5, A3, D6, C5, B4	I/O	LVTTL/ CMOS 8 mA	**Data Bus:** Bidirectional 32-bit data bus from MPC860. D0 is MSB.
$\overline{RDWR}$	D16	I	LVTTL	**Read/Write:** Indicates direction of the data transfer. 'I' = read, '0' = write.
$\overline{IRQ}$	A19	O (T)	CMOS 8mA	**Interrupt:** Active low level-based interrupt to MPC860.

ETHERNET 8 x SMII INTERFACES

Symbol	Lead No.	I/O/P*	Type	Name/Function
REF_CLK	N19	I	LVTTL	**SMII Reference Clock:** Maximum of 125 MHz.
SYNC_OUT	P21	O	CMOS 12mA	**Synchronization Output Pulse:** Global output signal that occurs every 10 REF_CLK clock cycles and will mark the start of data segments.
SYNC_IN	N20	I	LVTTL	**Synchronization Input Pulse:** Global input signal that occurs every 10 REF_CLK clock cycles and will mark the start of data segments.
SYNC_DIR	P22	I	LVTTL	**Synchronization Pulse Direction:** Determines the source of the synchronization pulse. When ='1', the sync pulse to the 8 SMII ports will be taken from SYNC_IN, when ='0', the sync pulse will be taken internally before the pad of the pin SYNC_OUT.
TX0	N21	O	CMOS 12mA	**Transmit Data Port 0:** SMII port 0 data out signal
RX0	M19	I	LVTTL	**Receive Data Port 0:** SMII port 0 data in signal
TX1	N22	O	CMOS 12mA	**Transmit Data Port 1:** SMII port 1 data out signal
RX1	M20	I	LVTTL	**Receive Data Port 1:** SMII port 1 data in signal
TX2	L22	O	CMOS 12mA	**Transmit Data Port 2:** SMII port 2 data out signal
RX2	L21	I	LVTTL	**Receive Data Port 2:** SMII port 2 data in signal
TX3	L20	O	CMOS 12mA	**Transmit Data Port 3:** SMII port 3 data out signal
RX3	K22	I	LVTTL	**Receive Data Port 3:** SMII port 3 data in signal
TX4	L19	O	CMOS 12mA	**Transmit Data Port 4:** SMII port 4 data out signal
RX4	K21	I	LVTTL	**Receive Data Port 4:** SMII port 4 data in signal
TX5	K20	O	CMOS 12mA	**Transmit Data Port 5:** SMII port 5 data out signal
RX5	J22	I	LVTTL	**Receive Data Port 5:** SMII port 5 data in signal
TX6	J21	O	CMOS 12mA	**Transmit Data Port 6:** SMII port 6 data out signal
RX6	K19	I	LVTTL	**Receive Data Port 6:** SMII port 6 data in signal
TX7	J20	O	CMOS 12mA	**Transmit Data Port 7:** SMII port 7 data out signal
RX7	H22	I	LVTTL	**Receive Data Port 7:** SMII port 7 data in signal
MDC	R22	O	CMOS 8mA	**Management Data Interface Clock:** Management data (MDIO signal) is clocked into and out of the device on the rising edge of this clock.

Symbol	Lead No.	I/O/P*	Type	Name/Function
MDIO	P20	I/O	LVTTL/ CMOS 8mA	**Management Data I/O:** I/O data pin for the IEEE 802.3u compliant management and status interface.

POS-PHY Level 2/SPI-3 INTERFACE - TRANSMIT

Symbol	Lead No.	I/O/P*	Type	Name/Function
TFCLK	W2	I	LVTTL	**Transmit Clock:** Maximum of 50 MHz for POS-PHY Level 2 emulating and 100 MHz for SPI-3 emulation.
TDAT(31-0)	AB4, AB5, AA6, Y7, W8, AB6, AA7, Y8, W9, AB7, AA8, AB8, Y9, W10, AA9, AB9, Y10, AA10, W11, AB10, Y11, AA11, Y12, AB13, W12, AA13, Y13, AB14, AA14, W13, Y14, AB15	I	LVTTL	**Transmit Data Bus:** 32-bit bus used to receive data from the Link Layer device. Note: For POS-PHY Level 2, only the lower 16-bits of the data bus is used.
TPRTY	T2	I	LVTTL	**Transmit Bus Parity:** This input signal indicates the parity calculated over the TDAT(31-0) bus.
TMOD(1-0)	U1, R4	I	LVTTL	**Transmit Word Modulo:** These 2 inputs indicate the number of valid bytes of date in TDAT(31-0). The TMOD bus should always be all zero, except during the last double-word transfer of a frame on TDAT(31-0). Note: For POS-PHY Level 2, only bit TMOD(0) is used.
TSOP	U4	I	LVTTL	**Transmit Start of Frame:** This active high input is used to delineate the frame boundaries on the TDAT bus. When TSOP is high, the start of the frame is present on TDAT.

Symbol	Lead No.	I/O/P*	Type	Name/Function
TEOP	V3	I	LVTTL	**Transmit End of Frame:** This input signal is used to delineate the frame boundaries on the TDAT bus. When high, the end of the frame is present on TDAT(31-0).
TSX	AA1	I	LVTTL	**Transmit Start of Transfer:** This active high input signal indicates when the in-bound port address is present on TDAT(31-0).
TERR	V4	I	LVTTL	**Transmit Error Indicator:** This active high input signal is used to indicate that the current frame should be discarded.
$\overline{\text{TENB}}$	W3	I	LVTTL	**Transmit Write Enable:** This active low input signal is used to control the flow of data to the transmit FIFO's.
TADR(7-0)	T3, U2, V1, W1, T4, U3, V2, Y1	I	LVTTL	**Transmit Address:** 8-bit bus containing the PHY address. Note: For POS-PHY Level 2, only bits(4-0) are used.
STPA	AA2	O	CMOS 8mA	**Selected-PHY Transmit Packet Available:** Active high output used to indicate that data is available in the transmit FIFO specified on the inbound address on TDAT. This signal is used only for byte-level transfer mode.
PTPA_L2	Y2	O	CMOS 8mA	**POS-PHY Level 2 Polled-PHY Transmit Packet Available:** Active high output used to indicate that data is available in the polled transmit FIFO. This signal is used only for packet-level transfer mode in POS-PHY level 2 mode.
PTPA_L3	L1	O	CMOS 8mA	**SPI3 Polled-PHY Transmit Packet Available:** Active high output used to indicate that data is available in the polled transmit FIFO. This signal is used only for packet-level transfer mode in SPI3 mode.
DTPA(7-0)	AA3, Y4, W5, AB2, Y5, AA5, Y6, W7	O	CMOS 8mA	**Direct Transmit Packet Available:** Active high output used to indicate that data is available in the transmit FIFO. The DTPA bus is used only for byte-level transfer mode when using the SPI-3 interface.

POS-PHY LEVEL 2/SPI-3 INTERFACE - RECEIVE

Symbol	Lead No.	I/O/P*	Type	Name/Function
RFCLK	L2	I	LVTTL	**Receive Clock:** Maximum of 50 MHz for Level 2 emulating and 100 MHz for Level 3 emulation.
RDAT(31-0)	L3, K1, L4, K2, J1, K3, J2, K4, J3, H1, H2, G1, J4, H3, G2, F1, H4, G3, F2, E1, D1, G4, F3, E2, F4, C1, D2, C2, E3, E4, B1, D3	O	CMOS 8mA	**Receive Data Bus:** 32-bit bus used to transmit data to the Link Layer device. Note: For POS-PHY Level 2, only the lower 16-bits of the data bus is used.
RPRTY	M2	O	CMOS 8mA	**Receive Bus Parity:** This output signal indicates the parity calculated over RDAT(31-0) bus.
RMOD(1-0)	M3, N1	O	CMOS 8mA	**Receive Word Module:** These 2 inputs indicate the number of valid bytes of date in RDAT(31-0). The RMOD bus should always be all zero, except during the last double-word transfer of a frame on RDAT(31-0). Note: For POS-PHY Level 2, only bit RMOD(0) is used.
RSOP	N4	O	CMOS 8mA	**Receive Start of Frame:** This active high input is used to delineate the frame boundaries on the RDAT(31-0) bus. When RSOP is high, the start of the frame is present on RDAT(31-0).
REOP	P3	O	CMOS 8mA	**Receive End of Frame:** This output signal is used to delineate the frame boundaries on the RDAT(31-0) bus. When high, the end of the frame is present on RDAT(31-0).
RSX	R1	O	CMOS 8mA	**Receive Start of Transfer:** This active high output signal indicates when the in-bound port address is present on RDAT(31-0). Used for Level 3 emulation only.
RERR	R2	O	CMOS 8mA	**Receive Error Indicator:** This active high output signal is used to indicate that the current frame is aborted and should be discarded.
$\overline{\text{RENB\_L2}}$	T1	I	LVTTL	**Receive Read Enable for POS-PHY Level 2:** This active low input signal is used to control the flow of data to the receive FIFO's. This signal is used only for POS-PHY Level 2 mode. If unused, connect to V_{DD33}.

Symbol	Lead No.	I/O/P*	Type	Name/Function
$\overline{\text{RENB\_L3}}$	C3	I	LVTTL	**Receive Read Enable for SPI-3:** This active low input signal is used to control the flow of data to the receive FIFO's. This signal is used only for SPI-3 mode. If unused, connect to V_{DD33}.
RADR(4-0)	M4, N2, N3, P1, P2	I	LVTTL	**Receive Address:** Used in Level 2 emulation only. 5-bit bus used to poll the status of the receive buffers in frame level flow control and also used to select a particular port of the PHY.
RVAL	P4	O	CMOS 8mA	**Receive Data Valid:** Active high input signal that validates the RDAT(31-0), RPRTY, RMOD(1:0), RSOP, REOP and RERR signals. RVAL will transition low when the receive FIFO is empty or at the end of a frame.
PRPA	R3	O	CMOS 8mA	**Receive Polled Multi-PHY Frame Available:** Active high output indicates when data is available in the polled receive FIFO. Used only in frame-level transfer mode for Level 2 emulation.

ABSOLUTE MAXIMUM RATINGS AND ENVIRONMENTAL LIMITATIONS

Parameter	Symbol	Min	Max	Unit	Conditions
Core Supply Voltage, +1.8V nominal	$V_{DD1.8}$	-0.3	2.1	V	Notes 1, 4
I/O Supply Voltage, +3.3V nominal	$V_{DD3.3}$	-0.3	3.9	V	Notes 1, 4
DC input voltage	V_{IN}	-0.5	5.5	V	Note 5
Storage temperature range	T_S	-55	150	°C	Note 1
Ambient operating temperature	T_A	-40	85	°C	0 ft/min. linear airflow
Moisture Exposure Level	ME	5		Level	per EIA/JEDEC JESD22-A112-A
Relative humidity, during assembly	RH	30	60	%	Note 2
Relative humidity, in-circuit	RH	0	100	%	non-condensing
ESD Classification	ESD	absolute value 2000		V	Note 3
Latch-Up	LU				Meets JEDEC STD-78

Notes:

1. Conditions exceeding the Min or Max values may cause permanent failure. Exposure to conditions near the Min or Max values for extended periods may impair device reliability.
2. Pre-assembly storage in non-drypack conditions is not recommended. Please refer to the instructions on the “CAUTION” label on the drypack bag in which devices are supplied.
3. Test method for ESD per MIL-STD-883E, Method 3015.7.
4. Device core is 1.8V only.
5. Envoy-8FE is 5V compatible in the sense that the output logic 1 (VOH) and output logic 0 (VOL) levels of the Envoy-8FE outputs have been specified at the same voltage levels that have been commonly recognized as logic 1 and logic 0 for the 5V environment. Envoy-8FE can generally be expected to drive 5V TTL compatible components. However, while Envoy-8FE outputs are able to meet the minimum input logic switching levels (VIH and VIL) of 5V TTL compatible components, the output logic 1 output voltage of some 5V components may exceed the maximum input voltage of Envoy-8FE. Depending on the technology and circuit implementation, the 5V TTL compatible components may drive their outputs anywhere from 3V to their VDD supply level.

CAUTION: Before connecting a 5V component to the Envoy-8FE, always check to be sure that the Maximum VOH of the 5V device does not exceed the specified Maximum VIN listed in the table above.

THERMAL CHARACTERISTICS

Parameter	Min	Typ	Max	Unit	Test Conditions
Thermal Resistance: junction to ambient		22		^{o}C/W	0 ft/min linear airflow.

POWER REQUIREMENTS

Parameter	Min	Typ	Max	Unit	Test Conditions
$V_{DD3.3}$	3.15	3.30	3.45	V	
$I_{DD3.3}$	34.0	35.5	38.0	mA	See Note 1
$P_{DD3.3}$	110	117	131	mW	See Note 1
$V_{DD1.8}$	1.71	1.80	1.89	V	
$I_{DD1.8}$	180	190	210	mA	See Note 1
$P_{DD1.8}$	306	364	403	mW	See Note 1
Total power	0.42	0.48	0.53	W	See Notes 1 and 2

Notes:

1. All I_{DD} and P_{DD} values are dependent upon V_{DD} and the bus operation.
2. Maximum power is at minimum operating temperature.

INPUT, OUTPUT AND INPUT/OUTPUT PARAMETERS

Input Parameters For LVTTL

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}	2.0			V	$3.14 \leq V_{DD33} \leq 3.46$
V_{IL}			0.8	V	$3.14 \leq V_{DD33} \leq 3.46$
Input leakage current	-10		10	µA	$V_{IN} = V_{DD33}$ or V_{SS}
Input capacitance		5		pF	

Input Parameters For LVTTLpu (internal pull-up resistor)

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}	2.0			V	$3.14 \leq V_{DD33} \leq 3.46$
V_{IL}			0.8	V	$3.14 \leq V_{DD33} \leq 3.46$
Input current	-90		-25	µA	$V_{IN} = V_{SS}$
Input leakage current	-10		10	µA	$V_{IN} = V_{DD33}$
Input capacitance		5		pF	

Output Parameters For CMOS 8mA

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{OH}	2.4			V	I_{OH} = -8 mA
V_{OL}			0.4	V	I_{OL} = 8 mA
I_{OL}			8.0	mA	
I_{OH}			-8.0	mA	
Leakage Tristate	-10		10	µA	

Output Parameters For CMOS 12mA

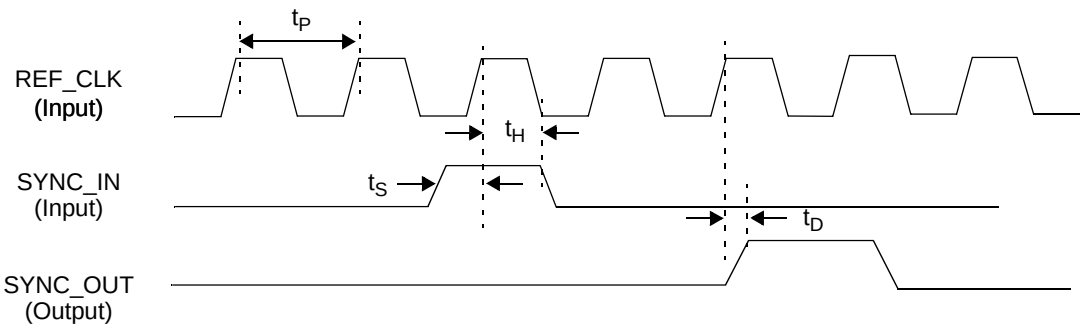
Parameter	Min	Typ	Max	Unit	Test Conditions
V_{OH}	2.4			V	I_{OH} = -12 mA
V_{OL}		0.2	0.4	V	I_{OL} = 12 mA
I_{OL}			12.0	mA	
I_{OH}			-12.0	mA	
Leakage Tristate	-10		10	µA	

Input/Output Parameters For LVTTL/CMOS 8mA

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}	2.0			V	$3.14 \leq V_{DD33} \leq 3.46$
V_{IL}			0.8	V	$3.14 \leq V_{DD33} \leq 3.46$
Input leakage current	-10		10	µA	V_{DD33} = 3.46
Input capacitance		5		pF	
V_{OH}	2.4			V	V_{DD33}= 3.14; I_{OH} = -8 mA
V_{OL}			0.4	V	V_{DD33}= 3.14; I_{OL} = 8 mA
I_{OL}			8.0	mA	
I_{OH}			-8.0	mA	

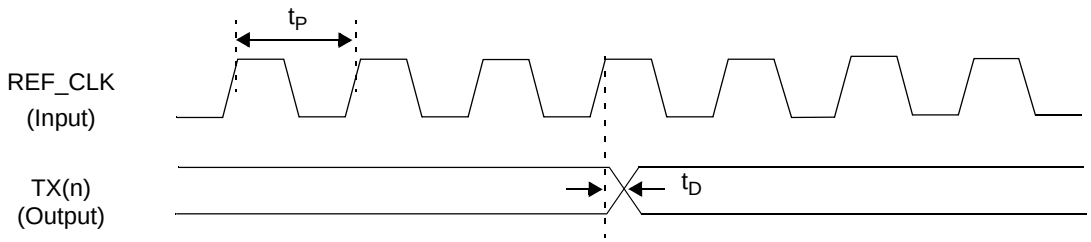
TIMING CHARACTERISTICS

Figure 3. SMII Sync In/Out Timing



Parameter	Symbol	Min	Typ	Max	Unit
REF_CLK period	t_P		8.0		ns
REF_CLK duty cycle		40		60	%
SYN_IN setup time to REF_CLK ↑	t_S	1.5			ns
SYN_IN hold time from REF_CLK ↑	t_H	1.0			ns
SYN_OUT delay from REF_CLK ↑	t_D	1.5		4.5	ns

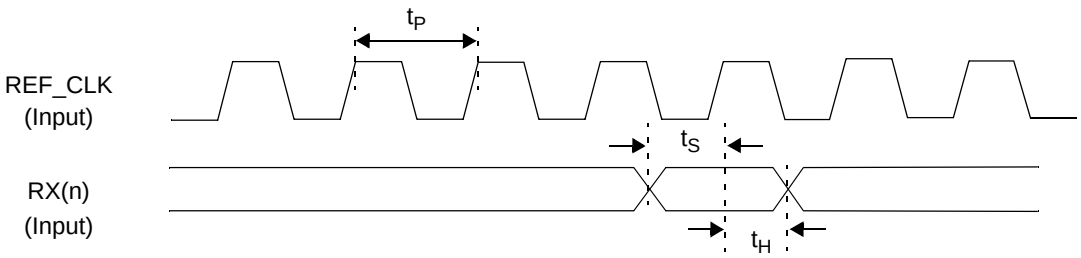
Figure 4. SMII Transmit Interface Timing



Notes: 10 pF load on all outputs
n = 0-7

Parameter	Symbol	Min	Typ	Max	Unit
TX(n) delay from REF_CLK ↑	t_D	1.5		4.5	ns

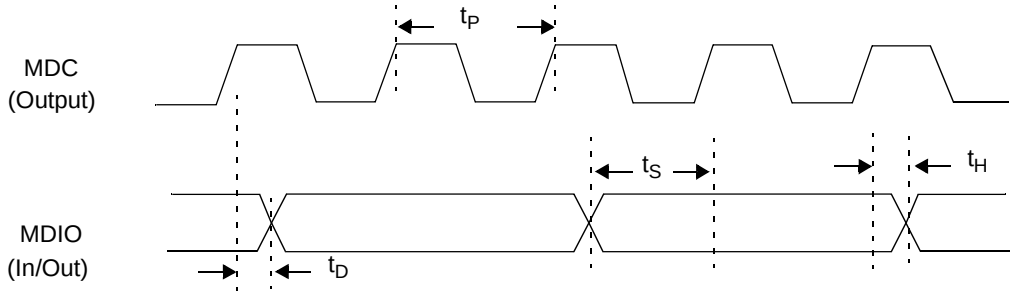
Figure 5. SMII Receive Interface Timing



Notes: n = 0-7

Parameter	Symbol	Min	Typ	Max	Unit
RX(n) setup to REF_CLK ↑	t_S	1.5			ns
RX(n) hold from REF_CLK ↑	t_H	1.0			ns

Figure 6. MII Interface Timing

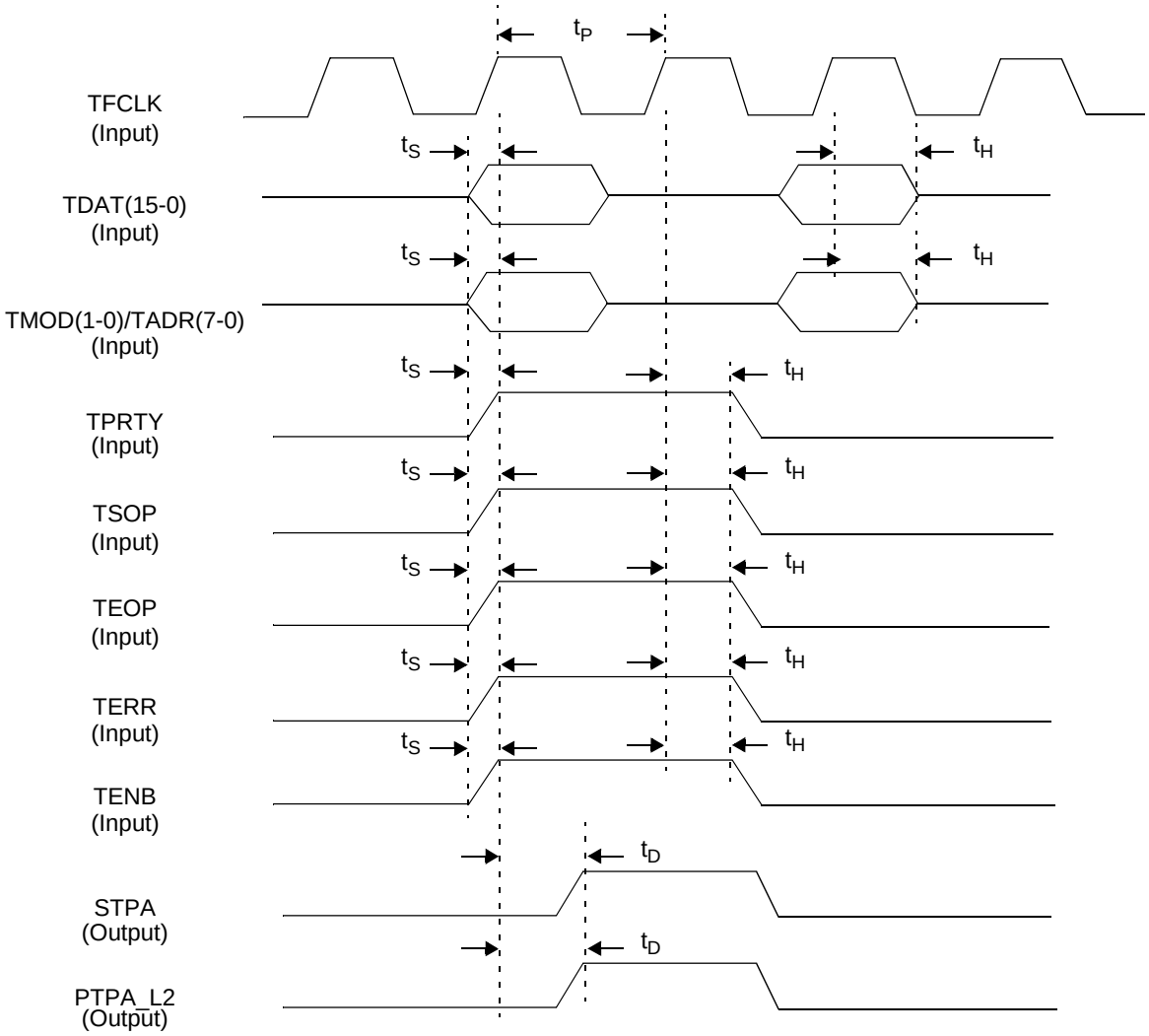


Note: 10 pF load on all MII outputs

Parameter	Symbol	Min	Typ	Max	Unit
MDC frequency	$1/t_P$	1.18		6.25	MHz
MDC duty cycle		40		60	ns
MDIO delay from MDC ↑	t_D	10		100	ns
MDIO setup to MDC ↑	t_S	15			ns
MDIO hold from MDC ↑	t_H	0.0			ns

POS-PHY LEVEL 2

Figure 7. Transmit Interface Timing (POS-PHY Level 2)

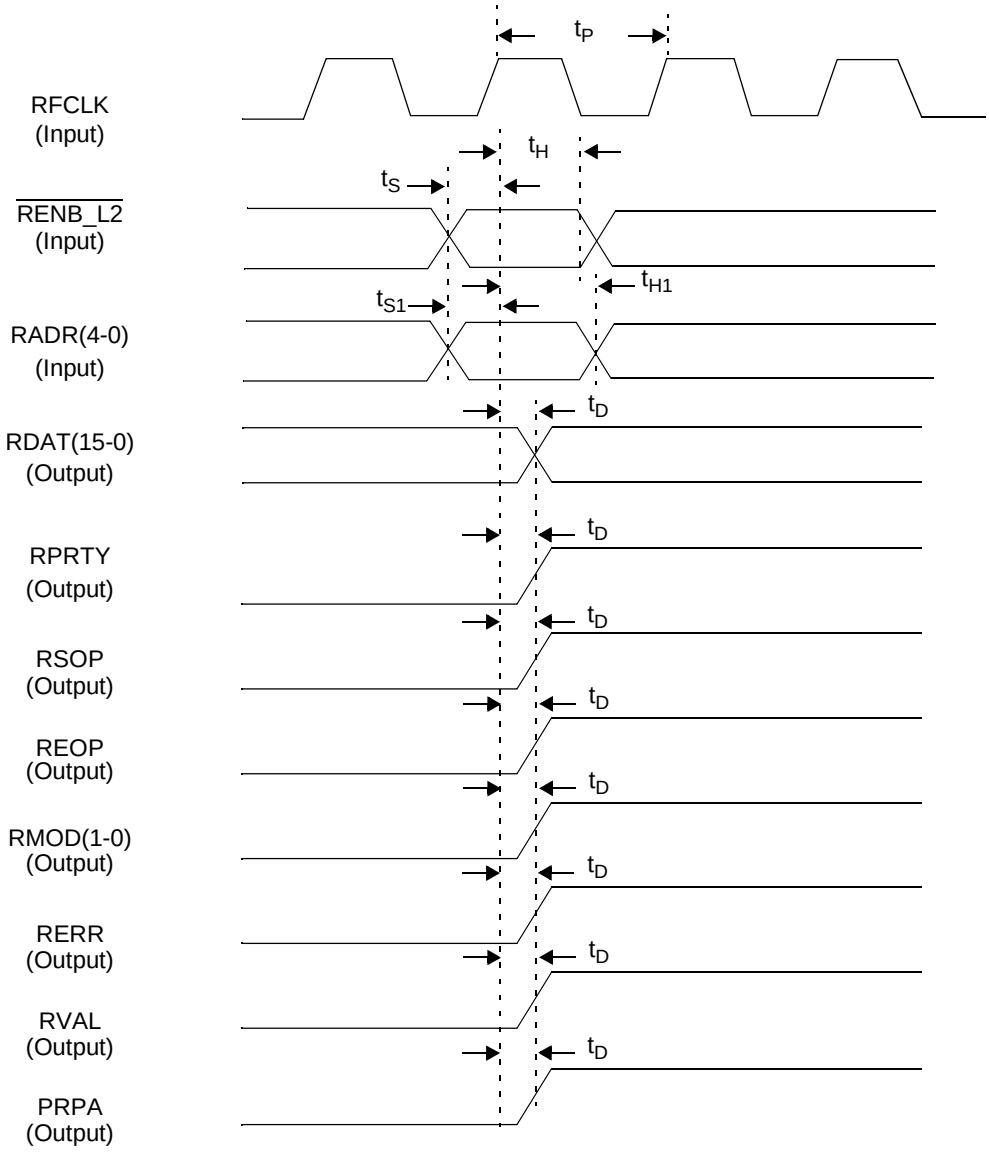


Notes: 10 pF load on POS-PHY interface outputs.

Please refer to POS-PHY Level 2 specification for protocol waveform.

Parameter	Symbol	Min	Typ	Max	Unit
TFCLK frequency	$1/t_P$	25		50	MHz
TFCLK duty cycle		40		60	%
TDAT(15-0), TADR(7-0), TMOD(1-0), TPRTY, TSOP, TEOP, TERR, TENB setup to TFCLK ↑	t_S	4.0			ns
TDAT(15-0), TADR(7-0), TMOD(1-0), TDRTY, TSOP, TEOP, TERR, TENB hold from TFCLK ↑	t_H	1.0			ns
STPA, PTPA_L2 delay from TFCLK ↑	t_D	2.0		12	ns

Figure 8. Receive Interface Timing (POS-PHY Level 2)

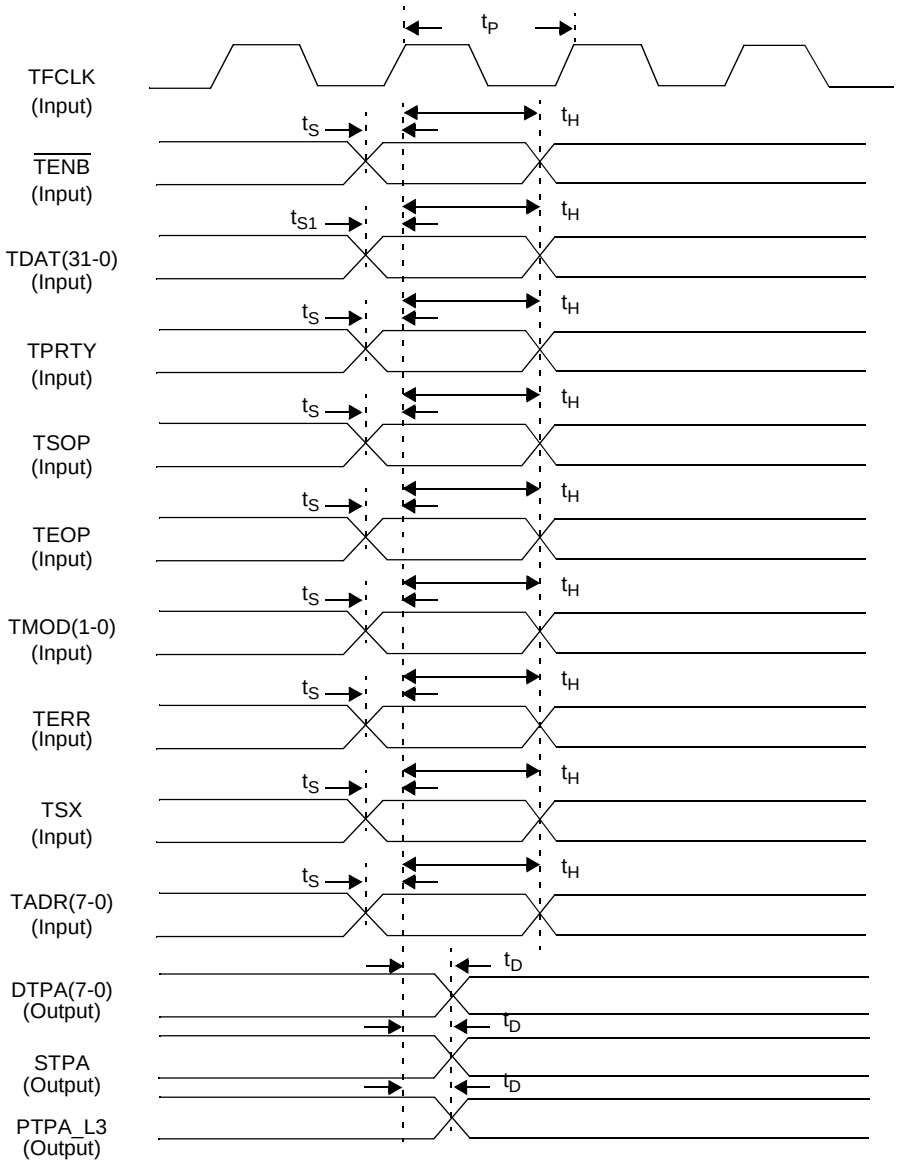


Notes: 10 pF load on POS-PHY interface outputs.
Please refer to POS-PHY Level 2 specification for protocol waveform.

Parameter	Symbol	Min	Typ	Max	Unit
RFCLK frequency	$1/t_P$	25		50	MHz
RFCLK duty cycle		40		60	%
$\overline{\text{RENB\_L2}}$ setup to RFCLK ↑	t_S	6.5			ns
$\overline{\text{RENB\_L2}}$ hold from RFCLK ↑	t_H	1.0			ns
RADR(4-0) setup to RFCLK ↑	t_{S1}	4.0			ns
RADR(4-0) hold from RFCLK ↑	t_{H1}	1.0			ns
RDAT(15-0), RPRTY, RSOP, REOP, RMOD(1-0), RERR, RVAL, PRPA delay from RFCLK ↑	t_D	2.0		12	ns

OIF SPI-3

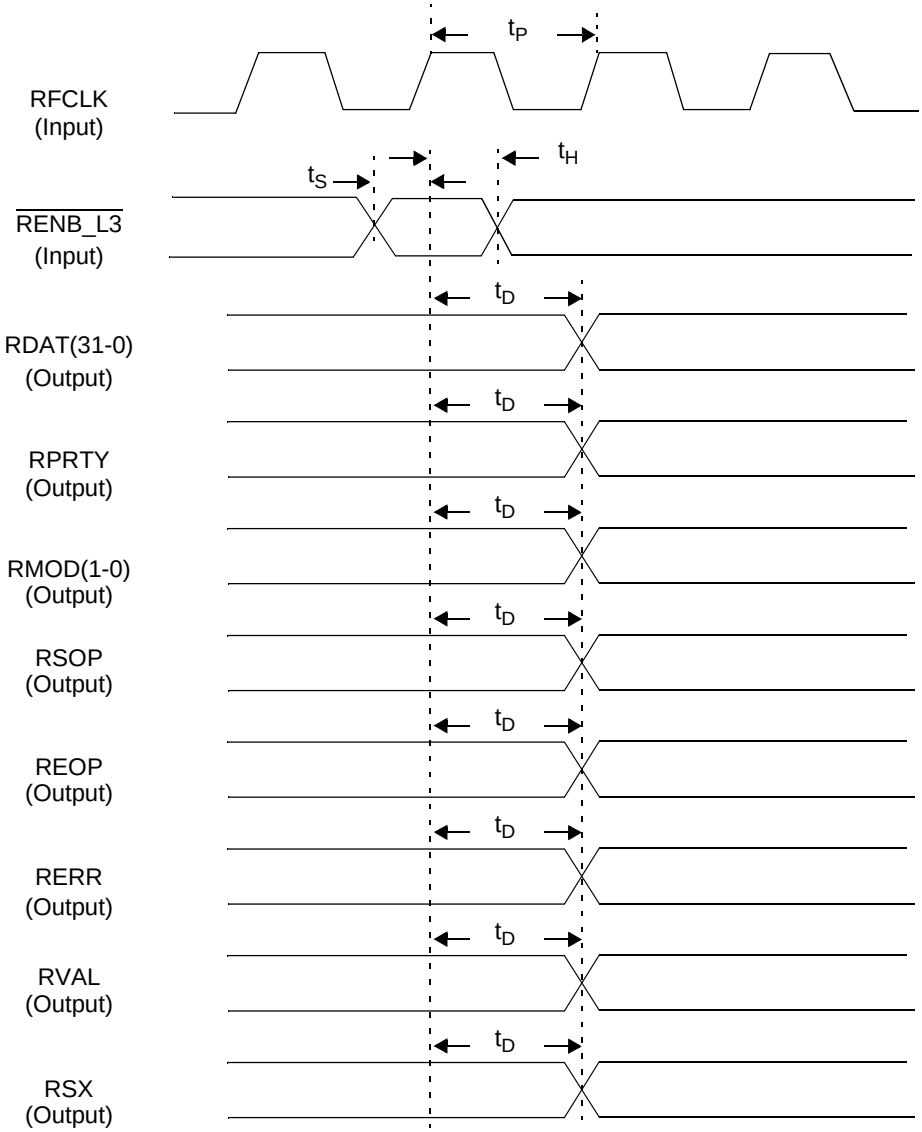
Figure 9. Transmit Interface Timing (OIF SPI-3)



Notes: 10 pF load on SPI-3 interface outputs.
Please refer to OIF SPI-3 specification for protocol waveform.

Parameter	Symbol	Min	Typ	Max	Unit
TFCLK frequency	$1/t_P$	50		100	MHz
TFCLK duty cycle		40		60	%
$\overline{\text{TENB}}$, TPRTY, TSOP, TEOP, TMOD(1-0), TERR, TSX, TADR(7-0) setup to TFCLK ↑	t_S	3.0			ns
TDAT(31-0) setup to TFCLK ↑	t_{S1}	3.5			ns
$\overline{\text{TENB}}$, TDAT(31-0), TPRTY, TSOP, TEOP, TMOD(1-0), TERR, TSX, TADR(7-0) hold from TFCLK ↑	t_H	1.0			ns
DTPA(7-0), STPA, PTPA_L3 delay from TFCLK ↑	t_D	1.0		5.5	ns

Figure 10. Receive Interface Timing (OIF SPI-3)

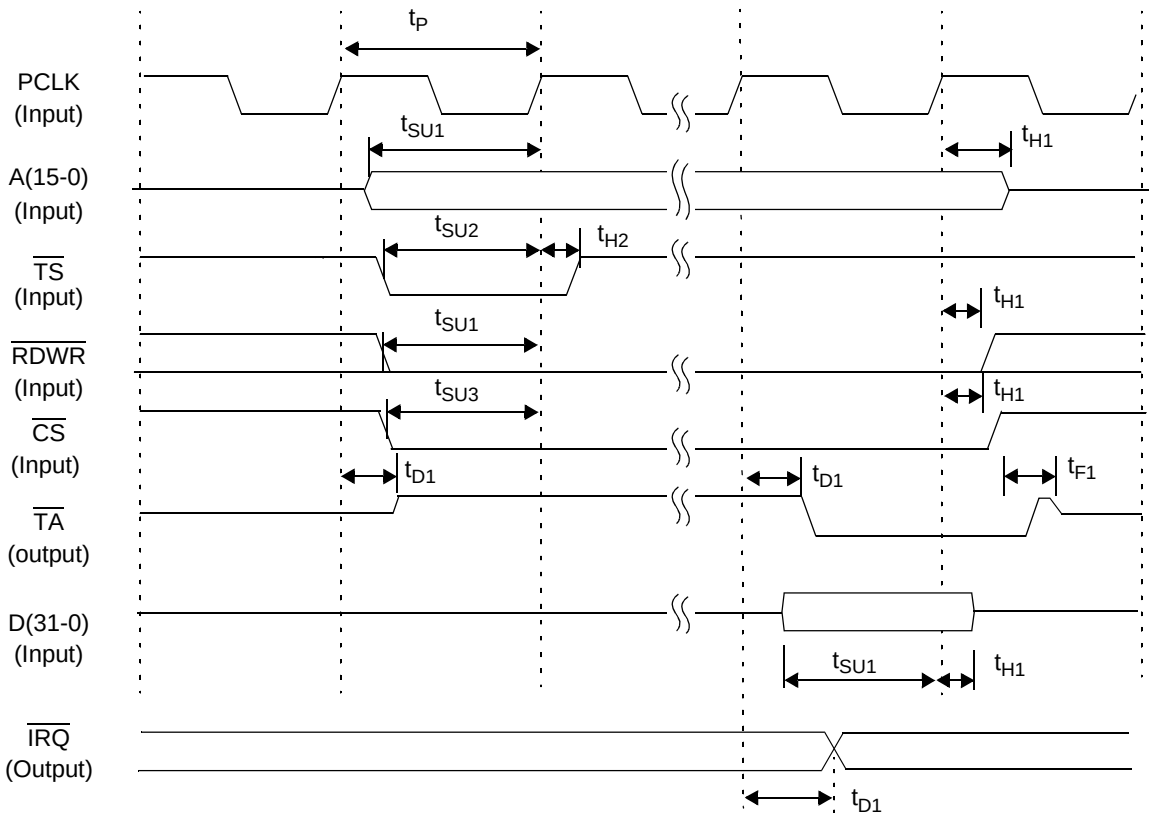


Notes: 10 pF load on SPI-3 interface outputs.

Please refer to OIF SPI-3 specification for protocol waveform.

Parameter	Symbol	Min	Typ	Max	Unit
RFCLK frequency	$1/t_P$	50		100	MHz
RFCLK duty cycle		40		60	%
$\overline{\text{RENB\_L3}}$ setup to RFCLK ↑	t_S	3.0			ns
$\overline{\text{RENB\_L3}}$ hold from RFCLK ↑	t_H	1.0			ns
RDAT(31-0), RPRTY, RMOD(1-0), RERR, RSOP, REOP, RVAL, RSX delay from RFCLK ↑	t_D	1.0		5.5	ns

Figure 11. MPC860 Single Write Cycle Timing

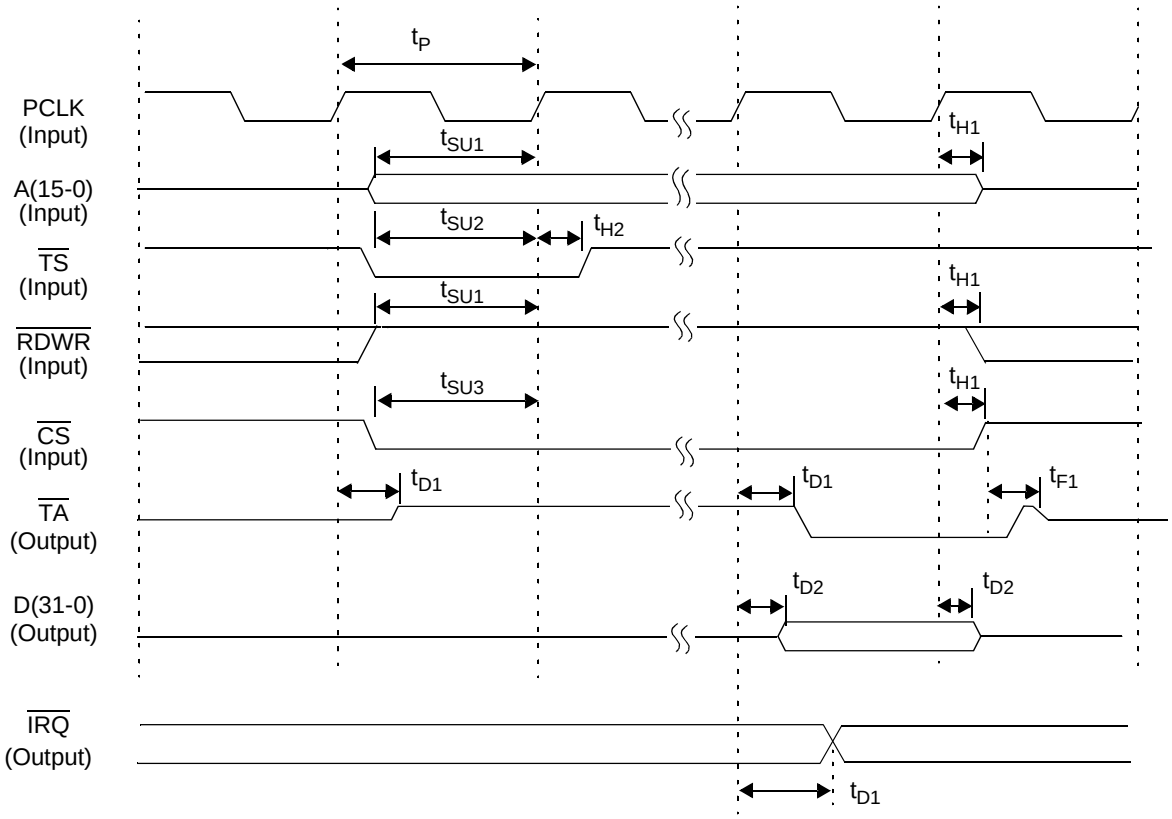


Notes: $\overline{TA}$ requires a pull-up resistor to V_{DD33} for proper operation.
25 pF load on all host interface outputs.

Parameter	Symbol	Min	Typ	Max	Unit
PCLK period	t_P	20.0		30.3	ns
A(15-0), $\overline{RDWR}$, D(31-0) setup to PCLK ↑	t_{SU1}	4.0			ns
A(15-0), D(31-0), $\overline{RDWR}$, $\overline{CS}$ hold from PCLK ↑	t_{H1}	1.0			ns
$\overline{TS}$ setup time to PCLK ↑	t_{SU2}	4.0			ns
$\overline{TS}$ hold time from PCLK ↑	t_{H2}	1.0			ns
$\overline{CS}$ setup to PCLK ↑	t_{SU3}	4.0			ns
$\overline{TA}$, $\overline{IRQ}$ delay from PCLK ↑	t_{D1}	2.0		12.0	ns
$\overline{TA}$ float time from $\overline{CS}$ ↑	t_{F1}	2.0		12.0	ns

MICROPROCESSOR INTERFACE TIMING

Figure 12. MPC860 Single Read Cycle Timing

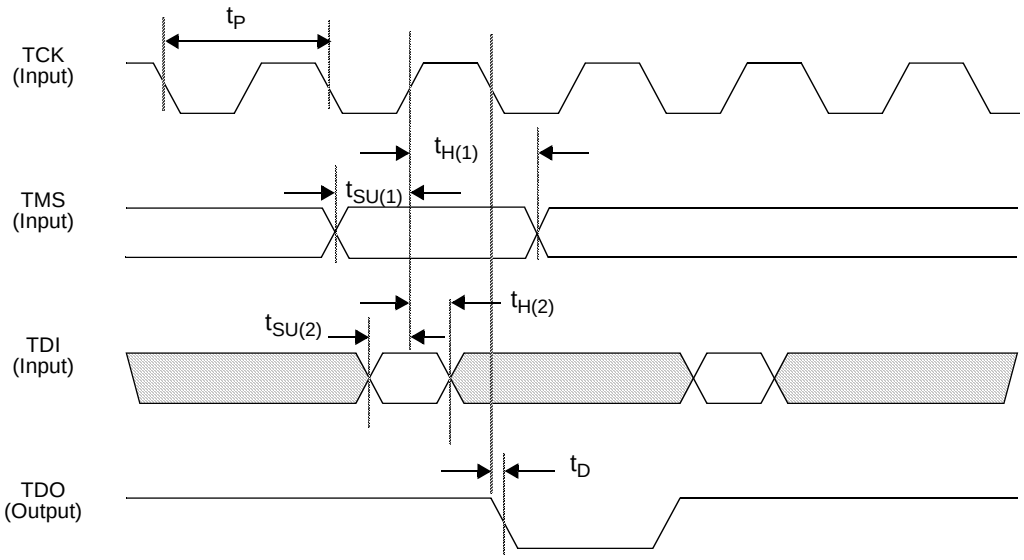


Note: 25 pF load on all host interface outputs

Parameter	Symbol	Min	Typ	Max	Unit
PCLK period	t_P	20.0		30.3	ns
A(15-0), $\overline{RDWR}$ setup to PCLK ↑	t_{SU1}	4.0			ns
A(15-0), $\overline{RDWR}$, $\overline{CS}$ hold from PCLK ↑	t_{H1}	1.0			ns
$\overline{TS}$ setup time to PCLK ↑	t_{SU2}	4.0			ns
$\overline{TS}$ hold time from PCLK ↑	t_{H2}	1.0			ns
CS setup to PCLK ↑	t_{SU3}	4.0			ns
$\overline{TA}$, $\overline{IRQ}$ delay from PCLK ↑	t_{D1}	2.0		12.0	ns
$\overline{TA}$ float time from $\overline{CS}$ ↑	t_{F1}	2.0		12.0	ns
D(31-0) delay from PCLK ↑	t_{D2}	2.0		12.0	ns

Note: $\overline{TA}$ requires a pull-up resistor to V_{DD33} for proper operation

Figure 13. Boundary Scan Timing Diagram



Note: 25 pF load on all Boundary Scan interface outputs

Parameter	Symbol	Min	Typ	Max	Unit
TCK period	t_P	50			ns
TCK clock duty cycle		40		60	%
TMS setup time before TCK ↑	$t_{SU(1)}$	4.0			ns
TMS hold time after TCK ↑	$t_{H(1)}$	1.0			ns
TDI setup time before TCK ↑	$t_{SU(2)}$	6.0			ns
TDI hold time after TCK ↑	$t_{H(2)}$	1.0			ns
TDO delay after TCK ↓	t_D			15.0	ns

OPERATION

SMII TO POS-PHY LEVEL 2/SPI-3 FLOW FUNCTIONAL OPERATION

Receive MAC Dataflow

Ethernet frames arriving at the SMII interface are qualified by Media Access Controller (MAC). Each SMII interface or each channel, has an individual MAC associated with it. The MAC operates in Full-Duplex or Half-Duplex mode and processes both standard Ethernet frames and VLAN tagged Ethernet frames. The MAC provides support for Control frames as stated in the IEEE 802.3 standard. At present, only PAUSE Control frames have been defined. The MAC can support Control frames other than PAUSE control frames. The SMII interface presents receive frames to the Receive MAC block and the MAC removes the PREAMBLE and the SFD (Start of Frame Delimiter) and writes the frames into the appropriate Ingress FIFO.

Receive MAC Checks

Following are the checks performed by the MAC on the incoming Ethernet frame.

FCS Check:

The Frame Check Sequence (FCS) is checked for its correctness. The FCS of the received frame is checked against the FCS calculated by the MAC over the Data field, address fields and length/type field. Frames failing the FCS check are discarded based on a programmable bit in the configuration register. This configuration bit is the FCS check failed discard bit.

Frame Length Check:

The length field of the received Ethernet frame is checked for correctness. The length of the Data field in the Ethernet frame is checked against the frames length field. The Frame length check enable is programmable. Frames failing the frame length check will be discarded if the frame length check discard configuration bit is set.

Maximum Frame Size Check:

The maximum size of the accepted Ethernet frame is programmable. The default value is 1536 (decimal) bytes. Frames exceeding the programmed maximum frame size are truncated. Truncated frames are discarded if the Discard Truncated Frame configuration bit is set. The maximum frame size check is disabled by setting the Huge Frame Enable configuration bit.

Interframe Gap check:

The Interframe Gap (IFG) is programmable. A received Ethernet frame violating the programmed Interframe gap value is dropped. The default value of the Minimum IFG is 80 (decimal) bits.

Destination Address Check:

The Destination address of the received Ethernet frame is compared to the programmed Station address of the device. If the destination address of the frame does not match the programmed station address, the frame will be filtered out based on the Destination Address match discard configuration bit.

Note: In the event that an incoming frame (from ethernet side) fails all the checks and the corresponding configuration bits to discard the frame are NOT SET, the frame will be output on the POS-PHY/SPI-3 Receive Interface. The only requirement on the incoming frame for the above to happen, is that the incoming frame has a valid PREAMBLE and SFD.

Receive MAC Statistics

The MAC provides statistics and performance monitoring, to facilitate remote network monitoring (RMON). The Receive MAC records other statistics over the statistics and performance monitoring for RMON.

Counters:

The MAC records the following statistics using CLEAR on READ counters:

- Length of the received frame in bytes (31 bit)
- Total number of frames received. This includes errored frames (25 bit)
- Count of frames received with FCS errors (17 bit)
- Count of Multicast frames received (25 bit)
- Count of Broadcast frames received (25 bit)
- Count of Control frames received (16 bit)
- Count of PAUSE Control frames received (16 bit)
- Count of Control frames received with unknown opcode (16 bit)
- Count of frames received with alignment error (16 bit)
- Count of frames received failing the Length field check (16 bit)
- Count of frames received with valid FCS and length less than 64 bytes (16 bit)
- Count of frames received with valid FCS and total byte count is between 1519 and maximum frame length (16 bit)
- Count of frames received with Invalid FCS and length less than 64 bytes (16 bit)
- Count of frames received with invalid FCS and total byte count is between 1519 and maximum frame length (16 bit)
- Count of frames dropped by the receive MAC (16 bit)
- Count of number of false carriers received during idle (16 bit)

Receive MAC Configuration Bits

Note: *n* = 0 . . . 7 for channels 0 . . . 7

Enable Receive MAC: Address (1000 + 200**n*) Bit 2; ‘1’ = Enable, ‘0’ = Disable.

Enable Length Field Check: Address (1000 + 200**n* +1) Bit 4; ‘1’ = Enable, ‘0’ = Disable.

Enable Huge Frame: Address (1000 + 200**n* +1) Bit 5; ‘1’ = Enable, ‘0’ = Disable.

Minimum Inter Frame Gap: Address (1000 + 200**n* +2) Bits 15 to 8; Default 96 decimal.

Maximum Frame Length: Address (1000 + 200**n* +4) Bits 15 to 0; Default 1536 decimal.

Enable Discard Truncated Frames: (1100 + 200**n* +1) Bit 23; ‘1’ = Enable, ‘0’ = Disable.

Enable Discard Length Check Failed: (1100 + 200**n* +1) Bit 24; ‘1’ = Enable, ‘0’ = Disable.

Enable Discard CRC Failed Frames: (1100 + 200**n* +1) Bit 25; ‘1’ = Enable, ‘0’ = Disable.

Enable Discard RX Errored Frames: (1100 + 200**n* +1) Bit 26; ‘1’ = Enable, ‘0’ = Disable.

Enable Discard Pause Frames: (1100 + 200**n* +1) Bit 27; ‘1’ = Enable, ‘0’ = Disable.

Enable Destination Address Filter: (1100 + 200**n* +2) Bit 1; ‘1’ = Enable, ‘0’ = Disable.

Enable Full Duplex: Address (1000 + 200*n + 1) Bit 0; ‘1’ = Enable, ‘0’ = Disable

Programmable Collision Window (Half-Duplex): Address (1000 + 200*n + 3) Bits 9 to 0;

Note: Please refer to “Memory Maps and Bit Descriptions” starting on page 47 for complete list of configuration bits.

Ingress FIFO Operations

Ingress FIFO Write:

Frames once qualified by the Receive MAC are written into the Ingress FIFO of the appropriate channel. The Ingress FIFO for each channel is 12 KBytes deep. This accommodates 7.7 standard ethernet frames (1526 Bytes). The Ingress FIFO is an integral part of Envoy-8FE's IEEE 802.3 compliant Flow control mechanism, which is used to back-pressure the Ethernet interface. In the event that the Ingress FIFO starts becoming full, the flow control is activated (if enabled) and the device transmitting the Ethernet traffic is back-pressured. A complete description of that procedure is outlined in section "Ethernet Full Duplex Flow Control" starting on page 44. If the Ethernet device transmitting frames, ignores the back-pressure indication and attempts to overflow the Ingress FIFO, the Envoy-8FE will truncate the frame. In the case of Half Duplex mode, the backpressure mechanism used is the "Raised Carrier" method. The description of this flow control mechanism is in the section under Ethernet "Half-Duplex Flow Control" starting on page 43.

Ingress FIFO Read:

Frames are read out from the Ingress FIFO by the POS-PHY Level 2/SPI-3 interface. Since the POS-PHY Level 2/SPI-3 interface aggregates the traffic from the channels, a channel selection is required. The selection of the Ingress FIFO (or channel selection) for frame reads, is done by the POS-PHY Level 2/SPI-3 interface. In the case of POS-PHY Level 2, the Link layer device connected to the Envoy-8FE on its POS-PHY interface, does the selection. For SPI-3, the selection is done by the scheduler in the Envoy-8FE's SPI-3 interface block. The scheduler in this case uses a round robin selection scheme.

Ingress FIFO Frame Availability for Transfer:

Frame data once stored in the Ingress FIFO, will be made available for transfer on the POS-PHY Level 2/SPI-3 interface, depending on two selectable modes of operation. In the first mode, when a complete frame has been written into the Ingress FIFO, the frame is available for transfer. In other words, frames are available for transfer, when an end of frame has been written into the Ingress FIFO. In the second mode (streaming), if enabled, a frame is available for transfer, when a selectable fixed number of bytes have been written into the Ingress FIFO. The selections for streaming are 256, 512, 768 or 1550 bytes. In the situation, where streaming is enabled and an end of frame is written into the Ingress FIFO, before the selected number of (streaming) bytes have been received, the frame data will be available for transfer across the POS-PHY Level 2/SPI-3 interface based on the end of frame condition. When streaming is enabled, Frame errors at the SMII interface are indicated on the POS-PHY Level 2/SPI-3 interface, during the transfer of the frame.

Ingress FIFO Configurations

Global Stream Enable: Address 1102 Bit 0; '1' = Enable, '0' = Disable.

Per channel Stream Enable: Address Bit 0; '1' = Enable, '0' = Disable.

Address (400B + n)* where n = 0 to 3 for channels 0 to 3 and Address (4012 + n) where n = 0 to 3 for channels 4 to 7.

Per channel Streaming Threshold: Address Bits 2 to 1; '00' = 256 bytes, "01" = 512 bytes, "10" = 768 bytes and "11" = 1550 bytes.

Address (400B + n)* where n = 0 to 3 for channels 0 to 3 and Address (4012 + n) where n = 0 to 3 for channels 4 to 7.

Per channel Ingress FIFO Threshold: Address Bits 5 to 3; '00' = 256 bytes, "01" = 512 bytes, "10" = 768 bytes and "11" = 1550 bytes.

Address (400B + n)* where n = 0 to 3 for channels 0 to 3 and Address (4012 + n) where n = 0 to 3 for channels 4 to 7.

Note: Please refer to "Memory Maps and Bit Descriptions" starting on page 47 for complete list of configuration bits.

Receive POS-PHY Level 2/SPI-3 Operations

Dataflow Operations:

Frames from the Ingress FIFO are read out by the Receive POS-PHY Level 2/SPI-3 interface. The Receive POS-PHY Level 2/SPI-3 interface is programmable in either POS-PHY Level 2 or OIF SPI-3 mode. Section "Packet Over SONET (POS-PHY) Level 2 / System Packet Interface (SPI) Level 3" starting on page 8 describes the interface in detail. In POS-PHY Level 2, the Link layer device selects the channel for frame transfer, and flow control on the interface is done by the link layer controlling the Read Enable and monitoring the POS-PHY "Available" signal PRPA, provided by Envoy-8FE. In SPI-3, the Link layer performs flow control by controlling the Read Enable. The channel selection in this case is done by Envoy-8FE. Once a channel has a frame to send, Envoy-8FE's SPI-3 scheduler selects the channel for frame transfer. The Envoy-8FE provides the option to restrict a channel from transmitting more than a fixed number of bytes once selected. Once this fixed number of bytes has been transmitted by the selected channel, a new channel is selected for frame transfer. This prevents a channel from using up all the bandwidth on the SPI-3 interface, by giving the other channels access to the SPI-3 interface. The selections for this fixed number of bytes are 256, 512, 768 and 1550.

POS-PHY Level 2/SPI-3 Receive Interface Frame Format:

Data at the Receive POS-PHY Level 2/SPI-3 interface (Envoy-8FE transmits data to POS-PHY Level 2/SPI-3) is an Ethernet frame (VLAN frames also), excluding the preamble and start of frame.

Standard Ethernet Frame at SMII interface

Preamble (7 bytes)	Start of Frame Delimiter (1 Byte)	Destination Address (6 bytes)	Source Address (6 bytes)	Length (2 bytes)	Data (46 to 1500)	Frame Check Sequence (4 Bytes)

Frame format at POS-PHY Level 2/SPI-3 Receive Interface

Destination Address (6 bytes)	Source Address (6 bytes)	Length (2 bytes)	Data (46 to 1500)	Frame Check Sequence (4 Bytes)

VLAN Tag Frame format at POS-PHY Level 2/SPI-3 Receive Interface

Destination Address (6 bytes)	Source Address (6 bytes)	Length (2 bytes)	VLAN TAG (2 bytes)	Data (46 to 1500)	Frame Check Sequence (4 Bytes)

Frame with Extension Field at POS-PHY Level 2/SPI-3 Receive Interface

Destination Address (6 bytes)	Source Address (6 bytes)	Length (2 bytes)	Data (46 to 1500)	Frame Check Sequence (4 Bytes)	Extension

POS-PHY LEVEL 2/SPI-3 TO SMII FLOW FUNCTIONAL OPERATION

Transmit POS-PHY Level 2/SPI-3 Operations

Transmit POS-PHY Level 2/SPI-3 Dataflow:

At the POS-PHY Level 2/SPI-3 Transmit interface, frames are transferred from the link layer device to the Envoy-8FE. An Envoy-8FE channel is selected for data transfer, by the link layer device. In both POS-PHY Level 2 and SPI-3 mode, the link layer device monitors the “Buffer Space Available” signals, STPA, PTPA and DTPA (SPI-3 only) and selects an Envoy-8FE channel for data transfer, based on these signals. Once a data transfer commences, the link layer device qualifies the frame data being transferred into the channel’s Egress FIFO, with the write enable signal. The “Buffer Space Available” signals reflect the full status of the channel’s Egress FIFO and gets de-asserted when the associated Egress FIFO becomes full.

Transmit POS-PHY Level 2/SPI-3 Interface Frame Format:

The Data format accepted by Envoy-8FE, at the Transmit POS-PHY Level 2/SPI-3 interface (Envoy-8FE receives data from POS-PHY Level 2/SPI-3), is an Ethernet frame (VLAN frames also), excluding the preamble and the Start of frame delimiter. If the Transmit MAC is configured to generate the Frame Check Sequence (FCS), then FCS is optional for the frame received by the Envoy-8FE at the POS-PHY interface. If the Transmit MAC is not configured to generate FCS, then the FCS needs to be included in the frame.

Standard Ethernet Frame at SMII Transmit interface

Preamble (7 bytes)	Start of Frame Delimiter (1 Byte)	Destination Address (6 bytes)	Source Address (6 bytes)	Length (2 bytes)	Data (46 to 1500)	Frame Check Sequence (4 Bytes)

Frame format at POS-PHY Level 2/SPI-3 Transmit Interface with Frame Check Sequence

Destination Address (6 bytes)	Source Address (6 bytes)	Length (2 bytes)	Data (46 to 1500)	Frame Check Sequence (4 Bytes)

Frame format at POS-PHY Level 2/SPI-3 Transmit Interface with-out Frame Check Sequence

Destination Address (6 bytes)	Source Address (6 bytes)	Length (2 bytes)	Data (46 to 1500)

VLAN Tagged and Extended frames may have the FCS included depending on whether Envoy-8FE is configured to generate FCS or not.

Egress FIFO Operations

Egress FIFO Write:

Each Egress FIFO is 4 KBytes deep. The Link layer device is responsible for selecting the channel into which the frame data is written. The selection criteria for the Link layer device is explained above. The “Buffer Space Available” signal for each channel is based on the Egress FIFO Near Full Threshold. The Egress FIFO back-pressures the POS-PHY Level 2/SPI-3 Transmit interface when the FIFO becomes full. The link layer device should never attempt to overflow the FIFO.

Egress FIFO Read:

Frame data from the Egress FIFO is read out by the Transmit MAC block. Each channel has a SMII Transmit block and interfaces to the appropriate Egress FIFO. Once a complete frame has been stored in the Egress FIFO, it is then available for transmission on the Ethernet Network through the SMII Transmit interface.

The Egress FIFO forms an integral part in the implementation of the 802.3 compliant Ethernet flow control mechanism in the Envoy-8FE, using PAUSE Control frames. In the event a PAUSE Control frame destined for the Envoy-8FE, is received at the SMII receive interface, the action taken by the Full-Duplex flow control block is to stop Egress FIFO read’s. This may result in the Egress FIFO becoming full. As mentioned above the POS-PHY Level 2/SPI-3 interface is backpressured when the Egress FIFO becomes full. A complete explanation of the Full-Duplex Ethernet flow control mechanism is outlined in section “Ethernet Full Duplex Flow Control” starting on page 44.

Egress FIFO Configurations

Note: *n* = 0 for channel 0 and 1 for channel 1.

Per Channel Egress FIFO Near Full Threshold: Addr (4001 + n) Bits 9 to 3; These 7 bits define the number of bytes before the Egress FIFO becomes full. This Threshold value needs to be programmed the same value as the Transmit Near Full Indicator Threshold (I/O Section - POS-PHY Level 2/SPI-3 - Addr (2000 + n) Bits 10 to 4) for proper operation.

Note: Please refer to “Memory Maps and Bit Descriptions” starting on page 47 for complete list of configuration bits.

Transmit MAC Dataflow

The Transmit MAC block is a IEEE 802.3 compliant Media Access Controller. The MAC operates in either Full-Duplex mode or Half Duplex mode. The mode of operation is configurable. The MAC transmits both standard Ethernet frames and VLAN tagged Ethernet frames. The MAC transmits control frames and at present only PAUSE control frames have been defined. The MAC can support Control frames other than PAUSE control frames. For every Envoy-8FE channel there is a dedicated MAC. The Egress FIFO indicates to the Transmit MAC availability of a Frame when a complete frame is stored in the Egress FIFO. The Transmit MAC reads the Egress FIFO and transmits the frame over the SMII transmit interface.

Transmit MAC Configurable Options and Checks

Following are the configurable options and checks for the MAC for the outgoing Ethernet frame.

FCS (Frame Check Sequence) Generation Option:

The MAC provides the option to append the correct FCS when Ethernet frames presented to the Envoy-8FE at the POS-PHY Level 2/SPI-3 Transmit interface, do not contain a valid FCS. Please note this option works in conjunction with the pad option.

Pad Short Ethernet Frames Option:

The MAC can be configured to pad short frames to 64 bytes and append the correct FCS. If this option is set, the FCS generation option needs to be disabled. The pad option is for Ethernet frames presented at the Transmit POS-PHY interface with lengths less than 64 bytes.

Frame Length Check:

The length field of the received Ethernet frame is checked for correctness. The length of the Data field in the Ethernet frame is checked against the frames length field. The Frame length check enable is programmable.

Maximum Frame Size Check:

The maximum size of the accepted Ethernet frame is programmable. The default value is 1536 (decimal) bytes. Frames exceeding the programmed maximum frame size are truncated. Truncated frames are tagged with RX_ER. The maximum frame size check is disabled by setting the Huge Frame Enable configuration bit.

Back to Back Interframe Gap Option:

The Interframe Gap (IFG) between two back to back transmitted Ethernet frames is programmable. The default value of the Minimum IFG is 96 bits (decimal).

Source Address Replace Option:

The Mac provides the option to replace the source address (SA field) of the Ethernet frame received at the POS-PHY Level 2/SPI-3 Transmit interface with the Programmed Station Address. The Envoy-8FE has a programmable Station Address register.

Preamble Length Option:

The Preamble length of the transmitted Ethernet frame is programmable by the MAC. The default value is 7 bytes.

Transmit MAC Statistics

The MAC provides statistics and performance monitoring, to facilitate remote network monitoring (RMON) as per Groups 1, 2, 3 and 9. The Transmit MAC records other statistics over the statistics and performance monitoring for RMON.

Counters:

The MAC records the following statistics using CLEAR on READ counters:

- Length of the transmitted frame in bytes (31 bit)
- Total number of frames transmitted. This includes all frames, broadcast and multicast (25 bit)
- Count of Multicast frames transmitted (25 bit)
- Count of Broadcast frames transmitted (25 bit)
- Count of PAUSE Control frames transmitted (16 bit)
- Count of Control frames transmitted (14 bit)
- Count of Oversize frames transmitted (14 bit)
- Count of Undersize frames transmitted (14 bit)

- Count of deferred frames transmitted (13 bit)
- Count of excessive deferred frames transmitted (13 bit)
- Count of single collision frames (13 bit)
- Count of multiple collision frames (13 bit)
- Count of late collision frames (13 bit)
- Count of excessive collision frames (13 bit)
- Count of total collision frames (13 bit)

Transmit MAC Configuration Bits

Note: *n* = 0 . . . 7 for channels 0 . . . 7

Enable Transmit MAC: Address (1000 + 200**n*) Bit 0; ‘1’ = Enable, ‘0’ = Disable.

Enable FCS (CRC) append: Address (1000 + 200**n* + 1) Bit 1; ‘1’ = Enable, ‘0’ = Disable.

Enable Frame Padding and FCS (CRC) append: Address (1000 + 200**n* + 1) Bit 2; ‘1’ = Enable, ‘0’ = Disable.

Preamble Length: Address (1000 + 200**n* + 1) Bits 15 to 12;

Enable Huge Frame: Address (1000 + 200**n* + 1) Bit 5; ‘1’ = Enable, ‘0’ = Disable.

Back to Back Interframe Gap: Address (1000 + 200**n* + 2) Bits 6 to 0; Default 96 decimal.

Maximum Frame Length: Address (1000 + 200**n* + 4) Bits 15 to 0; Default 1536 decimal.

Enable Substitute Station address for frame Source field: (1100 + 200**n* + 2) Bit 2; ‘1’ = Enable, ‘0’ = Disable.

Enable Full Duplex: Address (1000 + 200*n + 1) Bit 0; '1' = Enable, '0' = Disable.

Note: Please refer to “Memory Maps and Bit Descriptions” starting on page 47 for complete list of configuration bits.

ETHERNET HALF DUPLEX

In Half-Duplex mode of operation, two or more Ethernet devices are connected to a common transmission medium and when one Ethernet device transmits, the others listen. In the case where two Ethernet devices transmit at once, a “Collision” is said to have occurred. A “Jam Sequence” is transmitted by the transmitting Ethernet device indicating the occurrence of a collision. The contention is resolved by each of the Ethernet devices responsible for the collision, backing off, and attempting to re-transmit after a time period. This method is called Carrier Sense Multiple Access/Collision Detection (CSMA/CD). The Envoy-8FE Media Access Controller (MAC) implements the 802.3 compliant CSMA/CD algorithm. For a complete definition of this algorithm please refer to the IEEE 802.3 specification. Following is an outline based on the Envoy-8FE MAC.

Note: Carrier Sense and Collision detection status is indicated by the PHY device to the Envoy-8FE via the SMII interface. Please refer to the Serial Media Independent Interface (SMII) specification for further details.

Carrier Sense

Following the transmission of an Ethernet frame from the Envoy-8FE, the Envoy-8FE Media Access Controller (MAC) times the Inter Packet Gap (IPG) count as programmed in the Back-to-Back IPG configuration register. The MAC monitors the Carrier Sense status for the duration of IPG time before transmitting a new frame. Envoy-8FE provides an optional IPG mechanism where the IPG time is divided into a two-thirds/one-thirds ratio. During the first two-thirds of the IPG, the IPG timer is reset and Carrier Sense status is monitored or sensed. During the final one-third of the IPG, the Carrier sense status is ignored and the MAC begins transmission once the IPG timer has expired. This optional mechanism enhances system robustness. The configuration bits defining the two-third/one-third values are IPGR1 and IPGR2.

Collision Detection

In the event the Envoy-8FE MAC detects a Collision when the device is transmitting an Ethernet frame, the MAC outputs the 32-bit jam sequence. The jam sequence is made up of several bits of the CRC, inverted to guarantee an invalid CRC upon reception of the frame. The MAC then backs off transmission of the frame (retry) based on the “Truncated Binary Exponential Backoff” (BEB) algorithm. Following this backoff time, the frame is retried. The “No Backoff” configuration bit, when enabled, retransmits the frame without a backoff, following a collision. This option needs to be enabled with caution.

Alternate BEB Truncation

The backoff time following a collision is a controlled randomization process called “truncated binary exponential backoff”. It is defined as an integer multiple of the slot times. The number of slot times to delay before the n^{th} retransmission attempt is chosen as a uniformly distributed random integer r in the range: $0 \leq r \leq 2^k$ where k = min(n,10). So, after the first collision, the MAC will backoff either 0 or 1 slot times. After the fifth collision, the MAC will backoff between 0 and 32 slot times. After the tenth collision, the maximum number of slot times to backoff is 1024. The value of n is configurable and is called “Alternate Binary Exponential Backoff Truncation”.

Excessive Collisions

Upon collision, the MAC attempts re-transmission of the frame. As specified in the IEEE 802.3 specification, a frame has excessive collisions if 15 re-transmission attempts have occurred. The number of retransmission attempts for excessive collisions is configurable. In the event a frame has been excessively deferred, the frame is discarded and will not be transmitted. It is possible to configure the Envoy-8FE not to discard an excessively deferred frame.

Half-Duplex Flow Control

There is no IEEE 802.3 compliant backpressure mechanism for Half Duplex. The common industry implementation is the “Raise Carrier” method. The Envoy-8FE MAC uses the configurable “Raise Carrier” method for flow control in Half-Duplex mode. In the event the Envoy-8FE MAC needs to backpressure the transmission medium, it raises carrier by transmitting the preamble. Other devices on the transmission Medium defer to the carrier. If a collision occurs due to the raised carrier, the congestion is resolved using the standardized collision-detect, backoff method. The Host can not initiate flow control when raise carrier method is being used.

Half-Duplex MAC Configuration Bits

Note: n = 0. .7 for channels 0. .7

Back to Back Interframe Gap: Address(1000 + 200*n + 2) Bits 6 to 0; Default 96 Decimal

Non Back to Back Interframe Gap Part 1 (IPGR1): Address(1000 + 200*n + 2) Bits 30 to 24; Default 64 Decimal

Non Back to Back Interframe Gap Part 2 (IPGR2): Address(1000 + 200*n + 2) Bits 22 to 16; Default 96 Decimal

Minimum IFG Enforcement: Address(1000 + 200*n + 2) Bits 15 to 8; Default 80 Decimal

Programmable Collision Window (Half-Duplex): Address (1000 + 200*n + 3) Bits 9 to 0;

Programmable Max re-transmission attempts (Half-Duplex): Address (1000 + 200*n + 3) Bits 15 to 12;

Enable Excessive Defer: Address (1000 + 200*n + 3) Bit 16; '1' = Enable, '0' = Disable

Enable No Backoff: Address (1000 + 200*n + 3) Bit 17; '1' = Enable, '0' = Disable

Enable Backpressure No Backoff: Address (1000 + 200*n + 3) Bit 18; '1' = Enable, '0' = Disable

Enable Alternate Binary Exponential Backoff: Address (1000 + 200*n + 3) Bit 19; '1' = Enable, '0' = Disable

Alternate Binary Exponential Backoff Truncation Value: Address (1000 + 200*n + 3) Bit 23 to 20;

Note: Please refer to “Memory Maps and Bit Descriptions” starting on page 47 for complete list of configuration bits.

ETHERNET FULL DUPLEX FLOW CONTROL

Outline

The Envoy-8FE implements the IEEE 802.3 compliant flow control mechanism. This mechanism is used to prevent frame loss, resulting from frame discard due to a buffer becoming full. It is intended for a Full-Duplex link between two devices. For example, a link between a switch and an end device. The mechanism involves the generation of, and operation on, specific Ethernet Control frames called “PAUSE Control frames”. As of this writing, the only control frame defined is the PAUSE control frame. A PAUSE control frame has certain values for the Destination Address field, Type field, Opcode field, MAC control parameter field and must have a valid FCS. Following are the required PAUSE control frame field values.

The Destination address must either be the multicast address (01-80-C2-00-00-01) or the unicast address of the device the frame is being sent to. The TYPE field should have the reserved value of 0x8808 (MAC Control frame type). The Control Opcode should be equal to 0x0001. A MAC control parameter called pause_time parameter, specifies the time period, in 512-bit times, for which the device receiving the PAUSE control frame is paused.

The Flow control operation in the Envoy-8FE is divided into two operations. One, the action taken when a PAUSE control frame is received from a remote device and two, when Envoy-8FE generates a PAUSE control frame and transmits it to a remote device. The remote device is connected to the Envoy-8FE via a full duplex link. Envoy-8FE PAUSE frame processing needs to be enabled for the PAUSE frame flow control mechanism to take effect. An option is provided in the device to filter out the received PAUSE control frame.

PAUSE Control Frame Reception

Remote devices receiving Ethernet frames from Envoy-8FE can backpressure Envoy-8FE, by sending a PAUSE control frame to Envoy-8FE. The backpressure may be needed, due to the fact that the remote device on the link, has its buffer becoming full. On reception of the PAUSE control frame, Envoy-8FE will stop transmitting frames to the remote device. If Envoy-8FE is in the middle of transmission of a frame, when it receives a PAUSE control frame, it will complete transmission of the frame and then pause transmission of any further Data frames. When Envoy-8FE is in the pause state, it is allowed to transmit control frames, like PAUSE control frames. The period for which Envoy-8FE stays in a PAUSE state is defined by the pause_time parameter in the PAUSE control frame. The pause_time parameter is used as the initial value of an internal count down timer. The count down timer is started as soon as the pause_time parameter is loaded into the count down timer. Envoy-8FE will stay in this PAUSE state until the internal timer counts down to zero, in which case Envoy-8FE will resume transmission of data frames to the remote device. If a PAUSE control frame with a new non zero pause_time parameter is received, the new pause_time is loaded into the internal down counter and the Envoy-8FE stays in the PAUSE state for the time specified by the new pause-time. When a PAUSE frame with a timer parameter value of zero is received, the Envoy-8FE will resume sending data frames to the remote device.

PAUSE Control Frame Generation

There are two modes for PAUSE Control Frame generation, Automatic generation and Host initiated generation.

Automatic PAUSE Frame generation

In this mode, when the remote device sends Data frames to the Envoy-8FE and the Ingress FIFO fills to a programmable High Watermark, Envoy-8FE’s flow control mechanism is triggered and automatically generates a PAUSE control frame. Envoy-8FE transmits the frame to the remote device and hence backpressures, the remote device. The pause_time value for the generated PAUSE control is programmable. Once the PAUSE control frame is transmitted, Envoy-8FE will re-transmit another PAUSE control frame, every pause_retransmit_time, if a programmable Low Watermark is not reached in the Ingress FIFO. The effect of the re-transmitted PAUSE control frame on the remote device is that, it (remote device) is held in the PAUSE state and does not transmit data frames to Envoy-8FE. The value of pause_retransmit_time is programmable

and is kept by the pause retransmit counter (down counter). In the event the Low Watermark is reached before the pause retransmit counter counts down to zero, Envoy-8FE will transmit a PAUSE control frame with a pause_time value of zero to the remote device held in the pause state. The PAUSE control frame with pause_time value of zero, will initiate resumption of transmission of data frames from the remote device to the Envoy-8FE.

Host initiated PAUSE Frame generation

The Host device can query Envoy-8FE for the status of each Ingress FIFO (per channel). The values for the indication of near full status and near empty status, are programmable. They are the High Watermark and the Low Watermark. The Envoy-8FE provides the host the ability to generate a PAUSE control frame from the Envoy-8FE. This is done by the Host enabling the PAUSE generate configuration bit. This configuration bit gets reset automatically. The Host can generate a PAUSE control frame with a non zero value for pause_time, to the remote device across the link with Envoy-8FE, when the Ingress FIFO's reach the High Watermark and also generate a PAUSE control frame with a null value for pause_time, when the Ingress FIFO reaches the Low Watermark. This allows the Host to control the flow control mechanism.

Pause Frame Control Configuration Bits

n = 0 . . . 7 for channels 0 . . . 7.

Transmit Flow Control Enable - Addr (1000 + (200*n)), Bit 4

Receive Flow Control Enable - Addr (1000 + (200*n)), Bit 5

Pause Time Value (CFPT) - Addr (1100 + (200*n)), Bits 15 to 0

Pause Regen Time (REGEN) - Addr (1101 + (200*)), Bits 15 to 0

Host Initiated Pause Request (PAUSE_REQ) - Addr (1001 + (200*n)), Bit 16

Automatic Pause Frame Generation Enable (Auto_Pause_Enb) - Addr (1001 + (200*n)), Bit 17

Pause Generation High Watermark (PF_SEND_THOLD) - Addr (400B + n), where n = 0 to 3 for channels 0 to 3 and Addr (4012 + n) where n = 0 to 3 for channels 4 to 7, Bit 21 to 6

Pause Generation Low Watermark (PF_NFULL_THOLD) - Addr 400F, 4010, 4016 and 4017 for channels 0 to 7

Note: Please refer to "Memory Information" starting on page 46 for a complete list of configuration bits.

MEMORY INFORMATION

Table 1. Memory Map Overview

Address Range (Hex)	Description
0000-0002	Envoy ID and scratch pad registers
0010-0012	Interrupt handling registers
0020-0022	Transmit and receive buffer status, event and mask registers
1000-1081	SMII 0 configuration and status registers
1100-114F	SMII 0 RMON registers
1200-1281	SMII 1 configuration and status registers
1300-134F	SMII 1 RMON registers
1400-1481	SMII 2 configuration and status registers
1500-154F	SMII 2 RMON registers
1600-1681	SMII 3 configuration and status registers
1700-174F	SMII 3 RMON registers
1800-1881	SMII 4 configuration and status registers
1900-194F	SMII 4 RMON registers
1A00-1A81	SMII 5 configuration and status registers
1B00-1B4F	SMII 5 RMON registers
1C00-1C81	SMII 6 configuration and status registers
1D00-1D4F	SMII 6 RMON registers
1E00-1E81	SMII 7 configuration and status registers
1F00-1F4F	SMII 7 RMON registers
2000-200A	POS-PHY/SPI-3 interface - configuration registers
3000-3014	POS-PHY/SPI-3 interface - status registers
4000-4004	Transmit frame controller 0 - configuration and status registers
4005-4009	Transmit frame controller 1 - configuration and status registers
400A-4010	Receive frame controller 0 - configuration and status registers
4011-4017	Receive frame controller 1 - configuration and status registers

Note: Memory Map Register bit 31 is the MSB and Device pin D31 for the Host Interface (See “D(31-0)” on page 15.) is the LSB.

MEMORY MAPS AND BIT DESCRIPTIONS

Addr (hex)	Mode	Bit range	Default value after reset	Description
0000	RO	15-0	6840	**ENVOY ID**: This field contains the Envoy-8FE part number, TXC-06840.
		31-16	006B	**TXC Mfg. ID:** This field contains the manufacturer identification number for TranSwitch Corp., which is 0x006B.
0001	RO	3-0	0	**Device Growth Field.** This field is 0.
		7-4	0	**Device Mask Level.** This field is 0.
		11-8	0	**Device Version Level.** This field is 0.
		31-12		Reserved
0002	RW	31-0	0	**Scratchpad Memory.** 32-bits of memory storage available to the host processor.
				Interrupt Handler Registers
				Error Event Registers
0010		0	0	***MAC_ERR_0:*** MAC #0 error event register. This bit is set to '1' if the M_MAC_ERR_0 bit is not masked (0= unmasked) AND any bit within Carry Register 1 (0x114C) or Carry Register 2 (0x114D) is set to '1' AND the respective mask bit within mask registers Carry Mask 1 (0x114E) or Carry Mask 2 (0x114F) are not masked (0= unmasked). Note: This bit is cleared on a read, after the appropriate bit in Carry Register 1 or Carry Register 2 is also cleared. See registers 0x114C through 0x114F.
		1	0	***MAC_ERR_1:*** MAC #1 error event register. This bit is set to '1' if the M_MAC_ERR_0 bit is not masked (0= unmasked) AND any bit within Carry Register 1 (0x134C) or Carry Register 2 (0x134D) is set to '1' AND the respective mask bit within mask registers Carry Mask 1 (0x134E) or Carry Mask 2 (0x134F) are not masked (0= unmasked). Note: This bit is cleared on a read, after the appropriate bit in Carry Register 1 or Carry Register 2 is also cleared. See registers 0x134C through 0x134F.
		2	0	***MAC_ERR_2:*** MAC # 2 error event register. This bit is set to '1' if the M_MAC_ERR_0 bit is not masked (0= unmasked) AND any bit within Carry Register 1 (0x154C) or Carry Register 2 (0x154D) is set to '1' AND the respective mask bit within mask registers Carry Mask 1 (0x154E) or Carry Mask 2 (0x154F) are not masked (0= unmasked). Note: This bit is cleared on a read, after the appropriate bit in Carry Register 1 or Carry Register 2 is also cleared. See registers 0x154C through 0x154F.
		3	0	***MAC_ERR_3:*** MAC # 3 error event register. This bit is set to '1' if the M_MAC_ERR_0 bit is not masked (0= unmasked) AND any bit within Carry Register 1 (0x174C) or Carry Register 2 (0x174D) is set to '1' AND the respective mask bit within mask registers Carry Mask 1 (0x174E) or Carry Mask 2 (0x174F) are not masked (0= unmasked). Note: This bit is cleared on a read, after the appropriate bit in Carry Register 1 or Carry Register 2 is also cleared. See registers 0x174C through 0x174F.

Addr (hex)	Mode	Bit range	Default value after reset	Description
0010 (cont.)		4	0	***MAC_ERR_4:*** MAC # 4 error event register. This bit is set to '1' if the M_MAC_ERR_0 bit is not masked (0= unmasked) AND any bit within Carry Register 1 (0x194C) or Carry Register 2 (0x194D) is set to '1' AND the respective mask bit within mask registers Carry Mask 1 (0x194E) or Carry Mask 2 (0x194F) are not masked (0= unmasked). Note: This bit is cleared on a read, after the appropriate bit in Carry Register 1 or Carry Register 2 is also cleared. See registers 0x194C through 0x194F.
		5	0	***MAC_ERR_5:*** MAC # 5 error event register. This bit is set to '1' if the M_MAC_ERR_0 bit is not masked (0= unmasked) AND any bit within Carry Register 1 (0x1B4C) or Carry Register 2 (0x1B4D) is set to '1' AND the respective mask bit within mask registers Carry Mask 1 (0x1B4E) or Carry Mask 2 (0x1B4F) are not masked (0= unmasked). Note: This bit is cleared on a read, after the appropriate bit in Carry Register 1 or Carry Register 2 is also cleared. See registers 0x1B4C through 0x1B4F.
		6	0	***MAC_ERR_6:*** MAC # 6 error event register. This bit is set to '1' if the M_MAC_ERR_0 bit is not masked (0= unmasked) AND any bit within Carry Register 1 (0x1D4C) or Carry Register 2 (0x1D4D) is set to '1' AND the respective mask bit within mask registers Carry Mask 1 (0x1D4E) or Carry Mask 2 (0x1D4F) are not masked (0= unmasked). Note: This bit is cleared on a read, after the appropriate bit in Carry Register 1 or Carry Register 2 is also cleared. See registers 0x1D4C through 0x1D4F.
		7	0	***MAC_ERR_7:*** MAC # 7 error event register. This bit is set to '1' if the M_MAC_ERR_0 bit is not masked (0= unmasked) AND any bit within Carry Register 1 (0x1F4C) or Carry Register 2 (0x1F4D) is set to '1' AND the respective mask bit within mask registers Carry Mask 1 (0x1F4E) or Carry Mask 2 (0x1F4F) are not masked (0= unmasked). Note: This bit is cleared on a read, after the appropriate bit in Carry Register 1 or Carry Register 2 is also cleared. See registers 0x1F4C through 0x1F4F.
		8	0	***RX_PAUSE_FRM_IND_0:*** MAC # 0 Receive Pause Frame Indicator. Clear to '0' on a read. It indicates to the host that an error free, unicast or mutlicast Pause Frame has been received. Note: for this bit to become active, configuration bit TERM_PAUSE_FRM_IND must = '1' (reg. 0x1101, bit 22) AND mask bit (reg. 0x0012, bit 8) must = '0' (unmasked).
		9	0	***RX_PAUSE_FRM_IND_1:*** MAC # 1 Receive Pause Frame Indicator. Clear to '0' on a read. It indicates to the host that an error free, unicast or mutlicast Pause Frame has been received. Note: for this bit to become active, configuration bit TERM_PAUSE_FRM_IND must = '1' (reg. 0x1101, bit 22) AND mask bit (reg. 0x0012, bit 9) must = '0' (unmasked).
		10	0	***RX_PAUSE_FRM_IND_2:*** MAC # 2 Receive Pause Frame Indicator. Clear to '0' on a read. It indicates to the host that an error free, unicast or mutlicast Pause Frame has been received. Note: for this bit to become active, configuration bit TERM_PAUSE_FRM_IND must = '1' (reg. 0x1101, bit 22) AND mask bit (reg. 0x0012, bit 10) must = '0' (unmasked).

Addr (hex)	Mode	Bit range	Default value after reset	Description
0010 (cont.)		11	0	***RX_PAUSE_FRM_IND_3:*** MAC # 3 Receive Pause Frame Indicator. Clear to '0' on a read. It indicates to the host that an error free, unicast or mutlicast Pause Frame has been received. Note: for this bit to become active, configuration bit TERM_PAUSE_FRM_IND must = '1' (reg. 0x1101, bit 22) AND mask bit (reg. 0x0012, bit 11) must = '0' (unmasked).
		12	0	***RX_PAUSE_FRM_IND_4:*** MAC # 4 Receive Pause Frame Indicator. Clear to '0' on a read. It indicates to the host that an error free, unicast or mutlicast Pause Frame has been received. Note: for this bit to become active, configuration bit TERM_PAUSE_FRM_IND must = '1' (reg. 0x1101, bit 22) AND mask bit (reg. 0x0012, bit 12) must = '0' (unmasked).
		13	0	***RX_PAUSE_FRM_IND_5:*** MAC # 5 Receive Pause Frame Indicator. Clear to '0' on a read. It indicates to the host that an error free, unicast or mutlicast Pause Frame has been received. Note: for this bit to become active, configuration bit TERM_PAUSE_FRM_IND must = '1' (reg. 0x1101, bit 22) AND mask bit (reg. 0x0012, bit 13) must = '0' (unmasked).
		14	0	***RX_PAUSE_FRM_IND_6:*** MAC # 6 Receive Pause Frame Indicator. Clear to '0' on a read. It indicates to the host that an error free, unicast or mutlicast Pause Frame has been received. Note: for this bit to become active, configuration bit TERM_PAUSE_FRM_IND must = '1' (reg. 0x1101, bit 22) AND mask bit (reg. 0x0012, bit 14) must = '0' (unmasked).
		15	0	***RX_PAUSE_FRM_IND_7:*** MAC # 7 Receive Pause Frame Indicator. Clear to '0' on a read. It indicates to the host that an error free, unicast or mutlicast Pause Frame has been received. Note: for this bit to become active, configuration bit TERM_PAUSE_FRM_IND must = '1' (reg. 0x1101, bit 22) AND mask bit (reg. 0x0012, bit 15) must = '0' (unmasked).
		16	0	***POS_PHY_ERR:*** POS-PHY/SPI-3 Parity, SOP or TXERR error event register. This bit is set to '1' if the M_POS_PHY_ERR bit is not masked (0= unmasked) AND any bit within the POS-PHY/SPI-3 Event register (0x3013) is set to '1' AND the respective mask bit within the POS-PHY /SPI-3 Mask register (0x3014) is not masked (0= unmasked). Note: This bit is cleared on a read, after the appropriate bit in the POS-PHY/SPI-3 Event register is also cleared. See registers 0x3000 through 0x3014.
		17	0	***BUFFER_ERR:*** Buffer full or near-full error event register. This bit is set to '1' if the M_BUFFER_ERR bit is not masked (0= unmasked) AND any bit within the BUFFER Event register (0x0021) is set to '1' AND the respective mask bit within the BUFFER Mask register (0x0022) is not masked (0= unmasked). Note: This bit is cleared on a read, after the appropriate bit in the BUFFER Event register is also cleared. See registers 0x0021 through 0x0022. 4 bit 17 is set to clear read buffer event register (0x0021), confirm cleaning by reading (0x0010).

Addr (hex)	Mode	Bit range	Default value after reset	Description
0010 (cont.)		18	0	***VCI_ERR:*** VCI bus error event register. Clear to '0' on a READ, set to '1' when an internal bus error occurs within the device. Upon occurrence of this interrupt, the device should be re initialized. Repeated occurrences of this interrupt indicates a device failure.
		31-19		Reserved
0011		0	0	***RX_DROP_FRM_CARRY_0:*** MAC #0 Receive Drop Frame carry counter. It indicates to the host that the DROP_FRAME_COUNT counter in MAC 0 has reached its maximum value. Note: This bit is cleared when the counter DROP_FRAME_COUNT, address 0x1104 is cleared.
		1	0	***RX_DROP_FRM_CARRY_1:*** MAC #1 Receive Drop Frame carry counter. It indicates to the host that the DROP_FRAME_COUNT counter in MAC 1 has reached its maximum value. Note: This bit is cleared when the counter DROP_FRAME_COUNT, address 0x1304 is cleared.
		2	0	***RX_DROP_FRM_CARRY_2:*** MAC #2 Receive Drop Frame carry counter. It indicates to the host that the DROP_FRAME_COUNT counter in MAC 2 has reached its maximum value. Note: This bit is cleared when the counter DROP_FRAME_COUNT, address 0x1504 is cleared.
		3	0	***RX_DROP_FRM_CARRY_3:*** MAC #3 Receive Drop Frame carry counter. It indicates to the host that the DROP_FRAME_COUNT counter in MAC 3 has reached its maximum value. Note: This bit is cleared when the counter DROP_FRAME_COUNT, address 0x1704 is cleared.
		4	0	***RX_DROP_FRM_CARRY_4:*** MAC #4 Receive Drop Frame carry counter. It indicates to the host that the DROP_FRAME_COUNT counter in MAC 4 has reached its maximum value. Note: This bit is cleared when the counter DROP_FRAME_COUNT, address 0x1904 is cleared.
		5	0	***RX_DROP_FRM_CARRY_5:*** MAC #5 Receive Drop Frame carry counter. It indicates to the host that the DROP_FRAME_COUNT counter in MAC 5 has reached its maximum value. Note: This bit is cleared when the counter DROP_FRAME_COUNT, address 0x1B04 is cleared.
		6	0	***RX_DROP_FRM_CARRY_6:*** MAC #6 Receive Drop Frame carry counter. It indicates to the host that the DROP_FRAME_COUNT counter in MAC 6 has reached its maximum value. Note: This bit is cleared when the counter DROP_FRAME_COUNT, address 0x1D04 is cleared.
		7	0	***RX_DROP_FRM_CARRY_7:*** MAC #7 Receive Drop Frame carry counter. It indicates to the host that the DROP_FRAME_COUNT counter in MAC 7 has reached its maximum value. Note: This bit is cleared when the counter DROP_FRAME_COUNT, address 0x1F04 is cleared.
		31-8	0	Reserved

Addr (hex)	Mode	Bit range	Default value after reset	Description
0012	RW			***Error Event Mask Bits*** ***Notes:*** ***1) Register 0x0012 bits (0:7) are the mask bits for bits (0:7) in register 0x0010.*** ***2) Register 0x0012 bits (8:15) are the mask bits for bits (8:15) in register 0x0010.*** ***3) Register 0x0012 bit 16 is the mask bit for bit 16 in register 0x0010.*** ***4) Register 0x0012 bit 17 is the mask bit for bit 17 in register 0x0010.*** ***5) Register 0x0012 bit 18 is the mask bit for bit 18 in register 0x0010.*** ***6) Register 0x0012 bits (19:26) are the mask bits for bits (0:7) in register 0x0011.***
		0	1	***M_MAC_ERR_0:*** Mask bit for MAC_ERR_0. '1' = Mask
		1	1	***M_MAC_ERR_1:*** Mask bit for MAC_ERR_1. '1' = Mask
		2	1	***M_MAC_ERR_2:*** Mask bit for MAC_ERR_2. '1' = Mask
		3	1	***M_MAC_ERR_3:*** Mask bit for MAC_ERR_3. '1' = Mask
		4	1	***M_MAC_ERR_4:*** Mask bit for MAC_ERR_4. '1' = Mask
		5	1	***M_MAC_ERR_5:*** Mask bit for MAC_ERR_5. '1' = Mask
		6	1	***M_MAC_ERR_6:*** Mask bit for MAC_ERR_6. '1' = Mask
		7	1	***M_MAC_ERR_7:*** Mask bit for MAC_ERR_7. '1' = Mask
		8	1	***M_RX_PAUSE_FRM_IND_0:*** Mask bit for RX_Pause_Frm_Ind_0. '1' = Mask
		9		***M_RX_PAUSE_FRM_IND_1:*** Mask bit for RX_Pause_Frm_Ind_1. '1' = Mask
		10	1	***M_RX_PAUSE_FRM_IND_2:*** Mask bit for RX_Pause_Frm_Ind_2. '1' = Mask
		11		***M_RX_PAUSE_FRM_IND_3:*** Mask bit for RX_Pause_Frm_Ind_3. '1' = Mask
		12		***M_RX_PAUSE_FRM_IND_4:*** Mask bit for RX_Pause_Frm_Ind_4. '1' = Mask
		13		***M_RX_PAUSE_FRM_IND_5:*** Mask bit for RX_Pause_Frm_Ind_5. '1' = Mask
		14		***M_RX_PAUSE_FRM_IND_6:*** Mask bit for RX_Pause_Frm_Ind_6. '1' = Mask
		15		***M_RX_PAUSE_FRM_IND_7:*** Mask bit for RX_Pause_Frm_Ind_7. '1' = Mask
		16	1	***M_POS_PHY_ERR:*** Mask bit for POS-PHY I/F Parity, SOP or TXERR errors. '1' = Mask

Addr (hex)	Mode	Bit range	Default value after reset	Description
0012 (cont.)		17	1	***M_BUFFER_ERR:*** Global Mask for Buffer error flags. '1' = Mask. Note: upon reset, register 0x0022 is defaulted to mask all flags.
		18	1	***M_VCI_ERR:*** Global Mask bit for VCI bus error. '1' = Mask.
		19	1	***M_RX_DROP_FRM_CARRY_0:*** Mask bit for RX_Drop_Frm_Carry_0. '1' = Mask.
		20	1	***M_RX_DROP_FRM_CARRY_1:*** Mask bit for RX_Drop_Frm_Carry_1. '1' = Mask.
		21	1	***M_RX_DROP_FRM_CARRY_2:*** Mask bit for RX_Drop_Frm_Carry_2. '1' = Mask.
		22	1	***M_RX_DROP_FRM_CARRY_3:*** Mask bit for RX_Drop_Frm_Carry_3. '1' = Mask.
		23	1	***M_RX_DROP_FRM_CARRY_4:*** Mask bit for RX_Drop_Frm_Carry_4. '1' = Mask.
		24	1	***M_RX_DROP_FRM_CARRY_5:*** Mask bit for RX_Drop_Frm_Carry_5. '1' = Mask.
		25	1	***M_RX_DROP_FRM_CARRY_6:*** Mask bit for RX_Drop_Frm_Carry_6. '1' = Mask.
		26	1	***M_RX_DROP_FRM_CARRY_7:*** Mask bit for RX_Drop_Frm_Carry_7. '1' = Mask.
		31-27		Reserved
				Xmit & Receive Buffers - Status, Event & Mask Registers
				Buffer Status Register: **Note: Bits within register 0x0020 are not latched.**
0020		0	0	***RX_BUF_FS0:*** Receiver Buffer #0 Full Status register. SMII(0)
		1	0	***RX_BUF_NFS0:*** Receiver Buffer #0 Near-Full Status register. SMII(0)
		2	0	***TX_BUF_FS0:*** Transmitter Buffer #0 Full Status register. SMII(0)
		3	0	***TX_BUF_NFS0:*** Transmitter Buffer # 0 Near-Full status register. SMII(0)
		4	0	***RX_BUF_FS1:*** Receiver Buffer #1 Full Status register. SMII(1)
		5	0	***RX_BUF_NFS1:*** Receiver Buffer #1 Near-Full Status register. SMII(1)
		6	0	***TX_BUF_FS1:*** Transmitter Buffer #1 Full Status register. SMII(1)
		7	0	***TX_BUF_NFS1:*** Transmitter Buffer #1 Near-Full Status register. SMII(1)
		8	0	***RX_BUF_FS2:*** Receiver Buffer #2 Full Status register. SMII(2)
		9	0	***RX_BUF_NFS2:*** Receiver Buffer #2 Near-Full Status register. SMII(2)
		10	0	***TX_BUF_FS2:*** Transmitter Buffer #2 Full Status register. SMII(2)
		11	0	***TX_BUF_NFS2:*** Transmitter Buffer #2 Near-Full status register. SMII(2)

Addr (hex)	Mode	Bit range	Default value after reset	Description
0020 (cont.)		12	0	***RX_BUF_FS3:*** Receiver Buffer #3 Full Status register. SMII(3)
		13	0	***RX_BUF_NFS3:*** Receiver Buffer #3 Near-Full status register. SMII(3)
		14	0	***TX_BUF_FS3:*** Transmitter Buffer #3 Full Status register. SMII(3)
		15	0	***TX_BUF_NFS3:*** Transmitter Buffer #3 Near-Full status register. SMII(3)
		16	0	***RX_BUF_FS4:*** Receiver Buffer #4 Full Status register. SMII(4)
		17	0	***RX_BUF_NFS4:*** Receiver Buffer #4 Near-Full Status register. SMII(4)
		18	0	***TX_BUF_FS4:*** Transmitter Buffer #4 Full Status register. SMII(4)
		19	0	***TX_BUF_NFS4:*** Transmitter Buffer #4 Near-Full status register. SMII(4)
		20	0	***RX_BUF_FS5:*** Receiver Buffer #5 Full Status register. SMII(5)
		21	0	***RX_BUF_NFS5:*** Receiver Buffer #5 Near-Full Status register. SMII(5)
		22	0	***TX_BUF_FS5:*** Transmitter Buffer #5 Full Status register. SMII(5)
		23	0	***TX_BUF_NFS5:*** Transmitter Buffer #5 Near-Full Status register. SMII(5)
		24	0	***RX_BUF_FS6:*** Receiver Buffer #6 Full Status register. SMII(6)
		25	0	***RX_BUF_NFS6:*** Receiver Buffer #6 Near-Full Status register. SMII(6)
		26	0	***TX_BUF_FS6:*** Transmitter Buffer #6 Full Status register. SMII(6)
		27	0	***TX_BUF_NFS6:*** Transmitter Buffer #6 Near-Full Status register. SMII(6)
		28	0	***RX_BUF_FS7:*** Receiver Buffer #7 Full Status register. SMII(7)
		29	0	***RX_BUF_NFS7:*** Receiver Buffer #7 Near-Full Status register. SMII(7)
		30	0	***TX_BUF_FS7:*** Transmitter Buffer #7 Full Status register. SMII(7)
		31	0	***TX_BUF_NFS7:*** Transmitter Buffer #7 Near-Full Status register. SMII(7)
				Buffer Event Register: **Note: These bits are latched versions of the bits in register 0x0020.**
0021		0	0	***RX_BUF_FE0:*** Receiver Buffer #0 Full Event register. Clear to '0' on READ, set when flag changes from '0' to 1. SMII(0)
		1	0	***RX_BUF_NFE0:*** Receiver Buffer #0 Near-Full Event register. Clear to '0' on READ, set when flag changes from '0' to '1'. SMII(0)
		2	0	***TX_BUF_FE0:*** Transmitter Buffer #0 Full Event register. Clear to '0' on READ, set when flag changes from '0' to '1'. SMII(0)
		3	0	***TX_BUF_NFE0:*** Transmitter Buffer #0 Near-Full Event register. Clear to '0' on READ, set when flag changes from '0' to '1'. SMII(0)
		4	0	***RX_BUF_FE1:*** Receiver Buffer #1 Full Event register. Clear to '0' on READ, set when flag changes from '0' to '1'. SMII(1)
		5	0	***RX_BUF_NFE1:*** Receiver Buffer #1 Near-Full Event register. Clear to '0' on READ, set when flag changes from '0' to '1'. SMII(1)
		6	0	***TX_BUF_FE1:*** Transmitter Buffer #1 Full Event register. Clear to '0' on READ, set when flag changes from '0' to '1'. SMII(1)
		7	0	***TX_BUF_NFE1:*** Transmitter Buffer #1 Near-Full Event register. Clear to '0' on READ, set when flag changes from '0' to '1'. SMII(1)

Addr (hex)	Mode	Bit range	Default value after reset	Description
0021 (cont.)		8	0	***RX_BUF_FE2:*** Receiver Buffer #2 Full Event register. Clear to '0' on READ, set when flag changes from '0' to '1'. SMII(2)
		9	0	***RX_BUF_NFE2:*** Receiver Buffer #2 Near-Full Event register. Clear to '0' on READ, set when flag changes from '0' to '1'. SMII(2)
		10	0	***TX_BUF_FE2:*** Transmitter Buffer #2 Full Event register. Clear to '0' on READ, set when flag changes from '0' to '1'. SMII(2)
		11	0	***TX_BUF_NFE2:*** Transmitter Buffer #2 Near-Full Event register. Clear to '0' on READ, set when flag changes from '0' to '1'. SMII(2)
		12	0	***RX_BUF_FE3:*** Receiver Buffer #3 Full Event register. Clear to '0' on READ, set when flag changes from '0' to '1'. SMII(3)
		13	0	***RX_BUF_NFE3:*** Receiver Buffer #3 Near-Full Event register. Clear to '0' on READ, set when flag changes from '0' to '1'. SMII(3)
		14	0	***TX_BUF_FE3:*** Transmitter Buffer #3 Full Event register. Clear to '0' on READ, set when flag changes from '0' to '1'. SMII(3)
		15	0	***TX_BUF_NFE3:*** Transmitter Buffer #3 Near-Full Event register. Clear to '0' on READ, set when flag changes from '0' to '1'. SMII(3)
		16	0	***RX_BUF_FE4:*** Receiver Buffer #4 Full Event register. Clear to '0' on READ, set when flag changes from '0' to '1'. SMII(4)
		17	0	***RX_BUF_NFE4:*** Receiver Buffer #4 Near-Full Event register. Clear to '0' on READ, set when flag changes from '0' to '1'. SMII(4)
		18	0	***TX_BUF_FE4:*** Transmitter Buffer #4 Full Event register. Clear to '0' on READ, set when flag changes from '0' to '1'. SMII(4)
		19	0	***TX_BUF_NFE4:*** Transmitter Buffer #4 Near-Full Event register. Clear to '0' on READ, set when flag changes from '0' to '1'. SMII(4)
		20	0	***RX_BUF_FE5:*** Receiver Buffer #5 Full Event register. Clear to '0' on READ, set when flag changes from '0' to '1'. SMII(5)
		21	0	***RX_BUF_NFE5:*** Receiver Buffer #5 Near-Full Event register. Clear to '0' on READ, set when flag changes from '0' to '1'. SMII(5)
		22	0	***TX_BUF_FE5:*** Transmitter Buffer #5 Full Event register. Clear to '0' on READ, set when flag changes from '0' to '1'. SMII(5)
		23	0	***TX_BUF_NFE5:*** Transmitter Buffer #5 Near-Full Event register. Clear to '0' on READ, set when flag changes from '0' to '1'. SMII(5)
		24	0	***RX_BUF_FE6:*** Receiver Buffer #6 Full Event register. Clear to '0' on READ, set when flag changes from '0' to '1'. SMII(6)
		25	0	***RX_BUF_NFE6:*** Receiver Buffer #6 Near-Full Event register. Clear to '0' on READ, set when flag changes from '0' to '1'. SMII(6)
		26	0	***TX_BUF_FE6:*** Transmitter Buffer #6 Full Event register. Clear to '0' on READ, set when flag changes from '0' to '1'. SMII(6)
		27	0	***TX_BUF_NFE6:*** Transmitter Buffer #6 Near-Full Event register. Clear to '0' on READ, set when flag changes from '0' to '1'. SMII(6)
		28	0	***RX_BUF_FE7:*** Receiver Buffer #7 Full Event register. Clear to '0' on READ, set when flag changes from '0' to '1'. SMII(7)

Addr (hex)	Mode	Bit range	Default value after reset	Description
0021 (cont.)		29	0	***RX_BUF_NFE7:*** Receiver Buffer #7 Near-Full Event register. Clear to '0' on READ, set when flag changes from '0' to '1'. SMII(7)
		30	0	***TX_BUF_FE7:*** Transmitter Buffer #7 Full Event register. Clear to '0' on READ, set when flag changes from '0' to '1'. SMII(7)
		31	0	***TX_BUF_NFE7:*** Transmitter Buffer #7 Near-Full Event register. Clear to '0' on READ, set when flag changes from '0' to '1'. SMII(7)
				Buffer Mask Register: **Note: These are the mask bits for register 0x0021.**
0022		0	1	***M_RX_BUF_FE0:*** Mask RX_BUF_FE0. '1' = Mask. SMII(0)
		1	1	***M_RX_BUF_NFE0:*** Mask RX_BUF_NFE0. '1' = Mask. SMII(0)
		2	1	***M_TX_BUF_FE0:*** Mask TX_BUF_FE0. '1' = Mask. SMII(0)
		3	1	***M_TX_BUF_NFE0:*** Mask TX_BUF_NFE0. '1' = Mask. SMII(0)
		4	1	***M_RX_BUF_FE1:*** Mask RX_BUF_FE1. '1' = Mask. SMII(1)
		5	1	***M_RX_BUF_NFE1:*** Mask RX_BUF_NFE1. '1' = Mask. SMII(1)
		6	1	***M_TX_BUF_FE1:*** Mask TX_BUF_FE1. '1' = Mask. SMII(1)
		7	1	***M_TX_BUF_NFE1:*** Mask TX_BUF_NFE1. '1' = Mask. SMII(1)
		8	1	***M_RX_BUF_FE2:*** Mask RX_BUF_FE2. '1' = Mask. SMII(2)
		9	1	***M_RX_BUF_NFE2:*** Mask RX_BUF_NFE2. '1' = Mask. SMII(2)
		10	1	***M_TX_BUF_FE2:*** Mask TX_BUF_FE2. '1' = Mask. SMII(2)
		11	1	***M_TX_BUF_NFE2:*** Mask TX_BUF_NFE2. '1' = Mask. SMII(2)
		12	1	***M_RX_BUF_FE3:*** Mask RX_BUF_FE3. '1' = Mask. SMII(3)
		13	1	***M_RX_BUF_NFE3:*** Mask RX_BUF_NFE3. '1' = Mask. SMII(3)
		14	1	***M_TX_BUF_FE3:*** Mask TX_BUF_FE3. '1' = Mask. SMII(3)
		15	1	***M_TX_BUF_NFE3:*** Mask TX_BUF_NFE3. '1' = Mask. SMII(3)
		16	1	***M_RX_BUF_FE4:*** Mask RX_BUF_FE4. '1' = Mask. SMII(4)
		17	1	***M_RX_BUF_NFE4:*** Mask RX_BUF_NFE4. '1' = Mask. SMII(4)
		18	1	***M_TX_BUF_FE4:*** Mask TX_BUF_FE4. '1' = Mask. SMII(4)
		19	1	***M_TX_BUF_NFE4:*** Mask TX_BUF_NFE4. '1' = Mask. SMII(4)
		20	1	***M_RX_BUF_FE5:*** Mask RX_BUF_FE5. '1' = Mask. SMII(5)
		21	1	***M_RX_BUF_NFE5:*** Mask RX_BUF_NFE5. '1' = Mask. SMII(5)
		22	1	***M_TX_BUF_FE5:*** Mask TX_BUF_FE5. '1' = Mask. SMII(5)
		23	1	***M_TX_BUF_NFE5:*** Mask TX_BUF_NFE5. '1' = Mask. SMII(5)

Addr (hex)	Mode	Bit range	Default value after reset	Description
0022 (cont.)		24	1	***M_RX_BUF_FE6:*** Mask RX_BUF_FE6. '1' = Mask. SMII(6)
		25	1	***M_RX_BUF_NFE6:*** Mask RX_BUF_NFE6. '1' = Mask. SMII(6)
		26	1	***M_TX_BUF_FE6:*** Mask TX_BUF_FE6. '1' = Mask. SMII(6)
		27	1	***M_TX_BUF_NFE6:*** Mask TX_BUF_NFE6. '1' = Mask. SMII(6)
		28	1	***M_RX_BUF_FE7:*** Mask RX_BUF_FE7. '1' = Mask. SMII(7)
		29	1	***M_RX_BUF_NFE7:*** Mask RX_BUF_NFE7. '1' = Mask. SMII(7)
		30	1	***M_TX_BUF_FE7:*** Mask TX_BUF_FE7. '1' = Mask. SMII(7)
		31	1	***M_TX_BUF_NFE7:*** Mask TX_BUF_NFE7. '1' = Mask. SMII(7)
				SMII n Configuration and Status Registers. **Note:** Register addresses 0x1000 through 0x1081 & 0x1100 through 0x114F (shown below) are for MAC 0. An identical set of registers exist for MAC's 1 through 7. For the address ranges of these registers, see Table 1, "Memory Map Overview" starting on page 46.
1000	RW			**SMII Port 0 Configuration Register #1**
		0	0	**TRANSMIT ENABLE:** When = '1', the MAC will be allowed to transmit frames to the system. When = '0', transmission of frames will be prevented.
		1		**SYNCHRONIZED TRANSMIT:** When = '1', Transmit Enable is synchronized to the transmit stream.
		2	0	**RECEIVE ENABLE:** When = '1', the MAC is allowed to receive frames from the PHY. When = '0', the reception of frames is prevented.
		3		**SYNCHRONIZED RECEIVE ENABLE:** Receive Enable synchronized to the receive stream.
		4	0	**TRANSMIT FLOW CONTROL ENABLE:** When = '1', allows the Transmit MAC Control to send PAUSE Flow Control frames when requested by the system. When = '0', prevents the transmit MAC Control from sending Flow Control frames.
		5	0	**RECEIVE FLOW CONTROL ENABLE:** Setting this bit will cause the Receive MAC Control to detect, and act on, PAUSE Flow Control frames. Clearing this bit causes the Receive MAC Control to ignore PAUSE Flow Control frames.
		7-6		Reserved
		8	0	**LOOPBACK MODE:** When = '1', the MAC will "Loopback" all data received from the Egress FIFO controller, to the Ingress FIFO controller, i.e., this is a POS-PHY/SPI-3 interface loopback. When = '0', results in normal operation.
		15-9		Reserved
		16	0	**RESET TX FUNCTION:** When = '1', the Transmit Function block is placed in reset. This block performs the frame transmission protocol.
		17	0	**RESET RX FUNCTION:** When = '1', the Receive Function block is placed in reset. This block performs the receive frame protocol.

Addr (hex)	Mode	Bit range	Default value after reset	Description
1000 (cont.)		18	0	**RESET TX MAC CONTROL:** When = '1', the Transmit MAC Control block is placed in reset. This block multiplexes data and Control frame transfers. It also responds to XOFF PAUSE Control frames.
		19	0	**RESET RX MAC CONTROL:** When = '1', the Receive MAC Control block is placed in reset. This block detects Control frames and contains the pause timers.
		30	0	**SIMULATION RESET:** When = '1', this bit will reset those registers, such as the random back-off timer, which are not controlled by normal resets (for simulation only).
		31	1	**SOFT RESET:** Setting this bit will put all modules within the MAC in reset, except the Host Interface. The Host Interface is reset via HRST. Soft Reset should be performed in the absence of traffic.
1001	RW	**SMII Port 0 Configuration Register #2**		
		0	1	**FULL-DUPLEX:** When = '1', the MAC will be configured to operate in Full-Duplex mode. When = '0', the MAC will operate in Half-Duplex mode.
		1	0	**CRC ENABLE:** When = '1', the MAC will append a CRC on all frames. When = '0', frames presented to the MAC must have a valid length and contain a valid CRC. If the configuration bit PAD/CRC ENABLE or the per-frame PAD/CRC ENABLE is set, CRC ENABLE is ignored.
		2	0	**PAD / CRC ENABLE:** When = '1', the MAC will pad all short frames and append a CRC to every frame whether or not padding was required. When = '0', frames presented to the MAC must have a valid length and contain a CRC.
		3		Reserved
		4	0	**LENGTH FIELD CHECKING:** When = '1', the MAC will check the frame's length field to ensure it matches the actual data field length. When = '0', no length field checking is performed.
		5	0	**HUGE FRAME ENABLE:** When = '1', allows frames longer than the MAXIMUM FRAME LENGTH to be transmitted and received. When = '0', the MAC will limit the length of frames to the MAXIMUM FRAME LENGTH value.
		7-6		Reserved
		9-8	0	**INTERFACE MODE:** This field determines the type of interface the MAC is connected to. These 2-bits **must** be set to "01" to select the SMII interface.
		11-10		Reserved
		15-12	0x7	**PREAMBLE LENGTH:** This field determines the length of the preamble field of the frame, in bytes.
		31-16		Reserved

Addr (hex)	Mode	Bit range	Default value after reset	Description
1002	RW			**IPG/IFG SETTINGS**
		6-0	0x60	**BACK-TO-BACK INTER-FRAME-GAP:** This is a programmable field representing the IPG between Back-to-Back Frames. This is the IPG parameter used exclusively in Full-Duplex mode and in Half-Duplex mode when two transmit frames are sent back-to-back. Set this field to the number of bits of IPG desired. The default setting of 0x60 (96d).
		7		Reserved
		15-8	0x50	**MINIMUM IFG ENFORCEMENT:** This is a programmable field representing the minimum number of bits of IFG to enforce between frames. A frame whose IFG is less than that programmed is dropped. The default setting of 0x50 (80d) represents half of the nominal minimum IFG which is 160-bits.
		22-16	0x60	**NON-BACK-TO-BACK INTER-FRAME-GAP PART 2:** This is a programmable field representing the Non-Back-to-Back Inter-Frame-Gap in bits. Default value is 0x60 (96d). Note: For an IPG length of 96 and a 2/3 ration, the values 0x20 and 0x7c are required in the IPG1 and IPG2 locations.
		23		Reserved
		30-24	0x40	**NON-BACK-TO-BACK INTER-FRAME-GAP PART 1:** This is a programmable field representing the optional Carrier Sense window referenced in IEEE 802.3/4.2.3.2.1 'Carrier Deference'. If carrier is detected during the timing of IPGR1, the MAC defers to carrier. If, however, carrier becomes active after IPGR1, the MAC continues timing IPGR2 and transmits, knowingly causing a collision, thus ensuring fair access to medium. Its range of values is 0x0 to IPGR2. Default value is 0x40 (64d) which follows the two-thirds/one-thirds guideline. Note: For an IPG length of 96 and a 2/3 ration, the values 0x20 and 0x7c are required in the IPG1 and IPG2 locations.
		31		Reserved

Addr (hex)	Mode	Bit range	Default value after reset	Description
1003	RW			**HALF_DUPLEX REGISTER**
		9-0	0x37	**COLLISION WINDOW:** This is a programmable field representing the slot time or collision window during which collisions occur in properly configured networks. Since the collision window starts at the beginning of transmission, the preamble and SFD are included. Its default value of 0x37 (55d) corresponds to the count of frame bytes at the end of the window.
		11-10		Reserved
		15-12	0xF	**RETRANSMISSION MAXIMUM:** This is a programmable field specifying the number of retransmission attempts following a collision before aborting the frame due to excessive collisions. The Standard specifies the attempt limit to be 0xF (15d).
		16		Reserved
		17	0	**NO BACKOFF:** When = '1', configures the TX MAC to immediately re-transmit following a collision. When = '0', causes the TX MAC to follow the binary exponential back off rule.
		18	0	**BACKPRESSURE NO BACKOFF:** When = '1', the TX MAC is configured to immediately re-transmit, following a collision, during backpressure operation. When = '0', causes the TX MAC to follow the binary exponential back off rule.
		19	0	**ALTERNATE BINARY EXPONENTIAL BACKOFF ENABLE:** When = '1', the TX MAC is configured to use the ALTERNATE BINARY EXPONENTIAL BACKOFF TRUNCATION setting instead of the 802.3 standard tenth collision. The Standard specifies that any collision after the tenth uses "210 - 1" as the maximum backoff time. When = '0', causes the TX MAC to follow the standard binary exponential back off rule.
		23-20	0xA	**ALTERNATE BINARY EXPONENTIAL BACKOFF TRUNCATION:** This field is used when ALTERNATE BINARY EXPONENTIAL BACKOFF ENABLE is set. The value programmed is substituted for the Ethernet standard value of ten.
		31-24		Reserved
1004	RW			**MAXIMUM FRAME LENGTH REGISTER**
		15-0	0x0600	**MAXIMUM FRAME LENGTH:** This field resets to 0x0600 (1536d), which represents the maximum frame size in both the transmit and receive directions.
		31-16		Reserved
1005 to 1006		31-0	0	Reserved

<table>
<tr><th>Addr (hex)</th><th>Mode</th><th>Bit range</th><th>Default value after reset</th><th>Description</th></tr>
<tr><td>1007</td><td>RW</td><td colspan="2"></td><td>TEST REGISTER</td></tr>
<tr><td></td><td></td><td>0</td><td>0</td><td>SHORTCUT SLOT TIME: This bit allows the slot time counter to expire regardless of the current count. This bit is for testing purposes only.</td></tr>
<tr><td></td><td></td><td>1</td><td>0</td><td>TEST PAUSE: When = ‘1’, allows the MAC to be paused via the host interface. For testing purposes only.</td></tr>
<tr><td></td><td></td><td>2</td><td>0</td><td>REGISTERED TRANSMIT FLOW ENABLE: Register Transmit Half-Duplex Flow Enable, active high assertion.</td></tr>
<tr><td></td><td></td><td>3</td><td>0</td><td>MAXIMUM BACKOFF: When = ‘1’, the MAC is configured to backoff for the maximum possible length of time. This test bit is used to predict backoff times in Half-Duplex mode.</td></tr>
<tr><td></td><td></td><td>31-4</td><td></td><td>Reserved</td></tr>
<tr><td>1008</td><td>RW</td><td colspan="2"></td><td>MII MGMT: CONFIGURATION REGISTER</td></tr>
<tr><td></td><td></td><td>2-0</td><td>0</td><td>MGMT CLOCK SELECT: This field determines the clock frequency of the Mgmt Clock (MDC). Consult Table below - MGMT Clock Select Encoding on how to program this field.
MGMT Clock Select Encoding
<table>
<tr><th>Mgmt Clock Select bits</th><th>2</th><th>1</th><th>0</th></tr>
<tr><td>PCLK divided by 8</td><td>0</td><td>1</td><td>1</td></tr>
<tr><td>PCLK divided by 10</td><td>1</td><td>0</td><td>0</td></tr>
<tr><td>PCLK divided by 14</td><td>1</td><td>0</td><td>1</td></tr>
<tr><td>PCLK divided by 20</td><td>1</td><td>1</td><td>0</td></tr>
<tr><td>PCLK divided by 28</td><td>1</td><td>1</td><td>1</td></tr>
</table></td></tr>
<tr><td></td><td></td><td>3</td><td></td><td>Reserved</td></tr>
<tr><td></td><td></td><td>4</td><td>0</td><td>PREAMBLE SUPPRESSION: When = ‘1’, the MII MGMT will suppress preamble generation and reduce the Mgmt cycle from 64 clocks to 32 clocks. This is in accordance with IEEE 802.3/22.2.4.4.2. Clearing this bit causes the MII MGMT to perform Mgmt read/write cycles with the 32 clocks of preamble.</td></tr>
<tr><td></td><td></td><td>5</td><td>0</td><td>PHY INCREMENT: This bit is used only if bit 1 (SCAN CYCLE) of MAC register 0x09, is set to ‘1’. If SCAN CYCLE = ‘1’ AND PHY INCREMENT = ‘0’, then burst reads of the same PHY address will be performed. If SCAN CYCLE = ‘1’ AND PHY INCREMENT = ‘1’, then burst reads of incremental PHY address will be performed.</td></tr>
<tr><td></td><td></td><td>30-4</td><td></td><td>Reserved</td></tr>
<tr><td></td><td></td><td>31</td><td>0</td><td>RESET MII MGMT: When = ‘1’, will force the reset of the MII MGMT. When = ‘0’, allows the MII MGMT to perform Mgmt read/write cycles as requested via the Host Interface.</td></tr>
</table>

Addr (hex)	Mode	Bit range	Default value after reset	Description
1009	RW			**MII MGMT: COMMAND REGISTER**
		0	0	**READ CYCLE:** This bit causes the MII Management to perform a single Read cycle. The Read data is returned in Register 0xC (MII Mgmt Read Data).
		1	0	**SCAN CYCLE:** When = '1', causes the MII Management to perform Read cycles continuously. This is useful for monitoring Link Fail, for example. Note: refer to MAC register 0x1008, bit 5, for additional information on this feature.
		31-2		Reserved
100A	RW			**MII MGMT: ADDRESS REGISTER**
		4-0	0	**REGISTER ADDRESS:** This field represents the 5-bit Register Address field of Mgmt cycles. Up to 32 registers can be accessed.
		7-5		Reserved
		12-8	0	**PHY ADDRESS:** This field represents the 5-bit PHY Address field of Mgmt cycles. Up to 31 PHYs can be addressed (0 is reserved).
		31-13		Reserved
100B	WO			**MII MGMT: CONTROL**
		15-0	0	**MII MGMT CONTROL (PHY Control):** When written, an MII Mgmt write cycle is performed using the 16-bit data and the pre-configured PHY and Register addresses from the MII Mgmt Register (0x0A).
		31-16		Reserved
100C	RO			**MII MGMT: STATUS**
		15-0	0	**MII MGMT STATUS (PHY STATUS):** Following an MII Mgmt Read Cycle, the 16-bit data can be read from this location.
		31-16		Reserved
100D	RO			**MII MGMT: INDICATORS**
		0	0	**BUSY:** When '1' is returned, indicates MII Mgmt block is currently performing an MII Mgmt Read or Write cycle.
		1	0	**SCANNING:** When '1' is returned, indicates a scan operation (continuous MII Mgmt Read cycles) is in progress.
		2	0	**NOT VALID:** When '1' is returned, indicates MII Mgmt Read cycle has not completed and the Read Data is not yet valid.
		31-3		Reserved
100E	RW			**INTERFACE CONTROL REGISTER**
		0	0	**ENABLE JABBER PROTECTION:** This bit enables the Jabber Protection logic within the MAC. Jabber is the condition where a transmitter is stuck on for longer than 50ms preventing other stations from transmitting.
		6-1		Reserved

Addr (hex)	Mode	Bit range	Default value after reset	Description
100E (cont.)		7	0	**RESET GPSI:** When = '1' resets the internal logic which converts MII nibble streams to the serial bit stream of ENDEC PHYs. When = '0', normal operation is enabled.
		8	0	**DISABLE LINK FAIL:** When = '1', the 330ms Link Fail timer is disabled allowing for shorter simulations. Removes the 330 mS link-up time before reception of streams is allowed. When = '0', normal operation is enabled.
		9	0	**NO CIPHER:** When = '1' (enabled), the raw transmit 5B symbols are transmitted without ciphering. When = '0' (disabled), normal ciphering occurs.
		10	0	**FORCE QUIET:** When = '1', transmit data is quieted which allows the contents of the cipher to be output. When = '0', normal operation is enabled.
		14-11		Reserved
		15	0	**RESET PE100X:** When = '1', resets the PE100X module within the MAC, which contains the 4B/5B symbol encipher/decipher logic. When = '0', normal operation is enabled.
		16	0	**SPEED:** This bit configures the PERMII Reduced MII module with the current operating speed. When = '1', 100 Mb/s mode selected. When = '0', 10 Mb/s mode selected.
		22-17		Reserved
		23	0	**RESET PERMII:** When = '1', resets the PERMII Reduced MII module. When = '0', normal operation is enabled.
		24	1	**PHY MODE:** When = '1', the SMII Serial MII module is configured to be in PHY Mode. Link characteristics are taken directly from the RX segments supplied by the PHY. When = '0', the SMII is configured to be in MAC to MAC mode. In this configuration, the Serial MII module reverts to pre-defined settings of 100 Mb/s, Full-Duplex.
		30-25		Reserved
		31	0	**RESET SMII:** When = '1', resets the SMII Serial MII module. When = '0', normal operation is enabled.

Addr (hex)	Mode	Bit range	Default value after reset	Description
100F	RO			**INTERFACE STATUS REGISTER**
		0		**JABBER:** When = '1', the MAC has detected a Jabber condition. When = '0', the MAC has not detected a Jabber condition. This bit latches high.
		1		**SQE ERROR:** When = '1', the MAC has detected an SQE Error. When = '0', the MAC module has not detected an SQE Error. This bit latches high.
		2		**LOSS OF CARRIER**: When = '1', the MAC has detected a Loss of Carrier. When = '0', the MAC has not detected a Loss of Carrier. This bit latches high.
		3		**LINK FAIL:** When = '1', the MAC has not detected Signal Detect for at least 330 mS. When = '0', the MAC has detected Signal Detect for longer than 330 mS.
		4		**SPEED:** When = '1', the Serial MII PHY is operating at 100 Mb/s mode. When = '0', the Serial MII PHY is operating at 10 Mb/s.
		5		**FULL DUPLEX:** When = '1', the Serial MII PHY is operating in Full-Duplex mode. When = '0', the Serial MII PHY is operating in Half-Duplex mode.
		6		**LINK OK:** When = '1', the Serial MII PHY has detected a valid link. When = '0', the Serial MII PHY has not detected a valid link.
		7		**JABBER:** When = '1', the Serial MII PHY has detected a jabber condition on the link. When = '0', the Serial MII PHY has not detected a jabber condition.
		8		**CLASH:** When = '1', the Serial MII module is in MAC to MAC mode with the partner in 10 Mb/s and/or Half-Duplex mode indicative of a configuration error. When read as a '0', the Serial MII module is either in PHY mode or in a properly configured MAC to MAC mode.
		9	0	**EXCESS DEFER:** This bit sets when the MAC excessively defers a transmission. It clears when read. This bit latches high.
		31-10		Reserved
1010	RW			**STATION ADDRESS REGISTER, PART 1**
		7-0	0	**STATION ADDRESS, 4th octet**: This field holds the fourth octet of the station address. The fourth octet is stored in 7:0 and defaults to '0x00'.
		15-8	0	**STATION ADDRESS, 3rd octet:** This field holds the third octet of the station address. The third octet is stored in 15:8 and defaults to '0x00'.
		23-16	0	**STATION ADDRESS, 2nd octet:** This field holds the second octet of the station address. The second octet is stored in 23:16 and defaults to '0x00'.
		31-24	0	**STATION ADDRESS, 1st octet:** This field holds the first octet of the station address. The first octet is stored in 31:24 and defaults to '0x00'.

Addr (hex)	Mode	Bit range	Default value after reset	Description
1011	RW			**STATION ADDRESS REGISTER, PART 2**
		15-0		Reserved
		23-16	0	**STATION ADDRESS, 6th octet:** This field holds the sixth octet of the station address. The sixth octet is stored in 23:16 and defaults to '0x00'.
		31-24	0	**STATION ADDRESS, 5th octet:** This field holds the fifth octet of the station address. The fifth octet is stored in 31:24 and defaults to '0x00'.
1012-107F		31-0		Reserved Registers
				SMII n Configuration & RMON Registers
1100		15-0	0	***CFPT:*** Control Frame parameter to set the Pause Time parameter. 16-bit field containing the Pause Time value.
		31-16	0	***CFEP:*** Control Frame Extended Parameter. This extended parameters may contain additional information such as VLAN and/or priority information as contained in IEEE 802.1p.
1101	RW	15-0	0	***REGEN:*** The interval in slot time, to sense the Buffer_Near_Full flag after an automatic PAUSE frame is generated.
		16	0	***PAUSE_REQ:*** Control bit use to request the transmission of a Pause Frame. When this bit is set to '1', it will issue a request to send a Pause Frame, with the pause time parameter provided by the previous registers (CPFT & CFEP). This bit can only be set to a '1' by the host when the register bit PF_Ready_P = '1'. Once written, this bit will self-clear when the operation is complete.
		17	0	***AUTO_PAUSE_ENB:*** When = '0', enables automatic PAUSE frame generation based on the receive buffer going near-full. When = '1', disables it. When operating in SMII Half-Duplex mode, '0' allows THDF to be used automatically when the receive buffer is full, to indicate that backpressure should be applied to the transmitting media. When = '1', disables THDF.
		18	1	***STEN:*** Statistics Enable. When = '1', enables internal statistics counters to update. '0' will disable counter updates.
		19	1	***AUTOZ:*** Automatically Zero Addressed Statistics Counter values of the MAC. When = '1', the addressed counter value is zeroed on a host read, When = '0', the user must write the addressed counter zero after a host read.
		20	0	***CLRCNT:*** Clear All Statistics Counters in the MAC. When = '1', reset all statistics counters.
		21	1	Reserved
		22	0	***TERM_PAUSE_FRM_IND:*** Terminate Pause Frame indication. '0' -Don't indicate that MAC has acted on a PAUSE Frame, '1' - Set event to indicate that MAC acted on a Pause frame. Note: The MAC only reacts to Pause Frames when bit 5 of reg. 0x1000 (Receive Flow control enable) is '1'. Also, to discard this type of frame, you must enable the PAUSE_FILTER (bit 27 of this register).

Addr (hex)	Mode	Bit range	Default value after reset	Description
1101 (cont.)		23	0	***DISC_TRUNC_FRM:*** Discard Truncated frames. '0' = Don't discard the frame if it is truncated, '1' = Discard.
		24	0	***DISC_LENGTH_FLD:*** Discard unmatched length field. When = '0', don't discard the frame if the frame's length field does not match the actual data field length, when = '1', discard the frame.
		25	0	***DISC_CRC_FLD:*** Discard unmatched CRC field. When = '0', don't discard the frame if it has a CRC error, when = '1', discard the frame. Note: when operating in SMII Half-Duplex mode, this bit **MUST** be set to '1' to insure that the device does not receive frames of less than 64 bytes during a "collision" condition. 64 bytes is the minimum frame size specified for Envoy-8FE.
		26	0	***DISC_RX_ERR:*** Discard received frame with RXERR. When = '0', don't discard the frame if it has an RX error, when = '1', discard the frame.
		27	0	***PAUSE_FILTER:*** Active high signal to filter out PAUSE frames with DA matching the SA register (addresses 0x1010 & 0x1011) or if the DA is equal to the Multicast address.
		29-28	0	***I_THOLD:*** "00"= 256 bytes, "01" = 512 bytes, "10" = 768 bytes, "11" = 1550 bytes. This threshold setting is used to decide whether to discard a current errored frame, or pass it along but indicate that the frame contains errors.
		31-30		Reserved
1102		0	0	***STREAM_ENB0:*** Streaming enable bit for Port 0. When = '0', streaming is disabled, when = '1', streaming is enabled. Note: this register must be set with the same value as STREAM_ENB0 in the Receive Frame Buffer Controller (register 0x400B, bit 0).
		1	0	***RX_SA_FILTER_ENB:*** Receive Station Address Filter enable. When = '1', frames will be filtered out if the DA field does not match the programmed Station Address (SA) field programmed in addresses 0x1010 and 0x1011. When = '0', no filtering is performed.
		2	0	***TX_SA_SUB_ENB:*** Transmitter Station Address Substitution Enable. When = '1', substitute the outgoing SA field in the Ethernet header with the programmed station address in the MAC (addresses 0x1010 and 0x1011).
		4-3	0	***RESET_CONTROL:*** "00" = Clear to '0' during host writes, "10" = Clear on Read, "x1" = Reset the Drop_Frame_Count to zero and auto-change this bit to '0'.
		31-5		Reserved
1103	RO	0	0	***PF_READY_P:*** Transmitting Pause Control Frame. When = '0', this bit indicates that the Pause Control frame transmission is still in progress. During this time, the host is not allowed to write to the Pause_Request bit register. The host must read this bit as a '1' before attempting to write a Pause_Request. It is cleared to '0' after the Pause_Req bit has been set to '1', by the host.

Addr (hex)	Mode	Bit range	Default value after reset	Description
1103 (cont.)		1	0	***SMII STATUS:*** This read-only bit indicates the MAC operating mode for this port. This bit will always return a '0', indicating SMII mode.
		31-2		Reserved
1104		31-0	0	***DROP_FRAME_COUNT:*** This roll-over counter is incremented by the dropping of a received Frame. When this register reaches its maximum value, it will send a CARRY signal to the respective "event" register. This register can be cleared on a read or on a write, depending on the setting of the RESET_CNT bits. Note: This counter only increments for: (a) Frames that have SA not equal to DA, (b) are not Pause Frames, unicast, multicast, or broadcast frames and (c) are error-free. In addition, bit RX_SA_FILTER_ENB must = '1' for this counter to operate.
1105 to 111F				Reserved
				RMON Transmit and Receive Counters
1120	RW	24:0		***TR64:*** Transmit and Receive 64 Byte Frame Counter. Incremented for each good or bad frame transmitted and received which is 64 bytes in length inclusive (excluding framing Bits but including FCS bytes).
1121	RW	24:0		***TR127:*** Transmit and Receive 65 to 127 Byte Frame Counter. Incremented for each good or bad frame transmitted and received which is 65 to 127 bytes in length inclusive (excluding framing Bits but including FCS bytes).
1122	RW	24:0		***TR255:*** Transmit and Receive 128 to 255 Byte Frame Counter. Incremented for each good or bad frame transmitted and received which is 128 to 255 bytes in length inclusive (excluding framing Bits but including FCS bytes).
1123	RW	24:0		***TR511:*** Transmit and Receive 256 to 511 Byte Frame Counter. Incremented for each good or bad frame transmitted and received which is 256 to 511 bytes in length inclusive (excluding framing Bits but including FCS bytes).
1124	RW	24:0		***TR1K:*** Transmit and Receive 512 to 1023 Byte Frame Counter. Incremented for each good or bad frame transmitted and received which is 512 to 1023 bytes in length inclusive (excluding framing Bits but including FCS bytes).
1125	RW	24:0		***TRMAX:*** Transmit and Receive 1024 to 1518 Byte Frame Counter. Incremented for each good or bad frame transmitted and received which is 1024 to 1518 bytes in length inclusive (excluding framing Bits but including FCS bytes).
1126	RW	24:0		***TRMGV:*** Transmit and Receive 1519 to 1522 Byte Good VLAN Frame Counter. Incremented for each good or bad frame transmitted and received which is 1519 to 1522 bytes in length inclusive (excluding framing Bits but including FCS bytes).

Addr (hex)	Mode	Bit range	Default value after reset	Description
				RMON Receive Counters
1127	RW	30:0		***RBYT:*** Receive Byte Counter. The Statistic Counter register is incremented by the byte count of frames received with 0 to 1518 bytes, including those in bad frames, excluding framing Bits but including FCS bytes.
1128	RW	24:0		***RPKT:*** Receive Frame Counter. Incremented for each frame received frame (including bad frames, all Unicast, Broadcast, and Multicast frames).
1129	RW	15:0		***RFCS:*** Receive FCS Error Counter. Incremented for each frame received that has a integral 64 to 1518 length and contains a Frame Check Sequence error.
112A	RW	24:0		***RMCA:*** Receive Multicast Frame Counter. Incremented for each Multicast good frame of lengths 64 to 1518 (non VLAN) or 1522 (VLAN) excluding Broadcast frames. This does not look at range/length errors.
112B	RW	24:0		***RBCA:*** Receive Broadcast Frame Counter. Incremented for each Broadcast good frame of lengths 64 to 1518 (non VLAN) or 1522 (VLAN) excluding Multicast frames. This does not look at range/length errors.
112C	RW	15:0		***RXCF:*** Receive Control Frame Frame Counter. Incremented for each MAC Control frame received (PAUSE and Unsupported)
112D	RW	15:0		***RXPF:*** Receive PAUSE Frame Frame Counter. Incremented each time a valid PAUSE MAC Control frame is received.
112E	RW	15:0		***RXUO:*** Receive Unknown OPcode Counter. Incremented each time a MAC Control Frame is received which contains an opcode other than a PAUSE.
112F	RW	15:0		***RALN:*** Receive Alignment Error Counter. Incremented for each received frame from 64 to 1518 (non VLAN) or 1522 (VLAN) which contains an invalid FCS and is not an integral number of bytes.
1130	RW	15:0		***RFLR:*** Receive Frame Length Error Counter. Incremented for each frame received in which the 802.3 length field did not match the number of data bytes actually received (46 - 1500 bytes). The counter is not incremented if the length field is not a valid 802.3 length, such as an EtherType value.
1131	RW	15:0		***RCDE:*** Receive Code Error Counter. Incremented each time a valid carrier was present and at least one invalid data symbol was detected.
1132	RW	15:0		***RCSE:*** Receive Carrier Sense Error Counter. Incremented each time a false carrier is detected during idle, as defined by a 1 on RX_ER and an '0xE' on RXD. The event is reported along with the statistics generated on the next received frame. Only one false carrier condition can be detected and logged between frames.
1133	RW	15:0		***RUND:*** Receive Undersize Frame Counter. Incremented each time a frame is received which is less than 64 bytes in length and contains a valid FCS and were otherwise well formed. This does not look at Range Length errors. Note: This count includes late collisions and excessive collisions.

Addr (hex)	Mode	Bit range	Default value after reset	Description
1134	RW	15:0		***ROVR:*** Receive Oversize Frame Counter. Incremented each time a frame is received which exceeded 1518 (non VLAN) or 1522 (VLAN) and contains a valid FCS and were otherwise well formed. This does not look at Range Length errors.
1135	RW	15:0		***RFRG:*** Receive Fragments Counter. Incremented for each frame received which is less than 64 bytes in length and contains an invalid FCS, includes integral and non-integral lengths.
1136	RW	15:0		***RJBR:*** Receive Jabber Counter. Incremented for frames received which exceed 1518 (non VLAN) or 1522 (VLAN) bytes and contains an invalid FCS, includes alignment errors.
1137	RW	15:0		***RDRP:*** Receive Dropped Frames Counter. Incremented for frames received which are streamed to system but are later dropped due to lack of system resources.
				RMON Transmit Counters
1138	RW	30:0		***TBYT:*** Transmit Byte Counter. Incremented by the number of bytes that were put on the wire including fragments of frames that were involved with collisions. This count does not include preamble/SFD or jam bytes.
1139	RW	24:0		***TPKT:*** Transmit Frame Counter. Incremented for each transmitted frame (including bad frames, excessive deferred frames, excessive collision frames, late collision frames, all Unicast, Broadcast, and Multicast frames).
113A	RW	24:0		***TMCA:*** Transmit Multicast Frame Counter. Incremented for each Multicast valid frame transmitted (excluding Broadcast frames).
113B	RW	24:0		***TBCA:*** Transmit Broadcast Frame Counter. Incremented for each Broadcast frame transmitted (excluding Multicast frames).
113C	RW	15:0		***TXPF:*** Transmit PAUSE Control Frame Counter. Incremented each time a valid PAUSE MAC Control frame is transmitted.
113D	RW	12:0		***TDFR:*** Transmit Deferral Frame Counter.
113E	RW	12:0		***TEDF:*** Transmit Excessive Deferral Frame Counter.
113F	RW	12:0		***TSCL:*** Transmit Single Collision Frame Counter.
1140	RW	12:0		***TMCL:*** Transmit Multiple Collisions Frame Counter.
1141	RW	12:0		***TLCL:*** Transmit Late Collision Frame Counter.
1142	RW	12:0		***TXCL:*** Transmit Excessive Collision Frame Counter.
1143	RW	12:0		***TNCL:*** Transmit Total Collision Counter.
1144	RW	15:0		Reserved
1145	RW	15:0		***TDRP:*** Transmit Drop Frame Counter.
1146	RW	13:0		***TJBR:*** Transmit Jabber Frame Counter. Incremented for each oversized transmitted frame with an incorrect FCS value.
1147	RW	13:0		***TFCS:*** Transmit FCS Error Counter. Incremented for every valid sized frame with an incorrect FCS value.
1148	RW	13:0		***TXCF:*** Transmit Control Frame Counter. Incremented for every valid size frame with a Type Field signifying a Control frame.

Addr (hex)	Mode	Bit range	Default value after reset	Description
1149	RW	13:0		***TOVR:*** Transmit Oversize Frame Counter. Incremented for each oversized transmitted frame with an correct FCS value.
114A	RW	13:0		***TUND:*** Transmit Undersize Frame Counter. Incremented for every frame less then 64 bytes, with a correct FCS value.
114B	RW	13:0		***TFRG:*** Transmit Fragments Frame Counter. Incremented for every frame less then 64 bytes, with a incorrect FCS value.
				General MAC Registers
114C	RW	31:25 & 16:0	0	***CAR1:*** Carry Register #1. Host needs to clear this register. To clear an active bit, the host needs to write a '1' to the bit that is set to '1'. Note: Bits (31:25) are the carry bits for roll-over counters at addresses 0x1120 through 0x1126; bits (16:0) are the carry bits for roll-over counters at registers 0x1127 through 0x1137.
114D	RW	19:0	0	***CAR2:*** Carry Register #2. Host needs to clear this register. To clear an active bit, the host needs to write a '1' to the bit that is set to '1'. Note: Bits (19:0) are the carry bits for roll-over counters at addresses 0x1138 through 0x114B.
114E	RW	31:25 & 16:0	1	***CAM1:*** Carry Mask register #1. '1' = mask. Note: Bits (31:25) are the mask bits for roll-over interrupts from registers 0x1120 through 0x1126; bits (16:0) are the mask bits for roll-over interrupts from registers 0x1127 through 0x1137.
114F	RW	19:0	1	***CAM2:*** Carry Mask register #2. '1' = mask. Note: Bits (19:0) are the mask bits for counter roll-over interrupts from registers 0x1138 through 0x114B.
				POS-PHY 2/SPI-3 Port Configurations:
				Port 0 Configuration:
2000	RW	0	0	***EN-RX:*** Enable receiver. '1' = enable, '0' = disable. SPI-3 only.
		1	0	***EN-TX:*** Enable transmitter. '1' = enable, '0' = disable. SPI-3 only.
		2	0	***SOP_CNT_EN:*** SOP counter enable. '1' = enable, '0' = disable. POS-PHY Level 2 & SPI-3.
		3	0	***TERR_CNT_EN:*** TERR counter enable. '1' = enable, '0' = disable. POS-PHY Level 2 & SPI-3.
		10-4	0	***NF_THOLD:*** Near-Full High Threshold. The valid values are 0 to 63 (Threshold = 0 to 63) and 64 (Threshold = 256). Note: These 7-bits **must** be programmed with the same values as bits(9:3) in register EFIFO_TH0, address 0x4001. POS-PHY Level 2 & SPI-3.
		31-11		Reserved
				Port 1 Configuration:
2001	RW	0	0	***EN-RX:*** Enable receiver. '1' = enable, '0' = disable. SPI-3 only.
		1	0	***EN-TX:*** Enable transmitter. '1' = enable, '0' = disable. SPI-3 only.
		2	0	***SOP_CNT_EN:*** SOP counter enable. '1' = enable, '0' = disable. POS-PHY Level 2 & SPI-3.

Addr (hex)	Mode	Bit range	Default value after reset	Description
2001 (cont.)		3	0	***TERR_CNT_EN:*** TERR counter enable. '1' = enable, '0' = disable. POS-PHY Level 2 & SPI-3.
		10-4	0	***NF_THOLD:*** Near-Full High Threshold. The valid values are 0 to 63 (Threshold = 0 to 63) and 64 (Threshold = 256). Note: These 7-bits **must** be programmed with the same values as bits(9:3) in register EFIFO_TH1, address 0x4002. POS-PHY Level 2 & SPI-3.
		31-11		Reserved
				Port 2 Configuration
2002	RW	0	0	***EN-RX:*** Enable receiver. '1' = enable, '0' = disable. SPI-3 only.
		1	0	***EN-TX:*** Enable transmitter. '1' = enable, '0' = disable. SPI-3 only.
		2	0	***SOP_CNT_EN:*** SOP counter enable. '1' = enable, '0' = disable. POS-PHY Level 2 & SPI-3.
		3	0	***TERR_CNT_EN:*** TERR counter enable. '1' = enable, '0' = disable. POS-PHY Level 2 & SPI-3.
		10-4	0	***NF_THOLD:*** Near-Full High Threshold. The valid values are 0 to 63 (Threshold = 0 to 63) and 64 (Threshold = 256). Note: These 7-bits **must** be programmed with the same values as bits(9:3) in register EFIFO_TH2, address 0x4003. POS-PHY Level 2 & SPI-3.
		31-11		Reserved
				Port 3 Configuration
2003	RW	0	0	***EN-RX:*** Enable receiver. '1' = enable, '0' = disable. SPI-3 only.
		1	0	***EN-TX:*** Enable transmitter. '1' = enable, '0' = disable. SPI-3 only.
		2	0	***SOP_CNT_EN:*** SOP counter enable. '1' = enable, '0' = disable. POS-PHY Level 2 & SPI-3.
		3	0	***TERR_CNT_EN:*** TERR counter enable. '1' = enable, '0' = disable. POS-PHY Level 2 & SPI-3.
		10-4	0	***NF_THOLD:*** Near-Full High Threshold. The valid values are 0 to 63 (Threshold = 0 to 63) and 64 (Threshold = 256). Note: These 7-bits **must** be programmed with the same values as bits(9:3) in register EFIFO_TH3, address 0x4004. POS-PHY Level 2 & SPI-SPI-3.
		31-11		Reserved
				Port 4 Configuration
2004	RW	0	0	***EN-RX:*** Enable receiver. '1' = enable, '0' = disable. SPI-3 only.
		1	0	***EN-TX:*** Enable transmitter. '1' = enable, '0' = disable. SPI-3 only.
		2	0	***SOP_CNT_EN:*** SOP counter enable. '1' = enable, '0' = disable. POS-PHY Level 2 & SPI-3.
		3	0	***TERR_CNT_EN:*** TERR counter enable. '1' = enable, '0' = disable. POS-PHY Level 2 & SPI-3.

Addr (hex)	Mode	Bit range	Default value after reset	Description
2004 (cont.)		10-4	0	***NF_THOLD:*** Near-Full High Threshold. The valid values are 0 to 63 (Threshold = 0 to 63) and 64 (Threshold = 256). Note: These 7-bits **must** be programmed with the same values as bits(9:3) in register EFIFO_TH4, address 0x4006. POS-PHY Level 2 & SPI-3.
		31-11		Reserved
				Port 5 Configuration
2005		0	0	***EN-RX:*** Enable receiver. '1' = enable, '0' = disable. SPI-3 only.
		1	0	***EN-TX:*** Enable transmitter. '1' = enable, '0' = disable. SPI-3 only.
		2	0	***SOP_CNT_EN:*** SOP counter enable. '1' = enable, '0' = disable. POS-PHY Level 2 & SPI-3.
		3	0	***TERR_CNT_EN:*** TERR counter enable. '1' = enable, '0' = disable. POS-PHY Level 2 & SPI-3.
		10-4	0	***NF_THOLD:*** Near-Full High Threshold. The valid values are 0 to 63 (Threshold = 0 to 63) and 64 (Threshold = 256). Note: These 7-bits **must** be programmed with the same values as bits(9:3) in register EFIFO_TH5, address 0x4007. POS-PHY Level 2 & SPI-3.
		31-11		Reserved
				Port 6 Configuration
2006		0	0	***EN-RX:*** Enable receiver. '1' = enable, '0' = disable. SPI-3 only.
		1	0	***EN-TX:*** Enable transmitter. '1' = enable, '0' = disable. SPI-3 only.
		2	0	***SOP_CNT_EN:*** SOP counter enable. '1' = enable, '0' = disable. POS-PHY Level 2 & SPI-3.
		3	0	***TERR_CNT_EN:*** TERR counter enable. '1' = enable, '0' = disable. POS-PHY Level 2 & SPI-3.
		10-4	0	***NF_THOLD:*** Near-Full High Threshold. The valid values are 0 to 63 (Threshold = 0 to 63) and 64 (Threshold = 256). Note: These 7-bits **must** be programmed with the same values as bits(9:3) in register EFIFO_TH6, address 0x4008. POS-PHY Level 2 & SPI-3.
		31-11		Reserved
				Port 7 Configuration
2007		0	0	***EN-RX:*** Enable receiver. '1' = enable, '0' = disable. SPI-3 only.
		1	0	***EN-TX:*** Enable transmitter. '1' = enable, '0' = disable. SPI-3 only.
		2	0	***SOP_CNT_EN:*** SOP counter enable. '1' = enable, '0' = disable. POS-PHY Level 2 & SPI-3.
		3	0	***TERR_CNT_EN:*** TERR counter enable. '1' = enable, '0' = disable. POS-PHY Level 2 & SPI-3.
		10-4	0	***NF_THOLD:*** Near-Full High Threshold. The valid values are 0 to 63 (Threshold = 0 to 63) and 64 (Threshold = 256). The valid values are 0 to 64 (Threshold = 0 to 64) and 127 (Threshold = 256). Note: These 7-bits **must** be programmed with the same values as bits(9:3) in register EFIFO_TH7, address 0x4009. POS-PHY Level 2 & SPI-3.

Addr (hex)	Mode	Bit range	Default value after reset	Description
2007 (cont.)		31-11		Reserved
				POS-PHY 2/SPI-3 Global Registers
				Note: Control bit L2_L3 must = '1' to select SPI-3 mode, '0' to select Level 2 mode.
2008	RW	0	0	***L2_L3:*** POS-PHY 2/SPI-3 level select. '1' = SPI-3 mode, '0' = Level 2 mode.
		2-1	0	***RESET_CNTS:*** Global register. "00" = Clear on write, host processor needs to write the counter to zeros, "10" = Clear on read, "x1" = Reset all counters to zero, and auto-change these bits to "x0". Note: During Device Driver development, it is important to remember that when performing a "Reset all counters" ("x1"), the default mode will be the previous configuration. You can do "Reset all counters" and defaults back to Clear on write or Clear on read, depending on bit 2 of this register. "Reset all counters" only changes bit 1 back to '0'.
		3	0	***P_CNT_EN:*** Global register to enable the parity counters and SPI-3 parity detection. '0' = Disable, '1' = Enable.
		4	0	***TPA_SEL:*** Transmit Packet Available Signal Select. '1' = DTPA, '0' = PTPA.
		7-5	0	***L2_PARITY_MODE:*** POS-PHY L2 parity mode. 3-bit field that determines the type of parity generation for the Egress interface and the type of parity checking for the Ingress interface. The MSB high allow the generation of the parity signal for the Egress interface and the checking (generation of ParityError) for the Ingress interface. The 2 LSB bits are defined as follows. '00' = odd parity over data only, '01' = odd parity over data and control signals, '10' = even parity over data only, '11' = even parity over data and control signals. For the Ingress interface, (16-bit mode), the parity is over ITD, ITSOP, ITEOP and ITMS. The same rule is used for the egress interface.
		8	0	***SPI-3_PARITY_MODE:*** SPI-3 parity mode. '0' = odd parity, '1' = even parity.
		9	0	***SPI-3_PAUSE_CYCLE_TIME:*** SPI-3 pause cycle time. Receive direction to control the programmable pause to be 0 or 2 cycles between transfers. '0' = 0 cycles between transfers, '1' = 2 cycles between transfers.
		17-10	0	***SPI-3_ITADDR_OFFSET:*** SPI-3 Ingress base address offset. Base address corresponds to SPI-3 PHY Port 0, Port 1 will be the base address + 1 and so on.
		25-18	0	***SPI-3_ETADDR_OFFSET:*** SPI-3 Egress base address offset. Base address corresponds to SPI-3 PHY Port 0, Port 1 will be the base address + 1 and so on.

Addr (hex)	Mode	Bit range	Default value after reset	Description
2008 (cont.)		26	0	***SPI-3_FRS_ENB***: 0 - feature disabled (PHY reselection will be done when an EOP is sent for the current transfer), 1 - feature enabled (PHY selection will be done when n bytes have been sent where n depends on the value of the 2-bits stored in SPI-3_FRS_Size. The SPI-3 egress will send the number of bytes as indicated in SPI-3_FRS_Size (or until EOP is reached, whichever comes first) before selecting a new port. Of course, the round robin algorithm applies. This feature is decoupled from the streaming feature.
		28-27	0	***SPI-3_FRS_SIZE:*** Only used if SPI-3_Frs_Enb = 1. 00 - 256 bytes, 01 - 512 bytes, 10 - 768 bytes, 11 - 1550 bytes.
		31-29		Reserved
				POS-PHY Level 2 Configuration Registers (Note: control bit L2_L3 must = '0')
2009		0	0	***L2_IT_STATUS:*** Set to '1' when the ingress interface is online, '0' when off-line. This is a read only bit.
		1	0	***L2_ET_STATUS:*** Set to '1' when the egress interface is online, '0' when off-line. This is a read only bit.
		2	0	***L2_IT_ONLINE:*** Active high control bit allowing frames to be accepted from the Level 2 Ingress. When = '0', all bidirectional pins are tristate.
		3	0	***L2_ET_ONLINE:*** Active high control bit allowing frames to be accepted from the Level 2 Egress. When = '0', all bidirectional pins are tristate.
		4	0	***L2_IT_RESET:*** Active high control bit allowing a reset of the Ingress interface. This means that the current transfer is stopped and that the Ingress interface is ready to be selected. No mechanism exists to complete the current frame transfer.
		5	0	***L2_ET_RESET:*** Active high control bit allowing a reset of the Egress interface. This means that the current transfer is stopped and that the Egress interface is ready to be selected. No mechanism exists to complete the current frame transfer.
		10-6	0	***L2_IT_ADDR_OFFSET:*** Level 2 address offset for the Ingress interface. Note: The address increment is not a roll-over. Therefore, you should limit the value of this field to a maximum of 0x1E, not 0x1F.
		15-11	0	***L2_ET_ADDR_OFFSET:*** Level 2 address offset for the Egress interface. Note: The address increment is not a roll-over. Therefore, you should limit the value of this field to a maximum of 1E-(n-1) where n=2 to 8 (PHYs enabled), not 0x1F.
		23-16	0	***L2_IT_PHY_ENABLE_LIST:*** Each PHY listed from 7-0 contains its own 1 bit Ingress PHY enable. '1' in a particular bit means that a particular PHY is enable. When a PHY is disable, there is no response when polled by the Link Layer device.
		31-24	0	***L2_ET_PHY_ENABLE_LIST:*** Each PHY listed from 7-0 contains its own 1-bit Egress PHY enable. '1' in a particular bit means that a PHY is enable. When a PHY is disable, there is no response when polled by the Link Layer device.

Addr (hex)	Mode	Bit range	Default value after reset	Description
				POS-PHY 2/SPI-3 Error Counters/Event Registers/Masks
				Error Counters ***Note:*** Registers 0x3000 through 0x3013 can be programmed to: Clear on READ, clear on WRITE or RESET counter. The mode of clearing is determined by bits 2:1 in register RESET_CNTS, address 0x2008.
3000		31-0	0	***SOP_COUNT_0:*** 32-bit register containing the SOP error count for POS-PHY port #0. This is a roll-over counter.
3001		31-0	0	***SOP_COUNT_1:*** 32-bit register containing the SOP error count for POS-PHY port #1. This is a roll-over counter.
3002		31-0	0	***SOP_COUNT_2:*** 32-bit register containing the SOP error count for POS-PHY port #2. This is a roll-over counter.
3003		31-0	0	***SOP_COUNT_3:*** 32-bit register containing the SOP error count for POS-PHY port #3. This is a roll-over counter.
3004		31-0	0	***SOP_COUNT_4:*** 32-bit register containing the SOP error count for POS-PHY port #4. This is a roll-over counter.
3005		31-0	0	***SOP_COUNT_5:*** 32-bit register containing the SOP error count for POS-PHY port #5. This is a roll-over counter.
3006		31-0	0	***SOP_COUNT_6:*** 32-bit register containing the SOP error count for POS-PHY port #6. This is a roll-over counter.
3007		31-0	0	***SOP_COUNT_7:*** 32-bit register containing the SOP error count for POS-PHY port #7. This is a roll-over counter.
3008		31-0	0	***TERR_COUNT_0:*** 32-bit register containing the Transmit Error (TERR) count for POS-PHY port #0. This is a roll-over counter.
3009		31-0	0	***TERR_COUNT_1:*** 32-bit register containing the TERR error count for POS-PHY port #1. This is a roll-over counter.
300A		31-0	0	***TERR_COUNT_2:*** 32-bit register containing the TERR error count for POS-PHY port #2. This is a roll-over counter.
300B		31-0	0	***TERR_COUNT_3:*** 32-bit register containing the TERR error count for POS-PHY port #3. This is a roll-over counter.
300C		31-0	0	***TERR_COUNT_4:*** 32-bit register containing the TERR error count for POS-PHY port #4. This is a roll-over counter.
300D		31-0	0	***TERR_COUNT_5:*** 32-bit register containing the TERR error count for POS-PHY port #5. This is a roll-over counter.
300E		31-0	0	***TERR_COUNT_6:*** 32-bit register containing the TERR error count for POS-PHY port #6. This is a roll-over counter.
300F		31-0	0	***TERR_COUNT_7:*** 32-bit register containing the TERR error count for POS-PHY port #7. This is a roll-over counter.
3010		31-0	0	***PARITY_COUNT:*** 32-bit register containing the POS-PHY/SPI-3 I/F parity error count. This is a roll-over counter.
3011		31-0	0	***RUN_BYTE_COUNT:*** 32-bit register containing the POS-PHY/SPI-3 I/F missing SOP error count. This is a roll-over counter.

Addr (hex)	Mode	Bit range	Default value after reset	Description
3012		31-0	0	***TX_OVERFLOW_COUNT:*** 32-bit register containing the POS-PHY/SPI-3 I/F Transmit OverFlow error count. This is a roll-over counter.
				Event Register
3013		0	0	***SOP_EVENT_0:*** SOP_count_0 event register. Clear to '0' on READ, set to '1' when counter (address 0x3000) rolls-over.
		1	0	***TERR_EVENT_0:*** TERR_count_0 event register. Clear to '0' on READ, set to '1' when counter (address 0x3008) rolls-over.
		2	0	***SOP_EVENT_1:*** SOP_count_1 event register. Clear to '0' on READ, set to '1' when counter (address 0x3001) rolls-over.
		3	0	***TERR_EVENT_1:*** TERR_count_1 event register. Clear to '0' on READ, set to '1' when counter (address 0x3009) rolls-over.
		4	0	***SOP_EVENT_2:*** SOP_count_2 event register. Clear to '0' on READ, set to '1' when counter (address 0x3002) rolls-over.
		5	0	***TERR_EVENT_2:*** TERR_count_2 event register. Clear to '0' on READ, set to '1' when counter (address 0x300A) rolls-over.
		6	0	***SOP_EVENT_3:*** SOP_count_3 event register. Clear to '0' on a read, set to '1' when counter (address 0x3003) rolls-over.
		7	0	***TERR_EVENT_3:*** TERR_count_3 event register. Clear to '0' on a read, set to '1' when counter (address 0x300B) rolls-over.
		8	0	***SOP_EVENT_4:*** SOP_count_4 event register. Clear to '0' on a read, set to '1' when counter (address 0x3004) rolls-over.
		9	0	***TERR_EVENT_4:*** TERR_count_4 event register. Clear to '0' on a read, set to '1' when counter (address 0x300C) rolls-over.
		10	0	***SOP_EVENT_5:*** SOP_count_5 event register. Clear to '0' on a read, set to '1' when counter (address 0x3005) rolls-over.
		11	0	***TERR_EVENT_5:*** TERR_count_5 event register. Clear to '0' on a read, set to '1' when counter (address 0x300D) rolls-over.
		12	0	***SOP_EVENT_6:*** SOP_count_6 event register. Clear to '0' on a read, set to '1' when counter (address 0x3006) rolls-over.
		13	0	***TERR_EVENT_6:*** TERR_count_6 event register. Clear to '0' on a read, set to '1' when counter (address 0x300E) rolls-over.
		14	0	***SOP_EVENT_7:*** SOP_count_7 event register. Clear to '0' on a read, set to '1' when counter (address 0x3007) rolls-over.
		15	0	***TERR_EVENT_7:*** TERR_count_7 event register. Clear to '0' on a read, set to '1' when counter (address 0x300F) rolls-over.
		16	0	***PARITY_EVENT:*** POS-PHY/SPI-3 I/F Parity error roll-over counter. Clear to '0' on a read, set to '1' when counter (address 0x3010) rolls-over.
		17	0	***RUN_BYTE_EVENT:*** POS-PHY/SPI-3 I/F Run Byte error roll-over counter. Clear to '0' on a read, set to '1' when counter (address 0x3011) rolls-over.

Addr (hex)	Mode	Bit range	Default value after reset	Description
3013 (cont.)		18	0	***TX_OVERFLOW_EVENT:*** POS-PHY/SPI-3 I/F Transmit Overflow error roll-over counter. Clear to '0' on a read, set to '1' when counter (address 0x3012) rolls-over.
		31-19		Reserved
				Masks **Note:** Register 0x3014 bits (0:18) are the mask bits for bits (0:18) in register 0x3013.
3014		0	1	***M_SOP_0:*** SOP_count_0 mask register. '1' = Mask.
		1	1	***M_TERR_0:*** TERR_count_0 mask register. '1' = Mask.
		2	1	***M_SOP_1:*** SOP_count_1 mask register. '1' = Mask.
		3	1	***M_TERR_1:*** TERR_count_1 mask register. '1' = Mask.
		4	1	***M_SOP_2:*** SOP_count_2 mask register. '1' = Mask.
		5	1	***M_TERR_2:*** TERR_count_2 mask register. '1' = Mask.
		6	1	***M_SOP_3:*** SOP_count_3 mask register. '1' = Mask.
		7	1	***M_TERR_3:*** TERR_count_3 mask register. '1' = Mask.
		8	1	***M_SOP_4:*** SOP_count_4 mask register. '1' = Mask.
		9	1	***M_TERR_4:*** TERR_count_4 mask register. '1' = Mask.
		10	1	***M_SOP_5:*** SOP_count_5 mask register. '1' = Mask.
		11	1	***M_TERR_5:*** TERR_count_5 mask register. '1' = Mask.
		12	1	***M_SOP_6:*** SOP_count_6 mask register. '1' = Mask.
		13	1	***M_TERR_6:*** TERR_count_6 mask register. '1' = Mask.
		14	1	***M_SOP_7:*** SOP_count_7 mask register. '1' = Mask.
		15	1	***M_TERR_7:*** TERR_count_7 mask register. '1' = Mask.
		16	1	***M_PARITY:*** POS-PHY parity errors mask. '1' = Mask.
		17	1	***M_RUN_BYTE:*** PPIB "run byte" errors mask. '1' = Mask.
		18	1	***M_TX_OVERFLOW:*** POS-PHY 2/SPI-3 I/F Transmitter Over-Flow mask. '1' = Mask.
		31-19		Reserved
				Transmit Frame Buffer Controller 0 (Ports 0 to 3)
4000		31-0		Reserved
4001	RW	2-0	0	**RESERVED_LOW:** These 3 bits **must** be set to '0' for proper device operation.
		9-3	0	***EFIFO_TH0:*** These 7-bits indirectly control the Near-Full high threshold at the write side. (NF_HIGH_THOLD) for Port 0. The valid values are 0 to 63 (Threshold = 0 to 63) and 64 (Threshold = 256). Note: This register **must** be programmed with the same value as Port 0 NF_THOLD, address 0x2000.
		31-10		Reserved

Addr (hex)	Mode	Bit range	Default value after reset	Description
4002	RW	2-0	0	**RESERVED_LOW:** These 3 bits **must** be set to '0' for proper device operation.
		9-3	0	***EFIFO_TH1:*** These 7-bits indirectly control the near-full high threshold at the write side. (NF_HIGH_THOLD) for Port 1. The valid values are 0 to 63 (Threshold = 0 to 63) and 64 (Threshold = 256). Note: This register **must** be programmed with the same value as Port 1 NF_THOLD, address 0x2001.
		31-10		Reserved
4003	RW	2-0	0	**RESERVED_LOW:** These 3 bits **must** be set to '0' for proper device operation.
		9-3	0	***EFIFO_TH2:*** These 7-bits indirectly control the Near-Full high threshold at the write side. (NF_HIGH_THOLD) for Port 2. The valid values are 0 to 63 (Threshold = 0 to 63) and 64 (Threshold = 256). Note: This register **must** be programmed with the same value as Port 2 NF_THOLD, address 0x2002.
		31-10		Reserved
4004	RW	2-0	0	**RESERVED_LOW:** These 3 bits **must** be set to '0' for proper device operation.
		9-3	0	***EFIFO_TH3:*** These 7-bits indirectly control the Near-Full high threshold at the write side. (NF_HIGH_THOLD) for Port 3. The valid values are 0 to 63 (Threshold = 0 to 63) and 64 (Threshold = 256). Note: This register **must** be programmed with the same value as Port 3 NF_THOLD, address 0x2003.
		31-10		Reserved
Transmit Frame Buffer Controller 1 (Ports 4 to 7)				
4005		31-0		Reserved
4006	RW	2-0	0	**RESERVED_LOW:** These 3 bits **must** be set to '0' for proper device operation.
		9-3	0	***EFIFO_TH4:*** These 7-bits indirectly control the Near-Full high threshold at the write side. (NF_HIGH_THOLD) for Port 4. The valid values are 0 to 63 (Threshold = 0 to 63) and 64 (Threshold = 256). Note: This register **must** be programmed with the same value as Port 4 NF_THOLD, address 0x2004.
		31-10		Reserved
4007	RW	2-0	0	**RESERVED_LOW:** These 3 bits **must** be set to '0' for proper device operation.
		9-3	0	***EFIFO_TH5:*** These 7-bits indirectly control the Near-Full high threshold at the write side. (NF_HIGH_THOLD) for Port 5. The valid values are 0 to 63 (Threshold = 0 to 63) and 64 (Threshold = 256). Note: This register **must** be programmed with the same value as Port 5 NF_THOLD, address 0x2005.
		31-10		Reserved

Addr (hex)	Mode	Bit range	Default value after reset	Description
4008	RW	2-0	0	**RESERVED_LOW:** These 3 bits **must** be set to '0' for proper device operation.
		9-3	0	***EFIFO_TH6:*** These 7-bits indirectly control the Near-Full high threshold at the write side. (NF_HIGH_THOLD) for Port 6. The valid values are 0 to 63 (Threshold = 0 to 63) and 64 (Threshold = 256). Note: This register **must** be programmed with the same value as Port 6 NF_THOLD, address 0x2006.
		31-10		Reserved
4009	RW	2-0	0	**RESERVED_LOW:** These 3 bits **must** be set to '0' for proper device operation.
		9-3	0	***EFIFO_TH7:*** These 7-bits indirectly control the Near-Full high threshold at the write side. (NF_HIGH_THOLD) for Port 7. The valid values are 0 to 63 (Threshold = 0 to 63) and 64 (Threshold = 256). Note: This register **must** be programmed with the same value as Port 7 NF_THOLD, address 0x2007.
		31-10		Reserved
				Receive Frame Buffer Controller 0 (Ports 0 to 3)
400A		31-0		Reserved
400B	RW	0	0	***STREAM_ENB0:*** Streaming enable bit for Port 0. '0' = streaming disable, '1' = streaming enable. Note: this bit **must** be set with the same value as register 0x1102, bit 0.
		2-1	0	***THOLD0:*** Stream threshold for Port 0. ("00" = 256 bytes, "01" = 512 bytes, "10" = 768 bytes, "11" = 1550 bytes). These bits are valid only when STREAM_ENB='1'. Note: This register **must** be set with the same value as register ITHOLD, address 0x1101.
		5-3	0	***IFIFO_TH0:*** These 3-bits indirectly control the near empty low threshold at the read side (NE_LOW_THOLD) for Port 0.
		21-6	0	***PF_SEND_THOLD0:*** These 16-bits directly control the Near-Full high threshold (NF_HIGH_THOLD) for Port 0.
		31-22		Reserved
400C	RW	0	0	***STREAM_ENB1:*** Streaming enable bit for Port 1. '0' = streaming disable, '1' = streaming enable. Note: this bit **must** be set with the same value as register 0x1302, bit 0.
		2-1	0	***THOLD1:*** Stream threshold for Port 1. ("00" = 256 bytes, "01" = 512 bytes, "10" = 768 bytes, "11" = 1550 bytes). These bits are valid only when STREAM_ENB='1'. Note: This register **must** be set with the same value as register ITHOLD, address 0x1301.
		5-3	0	***IFIFO_TH1:*** These 3-bits indirectly control the near empty low threshold at the read side (NE_LOW_THOLD) for Port 1.
		21-6	0	***PF_SEND_THOLD1:*** These 16-bits directly control the Near-Full High threshold (NF_HIGH_THOLD) for Port 1.
		31-22		Reserved

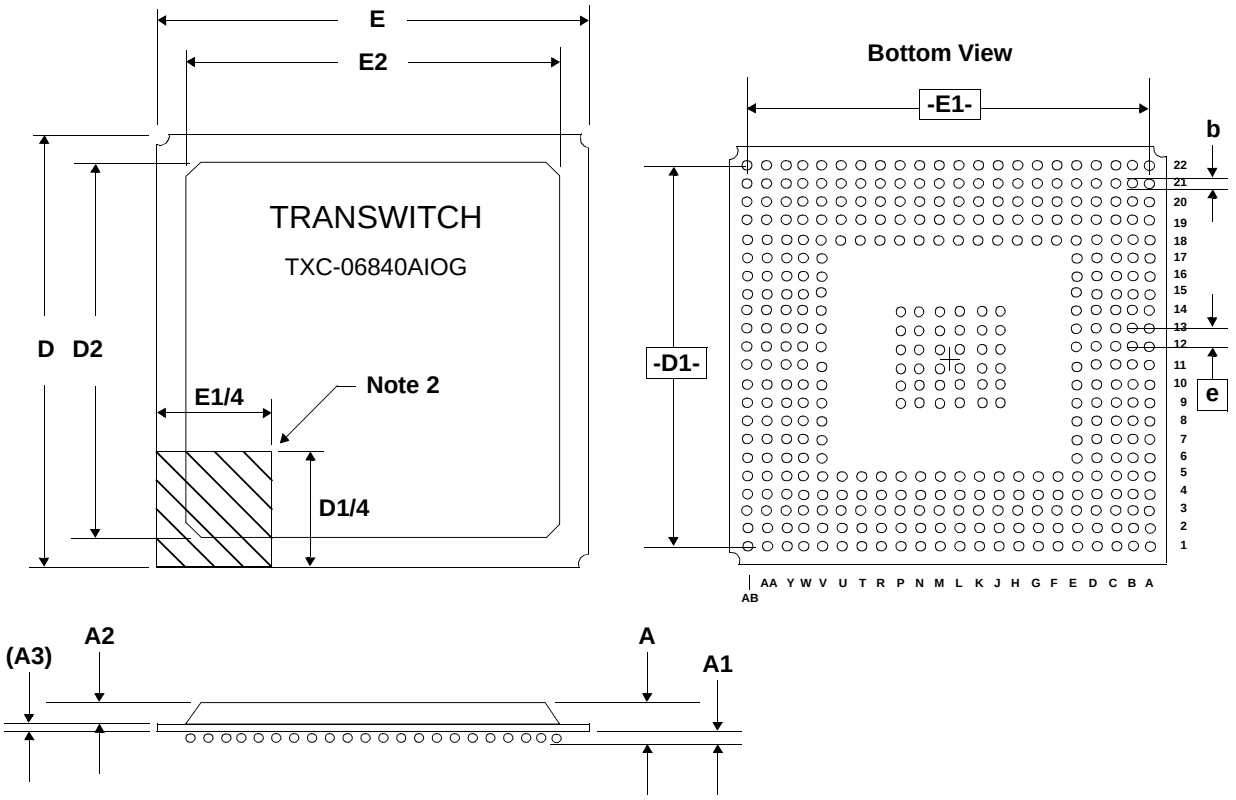
Addr (hex)	Mode	Bit range	Default value after reset	Description
400D	RW	0	0	***STREAM_ENB2:*** Streaming enable bit for Port 2. '0' = streaming disable, '1' = streaming enable. Note: this bit **must** be set with the same value as register 0x1502, bit 0.
		2-1	0	***THOLD2:*** Stream threshold for Port 2. ("00" = 256 bytes, "01" = 512 bytes, "10" = 768 bytes, "11" = 1550 bytes). These bits are valid only when STREAM_ENB='1'. Note: This register **must** be set with the same value as register ITHOLD, address 0x1501.
		5-3	0	***IFIFO_TH2:*** These 3-bits indirectly control the near empty low threshold at the read side (NE_LOW_THOLD) for Port 2.
		21-6	0	***PF_SEND_THOLD2:*** These 16-bits directly control the Near-Full High threshold (NF_HIGH_THOLD) for Port 2.
		31-22		Reserved
400E	RW	0	0	***STREAM_ENB3:*** Streaming enable bit for Port 3. '0' = streaming disable, '1' = streaming enable. Note: this bit **must** be set with the same value as register 0x1702, bit 0.
		2-1	0	***THOLD3:*** Stream threshold for Port 3. ("00" = 256 bytes, "01" = 512 bytes, "10" = 768 bytes, "11" = 1550 bytes). These bits are valid only when STREAM_ENB = '1'. Note: This register **must** be set with the same value as register ITHOLD, address 0x1701.
		5-3	0	***IFIFO_TH3:*** These 3-bits indirectly control the near empty low threshold at the read side (NE_LOW_THOLD) for Port 3.
		21-6	0	***PF_SEND_THOLD3:*** These 16-bits directly control the Near-Full High threshold (NF_HIGH_THOLD) for Port 3.
		31-22		Reserved
400F	RW	15-0	0	***PF_NFULL_THOLD0:*** These 16-bits directly control the Near-Full Low threshold (NF_LOW_THOLD) for Port 0.
		31-16	0	***PF_NFULL_THOLD1:*** These 16-bits directly control the Near-Full Low threshold (NF_LOW_THOLD) for Port 1.
4010	RW	15-0	0	***PF_NFULL_THOLD2:*** These 16-bits directly control the Near-Full Low threshold (NF_LOW_THOLD) for Port 2.
		31-16	0	***PF_NFULL_THOLD3:*** These 16-bits directly control the Near-Full Low threshold (NF_LOW_THOLD) for Port 3.
Receive Frame Buffer Controller 1 (Ports 4 to 7)				
4011		31-0		Reserved
4012	RW	0	0	***STREAM_ENB4:*** Streaming enable bit for Port 4. When = '0', streaming disable, '1' = streaming enable. Note: this bit **must** be set with the same value as register 0x1902, bit 0.
		2-1	0	***THOLD4:*** Stream threshold for Port 4. ("00" = 256 bytes, "01" = 512 bytes, "10" = 768 bytes, "11" = 1550 bytes). These 2-bits are valid only when STREAM_ENB='1'. Note: This register **must** be set with the same value as register ITHOLD, address 0x1901.
		5-3	0	***IFIFO_TH4:*** These 3-bits indirectly control the near empty low threshold at the read side (NE_LOW_THOLD) for Port 4.

Addr (hex)	Mode	Bit range	Default value after reset	Description
4012 (cont.)		21-6	0	***PF_SEND_THOLD4:*** These 16-bits directly control the Near-Full High threshold (NF_HIGH_THOLD) for Port 4.
		31-22		Reserved
4013	RW	0	0	***STREAM_ENB5:*** Streaming enable bit for Port 5. '0' = streaming disable, '1' = streaming enable. Note: this bit **must** be set with the same value as register 0x1B02, bit 0.
		2-1	0	***THOLD5:*** Stream threshold for Port 5. ("00" = 256 bytes, "01" = 512 bytes, "10" = 768 bytes, "11" = 1550 bytes). These 2-bits are valid only when STREAM_ENB='1'. Note: This register **must** be set with the same value as register ITHOLD, address 0x1B01.
		5-3	0	***IFIFO_TH5:*** These 3-bits indirectly control the near empty low threshold at the read side (NE_LOW_THOLD) for Port 5.
		21-6	0	***PF_SEND_THOLD5:*** These 16-bits directly control the Near-Full High threshold (NF_HIGH_THOLD) for Port 5.
		31-22		Reserved
4014	RW	0	0	***STREAM_ENB6:*** Streaming enable bit for Port 6. '0' = streaming disable, '1' = streaming enable. Note: this bit **must** be set with the same value as register 0x1D02, bit 0.
		2-1	0	***THOLD6:*** Stream threshold for Port 6. ("00" = 256 bytes, "01" = 512 bytes, "10" = 768 bytes, "11" = 1550 bytes). These 2-bits are valid only when STREAM_ENB='1'. Note: This register **must** be set with the same value as register ITHOLD, address 0x1D01.
		5-3	0	***IFIFO_TH6:*** These 3-bits indirectly control the near empty low threshold at the read side (NE_LOW_THOLD) for Port 6.
		21-6	0	***PF_SEND_THOLD6:*** These 16-bits directly control the Near-Full High threshold (NF_HIGH_THOLD) for Port 6.
		31-22		Reserved
4015	RW	0	0	***STREAM_ENB7:*** Streaming enable bit for Port 7. '0' = streaming disable, '1' = streaming enable. Note: this bit **must** be set with the same value as register 0x1F02, bit 0.
		2-1	0	***THOLD7:*** Stream threshold for Port 7. ("00" = 256 bytes, "01" = 512 bytes, "10" = 768 bytes, "11" = 1550 bytes). These 2-bits are valid only when STREAM_ENB='1'. Note: This register **must** be set with the same value as register ITHOLD, address 0x1F01.
		5-3	0	***IFIFO_TH7:*** These 3-bits indirectly control the near empty low threshold at the read side (NE_LOW_THOLD) for Port 7.
		21-6	0	***PF_SEND_THOLD7:*** These 16-bits directly control the Near-Full High threshold (NF_HIGH_THOLD) for Port 7.
		31-22		Reserved
4016	RW	15-0	0	***PF_NFULL_THOLD4:*** These 16-bits directly control the Near-Full Low threshold (NF_LOW_THOLD) for Port 4.
		31-16	0	***PF_NFULL_THOLD5:*** These 16-bits directly control the Near-Full Low threshold (NF_LOW_THOLD) for Port 5.

Addr (hex)	Mode	Bit range	Default value after reset	Description
4017	RW	15-0	0	***PF_NFULL_THOLD6:*** These 16-bits directly control the Near-Full Low threshold (NF_LOW_THOLD) for Port 6.
		31-16	0	***PF_NFULL_THOLD7:*** These 16-bits directly control the Near-Full Low threshold (NF_LOW_THOLD) for Port 7.

PACKAGE INFORMATION

The Envoy-8FE device is packaged in a 376-lead plastic ball grid array package suitable for surface mounting, as illustrated in Figure 14.



Notes:

1. All dimensions are in millimeters. Values shown are for reference only.
2. Identification of the solder ball A1 corner is contained within this shaded zone. This package corner may be a 90° angle for A1 identification.
3. Size of array: 22 x 22, JEDEC code MS-034.

Dimension (Note 1)	Min	Max
A A1 A2	2.02 0.40 1.12	2.44 0.60 1.22
A3 (Ref.)	0.56	
b	0.50	0.70
D	23.00	
D1 (Nom)	21.00	
D2	19.45	20.20
E	23.00	
E1 (Nom)	21.00	
E2	19.45	20.20
e (Ref.)	1.00	

Figure 14. Envoy-8FE TXC-06840 Package Diagram

ORDERING INFORMATION

Part Number:	TXC-06840AIOG	376-lead plastic ball grid array package

RELATED PRODUCTS

TXC-05802, CUBIT-*Pro* Device (*CellBus* Bus Switch). Implements cost effective ATM multiplexing and switching systems, based on the 32-bit *CellBus* architecture. A single-chip solution, the CUBIT has the ability to send and also receive cells for control purposes over the same *CellBus*. *CellBus* technology works at aggregate rates of up to 1 gigabit per second and provides header translation, multiplexing, concentration and switching functions for a wide variety of small-to-medium size ATM systems.

TXC-05804, CUBIT-3 Device (*CellBus* Bus Switch). A single-chip solution for implementing low-cost ATM multiplexing and switching systems, based on the *CellBus* architecture. Such systems are constructed from a number of CUBIT-3 devices, all interconnected by a 37-line common bus, the *CellBus.* CUBIT-3 supports unicast, broadcast and spatial multicast transfers, and has all necessary functions for implementing a switch: cell address translation, cell routing and outlet cell queuing. This device interfaces with CUBIT-*Pro* devices.

TXC-05805, CUBIT-622 Device (Multi-PHY *CellBus* Access Device). A single-chip solution for implementing low-cost ATM multiplexing and switching systems, based on the *CellBus* architecture. The CUBIT-622 device is an enhanced version of the CUBIT-3 (TXC-05804) device. The two major enhancements include a throughput increase to 622 Mbit/s and a port density increase to 64 ports. The rate decoupling FIFO have been increased from 4 to 32 cells on ingress to accommodate the higher bandwidth interface.

TXC-05806, ASPEN Express Device (Multi-PHY *CellBus* Access Device). A single-chip solution for implementing cost-effective ATM multiplexing and switching systems, based on the *CellBus* architecture. ASPEN Express provides enhanced traffic management to the *CellBus* family of ATM switching devices.

TXC-06212, PHAST®-12E Device (Programmable, High Performance ATM/PPP/TDM SDH/SONET Terminator for Level 12 with Enhanced Features). The PHAST-12E is a highly integrated SDH/SONET terminator device designed for ATM cell, frame, higher order multiplexing, and transmission applications. A single PHAST-12E device can terminate four individual STS-3c or STM-1 lines or a single STS-12/12c or STM-4/4c line.

TXC-06830, TEPro Device (Channelized DS3 Access Solution). A RISC processor-based device that supports the requirements of next-generation channelized DS3 access systems. TEPro integrates an M13 multiplexer, G.747 Mux/De-Mux framer, 28 DS1/21 E1 framers, T1/E1 cross connect and a 672 x 4,096-channel DS0 cross connect with an embedded high-performance microprocessor to provide a complete channelized DS3 solution on a single chip.

TXC-06842, Envoy-2GE Device (Dual Gigabit Ethernet Controller). A 2-port Gigabit Ethernet to POS-PHY Level 2/3 bridging device. Each GMII port is connected to a Media Access Control (MAC), operating at 1 Gbits/s mode. The MAC is programmable to provide Full-Duplex operation.

APPLICATION EXAMPLE

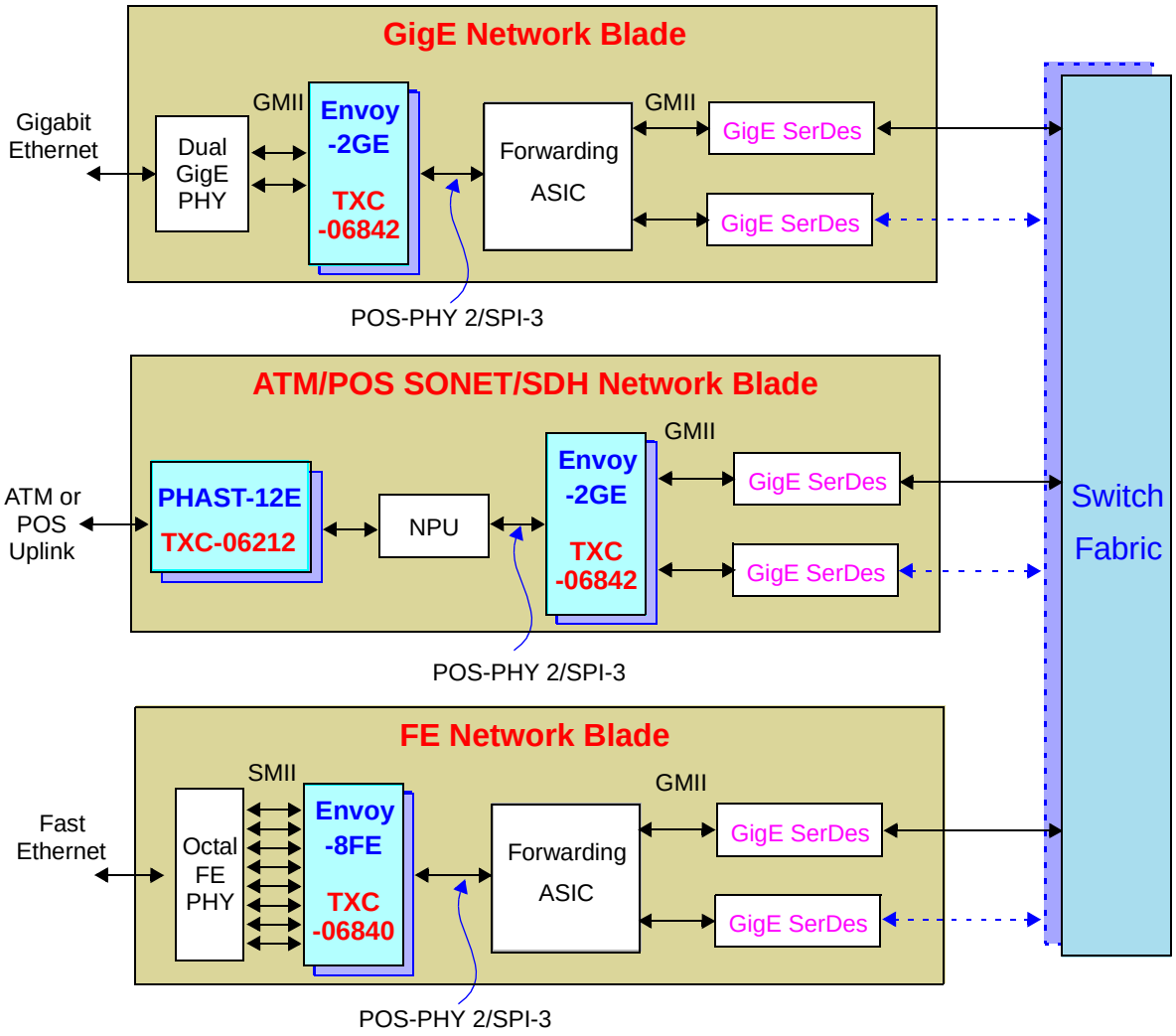


Figure 15. Edge Router Application for GigE, Fast Ethernet, and WAN ports

STANDARDS DOCUMENTATION SOURCES

Telecommunication technical standards and reference documentation may be obtained from the following organizations:

ANSI (U.S.A.):

American National Standards Institute
25 West 43rd Street
New York, New York 10036

Tel: (212) 642-4900
Fax: (212) 398-0023
Web: www.ansi.org

The ATM Forum (U.S.A., Europe, Asia):

404 Balboa Street
San Francisco, CA 94118

Tel: (415) 561-6275
Fax: (415) 561-6120
Web: www.atmforum.com

ATM Forum Europe Office

Kingsland House - 5th Floor
361-373 City Road
London EC1 1PQ, England

Tel: 20 7837 7882
Fax: 20 7417 7500

ATM Forum Asia-Pacific Office

Hamamatsucho Suzuki Building 3F
1-2-11, Hamamatsucho, Minato-ku
Tokyo 105-0013, Japan

Tel: 3 3438 3694
Fax: 3 3438 3698

Bellcore (See Telcordia)

CCITT (See ITU-T)

EIA (U.S.A.):

Electronic Industries Association
Global Engineering Documents
15 Inverness Way East
Englewood, CO 80112

Tel: (800) 854-7179 (within U.S.A.)
Tel: (303) 397-7956 (outside U.S.A.)
Fax: (303) 397-2740
Web: www.global.ihs.com

ETSI (Europe):

European Telecommunications Standards Institute
650 route des Lucioles
06921 Sophia-Antipolis Cedex, France

Tel: 4 92 94 42 00
Fax: 4 93 65 47 16
Web: www.etsi.org

GO-MVIP (U.S.A.):

The Global Organization for Multi-Vendor Integration Protocol (GO-MVIP)
3220 N Street NW, Suite 360
Washington, DC 20007

Tel: (800) 669-6857 (within U.S.A.)
Tel: (903) 769-3717 (outside U.S.A.)
Fax: (903) 769-3818
Web: www.mvip.org

IEEE (Corporate Office):

American Institute of Electrical Engineers
3 Park Avenue, 17th Floor
New York, New York 10016-5997 U.S.A.

Tel: (212) 419-7900 (within U.S.A.)
Tel: (800) 678-4333 (Members only)
Fax: (212) 752-4929
Web: www.ieee.org

ITU-T (International):

Publication Services of International Telecommunication Union
Telecommunication Standardization Sector
Place des Nations, CH 1211
Geneve 20, Switzerland

Tel: 22 730 5852
Fax: 22 730 5853
Web: www.itu.int

JEDEC (International):

Joint Electron Device Engineering Council
2500 Wilson Boulevard
Arlington, VA 22201-3834

Tel: (703) 907-7559
Fax: (703) 907-7583
Web: www.jedec.org

MIL-STD (U.S.A.):

DODSSP Standardization Documents Ordering Desk
Building 4 / Section D
700 Robbins Avenue
Philadelphia, PA 19111-5094

Tel: (215) 697-2179
Fax: (215) 697-1462
Web: www.dodssp.daps.mil

PCI SIG (U.S.A.):

PCI Special Interest Group
5440 SW Westgate Dr., #217
Portland, OR 97221

Tel: (800) 433-5177 (within U.S.A.)
Tel: (503) 291-2569 (outside U.S.A.)
Fax: (503) 297-1090
Web: www.pcisig.com

Telcordia (U.S.A.):

Telcordia Technologies, Inc.
Attention - Customer Service
8 Corporate Place Rm 3A184
Piscataway, NJ 08854-4157

Tel: (800) 521-2673 (within U.S.A.)
Tel: (732) 699-2000 (outside U.S.A.)
Fax: (732) 336-2559
Web: www.telcordia.com

TTC (Japan):

TTC Standard Publishing Group of the Telecommunication Technology Committee
Hamamatsu-cho Suzuki Building
1-2-11, Hamamatsu-cho, Minato-ku
Tokyo 105-0013, Japan

Tel: 3 3432 1551
Fax: 3 3432 1553
Web: www.ttc.or.jp

LIST OF DATA SHEET CHANGES

This change list identifies those areas within this updated Envoy-8FE device Data Sheet that have significant differences relative to the previous and now superseded Envoy-8FE Data Sheet:

Updated Envoy-8FE device Data Sheet: *PRELIMINARY* Edition 4, December 2003

Previous Envoy-8FE device Data Sheet: *PRELIMINARY* Edition 3, July 2003

The page numbers indicated below of this updated Data Sheet include changes relative to the previous Data Sheet.

Page Number of Updated Data Sheet	Summary of the Change
All	Changed edition number and date.
4	Changed third bullet item from bottom of section '10/100 Mbit/s Media Access Controller (MAC) Block'.
8	Modified sections for 'POS-PHY Level 2', and 'OIF SPI-3'.
9	Added last sentence to the last paragraph for section 'POS-PHY Level 2/SPI-3 Interface Configuration Bits (Note: n = 0 . . . 7 for ports 0 . . . 7)'.
18	Modified for Symbol 'PTPA_L2' and added Symbol 'PTPA_L3'.
27	Changed PTPA to PTPA_L2 in last row of table.
29	Changed Parameter of last row in table.
39	Modified paragraph for 'Egress FIFO Write:'.
46	Deleted Note 2.
69-72	Modified Description column for Addresses 2000 through 2007 of Bit ranges 10-4.
76	Modified Description column for Address 4001 of Bit ranges 9-3.
77	Modified Description column for Address 4002, 4003, 4004, 4006 and 4007 of Bit ranges 9-3.
78	Modified Description column for Address 4008 and 4009 of Bit ranges 9-3.
86	Added IEEE contact information.
87	Updated 'List of Data Sheet Changes' section.

- NOTES -

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