300-mA 40-V LOW-DROPOUT REGULATOR WITH ULTRALOW Iq

Check for Samples: TPS7A6301-Q1, TPS7A6333-Q1, TPS7A6350-Q1, TPS7A6401-Q1

FEATURES

- Qualified for Automotive Applications
- AEC-Q100 Test Guidance With the Following Results:
  - Device Temperature Grade 1: –40°C to 125°C Ambient Operating Temperature
  - Device HBM ESD Classification Level H2
  - Device CDM ESD Classification Level C2
- Low Dropout Voltage
  - 300 mV at I_{OUT} = 150 mA
- 4-V to 40-V Wide Input-Voltage Range With up to 45-V Transients
- 300-mA Maximum Output Current
- Ultralow Quiescent Current
  - $I_{QUIESCENT}$ = 35 µA (Typ.) at Light Loads
  - I_{SLEEP} < 2 µA When EN = Low
- Fixed (3.3-V and 5-V) and Adjustable (2.5-V to 7-V) Output Voltages
- Integrated Watchdog With Fault/Flag
- Stable With Low-ESR Ceramic Output Capacitor
- Integrated Power-On Reset
  - Programmable Delay
  - Open-Drain Reset Output
- Integrated Fault Protection
  - Short-Circuit/Overcurrent Protection
  - Thermal Shutdown
- Low Input-Voltage Tracking
- Thermally Enhanced 14-pin TSSOP - PWP Package and 10-pin VSON - DRK Package

APPLICATIONS

- Infotainment Systems With Sleep Mode
- Body Control Modules
- Always-On Battery Applications
  - Gateway Applications
  - Remote Keyless Entry Systems
  - Immobilizers

DESCRIPTION

The TPS7A63xx-Q1 and TPS7A6401-Q1 are a family of low-dropout linear voltage regulators designed for low power consumption and quiescent current less than 35 µA in light-load applications. These devices, designed to achieve stable operation even with a low-ESR ceramic output capacitor, feature an integrated programmable window watchdog and overcurrent protection. Designers can program the output voltage using external resistors. A low-voltage tracking feature allows for a smaller input capacitor and can possibly eliminate the need of using a boost converter during cold-crank conditions. The power-on-reset delay is fixed (250 µs typical), or an external capacitor can program the delay. Because of such features, these devices are well-suited in power supplies for various automotive applications.

TYPICAL APPLICATION SCHEMATIC

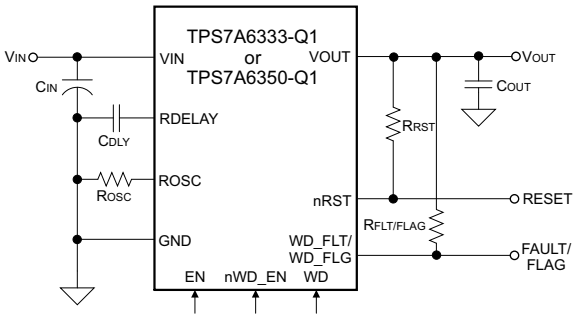


Figure 1. Fixed Output Voltage Option

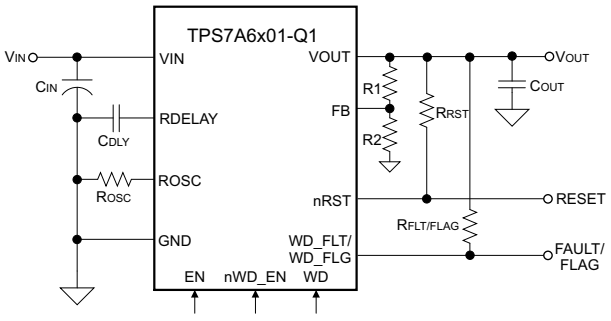


Figure 2. Adjustable Output Voltage Option

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

DESCRIPTION		VALUE	UNIT
V_{IN}, V_{EN}	Unregulated inputs(2)(3)	45	V
V_{OUT}	Regulated output	7	V
FB	Sense voltage for error amplifier(2)	7	V
ROSC	Constant-voltage reference(2)	7	V
nWD_EN, WD, WD_FLAG, WD_FLT	Watchdog inputs and outputs(2)	7	V
nRST	Open-drain reset output(2)	7	V
RDELAY	Reset delay timer output(2)	7	V
θ_{JP}	Thermal impedance junction to exposed pad TSSOP-PWP package	4.1	°C/W
	Thermal impedance junction to exposed pad VSON-DRK package	5.2	°C/W
θ_{JA}	Thermal impedance junction to ambient TSSOP-PWP package(4)	51	°C/W
	Thermal impedance junction to ambient VSON-DRK package(4)	51.7	°C/W
ESD	Electrostatic discharge(5)	2	kV
T_A	Operating ambient temperature	125	°C
T_{stg}	Storage temperature range	–65 to 150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. All voltage values are with respect to GND.
(2) Absolute negative voltage on these pins not to go below –0.3 V.
(3) Absolute maximum voltage for duration less than 480 ms.
(4) The thermal data is based on JEDEC standard high-K profile – JESD 51-5. The copper pad is soldered to the thermal land pattern. Also, the correct attachment procedure must be incorporated.
(5) The human body model is a 100-pF capacitor discharged through a 1.5-kΩ resistor into each pin.

DISSIPATION RATINGS

JEDEC STANDARD	PACKAGE	T_A < 25°C POWER RATING (W)	DERATING FACTOR ABOVE T_A = 25°C (°C/W)	T_A = 85°C POWER RATING (W)
JEDEC standard PCB, high-K, JESD 51-5	14 pin TSSOP-PWP	2.45	51	1.27
JEDEC Standard PCB high-K, JESD 51-5	10 pin VSON-DRK	2.41	51.7	1.25

RECOMMENDED OPERATING CONDITIONS

DESCRIPTION		MIN	MAX	UNIT
V_{IN}, V_{EN}	Unregulated input voltage	4	40	V
nRST, RDELAY, nWD_EN, WD_FLT(1) , WD_FLAG(2), WD, FB(3)	Low voltage input or output	0	5.25	V
T_J	Operating junction temperature range	-40	150	°C

(1) Applicable for TPS7A63xx-Q1 only
(2) Applicable for TPS746401-Q1 only
(3) Applicable for TPS7A6301-Q1 and TPS7A6401-Q1 only

ELECTRICAL CHARACTERISTICS

V_{IN} = 14 V, T_J = –40ºC to 150ºC (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input Voltage (VIN Pin)						
V_{IN}	Input voltage	V_{OUT} = 2.5 V to 7 V, I_{OUT} = 1 mA	V_{OUT} + 0.3 V		40	V
$I_{QUIESCENT}$	Quiescent current	V_{IN} = 8.2 V to 18 V, V_{EN} = 5 V, I_{OUT} = 0.01 mA to 0.75 mA		35		µA
I_{SLEEP}	Sleep or shutdown current	V_{IN} = 8.2 V to 18 V, V_{EN} < 0.8 V, I_{OUT} = 0 mA (no load), T_A = 125°C			3	µA
$V_{IN-UVLO}$	Undervoltage lockout voltage	Ramp V_{IN} down until output is turned OFF		3.16		V
$V_{IN(POWERUP)}$	Power-up voltage	Ramp V_{IN} up until output is turned ON		3.45		V
Device Enable Input (EN Pin)						
V_{IL}	Logic-input low level		0		0.8	V
V_{IH}	Logic-input high level		2.5		40	V
Regulated Output Voltage (VOUT Pin)						
V_{OUT}	Regulated output voltage	Fixed V_{OUT} value (3.3 V, 5 V or a programmed value), I_{OUT} = 10 mA to 200 mA, V_{IN} = V_{OUT} + 1 V to 16V	–2%		2%	
$\Delta V_{LINE-REG}$	Line regulation	V_{IN} = 6 V to 28 V, I_{OUT} = 10 mA, V_{OUT} = 5 V			15	mV
		V_{IN} = 6 V to 28 V, I_{OUT} = 10 mA, V_{OUT} = 3.3 V			20	mV
$\Delta V_{LOAD-REG}$	Load regulation	I_{OUT} = 10 mA to 200 mA, V_{IN}= 14 V, V_{OUT} = 5 V			25	mV
		I_{OUT} = 10 mA to 200 mA, V_{IN} = 14 V, V_{OUT} = 3.3 V			35	mV
$V_{DROPOUT}$	Dropout voltage (V_{IN} – V_{OUT})	I_{OUT} = 200 mA			500	mV
		I_{OUT} = 150 mA			300	mV
R_{SW}(1)	Switch resistance	VIN to VOUT resistance			2	Ω
I_{OUT}	Output current	V_{OUT} in regulation	0		200	mA
		[V_{OUT} in regulation, V_{OUT} = 3.3 V, V_{IN} = 6 V](2)	0		300	mA
I_{CL}	Output current limit	V_{OUT} = 0 V (VOUT pin is shorted to ground)	350		1000	mA

(1) This test is done with V_{OUT} in regulation, measuring the V_{IN} – V_{OUT} parameter when V_{OUT} drops by 100 mV from the programmed value (of V_{OUT}) at specified loads.
(2) Design Information - not tested; specified by characterization.

ELECTRICAL CHARACTERISTICS (continued)

V_{IN} = 14 V, T_J = –40ºC to 150ºC (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
PSRR(3)	Power-supply ripple rejection	$V_{IN-RIPPLE}$ = 0.5 Vpp, I_{OUT} = 200 mA, frequency = 100 Hz, V_{OUT} = 5 V and V_{OUT} = 3.3 V		60		dB
		$V_{IN-RIPPLE}$ = 0.5 Vpp, I_{OUT} = 200 mA, frequency = 150 kHz, V_{OUT} = 5 V and V_{OUT} = 3.3 V		30		
Reset (nRST Pin)						
V_{OL}	Reset pulled low	I_{OL} = 5 mA			0.4	V
I_{OH}	Leakage current	Reset pulled to VOUT through a 5-kΩ resistor			1	µA
$V_{TH(POR)}$	Power-on-reset threshold	V_{OUT} powered up above internally set tolerance, V_{OUT} = 5 V	4.5	4.65	4.77	V
		V_{OUT} powered up above internally set tolerance, V_{OUT} = 3.3 V		3.07		
UV_{THRES}	Reset threshold	V_{OUT} falling below internally set tolerance, V_{OUT} = 5 V	4.5	4.65	4.77	V
		V_{OUT} falling below internally set tolerance, V_{OUT} = 3.3 V		3.07		
t_{POR}(2)	Power-on-reset delay	C_{DLY} = 100 pF		300		µs
		C_{DLY} = 100 nF		300		ms
$t_{POR-PRESET}$	Internally preset Power-on-reset delay	C_{DLY} not connected, V_{OUT} = 5 V and V_{OUT} = 3.3 V		250		µs
$t_{DEGLITCH}$	Reset deglitch time			5.5		µs
Reset Delay (RDELAY Pin)						
$V_{TH(RDELAY)}$	Threshold to release nRST high	Voltage at RDELAY pin is ramped up		3	3.3	V
I_{DLY}	Delay capacitor charging current		0.75	1	1.25	µA
I_{OL}	Delay capacitor discharging current	Voltage at RDELAY pin = 1 V	5			mA
Current Voltage Reference (ROSC Pin)						
V_{ROSC}	Voltage reference		0.95	1	1.05	V
Watchdog Fault/ Flag Output (WD_FLT/ WD_FLAG Pin)						
V_{OL}	Logic output low level	I_{OL}= 5 mA			0.4	V
I_{OH}	Leakage current	WD_FLT/WD_FLG pulled to V_{OUT} through 5-kΩ resistor			1	µA
Watchdog Enable Input (nWD_EN Pin)						
V_{IL}	Logic input low level				0.8	V
V_{IH}	Logic input high level	5.25 V < V_{DD} < 3 V	2.5			
Watchdog Input Pulse (WD Pin)						
V_{IL}	Logic input low level				0.8	V
V_{IH}	Logic input high level	5.25 V < V_{DD} < 3 V	2.5			
t_{WD}	Watchdog window duration	R_{OSC} = 10 kΩ ± 1%		10		ms
		R_{OSC} = 20kΩ ± 1%		20		
t_{WD-tol}	Tolerance of watchdog period using external resistor	Excludes tolerance of R_{OSC} (external resistor connected to ROSC pin)	–10%		10%	
$t_{WD-DEFAULT}$	Default watchdog period	External resistor not connected, ROSC pin is floating or open	108	164	254	ms
$t_{WD-HOLD}$	Minimum pulse width for resetting watch dog timer			1.65		µs

(3) Specified by design - not tested.

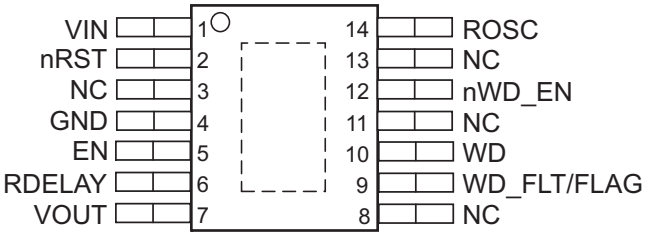
ELECTRICAL CHARACTERISTICS (continued)

V_{IN} = 14 V, T_J = –40ºC to 150ºC (unless otherwise noted)

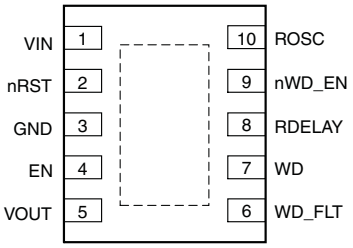
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Operating Temperature Range						
T_J	Operating junction temperature		–40		150	ºC
$T_{SHUTDOWN}$	Thermal shutdown trip point			165		ºC
T_{HYST}	Thermal shutdown hysteresis			10		ºC

DEVICE INFORMATION

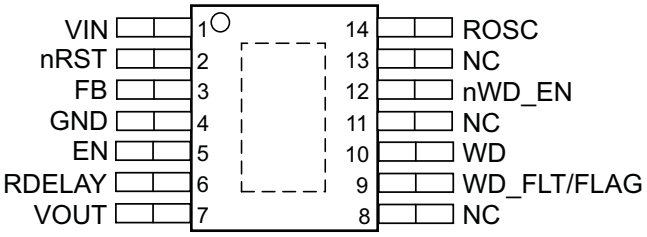
TSSOP PWP PACKAGE (TOP VIEW)
Fixed Output Voltage Option



VSON DRK PACKAGE (TOP VIEW)
Fixed Output Voltage Option



TSSOP PWP PACKAGE (TOP VIEW)
Adjustable Output Voltage Option



PIN FUNCTIONS

PIN NO.		PIN NAME	TYPE	DESCRIPTION
PWP	DRK			
1	1	VIN	I	Input voltage pin: The unregulated input voltage is supplied to this pin. A bypass capacitor connected between the VIN pin and GND pin dampens line transients on the input.
2	2	nRST	O	Reset pin: This is an open-drain reset output pin with an external pullup resistor connected to the VOUT pin.
3	–	FB	I	Feedback pin (only applicable for TPS7A6x01-Q1): Sense voltage for error amplifier
		NC	–	Not connected (only applicable for TPS7A6333-Q1/6350-Q1)
4	3	GND	I/O	Ground pin: This is signal ground pin of the IC.
5	4	EN	I	Chip enable pin: This is a high-voltage-tolerant input pin with an internal pulldown. A high input to this pin activates the device and turns the regulator ON. Connect this input to the VIN terminal for self-bias applications. If this pin remains unconnected, the device stays disabled.
6	8	RDELAY	O	Reset delay timer pin: This pin programs the reset delay timer using an external capacitor (C_{DLY}) to ground.
7	5	VOUT	O	Regulated output voltage pin: This is a regulated voltage output (V_{OUT} = 3.3 V or 5 V or a programmed value) pin with a limitation on maximum output current. For devices with adjustable output voltage (TPS7A6x01-Q1), connecting an external resistor network programs the output voltage. In order to achieve stable operation and prevent oscillation, connect an external output capacitor (C_{OUT}) with low ESR between this pin and GND pin.
8	–	NC	–	Not connected
9	6	WD_FLT	O	Watchdog fault pin (for TPS7A63xx-Q1 only): This is an active-low fault output pin with an external pullup resistor connected to the VOUT pin.
		WD_FLAG	O	Watchdog flag pin (for TPS746401-Q1 only): This is an active-high latched fault (that is, flag) output pin with an external pullup resistor connected to VOUT pin.
10	7	WD	I	Watchdog service pin: This is an input pin to provide a service signal to the watchdog.
11	–	NC	–	Not connected
12	9	nWD_EN	I	Watchdog enable pin: A high input to this pin disables the watchdog, and vice versa. This is an active-low input pin with an internal pulldown. Leaving this pin is unconnected and floating keeps the watchdog enabled. An external microcontroller can pull this pin high momentarily to disable and reinitialize the watchdog.
13	–	NC	–	Not connected
14	10	ROSC	O	ROscillator pin: This pin programs the internal oscillator frequency (and hence the duration of the watchdog window) by connecting an external resistor to ground.

FUNCTIONAL BLOCK DIAGRAMS

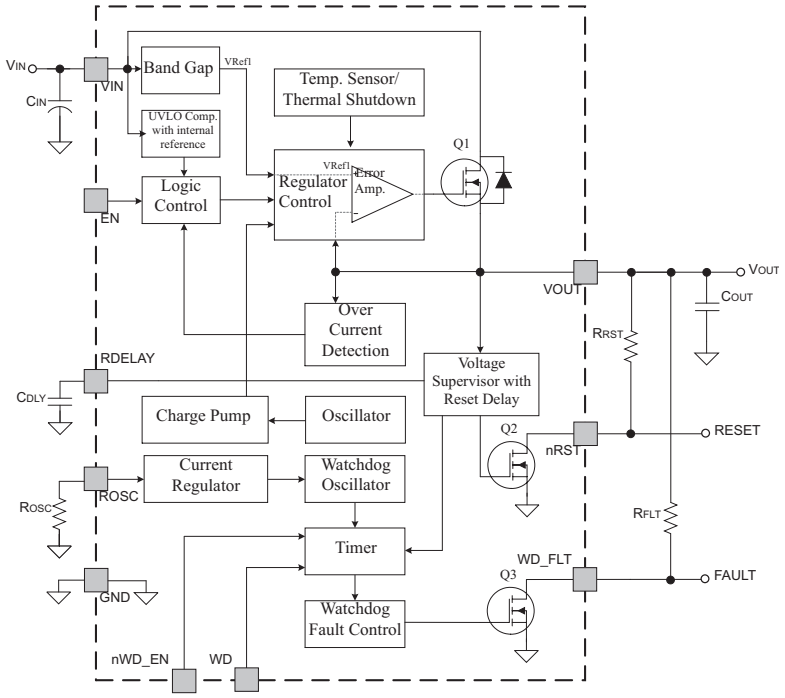


Figure 3. TPS7A6333-Q1 and TPS7A6350-Q1 (Fixed Output Voltage With FAULT Output)

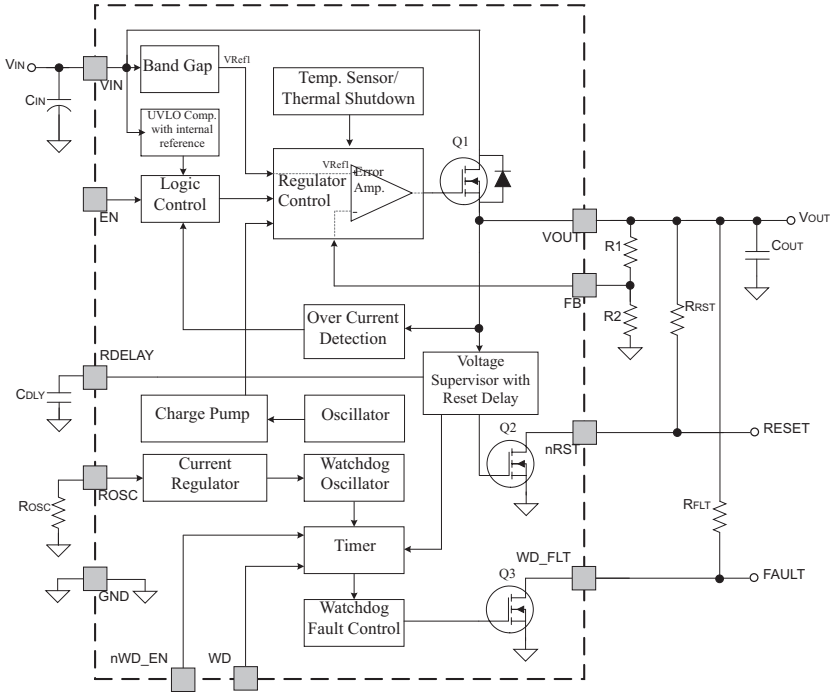


Figure 4. TPS7A6301 (Adjustable Output Voltage With FAULT Output)

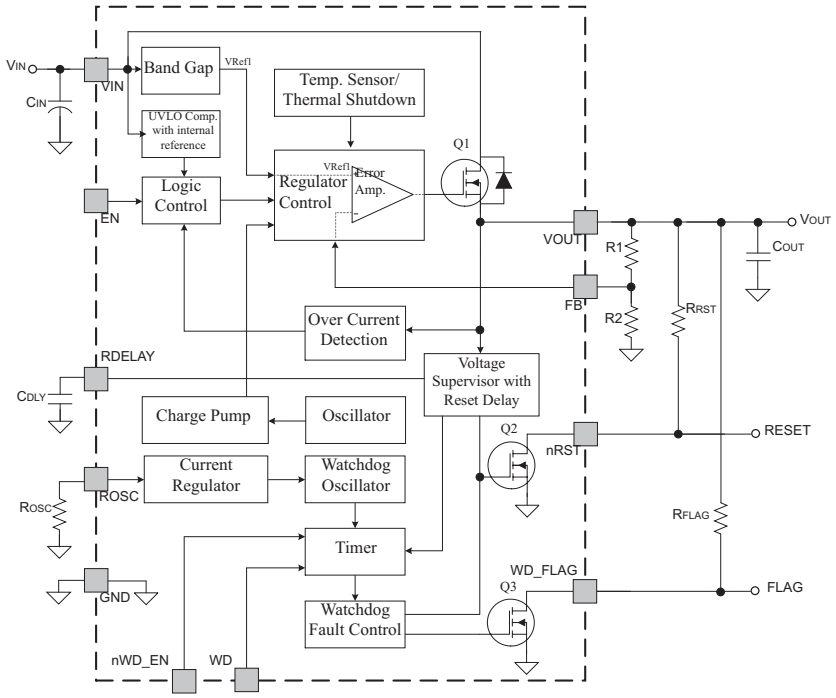


Figure 5. TPS7A6401-Q1 (Adjustable Output Voltage With FLAG Output)

TYPICAL CHARACTERISTICS

Graphs shown in the *Typical Characteristics* section for unreleased devices are for preview only.

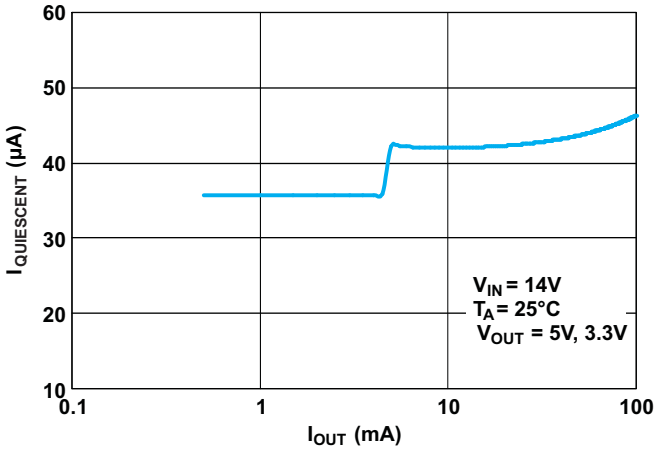


Figure 6. Quiescent Current versus Load Current

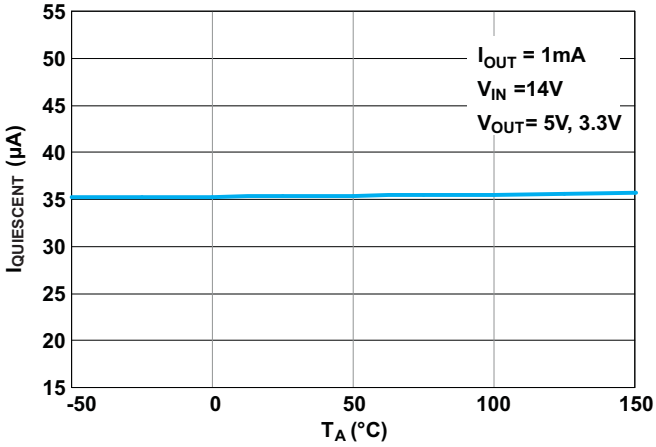


Figure 7. Quiescent Current versus Ambient Air Temperature

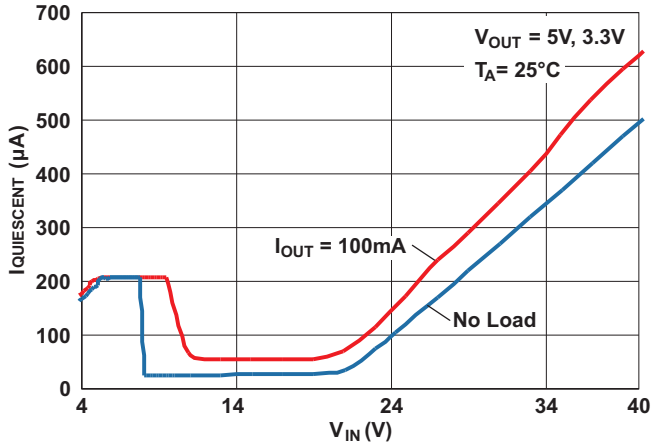


Figure 8. Quiescent Current versus Input Voltage

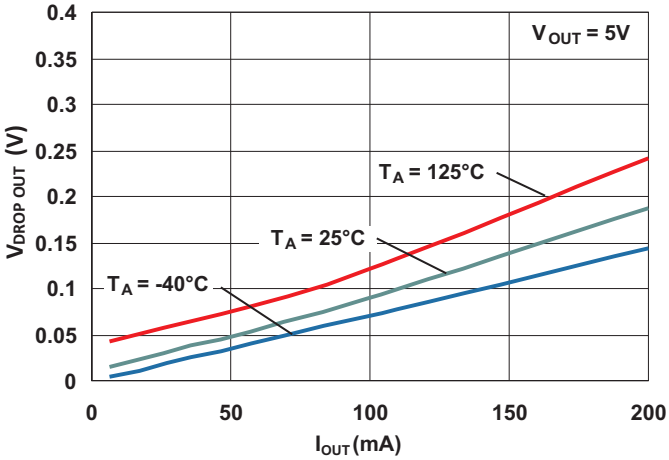


Figure 9. Dropout Voltage versus Load Current (1)

(1) Measure dropout voltage when the output voltage drops by 100 mV from the regulated output-voltage level. (For example, for an output voltage programmed to be 5 V, measure the dropout voltage when the output voltage drops down to 4.9 V from 5 V.)

TYPICAL CHARACTERISTICS (continued)

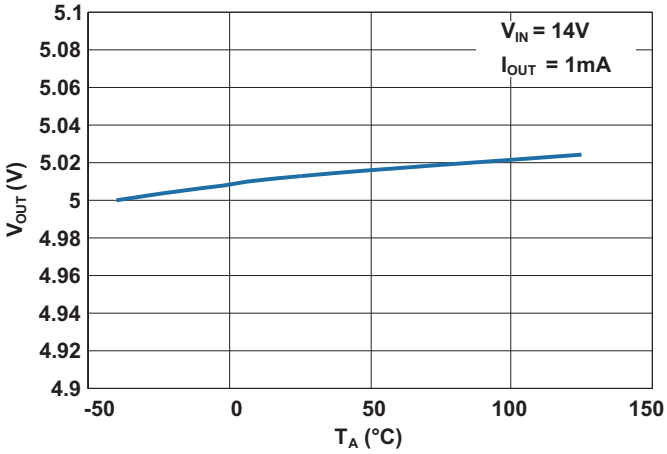


Figure 10. Output Voltage versus Ambient Air Temperature (V_{OUT} Set to 5 V)

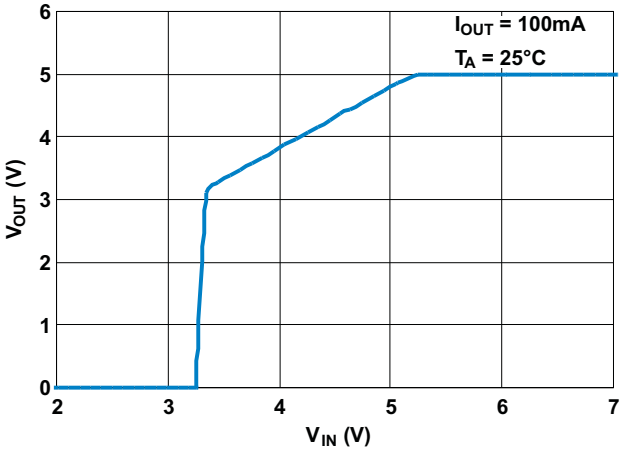


Figure 11. Output Voltage versus Input Voltage (V_{OUT} Set to 5 V)

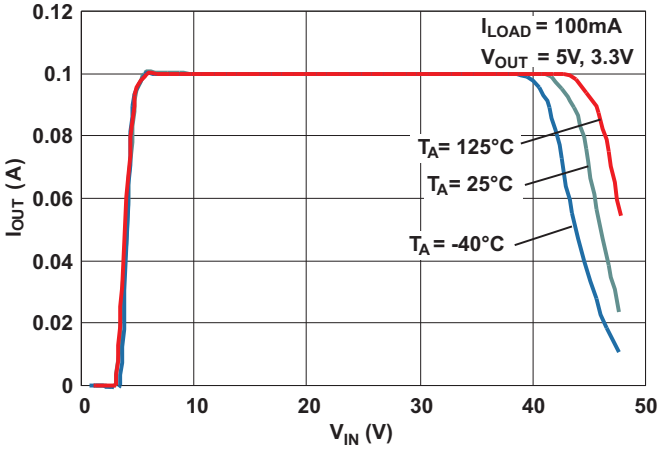


Figure 12. Output Voltage versus Input Voltage

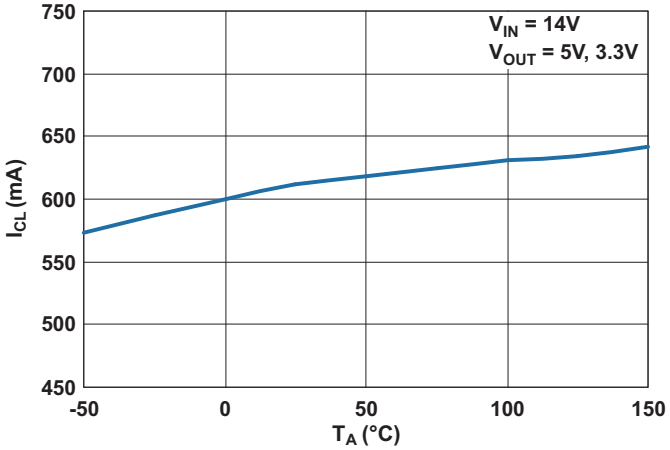


Figure 13. Output Current Limit versus Ambient Air Temperature

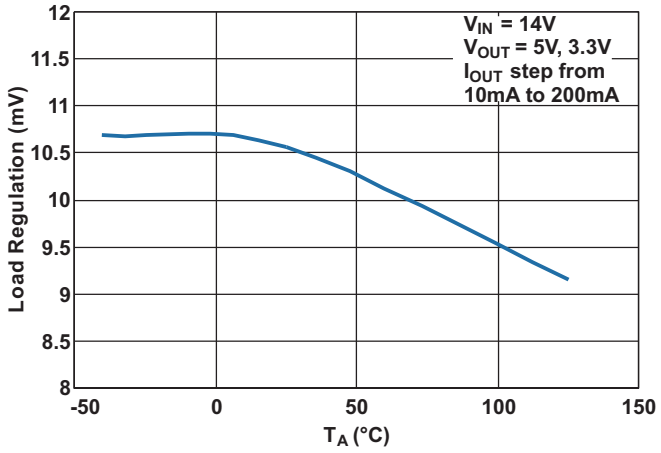


Figure 14. Load Regulation versus Ambient Air Temperature

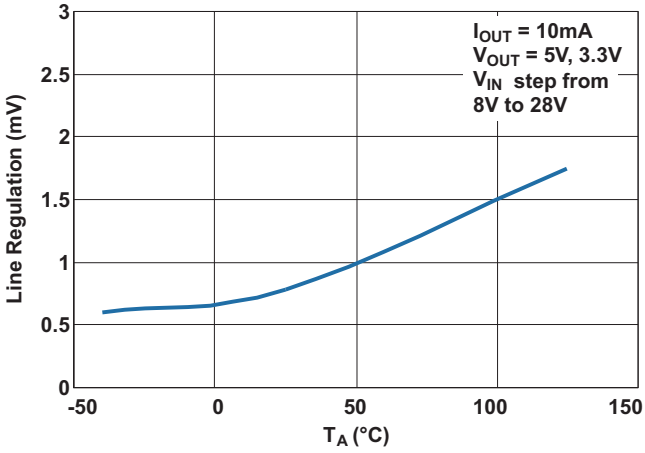


Figure 15. Line Regulation versus Ambient Air Temperature

TYPICAL CHARACTERISTICS (continued)

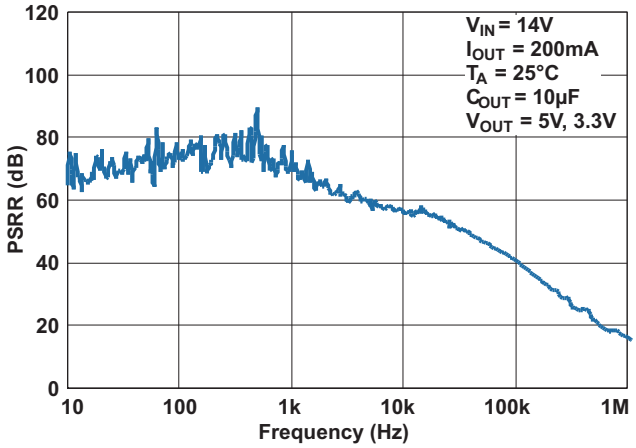


Figure 16. PSRR at Heavy Load Current

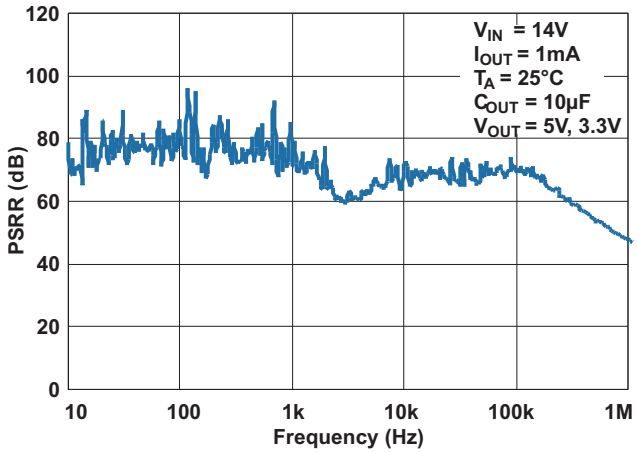


Figure 17. PSRR at Light Load Current

DETAILED DESCRIPTION

TPS7A63xx-Q1/6401-Q1 is a family of monolithic low-dropout linear voltage regulators with integrated watchdog and reset functionality. These voltage regulators are designed for low power consumption and quiescent current less than 25 µA in light-load applications. Because of an programmable reset delay (also called power-on-reset delay), these devices are well-suited in power supplies for microprocessors and microcontrollers.

These devices are available in two fixed and adjustable output-voltage versions as follows:

- Fault (WD_FLT) output version: TPS7A63xx-Q1
- Flag (WD_FLAG) output version: TPS7A6401-Q1

The following section describes the features of TPS7A63xx-Q1/6401-Q1 voltage regulators in detail.

Power Up, Reset Delay, and Reset Output

During power up, the regulator incorporates a protection scheme to limit the current through the pass element and output capacitor. When the input voltage exceeds a certain threshold ($VIN_{(POWERUP)}$) level, the output voltage begins to ramp up as shown in Figure 18.

When starting up, and also when the output recovers from a negative voltage spike due to a load step or a dip in the input voltage for a specified duration, the device implements reset delay to indicate that output voltage is stable and in regulation.

When the output voltage reaches the power-on-reset threshold ($V_{TH(POR)}$) level, that is, 93% of regulated output voltage (3.3 V or 5 V, or a programmed value), a constant output current charges an external capacitor (C_{DLY}) to an internal threshold ($V_{TH(RDELAY)}$) voltage level. Then, nRST asserts high and C_{DLY} discharges through an internal load. This allows C_{DLY} to charge from approximately 0 V during the next power cycle.

Program the reset delay time by connecting an external capacitor (C_{DLY} ,100 pF to 100 nF) to the RDELAY pin. Equation 1 gives the delay time:

$$t_{POR} = \frac{CDLY \times 3}{1 \times 10^{-6}} \quad (1)$$

where,

t_{POR} = reset delay time in seconds
C_{DLY} = reset delay capacitor value in farads

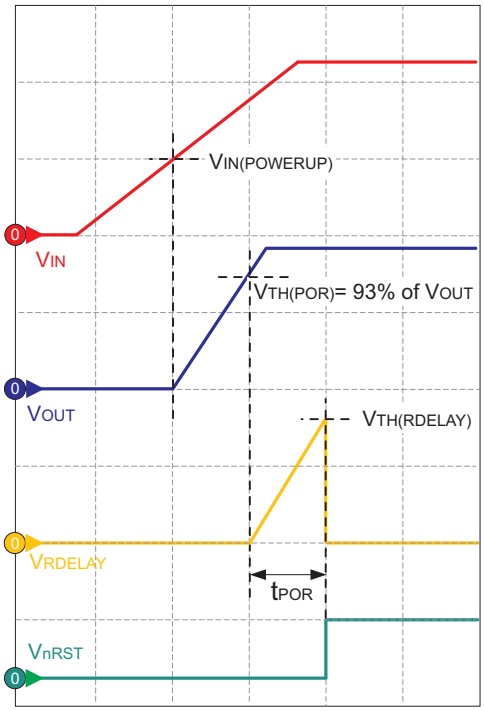


Figure 18. Power Up and Conditions for Activation of Reset

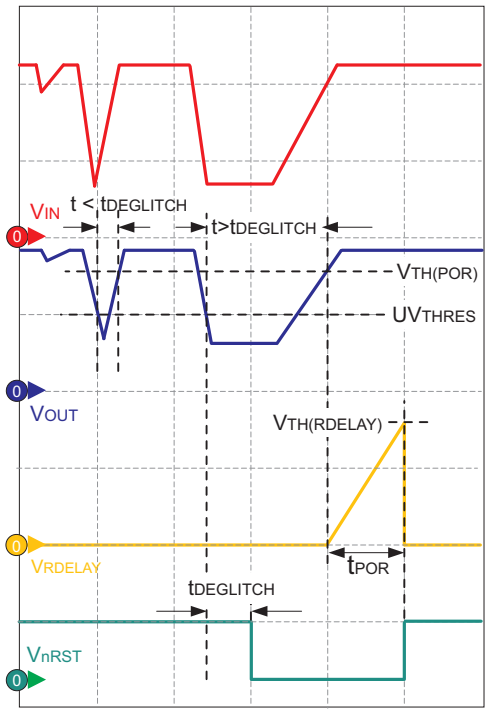


Figure 19. Reset Delay and Deglitch Filter

As Figure 19 shows, if the regulated output voltage falls below 93% of the set level, nRST asserts low after a short de-glitch time of approximately 5.5 µs (typical). In case of negative transients in the input voltage (V_{IN}), the reset signal asserts low only if the output (V_{OUT}) drops and stays below the reset threshold level ($V_{TH(POR)}$) for more than the deglitch time ($t_{DEGLITCH}$), as Figure 19 and Figure 22 illustrate. While nRST is low, if the input voltage returns to the nominal operating voltage, the normal power-up sequence ensues. nRST asserts high only if the output voltage exceeds the reset threshold voltage ($V_{TH(POR)}$) and the reset delay time (t_{POR}) has elapsed.

Adjustable Output Voltage

Program the regulated output voltage (V_{OUT}) by connecting external resistors to FB pin. Calculate the feedback resistor values using Equation 2.

$$V_{OUT} = V_{REF}\left[1 + \frac{R1}{R2}\right] \quad (2)$$

where,

V_{OUT}= desired output voltage

V_{REF} = reference voltage (V_{REF}= 1.23 V, typically)

R1, R2 = feedback resistors (see Figure 5)

Equation 3 gives the overall tolerance of the regulated output.

$$tol_{V_{OUT}} = tol_{V_{REF}} + \left[\frac{R1}{R1 + R2}\right]\left[tol_{R1} + tol_{R2}\right] \quad (3)$$

where,

tol_{VOUT} = tolerance of the output voltage

tol_{VREF} = tolerance of the internal reference voltage (tol_{VREF} = ± 1.5% typically)

tol_{R1},tol_{R2} = tolerance of feedback resistors R1, R2

For a tighter tolerance on V_{OUT}, select lower-value feedback resistors. TI recommends to select feedback resistors such that the sum of R1 and R2 is between 20 kΩ and 200 kΩ.

Chip Enable

These devices have a high-voltage-tolerant EN pin that an external microcontroller or a digital control circuit can use to enable and disable them. A high input to this pin activates the device and turns the regulator on. For self bias applications, connect this input to the VIN terminal . An internal pulldown resistor is connected to this pin, and therefore if this pin remains unconnected, the device stays disabled.

Charge-Pump Operation

These devices have an internal charge pump which turns on or off depending on the input voltage and the output current. The charge pump switching circuitry must not cause conducted emissions to exceed required thresholds on the input voltage line. For a given output current, the charge pump stays on at lower input voltages and turns off at higher input voltages. The charge-pump switching thresholds are hysteretic. Figure 20 and Figure 21 show typical switching thresholds for the charge pump at light (I_{OUT} < ~2 mA) and heavy (I_{OUT} > ~2 mA) loads, respectively.

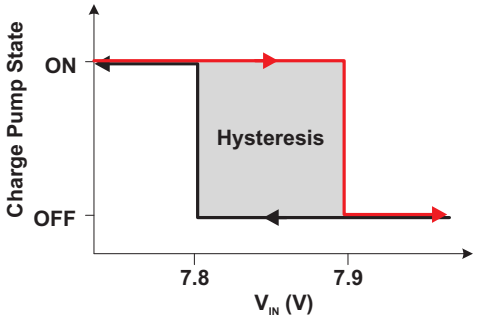


Figure 20. Charge-Pump Operation at Light Loads

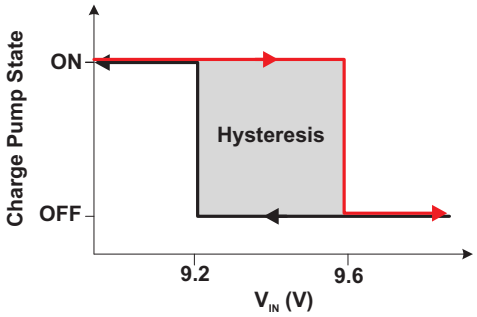


Figure 21. Charge-Pump Operation at Heavy Loads

Low-Power Mode

At light loads and high input voltages (V_{IN} > approximately 8 V, such that the charge pump is off), the device operates in low-power mode and the quiescent current consumption is reduced to 25 µA (typical) as shown in Table 1.

Table 1. Typical Quiescent Current Consumption

I_{OUT}	Charge Pump ON	Charge Pump OFF
I_{OUT} < approximately 2 mA (Light load)	250 µA	35 µA (Low-power mode)

Table 1. Typical Quiescent Current Consumption (continued)

I_{OUT}	Charge Pump ON	Charge Pump OFF
I_{OUT} > approximately 2 mA (Heavy load)	280 µA	70 µA

Undervoltage Shutdown

These devices have an integrated undervoltage lockout (UVLO) circuit to shut down the output if the input voltage (V_{IN}) falls below an internally fixed UVLO threshold level ($V_{IN-UVLO}$). This ensures that the regulator does not latch into an unknown state during low-input-voltage conditions. The regulator powers up when the input voltage exceeds the $V_{IN(POWERUP)}$ level, as Figure 22 shows.

Low-Voltage Tracking

At low input voltages, the regulator drops out of regulation, and the output voltage tracks the input minus a voltage based on the load current (I_{OUT}) and switch resistance (R_{SW}), as Figure 22 shows. This feature allows for a smaller input capacitor and can possibly eliminate the need of using a boost convertor during cold crank conditions, as Figure 22 shows.

Integrated Fault Protection

These devices feature integrated fault protection to make them ideal for use in automotive applications. In order to remain in a safe area of operation during certain fault conditions, the devices use internal current-limit protection and current-limit foldback to limit the maximum output current. This protects them from excessive power dissipation. For example, during a short-circuit condition on the output, fault protection limits the current through the pass element to I_{CL} to protect the device from excessive power dissipation.

Thermal Shutdown

These devices incorporate a thermal shutdown (TSD) circuit as a protection from overheating. For continuous normal operation, the junction temperature should not exceed the TSD trip point. The junction temperature exceeding the TSD trip point causes the output to turn off. When the junction temperature falls below TSD trip point, the output turns on again, as Figure 23 shows.

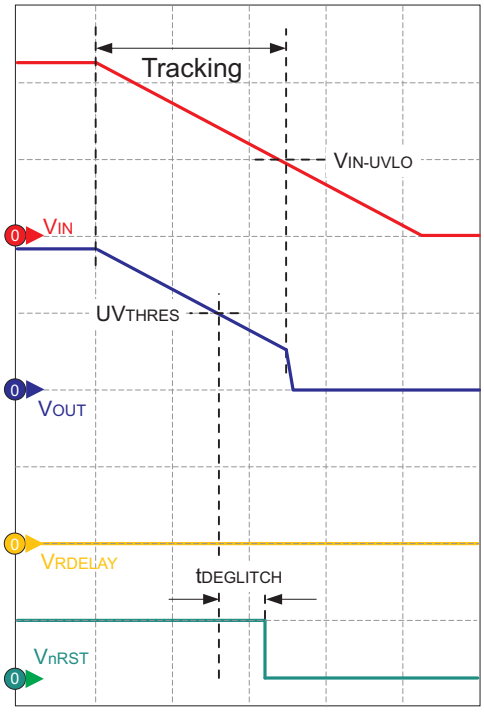


Figure 22. Low-Voltage Tracking and Undervoltage Lockout

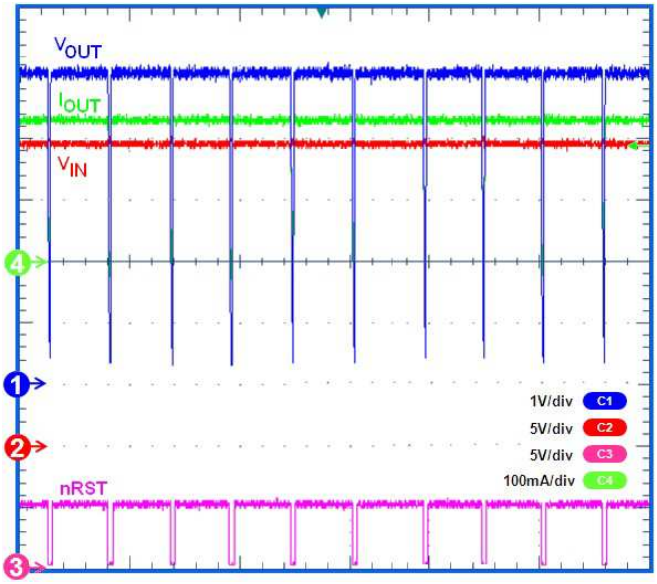


Figure 23. Thermal Cycling Waveform for TPS7A6350-Q1 (V_{IN}= 24 V, I_{OUT}= 200 mA, V_{OUT}= 5 V)

INTEGRATED WINDOW WATCHDOG

These devices have an integrated watchdog with fault (WD_FLT) and flag (WD_FLAG) output options. Both device options are available in fixed- and adjustable-output versions. The watchdog operation, service fault conditions, and difference between fault (TPS7A63xx-Q1) and flag (TPS746401-Q1) output versions are described as follows.

Programmable-Window Watchdog

Program the duration of the watchdog window by connecting an external resistor (R_{OSC}) to ground at the ROSC pin. The current through the resistor sets the clock frequency of the internal oscillator. The user can adjust the duration of the watchdog window (that is, the watchdog timer period) by changing the resistor value. The duration of the watchdog window and the duration of the fault output are multiples of the internal oscillator frequency and are given by the following equations:

$$t_{WD} = 10^{-6} \times R_{OSC} = 5000 \times 1 / f_{OSC} \quad (4)$$

$$t_{WD\_OUT} = 1 / f_{OSC} \quad (5)$$

$$t_{CW} = t_{OW} = 1 / 2\ t_{WD} \quad (6)$$

where,

- t_{WD} = width of watchdog window
- R_{OSC} = resistor connected at ROSC pin
- t_{WD_OUT} = duration of fault output
- f_{OSC} = frequency of internal oscillator
- t_{CW} = duration of closed window
- t_{OW} = duration of open window

As shown in Figure 24, each watchdog window consists of an open window and a closed window, each having a width approximately 50% of the watchdog window. However, there is an exception to this; the first open window after watchdog initialization is eight times the duration of the watchdog window. All open windows except the one after watchdog initialization are one-half the width of the watchdog window. On initialization, the watchdog must receive service (by software, external microcontroller, and so forth) only during an open window. A watchdog serviced during a closed window, or not serviced during a open window, creates a watchdog fault condition.

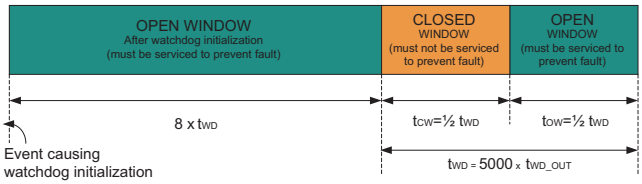


Figure 24. Watchdog Window Duration

Watchdog Enable

An external microcontroller or a digital circuit can apply an appropriate signal to the nWD_EN pin to enable or disable the watchdog. A low input to this pin turns the watchdog on. Because of an internal pulldown resistor connected to this pin, leaving the pin unconnected keeps the watchdog enabled.

Watchdog Service Signal

In order for the watchdog service signal (WD) to service an open window correctly, the service signal must stay high for a duration of at least t_{WD_HOLD}. The recommended value of t_{WD_HOLD} is given by Equation 7:

$$t_{WD\_HOLD} = 3 \times t_{WD\_OUT} \quad (7)$$

Watchdog Fault Outputs

The WD_FLT pin and WD_FLAG pin are fault output terminals for the TPS7A63xx-Q1 and TPS7A6401-Q1 devices, respectively. Typically, one pulls these fault outputs high to a regulated output supply. In the case of a watchdog fault condition, the TPS7A63xx-Q1 momentarily pulls WD_FLT low for a duration of t_{WD_OUT}, whereas the TPS746401-Q1 latches the WD_FLAG high and momentarily pulls nRST low for a duration of t_{WD_OUT}.

Watchdog Initialization

On power up and during normal operation, the watchdog initializes under the conditions shown in Table 2. The normal operation of the watchdog for the WD_FLT and WD_FLAG output device options is shown in Figure 25 and Figure 26, respectively.

Table 2. Conditions for Watchdog Initialization

Edge	What causes watchdog to initialize?	TPS7A63xx-Q1 (FAULT Option)	TPS746401-Q1 (FLAG Option)
	Rising edge of nRST (when V_{OUT} exceeds $V_{TH(POR)}$) while the watchdog is in the enabled state, for example, during soft power up	✓	✓
	Falling edge of nWD_EN while the nRST is already high, for example, when the microprocessor enables the watchdog after the device is powered up	✓	✓
	Rising edge of WD_FLT while the nRST is already high and the watchdog is in the enabled state, for example, right after a closed window is serviced	✓	X

Watchdog Operation

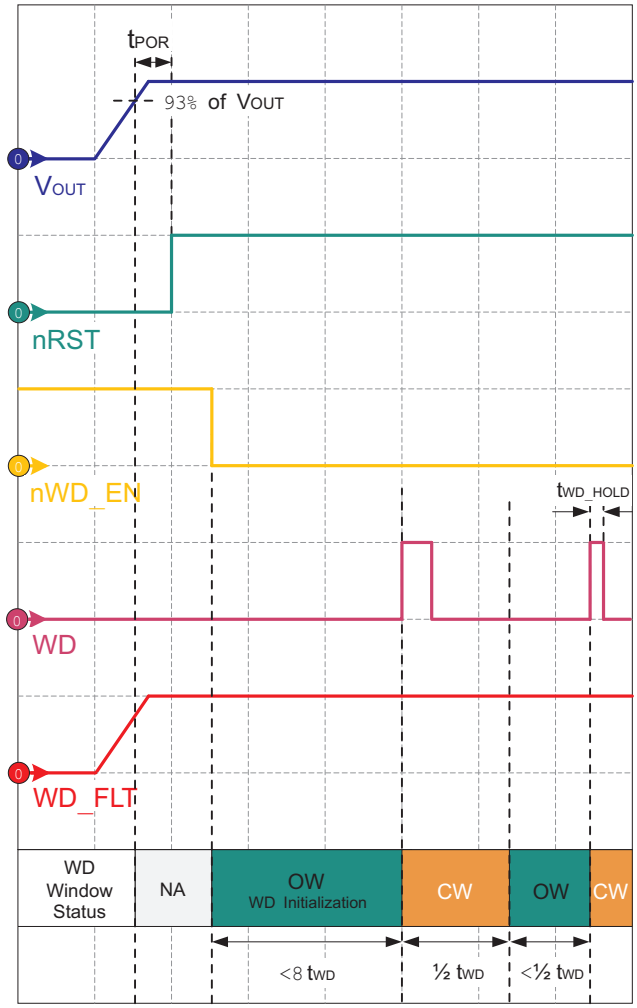


Figure 25. Power Up, Initialization, and Normal Operation for TPS7A63xx-Q1

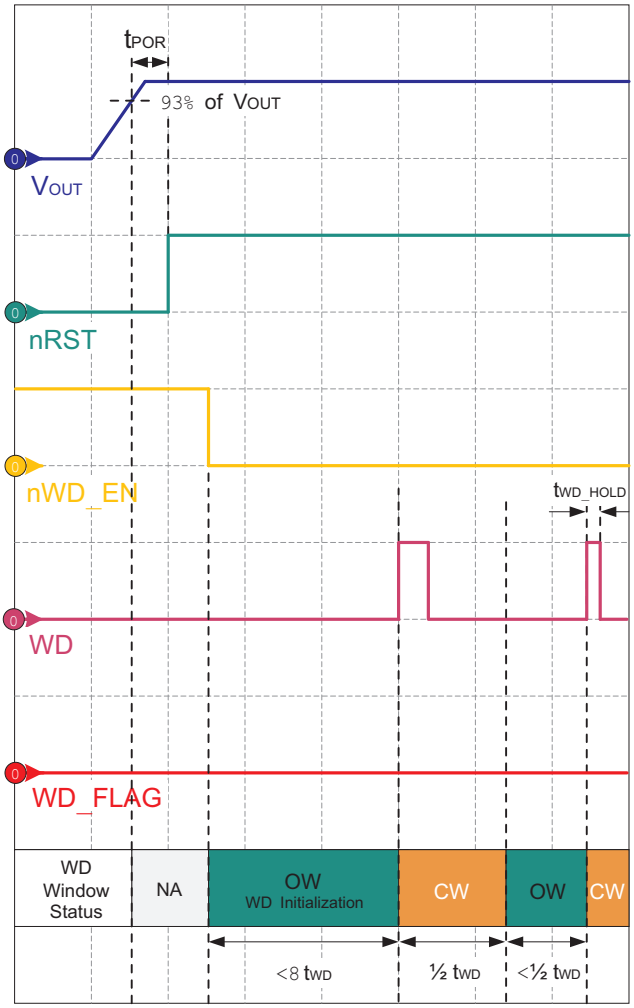


Figure 26. Power Up, Initialization, and Normal Operation for TPS7A6401-Q1

Figure 25 shows watchdog initialization and operation for the TPS7A63xx-Q1. After output voltage is in regulation and reset asserts high (clearly the chip-enable pin is high), the watchdog becomes enabled when an external signal pulls nWD_EN (the watchdog enable pin) low. This causes the watchdog to initialize and wait for a service signal during the first open window for 8× the duration of t_{WD}. A service signal applied to the WD pin during the first open window resets the watchdog counter and a closed window starts. To prevent a fault condition from occurring, watchdog service must not occur during the closed window. Watchdog service must occur during the following open window to prevent fault condition from occurring. The fault output (WD_FLT), externally pulled up to VOUT (typically), stays high as long as the watchdog receives proper serviced and there is no fault condition.

Figure 26 shows watchdog initialization and operation for FLAG output version (TPS7A6401-Q1). The fault output (WD_FLAG), externally pulled up to VOUT (typically), stays low as long as the watchdog receives proper service and there is no fault condition.

Likewise, enabling the watchdog before powering the device on (that is, pulling the nWD_EN pin low before power up), the watchdog initializes as soon as the output voltage is in regulation and reset asserts high (see Table 2 for Conditions for Watchdog Initialization).

Watchdog Fault Conditions

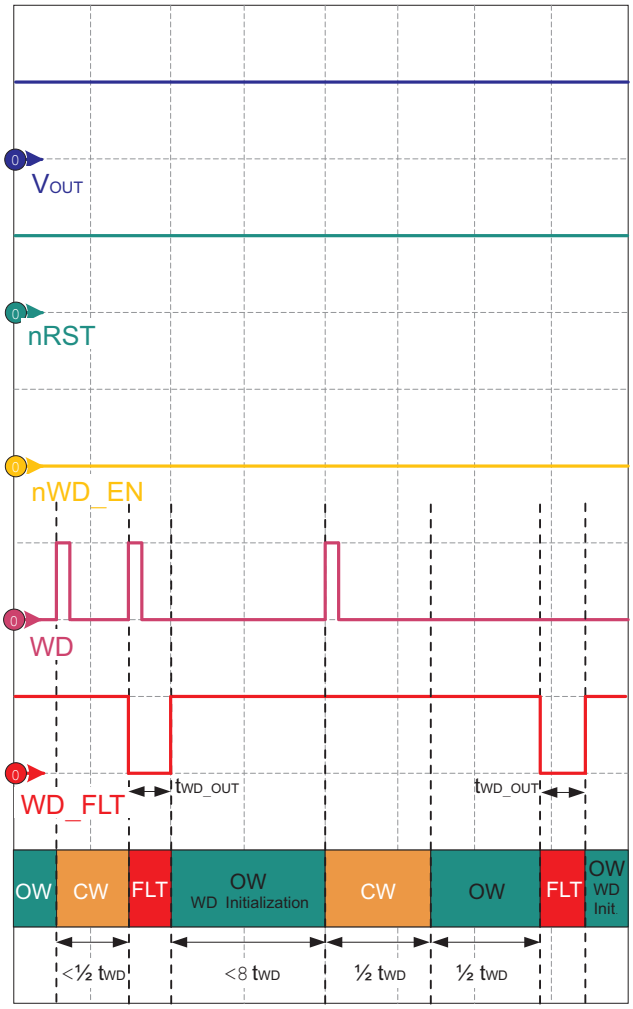


Figure 27. Watchdog Service Fault Conditions for TPS7A63xx-Q1

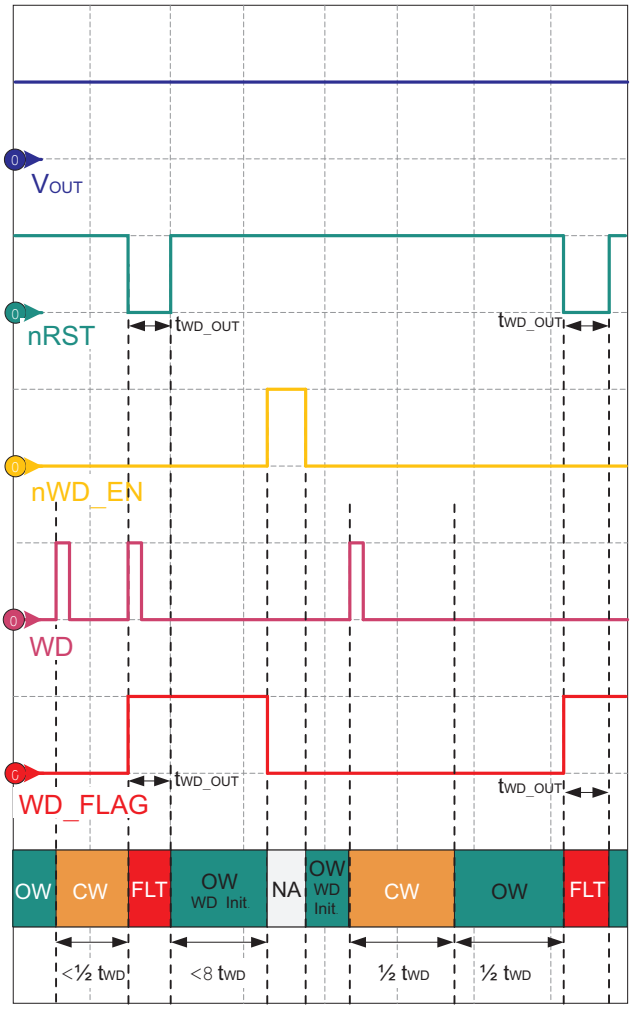


Figure 28. Watchdog Service Fault Conditions for TPS7A6401-Q1

For both device options, a watchdog fault condition occurs in following (non-exhaustive) cases:

i) When the watchdog receives service during a closed window

ii) When watchdog does not rexceive serviced during an open window (this open window could be the one after watchdog initialization, or the one following a closed window).

As shown in Figure 27, for TPS7A63xx-Q1 the first watchdog fault registers when the watchdog receives service during a closed window. This causes the watchdog fault pin (WD_FLT) to go low temporarily for a duration of t_{WD_OUT}. Following the fault, the watchdog reinitializes. Likewise, the second fault registers when the watchdog does not receive service during an open window (following a closed window). Again, the fault pin (WD_FLT) is asserts low for a duration of t_{WD_OUT}.

As shown in Figure 28, for TPS746401-Q1 the first watchdog fault registers when watchdog receives service during a closes window. This causes the watchdog flag pin (WD_FLAG) to become high and stay latched. At the same time, nRST pin goes low temporarily for the duration of t_{WD_OUT}. WD_FLAG remains high until toggling the nWD_EN pin disables and re-enables the watchdog or the watchdog receives service properly (while nWD_EN is low and nRST is high). The second fault registers when the watchdog does not receive service during an open window (following a closed window). While WD_FLAG is high (i.e. during a fault condition), if the watchdog stays enabled, and reset is high; a watchdog service signal can also bring WD_FLAG low (about 5 µs after the watchdog receives service).

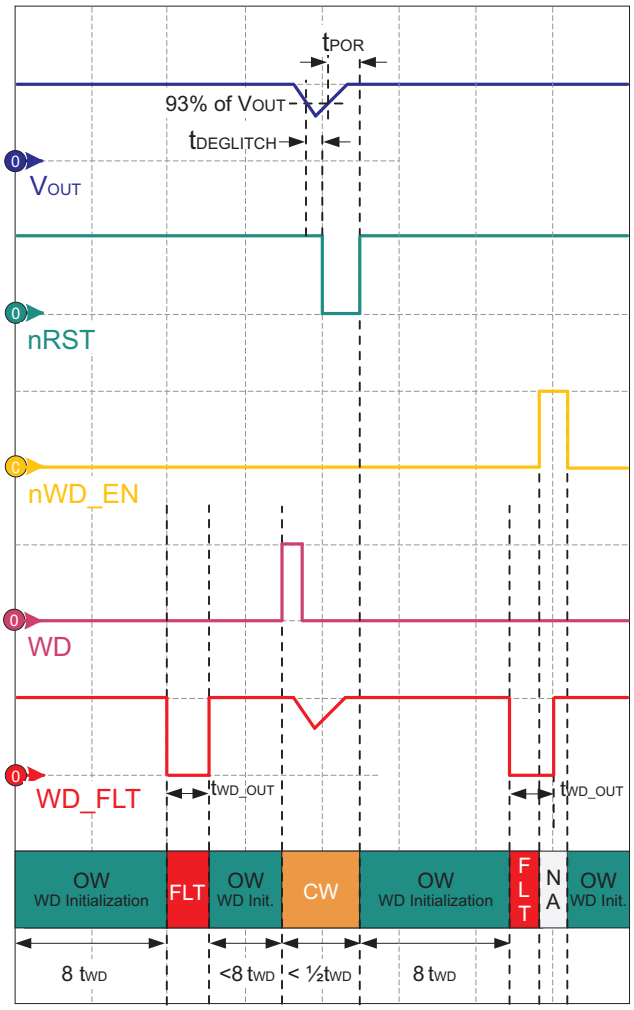


Figure 29. Watchdog Fault During Initialization, and Reinitialization During Reset for TPS7A63xx-Q1

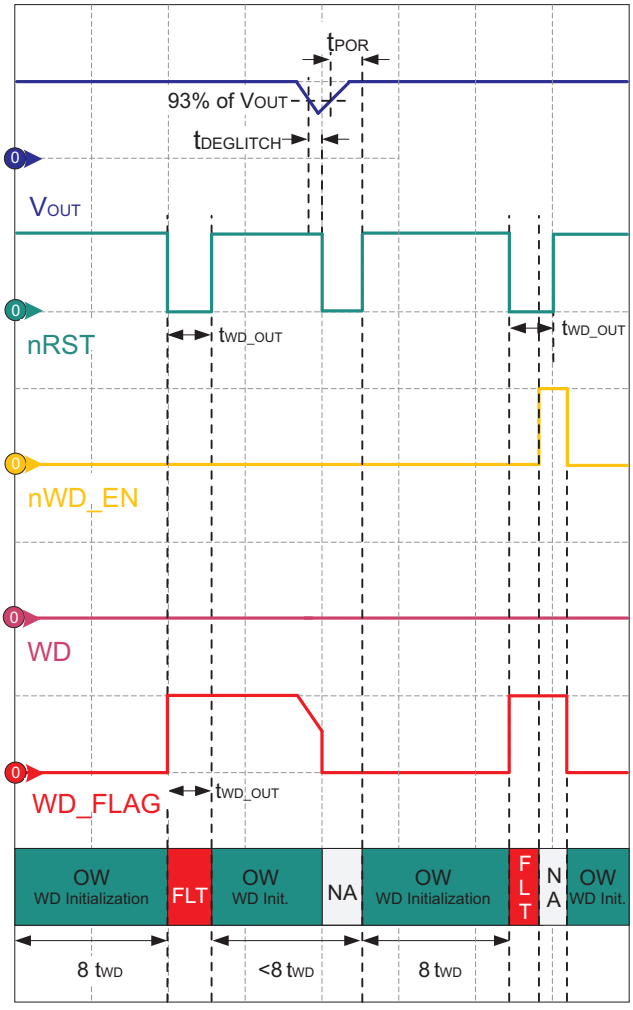


Figure 30. Watchdog Fault During Initialization, and Reinitialization During Reset for TPS7A6401-Q1

As shown in Figure 29 for the TPS7A6401-Q1, the watchdog fault condition also occurs if the watchdog does not receive service during the open window after watchdog initialization. That is, if the watchdog does not receive service during the first 8× t_{WD_OUT} period after initialization, a fault condition occurs. This causes the watchdog fault pin (WD_FLT) to go low temporarily for a duration of t_{WD_OUT}. In case of a load transient, if the regulated output voltage drops down causing reset (nRST) to go low, the rising edge on nRST causes the watchdog to reinitialize (that is, when reset becomes high with the watchdog still enabled). During a fault condition (that is, WD_FLT is low) with the watchdog disabled, the fault output continues to stay low until t_{WD_OUT} is elapsed. A falling edge on nWD_EN pin causes the watchdog to reinitialize while nRST is still high.

As shown in Figure 30 for the TPS7A6401-Q1, the watchdog fault condition also occurs if the watchdog does not receive service during the open window after watchdog initialization. That is, if the watchdog does not receive service in first 8× t_{WD_OUT} period after initialization, a fault condition occurs. This causes the watchdog flag pin (WD_FLAG) to become high and stay latched. At the same time, the nRST pin goes low temporarily for a duration of t_{WD_OUT}. In the case of a load transient, if the regulated output voltage drops down causing the reset output to go low, the WD_FLAG asserts low, and the rising edge on nRST causes the watchdog to reinitialize (while the watchdog remains enabled). During a fault condition (that is, WD_FLAG is high), and with a disabled watchdog, the flag output continues to stay

high as long as the watchdog remains enabled or receives proper service. However, nRST stays low until t_{WD_OUT} elapses. Re-enabling the watchdog causes watchdog to reinitialize (while nRST is still high).

APPLICATION INFORMATION

Typical application circuits for TPS7A6401-Q1 and TPS76333-Q1/6350-Q1 are shown in Figure 31 and Figure 32. Depending on the end application, one may use different values of external components. Carefully select feedback resistors (R1 and R2), used to program the output voltage. Using smaller resistors results in higher current consumption, whereas using very large resistors impacts the sensitivity of the regulator. Therefore, TI recommends selecting feedback resistors such that the sum of R1 and R2 is between 20 kΩ and 200 kΩ.

Example

If the desired regulated output voltage is 5 V, after selecting R2 then one can calculate R1 using (or vice versa) Equation 2. Knowing V_{REF} = 1.23 V (typical), V_{OUT} = 5 V, selecting R2 = 20 kΩ, the calculated value of R1 is 61.3 kΩ.

During fast load steps, an application may require a larger output capacitor to prevent the output from temporarily dropping down. TI recommends a low-ESR ceramic capacitor with dielectric of type X5R or X7R. One can also connect a bypass capacitor at the output to decouple high-frequency noise as per the end application.

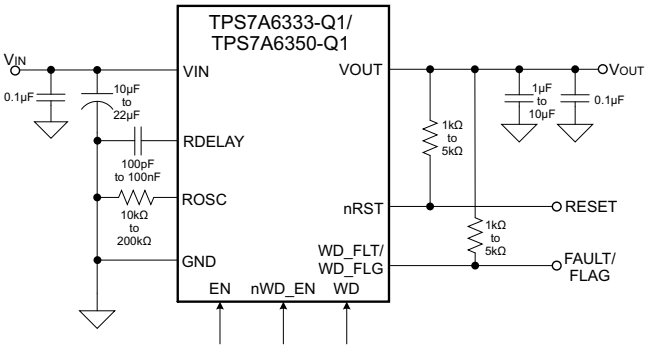


Figure 31. Typical Application Schematic, TPS7A6333-Q1/6350-Q1

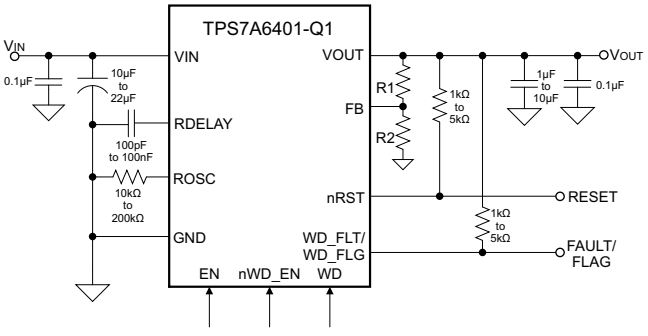


Figure 32. Typical Application Schematic TPS7A6401-Q1

Power Dissipation and Thermal Considerations

Calculated the power dissipated in the device using Equation 8.

$$P_D = I_{OUT} \times (V_{IN} - V_{OUT}) + I_{QUIESCENT} \times V_{IN} \quad (8)$$

where,

P_D = continuous power dissipation
I_{OUT} = output current
V_{IN} = input voltage
V_{OUT} = output voltage
$I_{QUIESCENT}$ = quiescent current

As $I_{QUIESCENT} << I_{OUT}$, therefore, ignore the term $I_{QUIESCENT} \times V_{IN}$ in Equation 8.

For a device in operation at a given ambient air temperature (T_A), calculate the junction temperature (T_J) using Equation 9.

$$T_J = T_A + (\theta_{JA} \times P_D) \quad (9)$$

where,

θ_{JA} = junction-to-ambient-air thermal impedance

Calculate the rise in junction temperature due to power dissipation using Equation 10.

$$\Delta T = T_J - T_A = (\theta_{JA} \times P_D) \quad (10)$$

For a given maximum junction temperature ($T_{J\text{-}Max}$), calculate the maximum ambient air temperature ($T_{A\text{-}Max}$) at which the device can operate using Equation 11.

$$T_{A\text{-}Max} = T_{J\text{-}Max} - (\theta_{JA} \times P_D) \quad (11)$$

Example

If I_{OUT} = 100 mA, V_{OUT} = 5 V, V_{IN} = 14 V, $I_{QUIESCENT}$ = 250 µA, and θ_{JA}= 50°C/W, the continuous power dissipated in the device is 0.9 W. The rise in junction temperature due to power dissipation is 45°C. For a maximum junction temperature of 150°C, the maximum ambient air temperature at which the device can operate is 105°C.

For adequate heat dissipation, TI recommends soldering the thermal pad (exposed heat sink) to the thermal land pad on the PCB. Doing this provides a heat conduction path from the die to the PCB and reduces overall package thermal resistance. Power derating curves for the TPS7A63xx-Q1/6401-Q1 PWP package and TPS7A6333-Q1 DRK are comparable; see Figure 33.

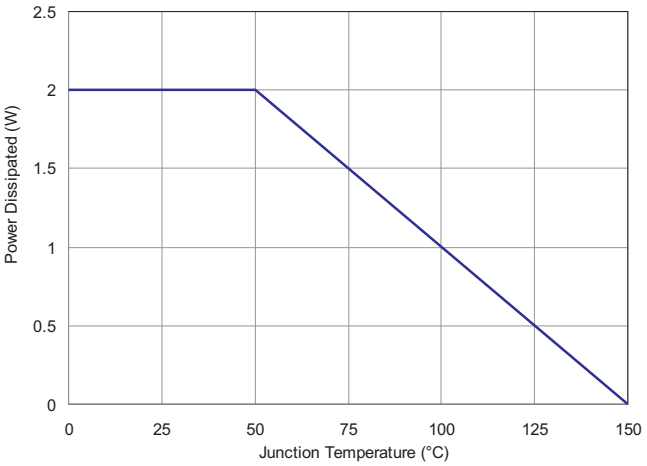
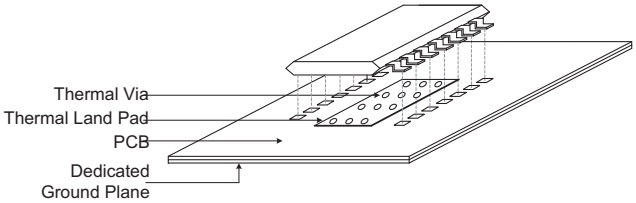
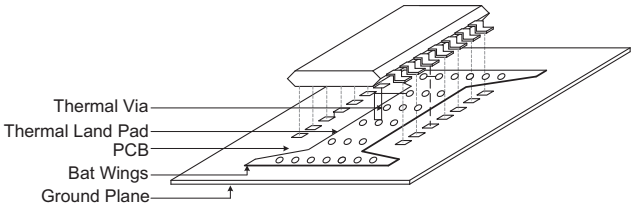


Figure 33. Power Derating Curve

For optimum thermal performance, TI recommends using a high-K PCB with thermal vias between the ground plane and solder pad or thermal land pad; see Figure 34 (a) and (b). Further, use a thicker ground plane and a thermal land pad with a larger surface area to inprove considerably the heat-spreading capabilities of a PCB. For a two-layer PCB, a bat wing layout can enhance the heat-spreading capabilities.



(a) Multilayer PCB with a dedicated ground plane



(b) Dual layer PCB with Bat wings for enhanced heat spreading

Figure 34. Using Multilayer PCB and Thermal Vias for Adequate Heat Dissipation

Keeping other factors constant, surface area of the thermal land pad contributes to heat dissipation only to a certain extent.

REVISION HISTORY

Changes from Original (June 2011) to Revision A **Page**

- Deleted the Ordering Information Table 2
- Changed values for V_{IL} and V_{IH} in the Watchdog Enable Input (nWD_EN pin) section 4
- Changed values for V_{IL} and V_{IH} in the Watchdog Input Pulse (WD pin) section 4

Changes from Revision A (August 2011) to Revision B **Page**

- Deleted devices TPS7A64333-Q1 and TPSA6450-Q1 1

Changes from Revision B (December 2011) to Revision C **Page**

- Changed regulated output voltage (6.1), added text to the test conditions (10mA to 200mA, $V_{IN} = V_{OUT}$ + 1V to 16V) 3

Changes from Revision C (April 2012) to Revision D **Page**

- Added new bullets at top of Features list 1
- Corrected part number in numerous locations throughout the data sheet 1
- Deleted the NO. column from the electrical tables 2
- 9
- Deleted two Typical Characteristics graphs 9

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS7A6301QPWPRQ1	ACTIVE	HTSSOP	PWP	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	7A6301	Samples
TPS7A6333QDRKRQ1	ACTIVE	VSON	DRK	10	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	PRGQ	Samples
TPS7A6333QPWPRQ1	ACTIVE	HTSSOP	PWP	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	7A6333	Samples
TPS7A6350QPWPRQ1	ACTIVE	HTSSOP	PWP	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	7A6350	Samples
TPS7A6401QPWPRQ1	ACTIVE	HTSSOP	PWP	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	7A6401	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

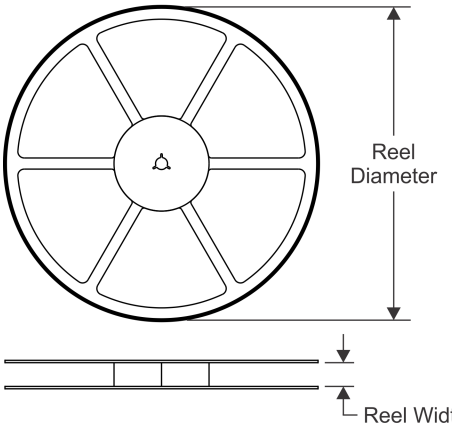
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

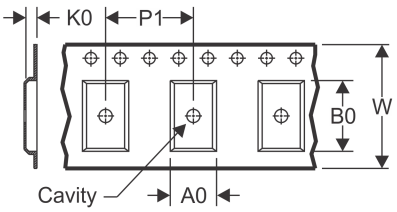
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

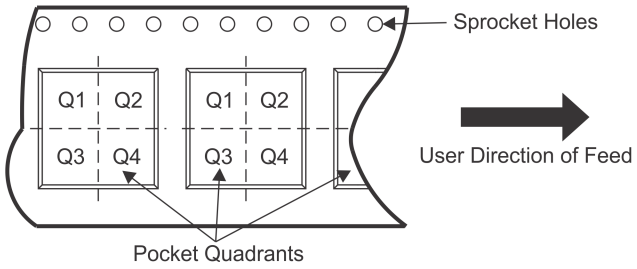


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

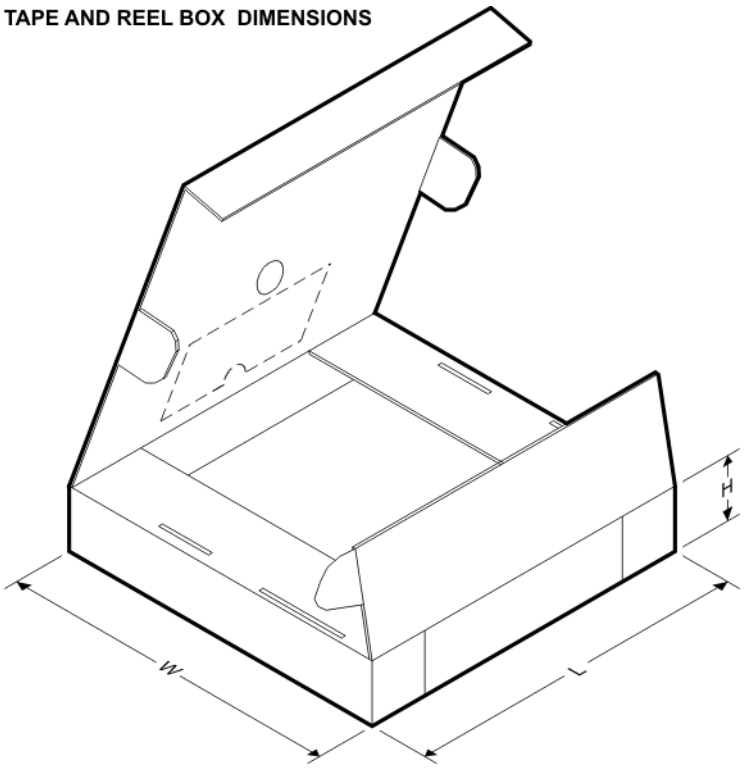
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS7A6301QPWPRQ1	HTSSOP	PWP	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TPS7A6333QDRKRQ1	VSON	DRK	10	3000	330.0	12.4	3.3	4.3	1.1	8.0	12.0	Q2
TPS7A6333QPWPRQ1	HTSSOP	PWP	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TPS7A6350QPWPRQ1	HTSSOP	PWP	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TPS7A6401QPWPRQ1	HTSSOP	PWP	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

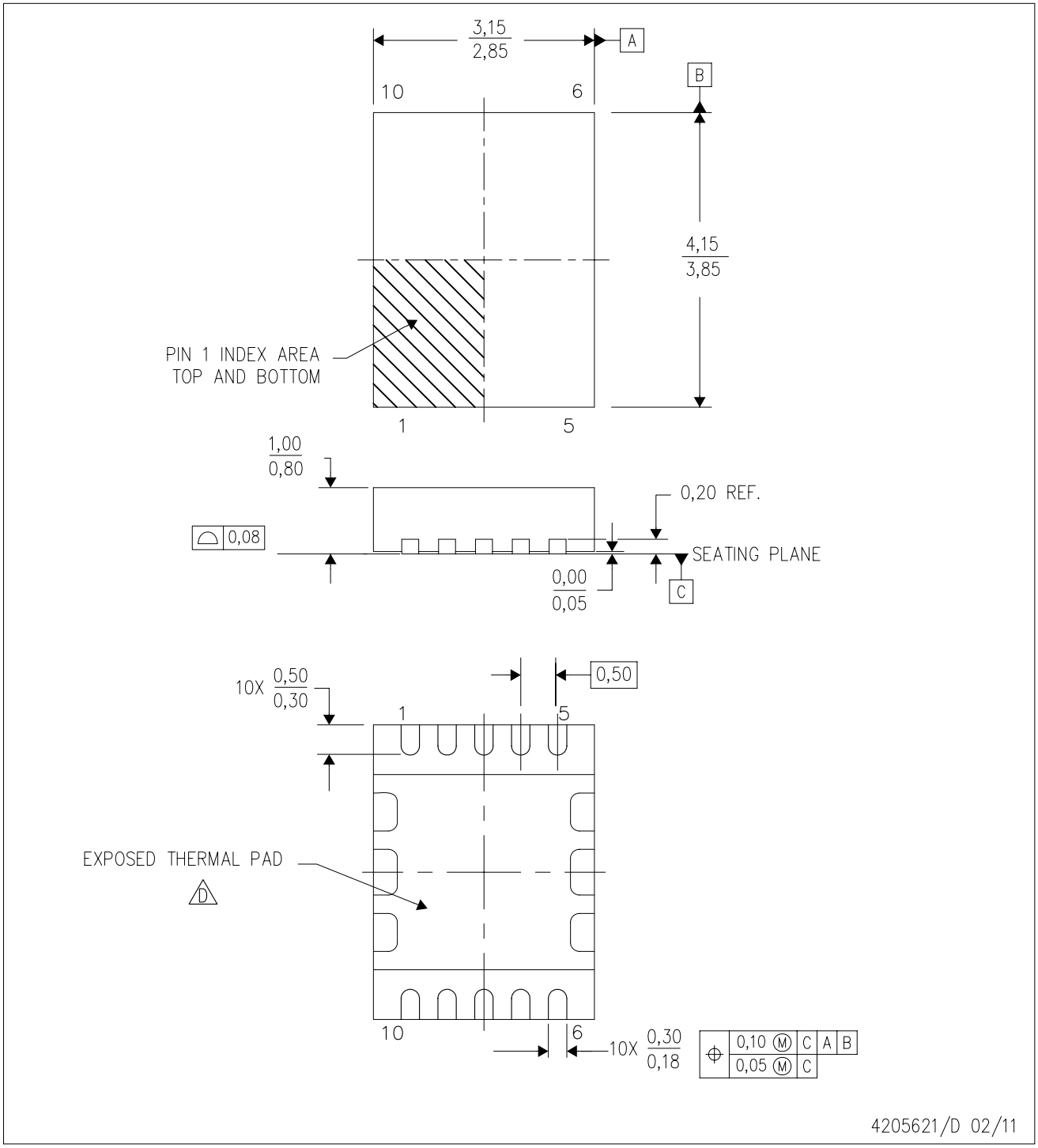
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS7A6301QPWPRQ1	HTSSOP	PWP	14	2000	367.0	367.0	35.0
TPS7A6333QDRKRQ1	VSON	DRK	10	3000	367.0	367.0	35.0
TPS7A6333QPWPRQ1	HTSSOP	PWP	14	2000	367.0	367.0	35.0
TPS7A6350QPWPRQ1	HTSSOP	PWP	14	2000	367.0	367.0	35.0
TPS7A6401QPWPRQ1	HTSSOP	PWP	14	2000	367.0	367.0	35.0

DRK (S–PVSON–N10) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5–1994.
B. This drawing is subject to change without notice.
C. Small Outline No–Lead (SON) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.

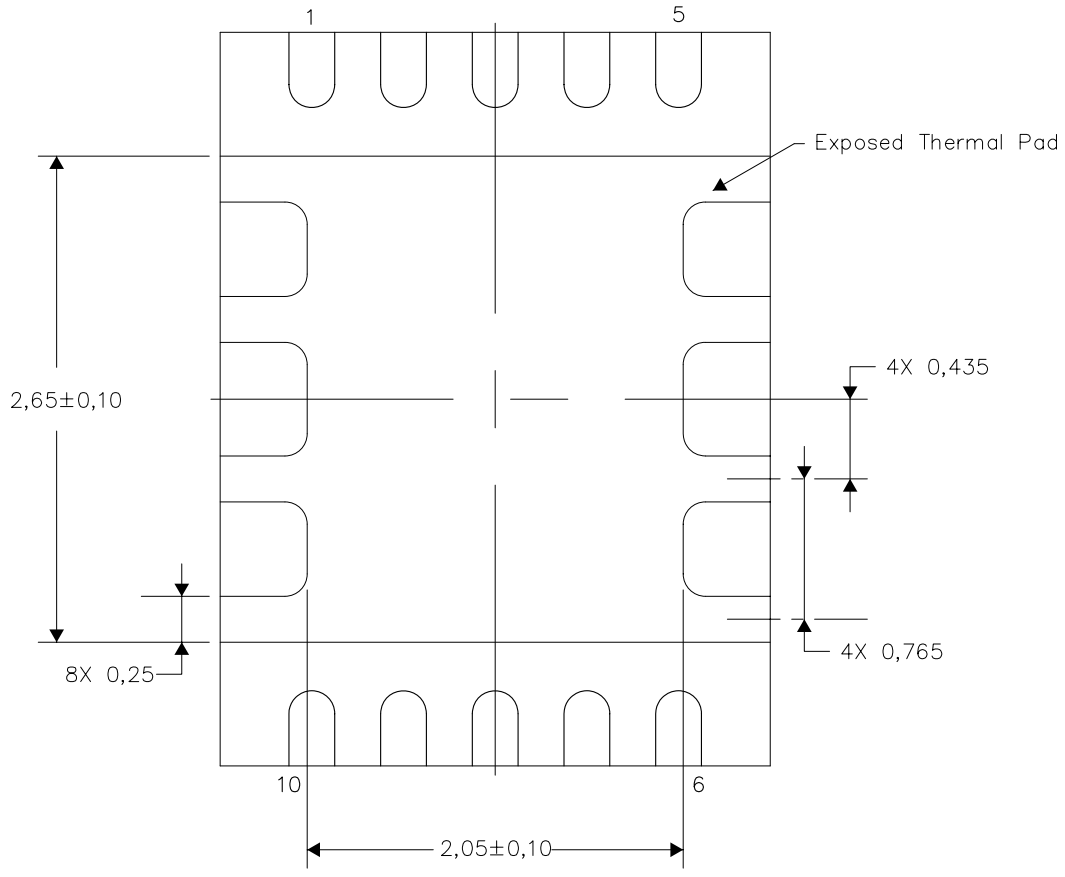
DRK (S–PVSON–N10) PLASTIC SMALL OUTLINE NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



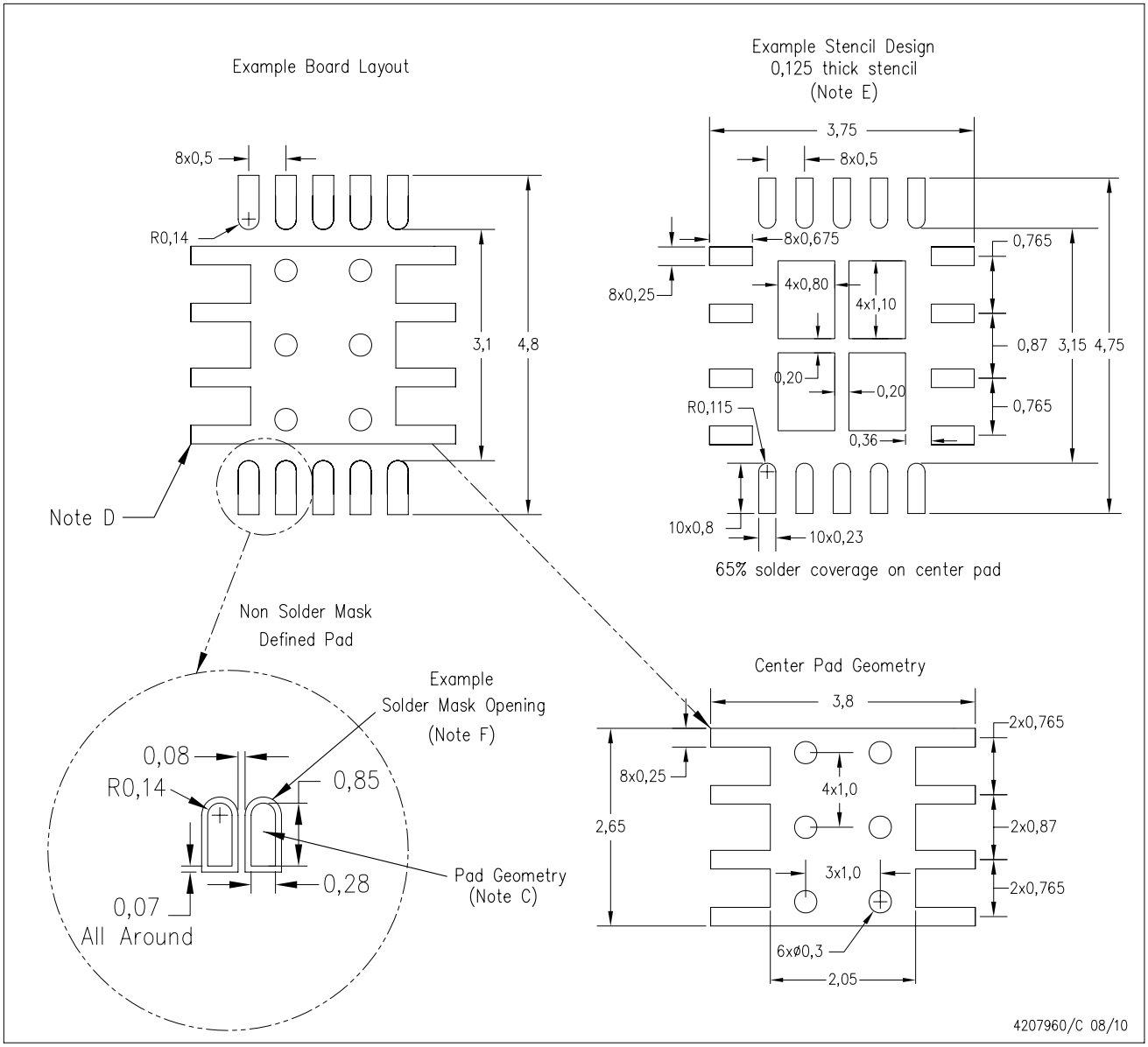
Bottom View

Exposed Thermal Pad Dimensions

4206317/F 08/10

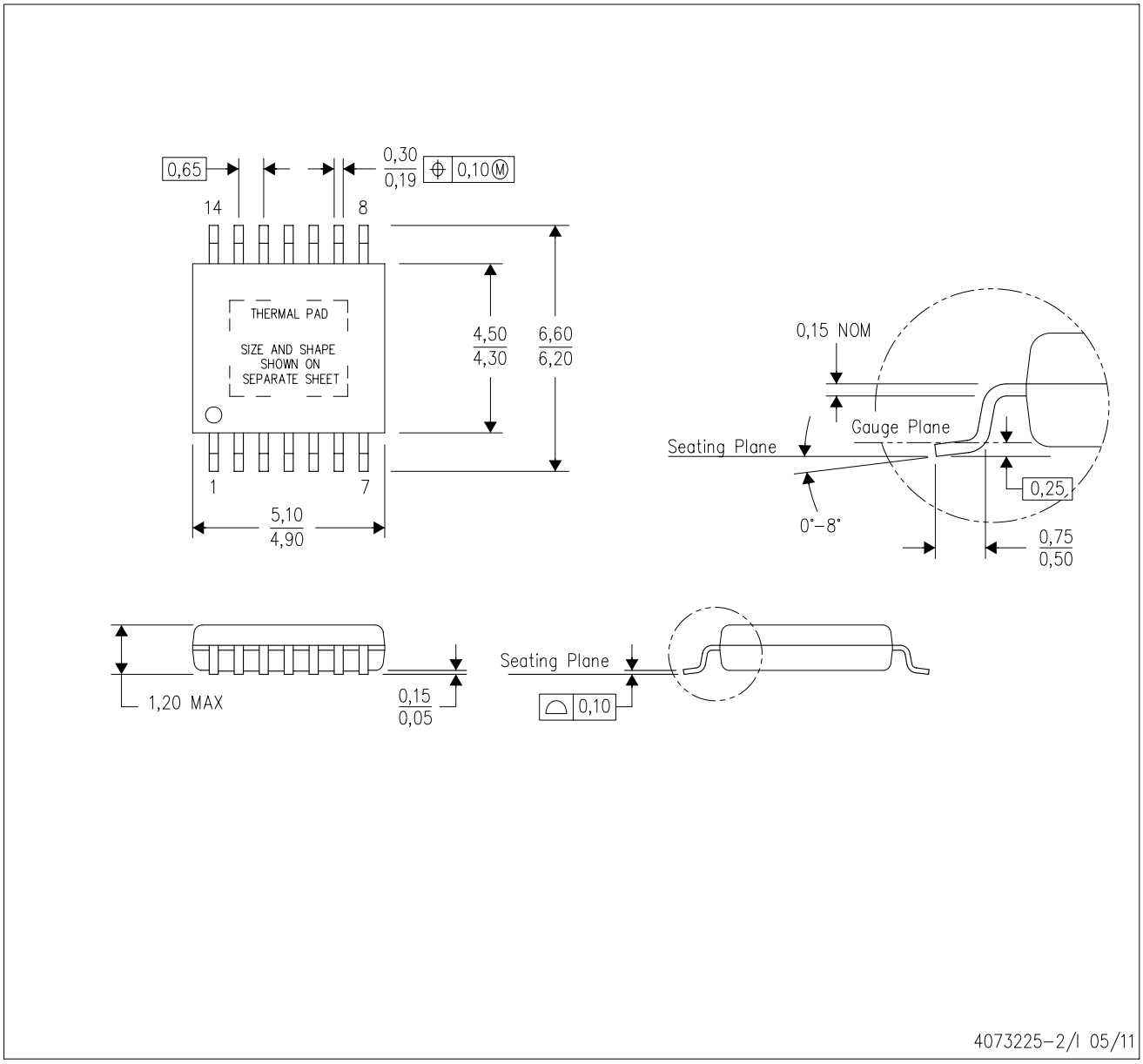
NOTE: A. All linear dimensions are in millimeters

DRK (S–PVSON–N10) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

PWP (R–PDSO–G14) PowerPAD™ PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
E. Falls within JEDEC MO–153

PowerPAD is a trademark of Texas Instruments.

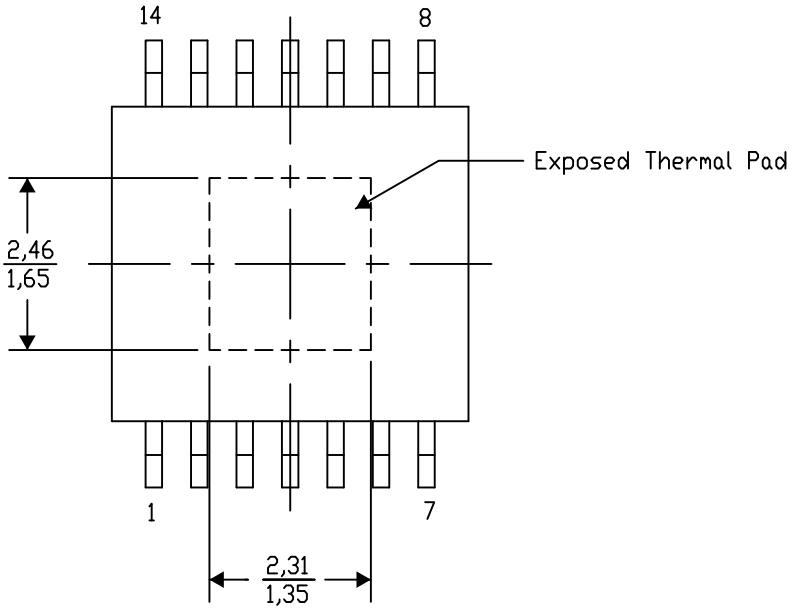
PWP (R–PDSO–G14) PowerPAD™ SMALL PLASTIC OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

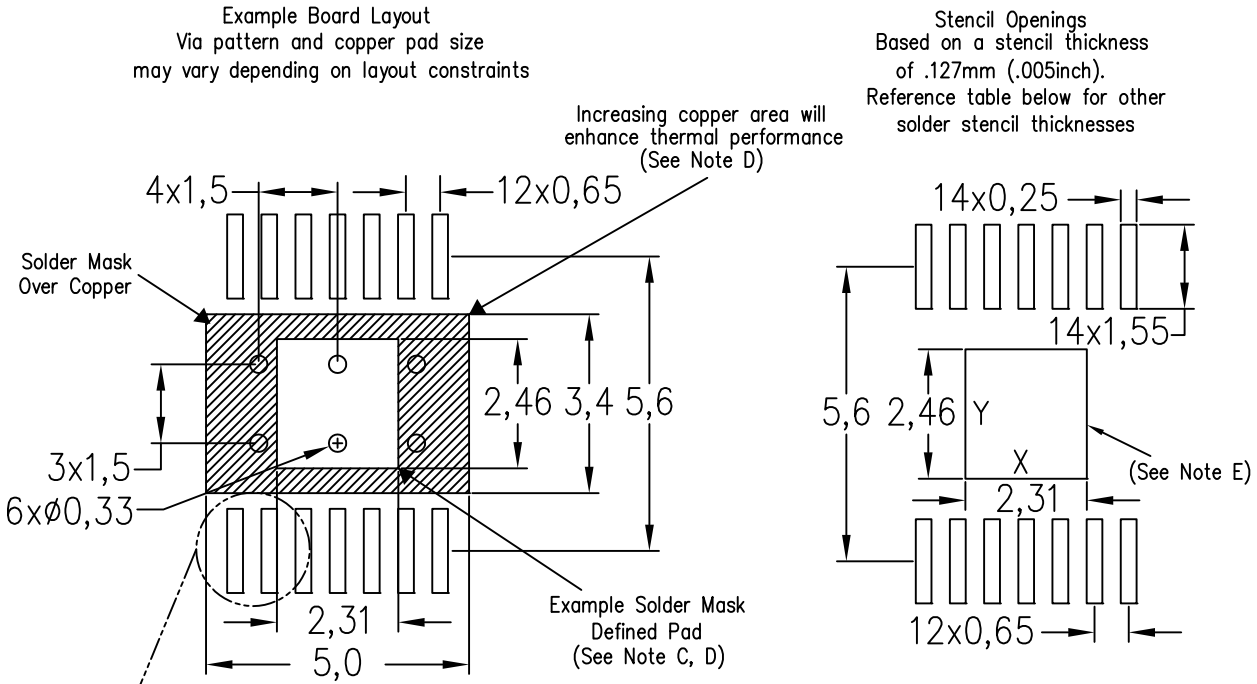
Exposed Thermal Pad Dimensions

4206332–2/AJ 10/14

NOTE: A. All linear dimensions are in millimeters

PowerPAD is a trademark of Texas Instruments

PWP (R–PDSO–G14) PowerPAD™ PLASTIC SMALL OUTLINE



Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	2.5	2.65
0.127mm	2.31	2.46
0.152mm	2.15	2.3
0.178mm	2.05	2.15

4207609–2/U 10/14

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

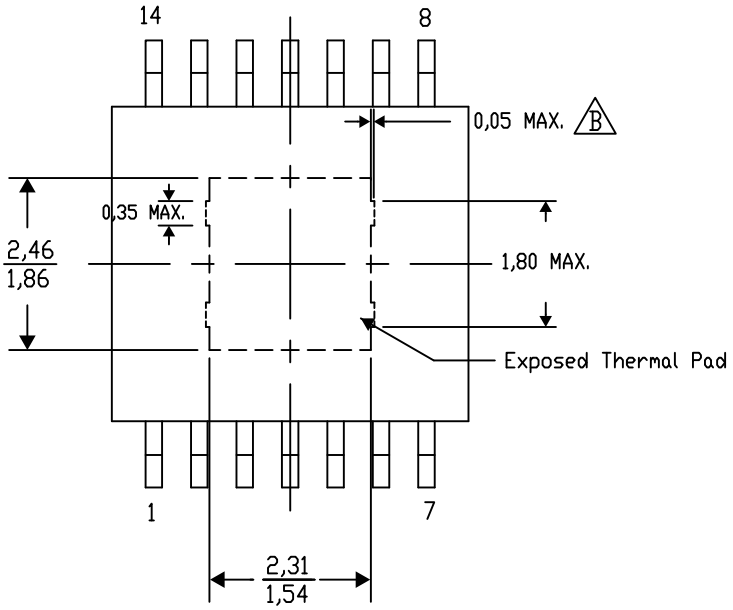
PWP (R–PDSO–G14) PowerPAD™ SMALL PLASTIC OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

Exposed Thermal Pad Dimensions

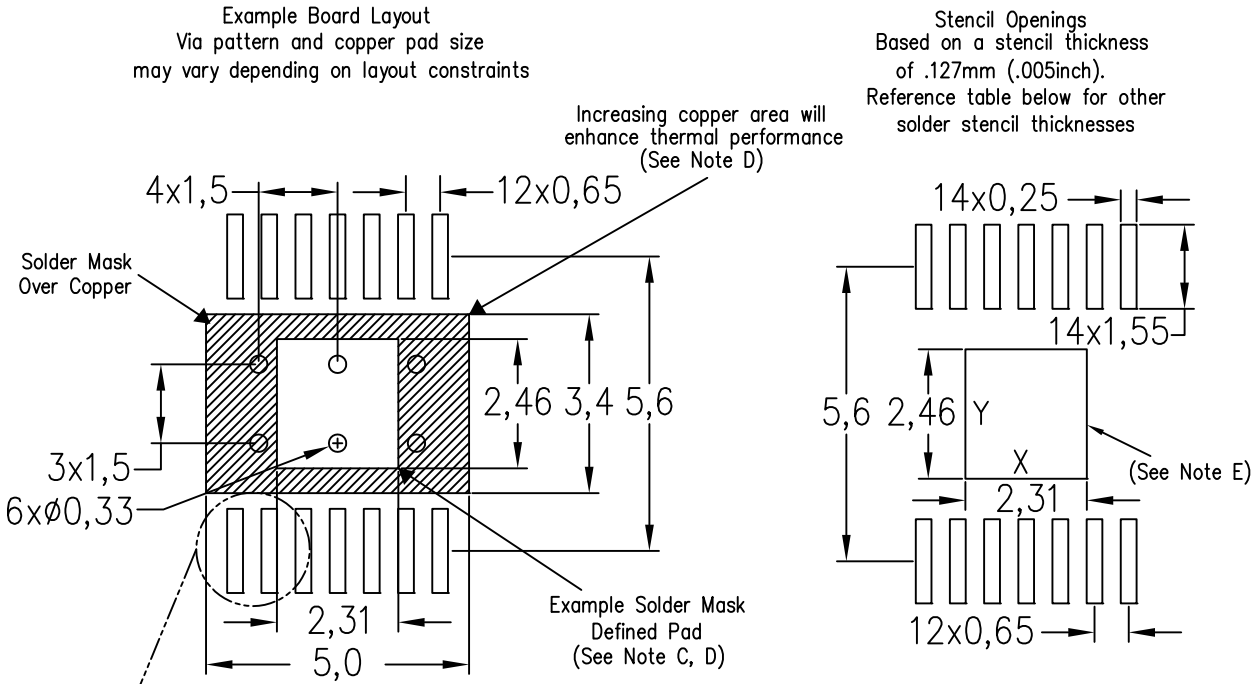
4206332–44/AJ 10/14

NOTE: A. All linear dimensions are in millimeters

B. Exposed tie strap features may not be present.

PowerPAD is a trademark of Texas Instruments

PWP (R–PDSO–G14) PowerPAD™ PLASTIC SMALL OUTLINE



Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	2.5	2.65
0.127mm	2.31	2.46
0.152mm	2.15	2.3
0.178mm	2.05	2.15

4207609–2/U 10/14

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
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F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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