

TPS7A30 –35-V, –200-mA, Ultralow-Noise, Negative Linear Regulator

1 Features

- Input Voltage Range: –3 V to –35 V
- Noise:
 - 14 μV_{RMS} (20 Hz to 20 kHz)
 - 15.1 μV_{RMS} (10 Hz to 100 kHz)
- Power-Supply Ripple Rejection:
 - 72 dB (120 Hz)
 - ≥ 55 dB (10 Hz to 700 kHz)
- Adjustable Output: –1.18 V to –33 V
- Maximum Output Current: 200 mA
- Dropout Voltage: 216 mV at 100 mA
- Stable With Ceramic Capacitors $\geq 2.2 \mu\text{F}$
- CMOS Logic-Level-Compatible Enable Pin
- Built-In, Fixed, Current Limit and Thermal Shutdown Protection
- Available in High Thermal Performance MSOP-8 PowerPAD™ Package
- Operating Temperature Range: –40°C to +125°C

2 Applications

- Supply Rails for Operational Amplifiers, DACs, ADCs, and Other High-Precision Analog Circuitry
- Audio
- Post DC-DC Converter Regulation and Ripple Filtering
- Test and Measurement
- RX, TX, and PA Circuitry
- Industrial Instrumentation
- Base Stations and Telecom Infrastructure
- –12-V and –24-V Industrial Buses

3 Description

The TPS7A30 series of devices are negative, high-voltage (–35 V), ultralow-noise (15.1 μV_{RMS} , 72-dB PSRR) linear regulators that can source a maximum load of 200 mA.

These linear regulators include a CMOS logic-level-compatible enable pin and capacitor-programmable soft-start function that allows for customized power-management schemes. Other features include built-in current limit and thermal shutdown protection to safeguard the device and system during fault conditions.

The TPS7A30 family is designed using bipolar technology, and is ideal for high-accuracy, high-precision instrumentation applications where clean voltage rails are critical to maximize system performance. This design makes the device an excellent choice to power operational amplifiers, analog-to-digital converters (ADCs), digital-to-analog converters (DACs), and other high-performance analog circuitry.

In addition, the TPS7A30 family of linear regulators is suitable for post DC-DC converter regulation. By filtering out the output voltage ripple inherent to DC-DC switching conversion, maximum system performance is provided in sensitive instrumentation, test and measurement, audio, and RF applications.

For applications that require positive and negative high-performance rails, consider TI's [TPS7A49](#) family of positive high-voltage, ultralow-noise linear regulators.

Device Information⁽¹⁾

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS7A30	HVSSOP (8)	3.00 mm x 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Post DC-DC Converter Regulation for High-Performance Analog Circuitry

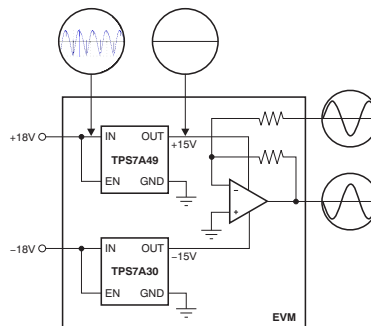


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4 Revision History

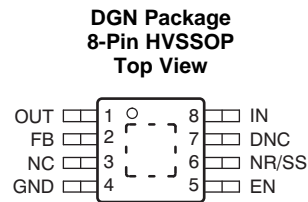
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (December 2013) to Revision C	Page
• Added <i>ESD Ratings</i> table, <i>Feature Description</i> section, <i>Device Functional Modes</i> , <i>Application and Implementation</i> section, <i>Power Supply Recommendations</i> section, <i>Layout</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section	1
• Changed document title	1
• Changed <i>Thermal Information</i> table; updated values	5
• Deleted <i>Dissipation Ratings</i> table	5
• Changed condition statement for <i>Electrical Characteristics</i> table	6
• Added footnote about measuring V_{REF} to <i>Electrical Characteristics</i> table	6
• Added V_{FB} parameter to <i>Electrical Characteristics</i> table	6
• Changed parametric symbol for current limit from I_{LIM} to I_{CL}	6
• Changed C_{BYP} notation to C_{FF} throughout data sheet	6
• Changed condition statement for <i>Typical Characteristics</i>	7
• Changed Figure 14 ; changed notation for C_{BYP} to C_{FF}	8
• Changed Figure 16 ; changed notation for C_{BYP} to C_{FF}	8
• Changed Figure 18 ; changed notation for C_{BYP} to C_{FF}	8
• Changed Figure 32 ; changed C_{BYP} to C_{FF}	18

Changes from Revision A (March 2011) to Revision B	Page
• Changed V_{REF} parameter typical specification in <i>Electrical Characteristics</i> table	6

Changes from Original (August 2010) to Revision A	Page
• Switched colors for 10mA and 200mA curves in Figure 10	7

5 Pin Configuration and Functions



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
OUT	1	O	Regulator output. A capacitor $\geq 2.2 \mu\text{F}$ must be tied from this pin to ground to ensure stability.
FB	2	I	This pin is the feedback pin that sets the output voltage of the device.
NC	3	—	Not internally connected. This pin must either be left open or tied to GND.
GND	4	—	Ground
EN	5	I	This pin turns the regulator on or off. If $V_{\text{EN}} \geq V_{\text{EN}(+\text{HI})}$ or $V_{\text{EN}} \leq V_{\text{EN}(-\text{HI})}$, the regulator is enabled. If $V_{\text{EN}(+\text{LO})} \geq V_{\text{EN}} \geq V_{\text{EN}(-\text{LO})}$, the regulator is disabled. The EN pin can be connected to IN, if not used. $ V_{\text{EN}} \leq V_{\text{IN}} $.
NR/SS	6	—	Noise reduction pin. Connecting an external capacitor to this pin filters the noise generated by the internal bandgap. This capacitor allows RMS noise to be reduced to very low levels and also controls the soft-start function.
DNC	7	—	DO NOT CONNECT. Do not route this pin to any electrical net, not even GND or IN.
IN	8	I	Input supply
PowerPAD	—	—	Must either be left open or tied to GND. Solder to printed-circuit-board (PCB) plane to enhance thermal performance.

6 Specifications

6.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted).⁽¹⁾

		MIN	MAX	UNIT
Voltage	IN pin to GND pin	–36	0.3	V
	OUT pin to GND pin	–33	0.3	
	OUT pin to IN pin	–0.3	36	
	FB pin to GND pin	–2	0.3	
	FB pin to IN pin	–0.3	36	
	EN pin to IN pin	–0.3	36	
	EN pin to GND pin	–36	36	
	NR/SS pin to IN pin	–0.3	36	
	NR/SS pin to GND pin	–2	0.3	
Current	Peak output	Internally limited		
Temperature	Operating virtual junction, T _J	–40	125	°C
	Storage, T _{stg}	–65	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated is not implied. Exposure to absolute-maximum rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

		VALUE	UNIT
V _(ESD) Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins ⁽¹⁾	±1500	V
	Charged device model (CDM), per JEDEC specification JESD22-C101, all pins ⁽²⁾	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V _{IN}	Input supply voltage	–35		–3	V
V _{EN}	Enable supply voltage	0		V _{IN}	V
V _{OUT}	Output voltage	V _{REF}		33	V
I _{OUT}	Output current	0		200	mA
T _J	Operating junction temperature	–40		125	°C
C _{IN}	Input capacitor	2.2	10		μF
C _{OUT}	Output capacitor	2.2	10		μF
C _{NR}	Noise reduction capacitor	0	10		nF
C _{FF}	Feed-forward capacitor	0	10		nF
R ₂	Lower feedback resistor			237	kΩ

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		TPS7A30	UNIT
		DGN [HVSSOP]	
		8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	63.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case(top) thermal resistance	53	
$R_{\theta JB}$	Junction-to-board thermal resistance	37.4	
ψ_{JT}	Junction-to-top characterization parameter	3.7	
ψ_{JB}	Junction-to-board characterization parameter	37.1	
$R_{\theta JC(bot)}$	Junction-to-case(bottom) thermal resistance	13.5	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

6.5 Electrical Characteristics⁽¹⁾

At $T_J = -40^\circ\text{C}$ to $+125^\circ\text{C}$, $|V_{IN}| = |V_{OUT(nom)}| + 1\text{ V}$ or $|V_{IN}| = 3\text{ V}$ (whichever is greater), $V_{EN} = V_{IN}$, $I_{OUT} = 1\text{ mA}$, $C_{IN} = 2.2\text{ }\mu\text{F}$, $C_{OUT} = 2.2\text{ }\mu\text{F}$, $C_{NR/SS} = 0\text{ nF}$, and the FB pin tied to OUT, unless otherwise noted. Typical values are at $T_A = 25^\circ\text{C}$.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN}	Input voltage		-35		-3	V
V_{REF}	Internal reference ⁽²⁾	$T_J = 25^\circ\text{C}$, $V_{NR/SS} = V_{REF}$	-1.202	-1.179	-1.166	V
V_{FB}	Feedback voltage			-1.176		V
V_{OUT}	Output voltage range ⁽³⁾	$ V_{IN} \geq V_{OUT(nom)} + 1\text{ V}$	-33		V_{REF}	V
	Nominal accuracy	$T_J = 25^\circ\text{C}$, $ V_{IN} = V_{OUT(nom)} + 0.5\text{ V}$	-1.5		1.5	% V_{OUT}
	Overall accuracy	$ V_{OUT(nom)} + 1\text{ V} \leq V_{IN} \leq 35\text{ V}$ $1\text{ mA} \leq I_{OUT} \leq 200\text{ mA}$	-2.5		2.5	
$\frac{ \Delta V_{OUT}(\Delta V_{IN}) }{V_{OUT(NOM)}}$	Line regulation	$T_J = 25^\circ\text{C}$, $ V_{OUT(nom)} + 1\text{ V} \leq V_{IN} \leq 35\text{ V}$		0.14		% V_{OUT}
$\frac{ \Delta V_{OUT}(\Delta I_{OUT}) }{V_{OUT(NOM)}}$	Load regulation	$T_J = 25^\circ\text{C}$, $1\text{ mA} \leq I_{OUT} \leq 200\text{ mA}$		0.04		% V_{OUT}
$ V_{DO} $	Dropout voltage	$V_{IN} = 95\% V_{OUT(nom)}$, $I_{OUT} = 100\text{ mA}$		216		mV
		$V_{IN} = 95\% V_{OUT(nom)}$, $I_{OUT} = 200\text{ mA}$		325	600	
I_{CL}	Current limit	$V_{OUT} = 90\% V_{OUT(nom)}$	220	330	500	mA
I_{GND}	Ground current	$I_{OUT} = 0\text{ mA}$		55	100	μA
		$I_{OUT} = 100\text{ mA}$		950		
$ I_{SHDN} $	Shutdown supply current	$V_{EN} = 0.4\text{ V}$		1	3	μA
		$V_{EN} = -0.4\text{ V}$		1	3	
I_{FB}	Feedback current ⁽⁴⁾			14	100	nA
$ I_{EN} $	Enable current	$V_{EN} = V_{IN} = V_{OUT(nom)} + 1\text{ V}$		0.48	1	μA
		$V_{IN} = V_{EN} = -35\text{ V}$		0.51	1	
		$V_{IN} = -35\text{ V}$, $V_{EN} = +15\text{ V}$		0.5	1	
$V_{EN(+HI)}$	Positive enable high-level voltage	$T_J = -40^\circ\text{C}$ to $+125^\circ\text{C}$	2		15	V
		$T_J = -40^\circ\text{C}$ to $+85^\circ\text{C}$	1.8		15	
$V_{EN(+LO)}$	Positive enable low-level voltage		0		0.4	V
$V_{EN(-HI)}$	Negative enable high-level voltage		V_{IN}		-2	V
$V_{EN(-LO)}$	Negative enable low-level voltage		-0.4		0	V
V_n	Output noise voltage	$V_{IN} = -3\text{ V}$, $V_{OUT(nom)} = V_{REF}$, $C_{OUT} = 10\text{ }\mu\text{F}$, $C_{NR/SS} = 10\text{ nF}$, $BW = 10\text{ Hz to }100\text{ kHz}$		15.1		μV_{RMS}
		$V_{IN} = -6.2\text{ V}$, $V_{OUT(nom)} = -5\text{ V}$, $C_{OUT} = 10\text{ }\mu\text{F}$, $C_{NR/SS} = C_{FF}^{(5)} = 10\text{ nF}$, $BW = 10\text{ Hz to }100\text{ kHz}$		17.5		
PSRR	Power-supply rejection ratio	$V_{IN} = -6.2\text{ V}$, $V_{OUT(nom)} = -5\text{ V}$, $C_{OUT} = 10\text{ }\mu\text{F}$, $C_{NR/SS} = C_{FF}^{(5)} = 10\text{ nF}$, $f = 120\text{ Hz}$		72		dB
T_{SD}	Thermal shutdown temperature	Shutdown, temperature increasing		170		$^\circ\text{C}$
		Reset, temperature decreasing		150		
T_J	Operating junction temperature range		-40		125	$^\circ\text{C}$

(1) At operating conditions, $V_{IN} \leq 0\text{ V}$, $V_{OUT(nom)} \leq V_{REF} \leq 0\text{ V}$. At regulation, $V_{IN} \leq V_{OUT(nom)} - |V_{DO}|$. $I_{OUT} > 0$ flows from OUT to IN.

(2) V_{REF} is measured at the NR/SS pin.

(3) To ensure stability at no load conditions, a current from the feedback resistive network equal to or greater than $5\text{ }\mu\text{A}$ is required.

(4) $I_{FB} > 0$ flows into the device.

(5) C_{FF} refers to a feed-forward capacitor connected to the FB and OUT pins.

6.6 Typical Characteristics

At $T_J = -40^\circ\text{C}$ to $+125^\circ\text{C}$, $|V_{IN}| = |V_{OUT(nom)}| + 1\text{ V}$ or $|V_{IN}| = 3\text{ V}$ (whichever is greater), $V_{EN} = V_{IN}$, $I_{OUT} = 1\text{ mA}$, $C_{IN} = 2.2\ \mu\text{F}$, $C_{OUT} = 2.2\ \mu\text{F}$, $C_{NR/SS} = 0\text{ nF}$, and $V_{OUT} = V_{FB}$, unless otherwise noted. Typical values are at $T_A = 25^\circ\text{C}$.

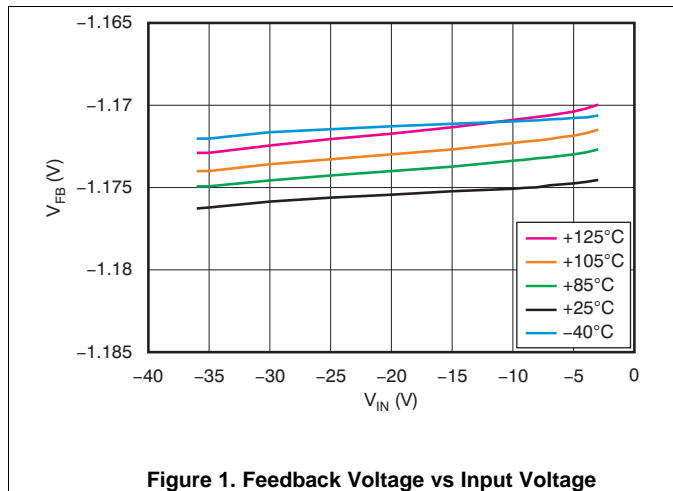


Figure 1. Feedback Voltage vs Input Voltage

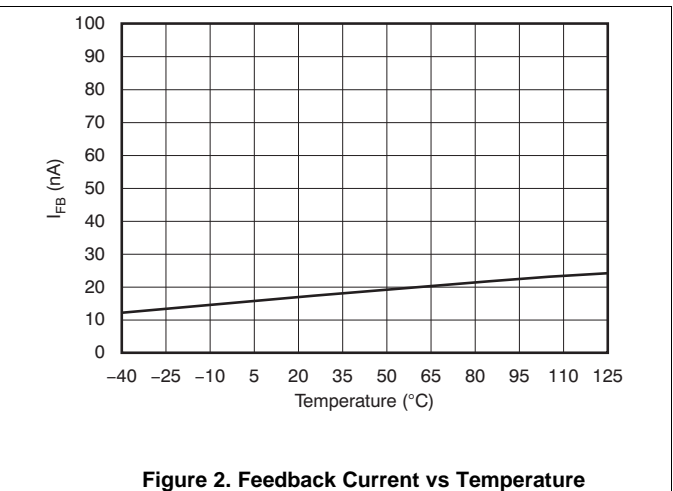


Figure 2. Feedback Current vs Temperature

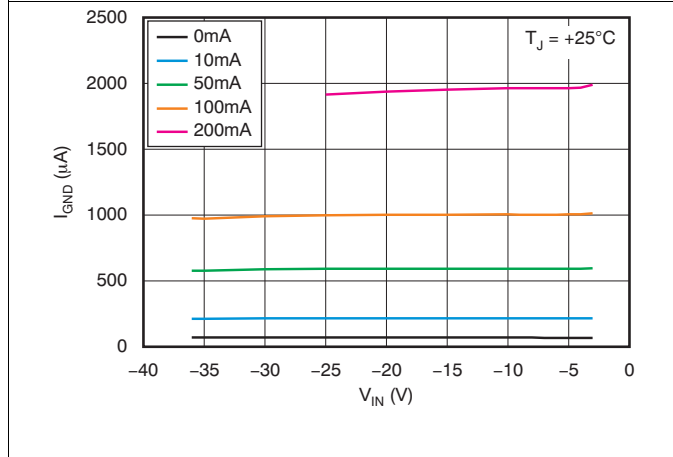


Figure 3. Ground Current vs Input Voltage

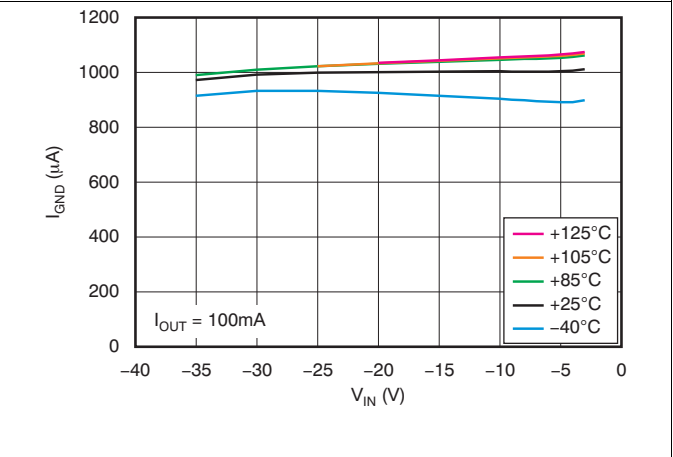


Figure 4. Ground Current vs Input Voltage

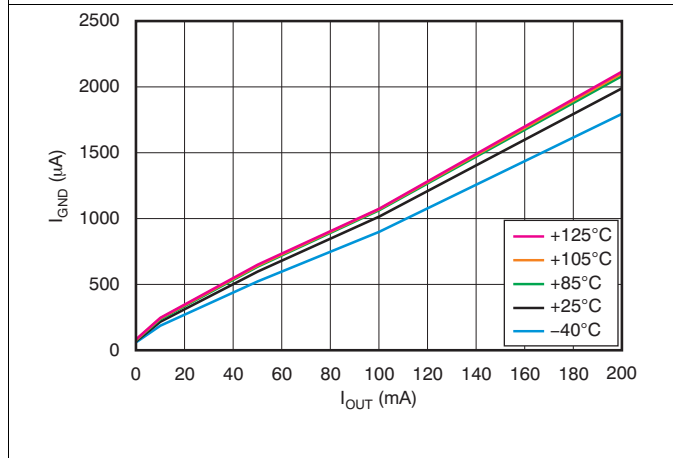


Figure 5. Ground Current vs Output Current

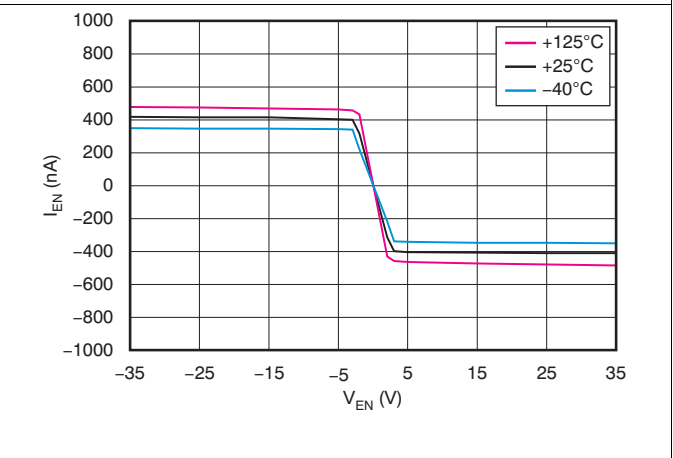


Figure 6. Enable Current vs Enable Voltage

Typical Characteristics (continued)

At $T_J = -40^\circ\text{C}$ to $+125^\circ\text{C}$, $|V_{IN}| = |V_{OUT(nom)}| + 1\text{ V}$ or $|V_{IN}| = 3\text{ V}$ (whichever is greater), $V_{EN} = V_{IN}$, $I_{OUT} = 1\text{ mA}$, $C_{IN} = 2.2\ \mu\text{F}$, $C_{OUT} = 2.2\ \mu\text{F}$, $C_{NR/SS} = 0\text{ nF}$, and $V_{OUT} = V_{FB}$, unless otherwise noted. Typical values are at $T_A = 25^\circ\text{C}$.

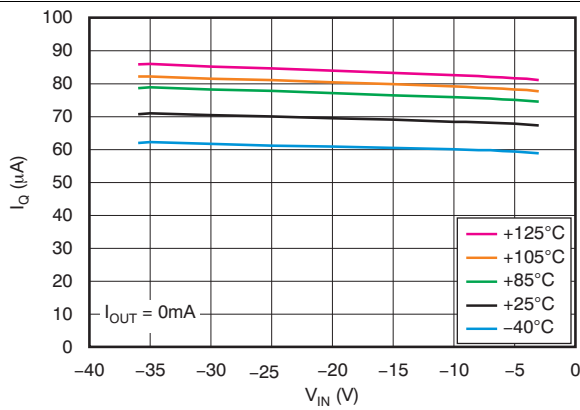


Figure 7. Quiescent Current vs Input Voltage

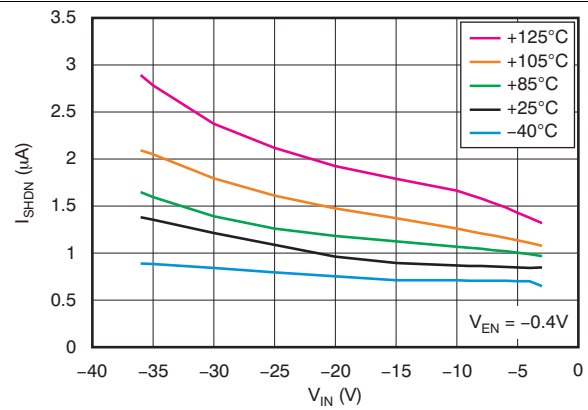


Figure 8. Shutdown Current vs Input Voltage

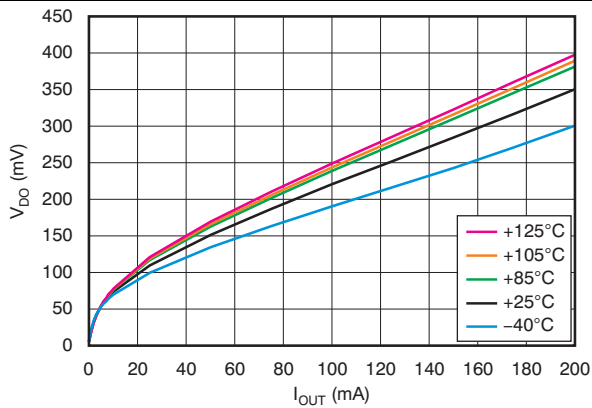


Figure 9. Dropout Voltage vs Output Current

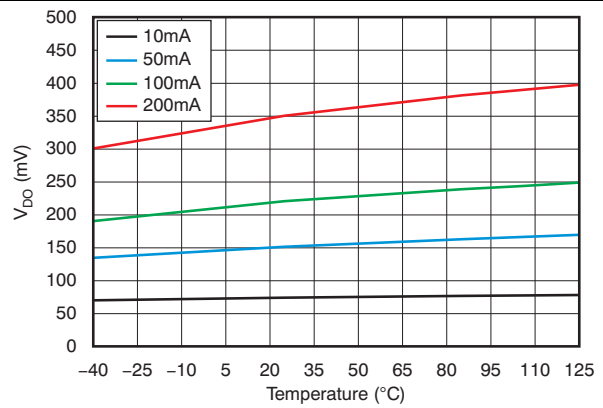


Figure 10. Dropout Voltage vs Temperature

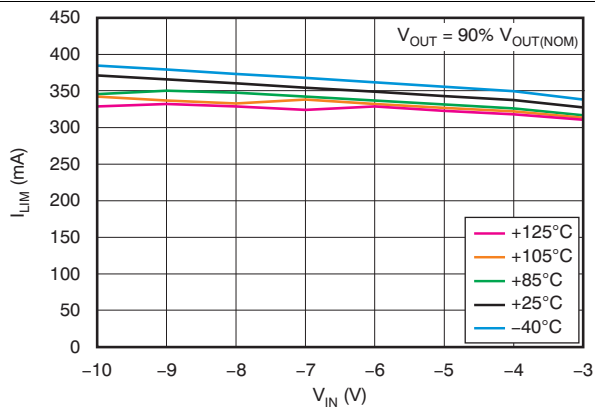


Figure 11. Current Limit vs Input Voltage

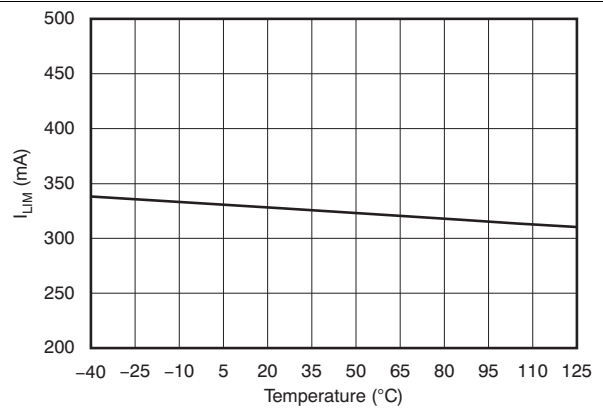


Figure 12. Current Limit vs Temperature

Typical Characteristics (continued)

At $T_J = -40^\circ\text{C}$ to $+125^\circ\text{C}$, $|V_{IN}| = |V_{OUT(nom)}| + 1\text{ V}$ or $|V_{IN}| = 3\text{ V}$ (whichever is greater), $V_{EN} = V_{IN}$, $I_{OUT} = 1\text{ mA}$, $C_{IN} = 2.2\text{ }\mu\text{F}$, $C_{OUT} = 2.2\text{ }\mu\text{F}$, $C_{NR/SS} = 0\text{ nF}$, and $V_{OUT} = V_{FB}$, unless otherwise noted. Typical values are at $T_A = 25^\circ\text{C}$.

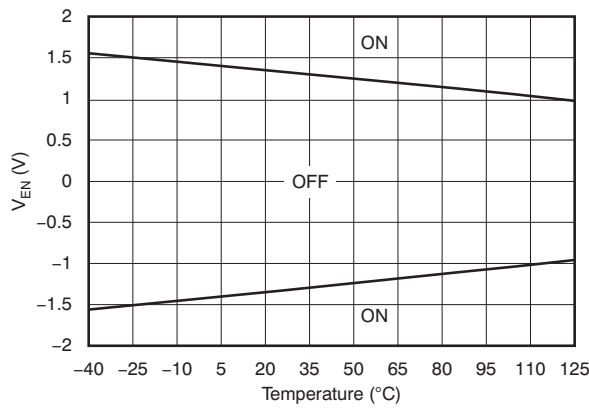


Figure 13. Enable Threshold Voltage vs Temperature

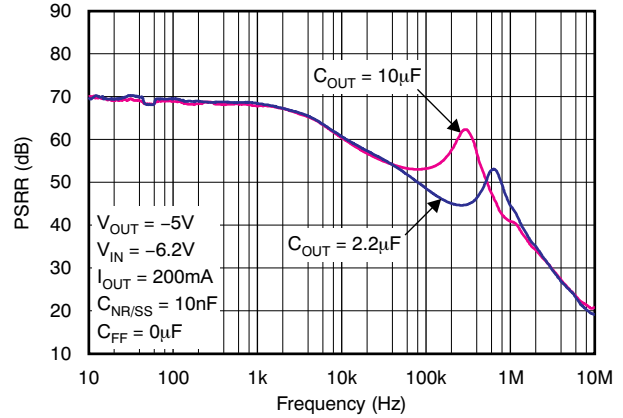


Figure 14. Power Supply Rejection Ratio vs C_{OUT}

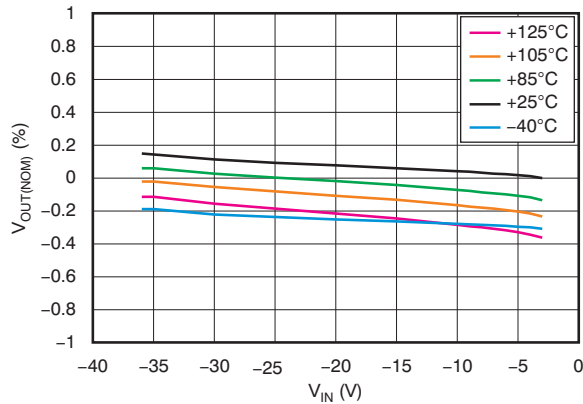


Figure 15. Line Regulation

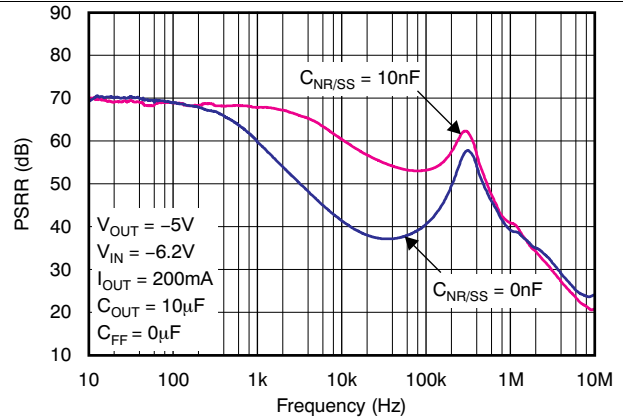


Figure 16. Power Supply Rejection Ratio vs $C_{NR/SS}$

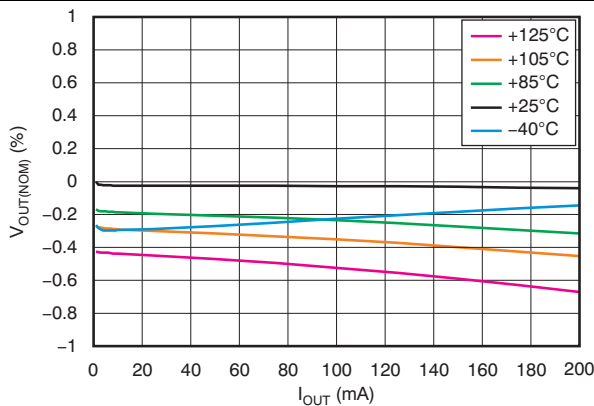


Figure 17. Load Regulation

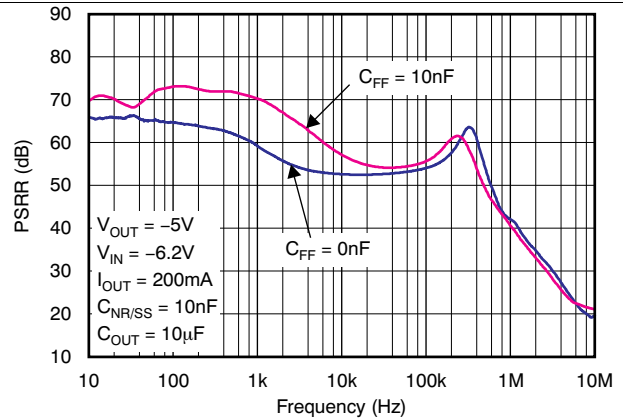


Figure 18. Power Supply Rejection Ratio vs C_{FF}

Typical Characteristics (continued)

At $T_J = -40^\circ\text{C}$ to $+125^\circ\text{C}$, $|V_{IN}| = |V_{OUT(nom)}| + 1\text{ V}$ or $|V_{IN}| = 3\text{ V}$ (whichever is greater), $V_{EN} = V_{IN}$, $I_{OUT} = 1\text{ mA}$, $C_{IN} = 2.2\text{ }\mu\text{F}$, $C_{OUT} = 2.2\text{ }\mu\text{F}$, $C_{NR/SS} = 0\text{ nF}$, and $V_{OUT} = V_{FB}$, unless otherwise noted. Typical values are at $T_A = 25^\circ\text{C}$.

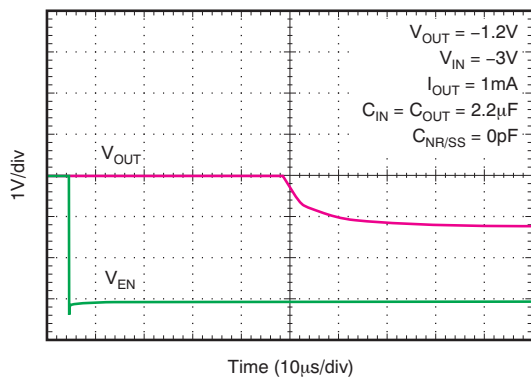


Figure 19. Capacitor-Programmable Soft-Start

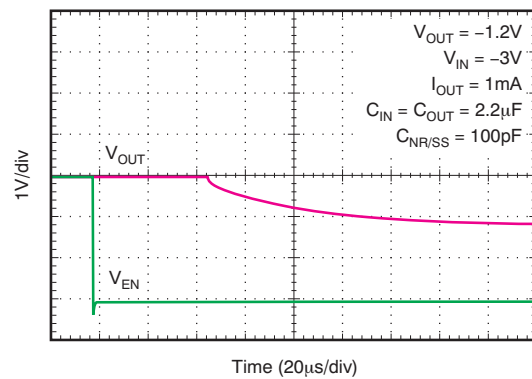


Figure 20. Capacitor-Programmable Soft-Start

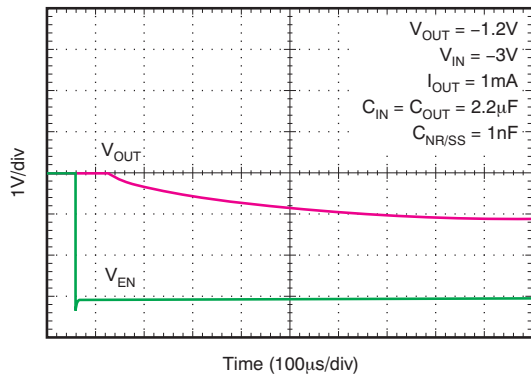


Figure 21. Capacitor-Programmable Soft-Start

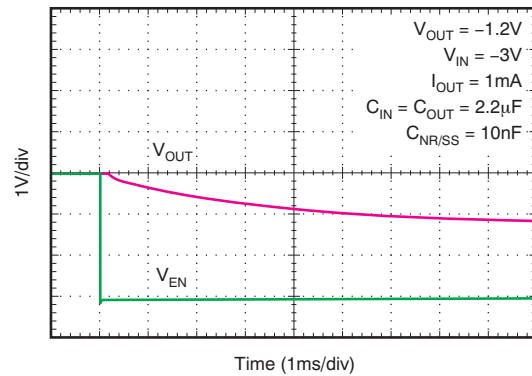


Figure 22. Capacitor-Programmable Soft-Start

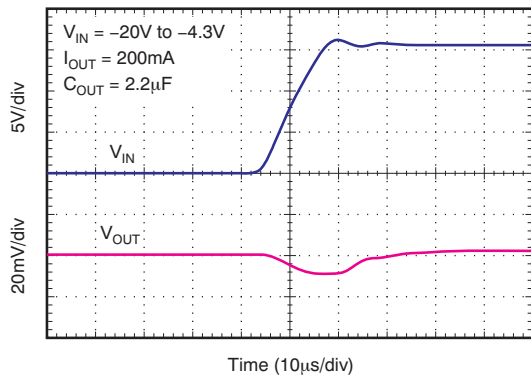


Figure 23. Line Transient Response

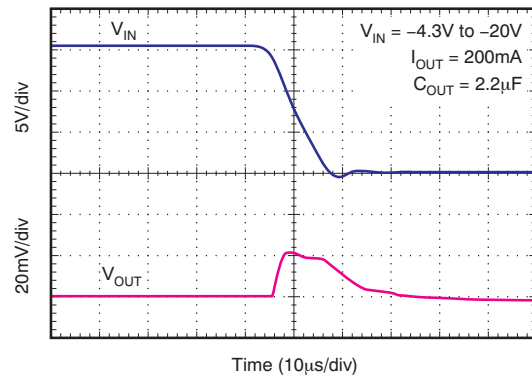


Figure 24. Line Transient Response

Typical Characteristics (continued)

At $T_J = -40^\circ\text{C}$ to $+125^\circ\text{C}$, $|V_{IN}| = |V_{OUT(nom)}| + 1\text{ V}$ or $|V_{IN}| = 3\text{ V}$ (whichever is greater), $V_{EN} = V_{IN}$, $I_{OUT} = 1\text{ mA}$, $C_{IN} = 2.2\text{ }\mu\text{F}$, $C_{OUT} = 2.2\text{ }\mu\text{F}$, $C_{NR/SS} = 0\text{ nF}$, and $V_{OUT} = V_{FB}$, unless otherwise noted. Typical values are at $T_A = 25^\circ\text{C}$.

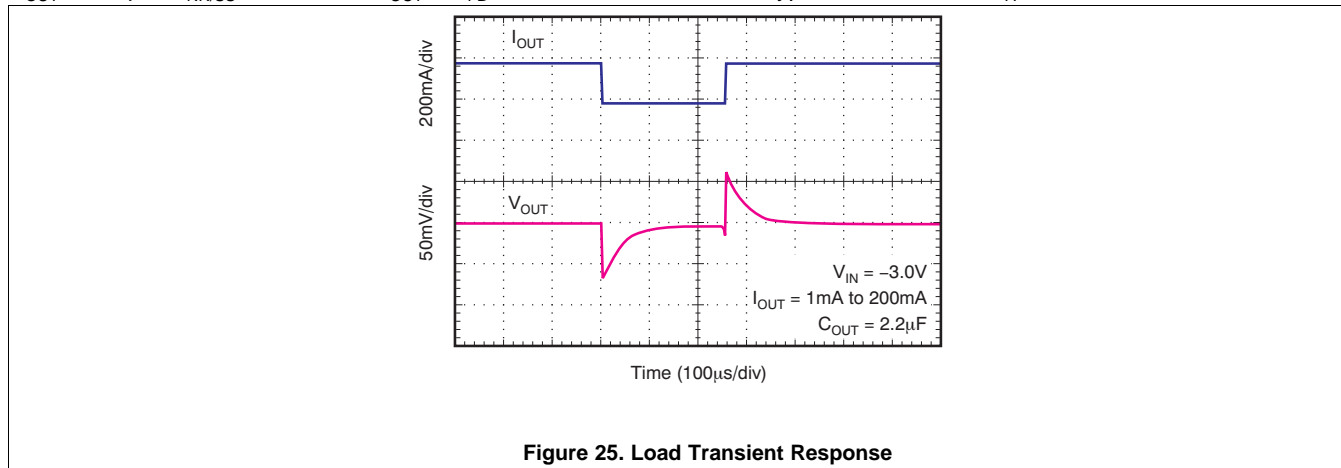
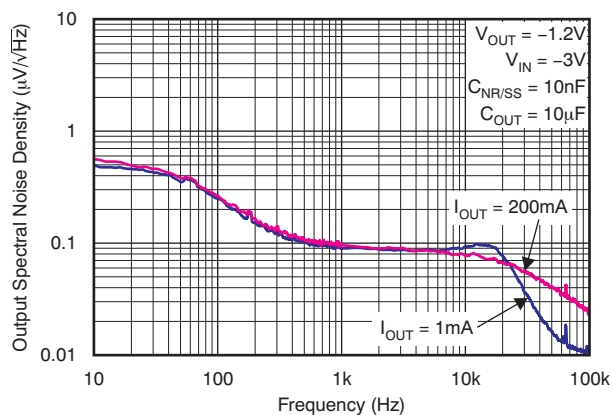


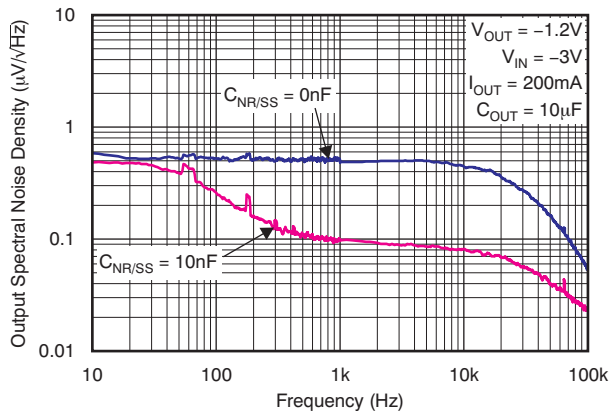
Figure 25. Load Transient Response

7 Parameter Measurement Information



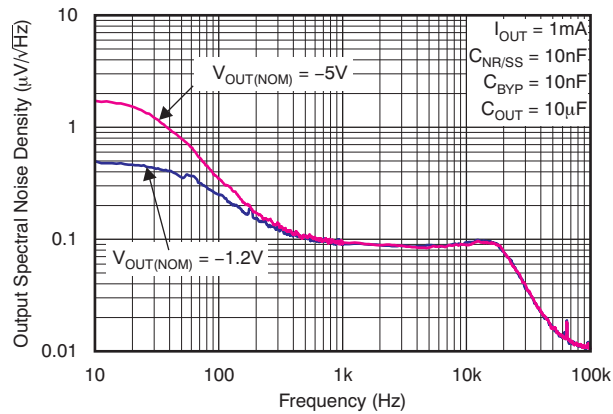
I_{OUT}	RMS NOISE	
	10Hz to 100kHz	100Hz to 100kHz
1mA	15.13	14.73
200mA	17.13	16.71

Figure 26. Output Spectral Noise Density vs Output Current



$C_{NR/SS}$	RMS NOISE	
	10Hz to 100kHz	100Hz to 100kHz
0nF	80.00	79.83
10nF	17.29	16.81

Figure 27. Output Spectral Noise Density vs $C_{NR/SS}$

Parameter Measurement Information (continued)


$V_{OUT(NOM)}$	RMS NOISE	
	10Hz to 100kHz	100Hz to 100kHz
-5V	17.50	15.04
-1.2V	15.13	14.73

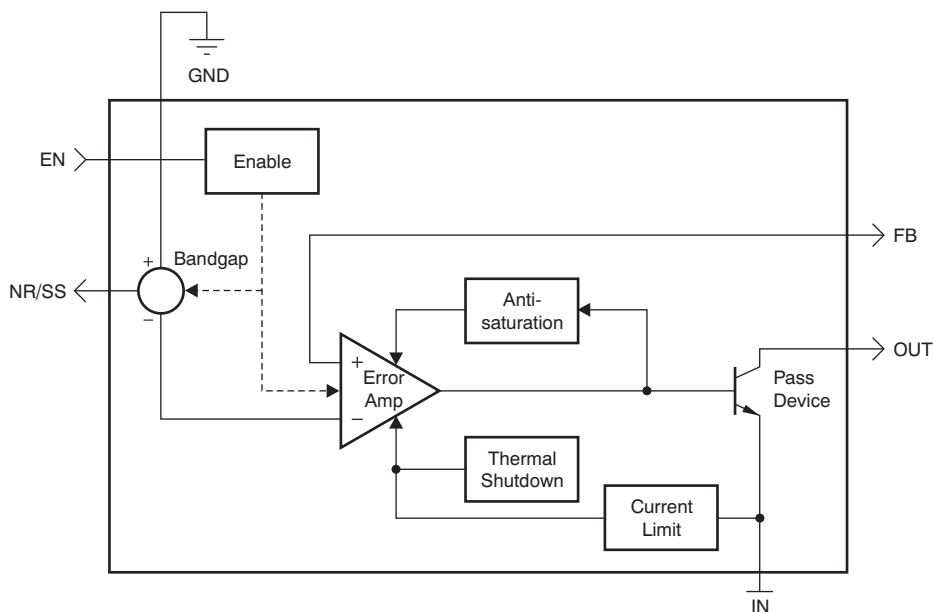
Figure 28. Output Spectral Noise Density vs $V_{OUT(nom)}$

8 Detailed Description

8.1 Overview

The TPS7A30 family of devices are wide V_{IN} , low-noise, 150-mA linear regulators (LDOs). These devices feature an enable pin, programmable soft-start, current limiting, and thermal protection circuitry that allow the device to be used in a wide variety of applications. As bipolar-based devices, the TPS7A30 devices are ideal for high-accuracy, high-precision applications at higher voltages.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Internal Current Limit

The fixed internal current limit of the TPS7A30 family helps protect the regulator during fault conditions. The maximum amount of current the device can source is the current limit (330 mA, typical), and it is largely independent of output voltage. For reliable operation, do not operate the device in current limit for extended periods of time.

8.3.2 Programmable Soft-Start

The NR/SS capacitor also acts as a soft-start capacitor to slow down the rise time of the output. The rise time of the output when using an NR/SS capacitor is governed by Equation 1. In Equation 1, t_{SS} is the soft-start time in milliseconds, and $C_{NR/SS}$ is the capacitance at the NR pin in nanofarads. Figure 29 shows the relationship between the $C_{NR/SS}$ size and the start-up time without a C_{FF} .

$$t_{SS} \text{ (ms)} = 0.9 \times C_{NR/SS} \text{ (nF)} \quad (1)$$

Feature Description (continued)

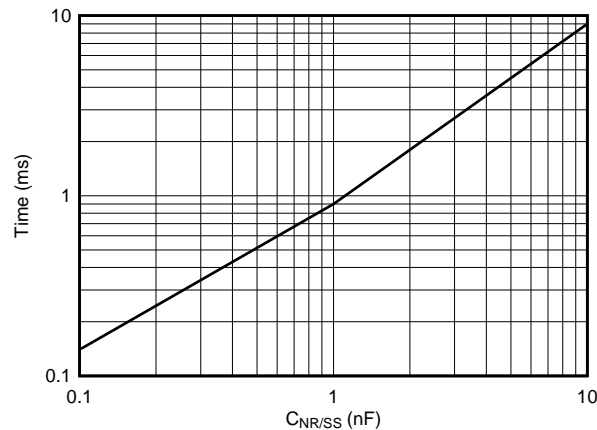


Figure 29. Soft-Start Time vs $C_{NR/SS}$

8.3.3 Enable Pin Operation

The TPS7A30 provides a dual polarity enable pin (EN) that turns on the regulator when $|V_{EN}| > 2$ V, whether the voltage is positive or negative, as shown in Figure 30.

This functionality allows for different system power management topologies:

- Connecting the EN pin directly to a negative voltage, such as V_{IN-} .
- Connecting the EN pin directly to a positive voltage, such as the output of digital logic circuitry.

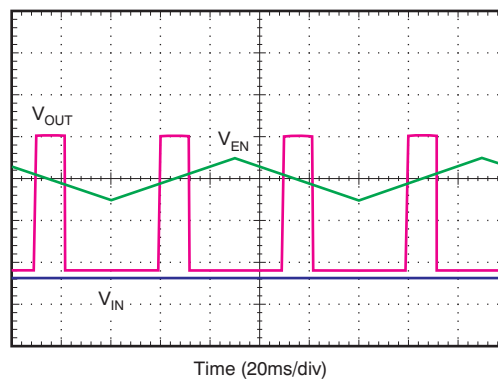


Figure 30. Enable Pin Positive and Negative Threshold

8.4 Device Functional Modes

8.4.1 Normal Operation

The device regulates to the nominal output voltage under the following conditions:

- The input voltage is at least as high as the $|V_{IN(min)}|$.
- The input voltage magnitude is greater than the nominal output voltage magnitude added to the dropout voltage.
- $|V_{EN}| > |V_{(HI)}|$
- The output current is less than the current limit.
- The device junction temperature is less than the maximum specified junction temperature.

Device Functional Modes (continued)

8.4.2 Dropout Operation

If the input voltage magnitude is lower than the nominal output voltage magnitude plus the specified dropout voltage magnitude, but all other conditions are met for normal operation, the device operates in dropout mode. In this mode of operation, the output voltage magnitude is the same as the input voltage magnitude minus the dropout voltage magnitude. The transient performance of the device is significantly degraded because the pass device (as a bipolar junction transistor, or BJT) is in saturation and no longer controls the current through the LDO. Line or load transients in dropout can result in large output voltage deviations.

8.4.3 Disabled

The device is disabled under the following conditions:

- $|V_{EN}| < |V_{(HI)}|$
- The device junction temperature is greater than the thermal shutdown temperature.

[Table 1](#) shows the conditions that lead to the different modes of operation.

Table 1. Device Functional Mode Comparison

OPERATING MODE	PARAMETER			
	V_{IN}	V_{EN}	I_{OUT}	T_J
Normal mode	$ V_{IN} > \{ V_{OUT(nom)} + V_{DO} , V_{IN(min)} \}$	$ V_{EN} > V_{(HI)} $	$I_{OUT} < I_{CL}$	$T_J < 125^\circ\text{C}$
Dropout mode	$ V_{IN(min)} < V_{IN} < V_{OUT(nom)} + V_{DO} $	$ V_{EN} > V_{(HI)} $	—	$T_J < 125^\circ\text{C}$
Disabled mode (any true condition disables the device)	—	$ V_{EN} < V_{(HI)} $	—	$T_J > 170^\circ\text{C}$

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TPS7A30 belongs to a family of new generation linear regulators that use an innovative bipolar process to achieve ultralow-noise. As bipolar-based devices, the TPS7A30 devices are ideal for high-accuracy, high-performance analog applications at higher voltages.

9.1.1 Adjustable Operation

The TPS7A3001 has an output voltage range of -1.174 V to -33 V . The nominal output voltage of the device is set by two external resistors, as shown in [Figure 32](#).

R_1 and R_2 can be calculated for any output voltage range using the formula shown in [Equation 2](#). To ensure stability under no load conditions, this resistive network must provide a current equal to or greater than $5\text{ }\mu\text{A}$.

$$R_1 = R_2 \left(\frac{V_{\text{OUT}}}{V_{\text{FB(nom)}}} - 1 \right), \text{ where } \frac{|V_{\text{FB(nom)}}|}{R_2} > 5\text{ }\mu\text{A} \quad (2)$$

If greater voltage accuracy is required, take into account the output voltage offset contributions because of the feedback pin current and use 0.1% tolerance resistors.

9.1.2 Capacitor Recommendations

Low-ESR capacitors should be used for the input, output, noise reduction, and feed-forward capacitors. Ceramic capacitors with X7R and X5R dielectrics are preferred. These dielectrics offer more stable characteristics. Ceramic X7R capacitors offer improved overtemperature performance, while ceramic X5R capacitors are the most cost-effective and are available in higher values.

NOTE

High-ESR capacitors may degrade PSRR.

9.1.2.1 Input and Output Capacitor Requirements

The TPS7A30 family of negative, high-voltage linear regulators achieve stability with a minimum input and output capacitance of $2.2\text{ }\mu\text{F}$; however, TI highly recommends using a $10\text{-}\mu\text{F}$ capacitor to maximize AC performance.

9.1.2.2 Noise Reduction and Feed-Forward Capacitor Requirements

Although noise reduction and feed-forward capacitors ($C_{\text{NR/SS}}$ and C_{FF} , respectively) are not needed to achieve stability, TI highly recommends using 10-nF capacitors to minimize noise and maximize AC performance.

For more information on C_{FF} , refer to Application Report, *Pros and Cons of Using a Feedforward Capacitor with a Low-Dropout Regulator* ([SBVA042](#)). This application report explains the advantages of using C_{FF} (also known as C_{BYP}), and the problems that can occur while using this capacitor.

9.1.3 Maximum AC Performance

To maximize noise and PSRR performance, TI recommends including a $10\text{-}\mu\text{F}$ or higher input and output capacitors, and 10-nF noise reduction and bypass capacitors, as shown in [Figure 32](#). The solution shown delivers minimum noise levels of $15.1\text{ }\mu\text{V}_{\text{RMS}}$ and power-supply rejection levels above 55 dB from 10 Hz to 700 kHz ; see [Figure 18](#) and [Figure 26](#).

9.1.4 Output Noise

The TPS7A30 provides low output noise when a noise reduction capacitor ($C_{\text{NR/SS}}$) is used.

Application Information (continued)

The noise reduction capacitor serves as a filter for the internal reference. By using a 10-nF noise reduction capacitor, the output noise is reduced by almost 80% (from 80 μV_{RMS} to 17 μV_{RMS}); see [Figure 27](#).

The TPS7A30 low output voltage noise makes it an ideal solution for powering noise-sensitive circuitry.

9.1.5 Power-Supply Rejection

The 10-nF noise reduction capacitor greatly improves TPS7A30 power-supply rejection, achieving up to 20 dB of additional power-supply rejection for frequencies between 110 Hz and 400 kHz.

Additionally, AC performance can be maximized by adding a 10-nF bypass capacitor (C_{FF}) from the FB pin to the OUT pin. This capacitor greatly improves power-supply rejection at lower frequencies, for the band from 10 Hz to 200 kHz; see [Figure 18](#).

The very high power-supply rejection of the TPS7A30 makes it a good choice for powering high-performance analog circuitry, such as operational amplifiers, ADCs, DACs, and audio amplifiers.

9.1.6 Transient Response

As with any regulator, increasing the size of the output capacitor reduces overshoot and undershoot magnitude but increases duration of the transient response.

9.1.7 Post DC-DC Converter Filtering

Most of the time, the voltage rails available in a system do not match the voltage specifications demanded by one or more of its circuits; these rails must be stepped up or down, depending on specific voltage requirements.

DC-DC converters are the preferred solution to step up or down a voltage rail when current consumption is not negligible. They offer high efficiency with minimum heat generation, but they have one primary disadvantage: they introduce a high-frequency component, and the associated harmonics, on top of the DC output signal.

This high-frequency component, if not filtered properly, degrades analog circuitry performance, reducing overall system accuracy and precision.

The TPS7A30 offers a wide-bandwidth, very-high power-supply rejection ratio. This specification makes it ideal for post DC-DC converter filtering, as shown in [Figure 31](#). TI highly recommends using the maximum performance schematic shown in [Figure 32](#). Also, verify that the fundamental frequency (and its first harmonic, if possible) is within the bandwidth of the regulator PSRR, shown in [Figure 18](#).

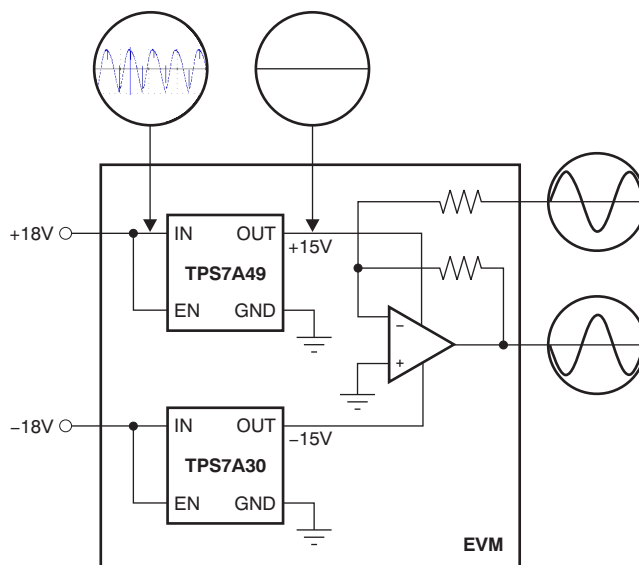


Figure 31. Post DC-DC Converter Regulation to High-Performance Analog Circuitry

Application Information (continued)

9.1.8 Audio Applications

Audio applications are extremely sensitive to any distortion and noise in the audio band from 20 Hz to 20 kHz. This stringent requirement demands clean voltage rails to power critical high-performance audio systems.

The very-high power-supply rejection ratio (> 55 dB) and low noise at the audio band of the TPS7A30 maximize performance for audio applications; see [Figure 18](#).

9.1.9 Power for Precision Analog

One of the primary TPS7A30 applications is to provide ultralow noise voltage rails to high-performance analog circuitry in order to maximize system accuracy and precision.

In conjunction with its positive counterpart, the [TPS7A49xx](#) family of positive high-voltage linear regulators, the TPS7A30 family of negative high voltage linear regulators provides ultralow noise positive and negative voltage rails to high-performance analog circuitry, such as operational amplifiers, ADCs, DACs, and audio amplifiers.

Because of the ultralow noise levels at high voltages, analog circuitry with high-voltage input supplies can be used. This characteristic allows for high-performance analog solutions to optimize the voltage range, maximizing system accuracy.

9.2 Typical Application

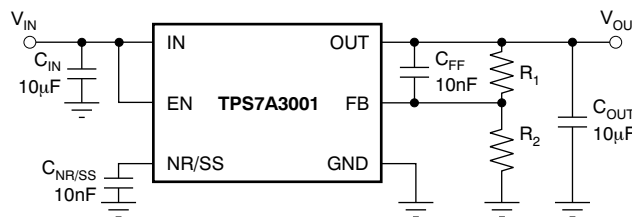


Figure 32. Adjustable Operation for Maximum AC Performance

9.2.1 Design Requirements

The design goals are $V_{IN} = -3$ V, $V_{OUT} = -1.2$ V, and $I_{OUT} = 150$ mA, maximum. The design should optimize transient response while meeting a start-up time of 14 ms with a start-up dominated by the soft-start feature. The input supply comes from a supply on the same printed-circuit-board (PCB). The design circuit is shown in [Figure 32](#).

The design space consists of C_{IN} , C_{OUT} , $C_{NR/SS}$, R_1 , and R_2 , at $T_{A(max)} = 75^{\circ}\text{C}$.

9.2.2 Detailed Design Procedure

The first step when designing with a linear regulator is to examine the maximum load current along with the input and output voltage requirements, to determine if the device thermal and dropout voltage requirements can be met. At 150 mA, the input dropout voltage of the TPS7A30 family is a maximum of 600 mV over temperature; therefore, the dropout headroom of 1.8 V is sufficient for operation over both input and output voltage accuracy. Dropout headroom is calculated as $V_{IN} - V_{OUT} - V_{DO(max)}$, and should be greater than 0 for reliable operation. $V_{DO(max)}$ is the maximum dropout allowed, given worst-case load conditions.

The maximum power dissipated in the linear regulator is the maximum voltage dropped across the pass element from the input to the output, multiplied by the maximum load current. In this example, the maximum voltage drop across in the pass element is $|3\text{ V} - 1.2\text{ V}|$, giving us a $V_{DO} = 1.8$ V. The power dissipated in the pass element is calculated by taking this voltage drop multiplied by the maximum load current. For this example, the maximum power dissipated in the linear regulator is 0.273 W, and is calculated as [Equation 3](#):

$$P_D = (V_{DO}) (I_{MAX}) + (V_{IN}) (I_Q) \quad (3)$$

Typical Application (continued)

Once the power dissipated in the linear regulator is known, the corresponding junction temperature rise can be calculated. To calculate the junction temperature rise above ambient, the power dissipated must be multiplied by the junction-to-ambient thermal resistance. This calculation gives the worst-case junction temperature; good thermal design can significantly reduce this number. For thermal resistance information, refer to [Thermal Information](#). For this example, using the DGN package, the maximum junction temperature rise is calculated to be 17.3°C. The maximum junction temperature rise is calculated by adding junction temperature rise to the maximum ambient temperature, which is 75°C for this example. For this example, the designer calculates the maximum junction temperature is 92.3°C. Keep in mind the maximum junction temperature must be below 125°C for reliable device operation. Additional ground planes, added thermal vias, and air flow all help to lower the maximum junction temperature.

Use the following equations to pick the rest of the components:

To ensure stability under no-load conditions, the current through the resistor network must be greater than 5 μA, as shown in [Equation 4](#).

$$\frac{V_{FB}}{R_2} > 5\mu A \rightarrow R_2 < 242.4 \text{ k}\Omega \quad (4)$$

To set $R_2 = 100 \text{ k}\Omega$ for a standard 1% value resistor, we calculate R_1 as shown in [Equation 5](#).

$$R_1 = R_2 \left(\frac{V_{OUT}}{V_{REF(nom)}} - 1 \right) = 100 \text{ k}\Omega \left(\frac{1.2 \text{ V}}{1.176 \text{ V}} - 1 \right) = 2.04 \text{ k}\Omega \quad (5)$$

Use a standard, 1%, 2.05-kΩ resistor for R_1 .

[Equation 6](#) calculates the start-up time, t_{SS} .

$$t_{SS} \text{ (ms)} = 0.9 \times C_{NR/SS} = 14 \text{ ms}$$

$$C_{SS} = 15 \text{ nF} \quad (6)$$

For the soft-start to dominate the start-up conditions, place the start-up time as a result of the current limit at two decades below the soft-start time, at 140 μs. C_{OUT} must be at least 2.2 μF for stability, as shown in [Equation 7](#) and [Equation 8](#).

$$t_{SS(CL)} = V_{OUT} \left(\frac{C_{OUT}}{I_{CL(max)}} \right) \quad (7)$$

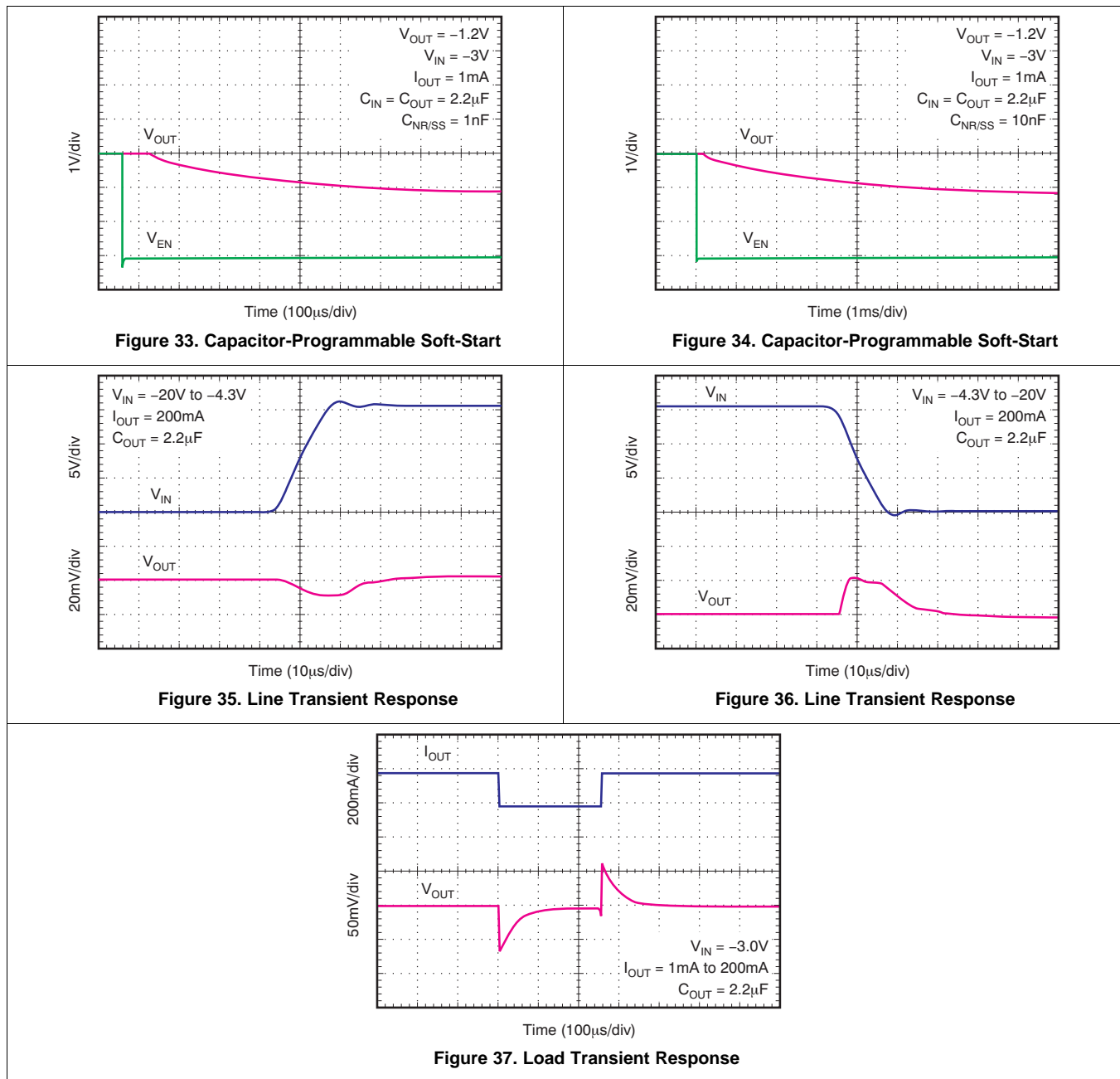
$$C_{OUT(max)} = t_{SS(CL)} \left(\frac{I_{CL(max)}}{V_{OUT}} \right) = 140 \mu s \times \frac{500 \text{ mA}}{2 \text{ V}} = 35 \mu F \quad (8)$$

Now for C_{IN} , assume that the –3-V supply has some inductance, and is placed several inches away from the PCB. For this case, we select a 2.2-μF ceramic input capacitor to ensure that the input impedance is negligible to the LDO control loop while keep the physical size and cost of the capacitor low; this component is a common-value capacitor.

For better PSRR for this design, use a 10-μF input and output capacitor. To reduce the peaks from transients but slow down the recovery time, increase the output capacitor size or add additional output capacitors.

Typical Application (continued)

9.2.3 Application Curves



9.3 Do's and Don'ts

Place at least one, low-ESR, 2.2- μ F capacitor as close as possible to both the IN and OUT terminals of the regulator to the GND pin.

Provide adequate thermal paths away from the device.

Do not place the input or output capacitor more than 10 mm away from the regulator.

Do not exceed the absolute maximum ratings.

Float the Enable (EN) pin.

Do not resistively or inductively load the NR/SS pin.

10 Power Supply Recommendations

The input supply for the LDO should be within its recommended operating conditions, that is, between -3 V and -35 V. The input voltage should provide adequate headroom in order for the device to have a regulated output. If the input supply is noisy, additional input capacitors with low-ESR can help improve the output noise performance.

The input and output supplies should also be bypassed with at least a 2.2- μ F capacitor located near the input and output pins. There should be no other components located between these capacitors and the pins.

11 Layout

11.1 Layout Guidelines

Layout is a critical part of good power-supply design. There are several signal paths that conduct fast-changing currents or voltages that can interact with stray inductance or parasitic capacitance to generate noise or degrade the power-supply performance. To help eliminate these problems, the IN pin should be bypassed to ground with a low ESR ceramic bypass capacitor with an X5R or X7R dielectric.

The GND pin should be tied directly to the PowerPAD under the IC. The PowerPAD should be connected to any internal PCB ground planes using multiple vias directly under the IC.

Equivalent series inductance (ESL) and equivalent series resistance (ESR) must be minimized to maximize performance and ensure stability. Every capacitor (C_{IN} , C_{OUT} , $C_{NR/SS}$, C_{FF}) must be placed as close as possible to the device and on the same side of the PCB as the regulator itself.

Do not place any of the capacitors on the opposite side of the PCB from where the regulator is installed. The use of vias and long traces is strongly discouraged because these circuits may impact system performance negatively, and even cause instability.

11.1.1 Board Layout Recommendations to Improve PSRR and Noise Performance

To improve AC performance (such as PSRR, output noise, and transient response), TI recommends designing the board with separate ground planes for V_{IN} and V_{OUT} , with each ground plane star connected only at the GND pin of the device. In addition, the ground connection for the bypass capacitor must connect directly to the GND pin of the device.

11.2 Layout Example

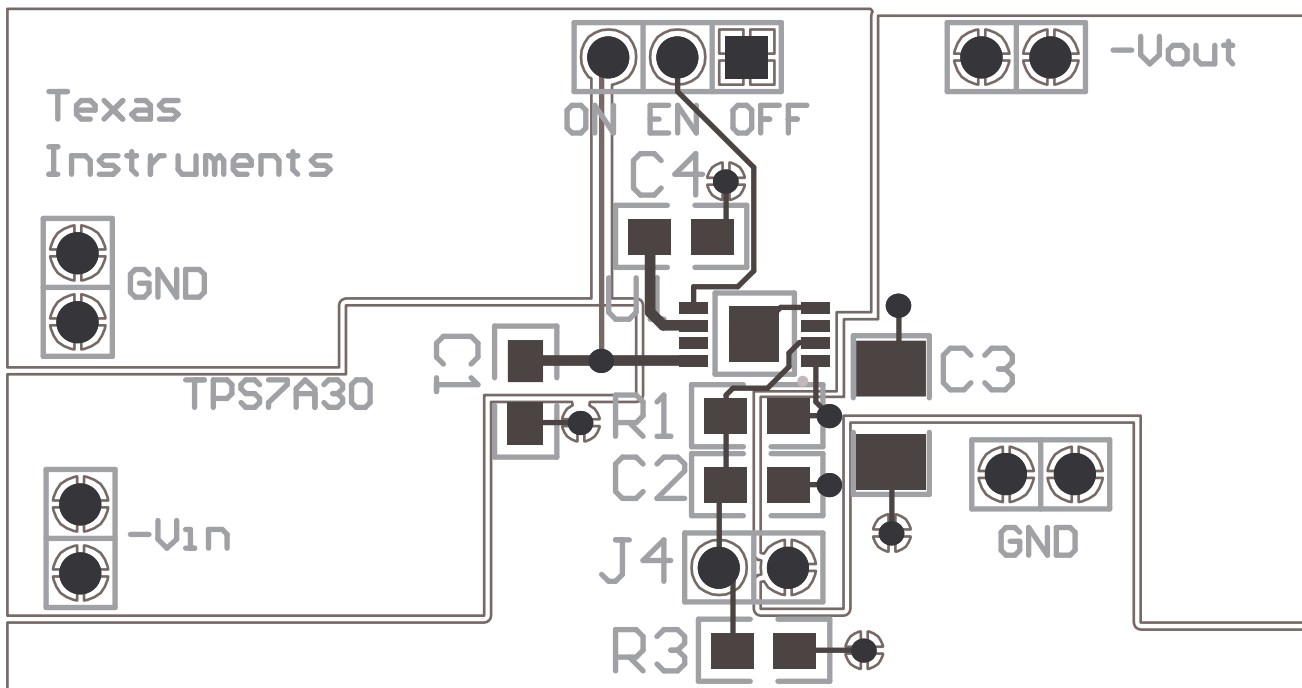


Figure 38. PCB Layout Example

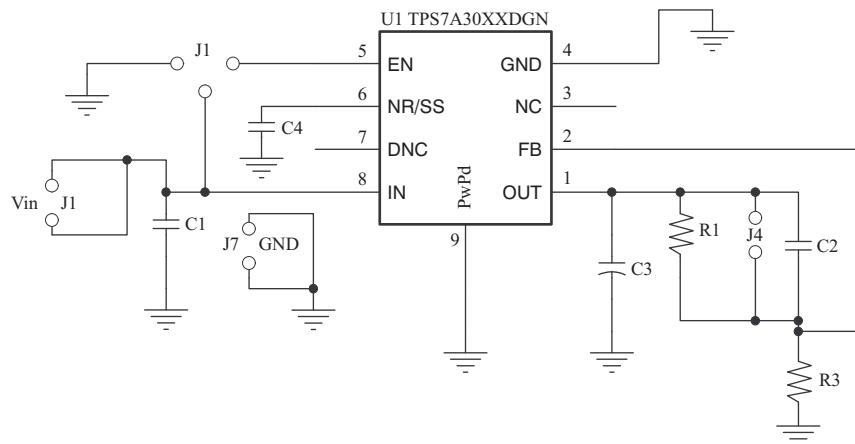
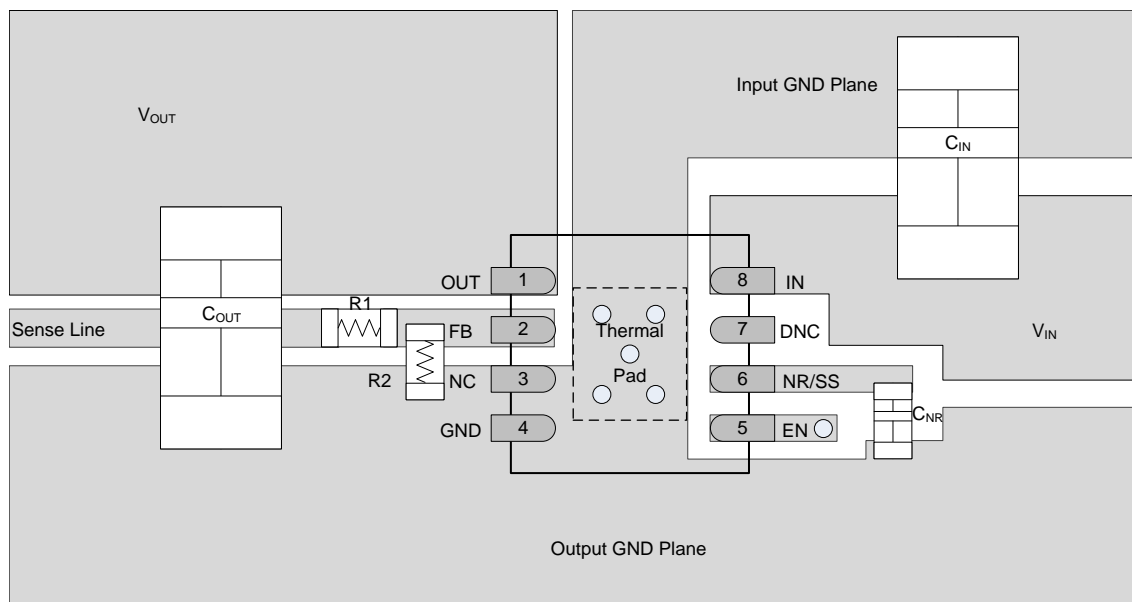


Figure 39. Schematic for PCB Layout Example



NOTE: C_{IN} and C_{OUT} are size 1208 capacitors, while C_{NR} , R1, and R2 are size 0402.

Figure 40. PCB Layout Example

11.3 Thermal Considerations

Thermal protection disables the output when the junction temperature rises to approximately 170°C, allowing the device to cool. When the junction temperature cools to approximately 150°C, the output circuitry is enabled. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This cycling limits the dissipation of the regulator, protecting it from damage as a result of overheating.

Any tendency to activate the thermal protection circuit indicates excessive power dissipation or an inadequate heatsink. For reliable operation, junction temperature should be limited to a maximum of 125°C. To estimate the margin of safety in a complete design (including heatsink), increase the ambient temperature until the thermal protection is triggered; use worst-case loads and signal conditions. For good reliability, thermal protection should trigger at least 35°C above the maximum expected ambient condition of your particular application. This configuration produces a worst-case junction temperature of 125°C at the highest expected ambient temperature and worst-case load.

Thermal Considerations (continued)

The internal protection circuitry of the TPS7A30 has been designed to protect against overload conditions. It was not intended to replace proper heatsinking. Continuously running the TPS7A30 into thermal shutdown degrades device reliability.

11.4 Power Dissipation

The ability to remove heat from the die is different for each package type, presenting different considerations in the PCB layout. The PCB area around the device that is free of other components moves the heat from the device to the ambient air. Performance data on JEDEC low- and high-K boards are given in [Thermal Information](#). Using heavier copper increases the effectiveness in removing heat from the device. The addition of plated through-holes to heat dissipating layers also improves the heatsink effectiveness.

Power dissipation depends on input voltage and load conditions. Power dissipation (P_D) can be approximated by the product of the output current times the voltage drop across the output pass element, as shown in [Equation 9](#).

$$P_D = (V_{IN} - V_{OUT}) I_{OUT} \quad (9)$$

Power Dissipation (continued)

Estimating the junction temperature can be done by using the thermal metrics Ψ_{JT} and Ψ_{JB} , shown in [Thermal Information](#). These metrics are a more accurate representation of the heat transfer characteristics of the die and the package than $R_{\theta JA}$. The junction temperature can be estimated with [Equation 10](#).

$$\Psi_{JT}: T_J = T_T + \Psi_{JT} \cdot P_D$$

$$\Psi_{JB}: T_J = T_B + \Psi_{JB} \cdot P_D$$

where

- P_D is the power dissipation shown by [Equation 9](#),
 - T_T is the temperature at the center-top of the IC package,
 - T_B is the PCB temperature measured 1 mm away from the IC package *on the PCB surface*. (10)
-

NOTE

Both T_T and T_B can be measured on actual application boards using a thermo-gun (an infrared thermometer).

For more information about measuring T_T and T_B , see the application note [Using New Thermal Metrics \(SBVA025\)](#), available for download at www.ti.com.

12 Device and Documentation Support

12.1 Device Support

12.1.1 Development Support

12.1.1.1 Evaluation Modules

An evaluation module (EVM) is available to assist in the initial circuit performance evaluation using the TPS7A30. The [TPS7A30-49EVM-567 evaluation module](#) (and [related user's guide](#)) can be requested at the TI website through the product folders or purchased directly from the [TI eStore](#).

12.1.1.2 Spice Models

Computer simulation of circuit performance using SPICE is often useful when analyzing the performance of analog circuits and systems. A SPICE model for the TPS7A30 is available through the product folders under the *Tools & Software* tab.

12.1.2 Device Nomenclature

Table 2. Ordering Information⁽¹⁾

PRODUCT	V _{OUT}
TPS7A30xx yyy z	XX is nominal output voltage (01 = Adjustable). ⁽²⁾ YYY is package designator. Z is package quantity.

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or visit the device product folder on www.ti.com.

(2) For fixed –1.2-V operation, tie FB to OUT.

12.2 Documentation Support

12.2.1 Related Documentation

For related documentation see the following:

- *Pros and Cons of Using a Feedforward Capacitor with a Low-Dropout Regulator*, [SBVA042](#).
- *Using New Thermal Metrics*, [SBVA025](#)
- *TPS7A30-49EVM-567 Evaluation Module User's Guide*, [SLVU405](#)

12.3 Trademarks

PowerPAD is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.4 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.5 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS7A3001DGNR	ACTIVE	MSOP-PowerPAD	DGN	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	PSZQ	Samples
TPS7A3001DGNT	ACTIVE	MSOP-PowerPAD	DGN	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	PSZQ	Samples
TPS7A3001DRBR	PREVIEW	SON	DRB	8	2500	TBD	Call TI	Call TI			
TPS7A3001DRBT	PREVIEW	SON	DRB	8	250	TBD	Call TI	Call TI			

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF TPS7A3001 :

- Enhanced Product: [TPS7A3001-EP](#)

NOTE: Qualified Version Definitions:

- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS7A3001DGNR	MSOP-Power PAD	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPS7A3001DGNT	MSOP-Power PAD	DGN	8	250	180.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

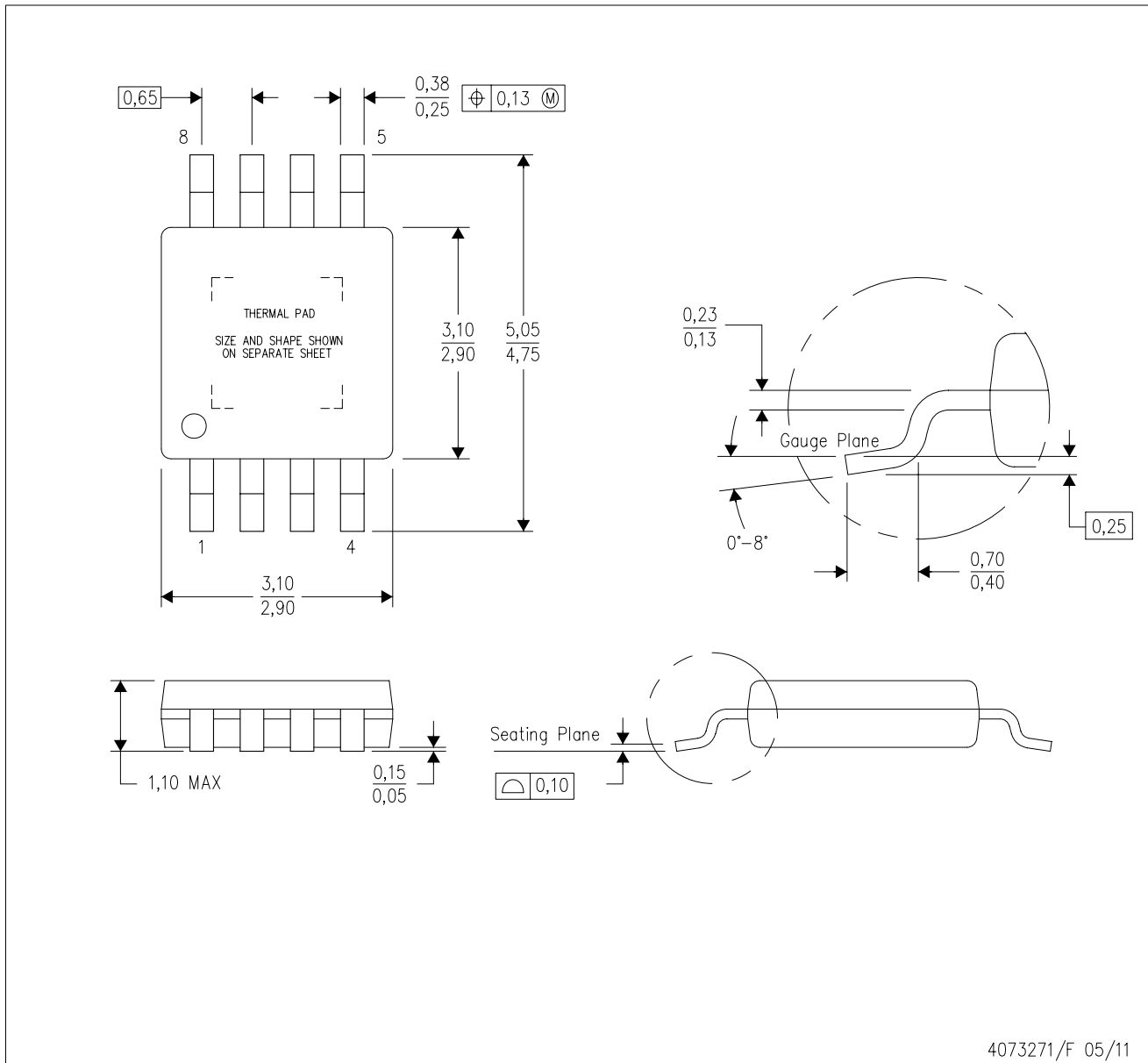
TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS7A3001DGNR	MSOP-PowerPAD	DGN	8	2500	367.0	367.0	35.0
TPS7A3001DGNT	MSOP-PowerPAD	DGN	8	250	210.0	185.0	35.0

DGN (S-PDSO-G8)

PowerPAD™ PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion.
 - This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <<http://www.ti.com>>.
 - See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
 - Falls within JEDEC MO-187 variation AA-T

PowerPAD is a trademark of Texas Instruments.

DGN (S-PDSO-G8)

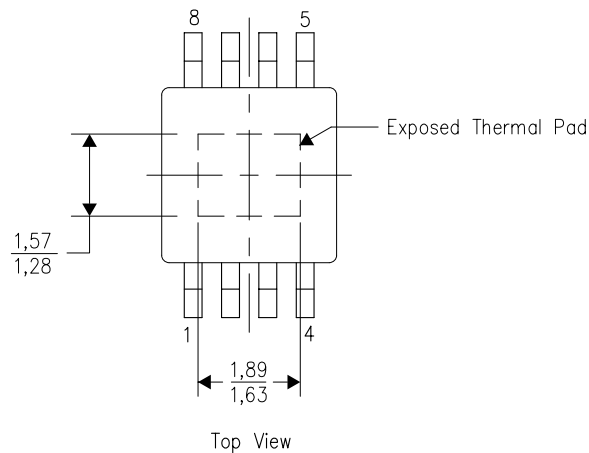
PowerPAD™ PLASTIC SMALL OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

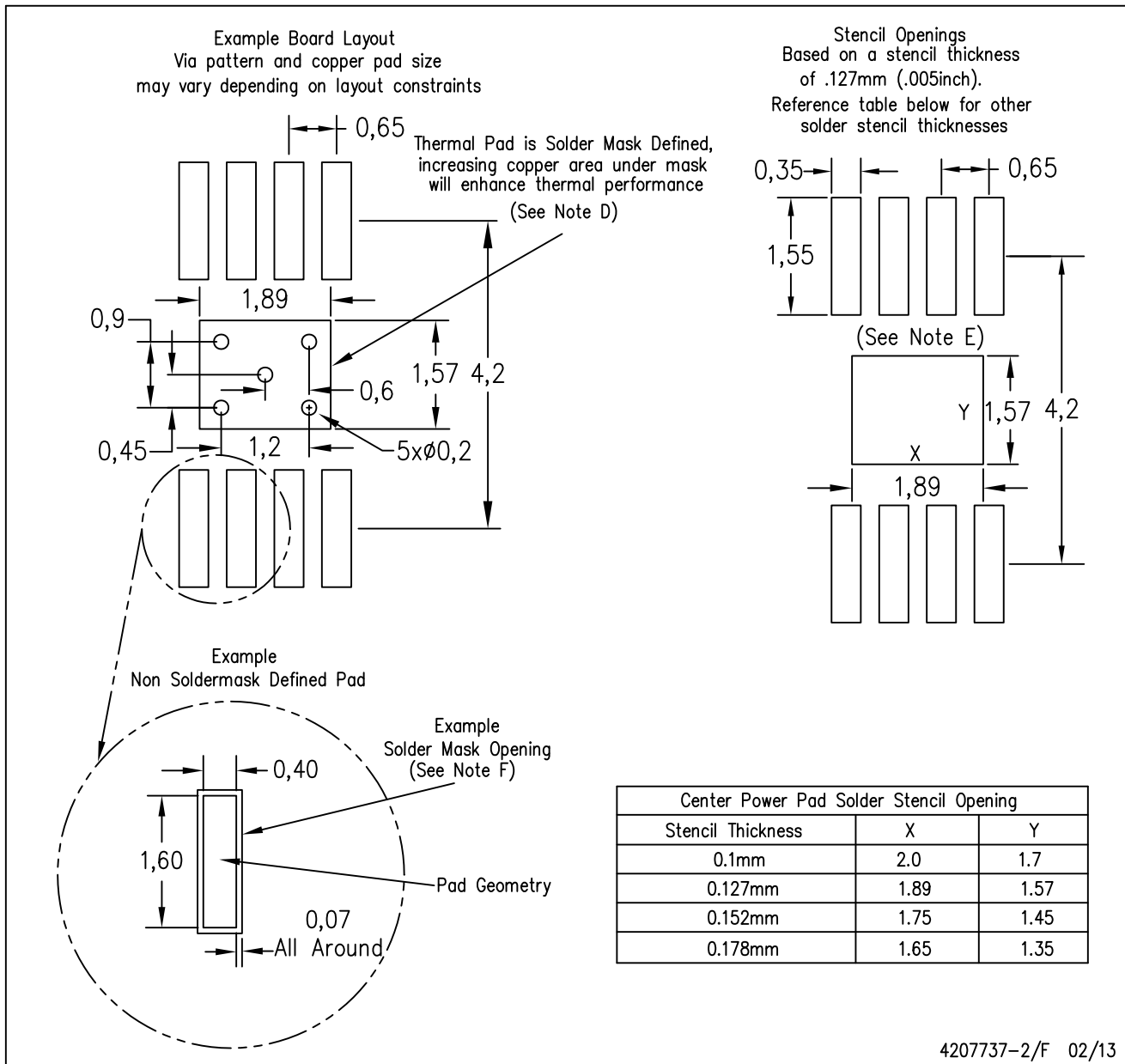


Exposed Thermal Pad Dimensions

4206323-2/1 12/11

NOTE: All linear dimensions are in millimeters

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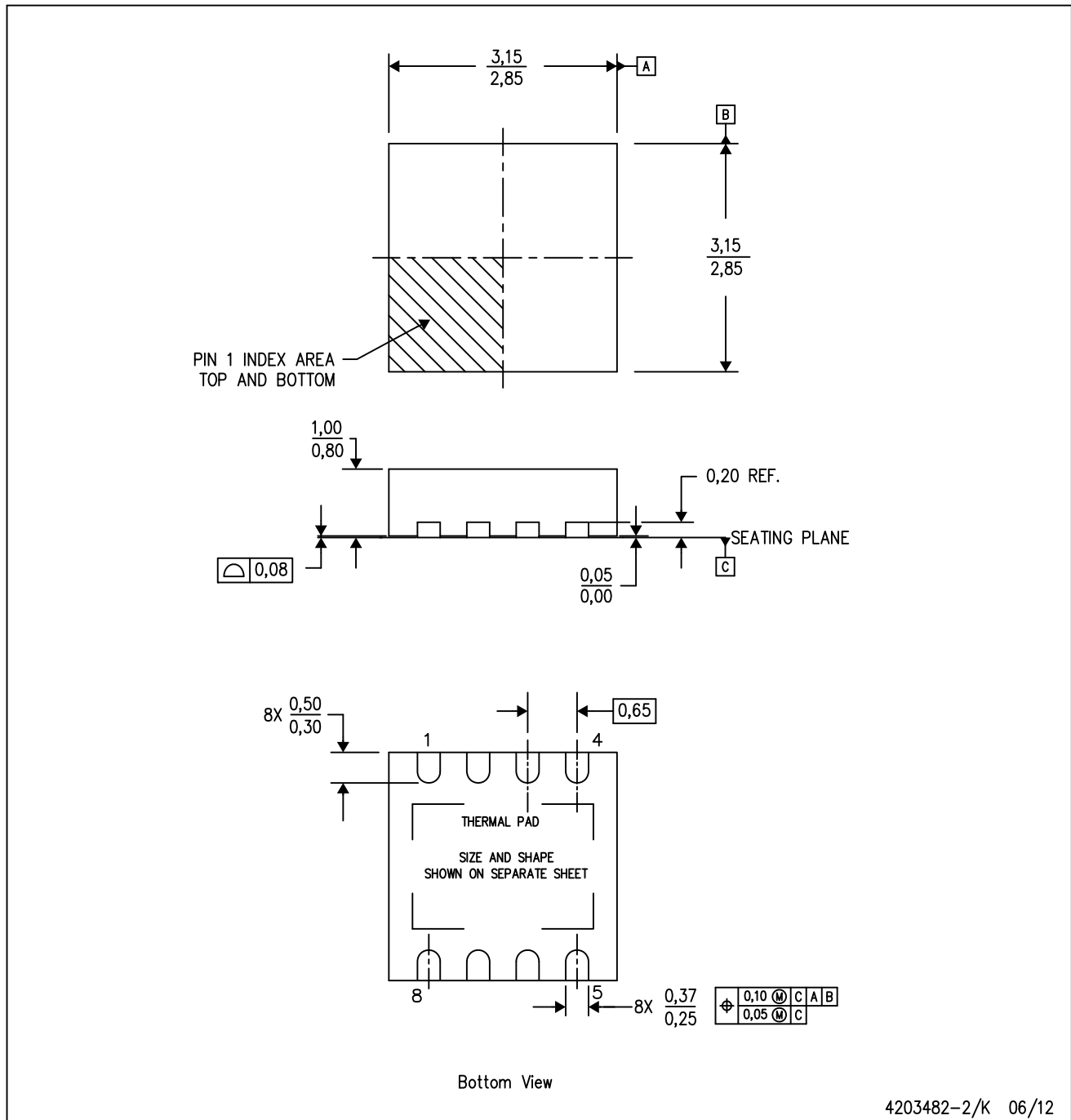


- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
 - D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <<http://www.ti.com>>.
 - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.
 - F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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DRB (S-PVSON-N8)

PLASTIC SMALL OUTLINE NO-LEAD



- NOTES:
- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - This drawing is subject to change without notice.
 - Small Outline No-Lead (SON) package configuration.
 - The package thermal pad must be soldered to the board for thermal and mechanical performance.
 - See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.

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