

TPS65086xx Configurable Multi-Rail PMU for 2S and 3S Li-Ion Battery-Operated Devices

1 Device Overview

1.1 Features

- 3 Variable Output Voltage Step-Down Controllers
 - Wide V_{IN} Range From 5.4 V to 21 V
 - Up to 7-A Output Current for BUCK1 and BUCK6, and 21-A for BUCK2 Using External FETs
 - I²C DVS Control (0.41 V to 1.67 V in 10-mV Steps, 1 V to 3.575 V in 25-mV Steps)
- 3 Variable Output Voltage Synchronous Step-Down Converters
 - V_{IN} Range From 4.5 V to 5.5 V
 - Up to 3.5-A Output Current for BUCK3, and 3-A for BUCK4 and BUCK5
 - I²C DVS Control (0.41 V to 1.67 V in 10-mV Steps, 0.4125 V to 1.9875 V in 12.5-mV Steps, or 0.425 V to 3.575 V in 25-mV Steps)
- 3 LDO Regulators
 - LDOA1: I²C-Selectable Output Voltage From 1.35 V to 3.3 V for up to 200-mA Output Current
 - LDOA2 and LDOA3: I²C-Selectable Output Voltage From 0.7 V to 1.5 V for up to 600-mA Output Current
- VTT LDO for DDR3 and DDR4 Memory Termination
 - Fixed Output Voltage of $0.5 \times V_{BUCK6}$
 - Can Sink and Source Output Current up to 1000 mA
- 3 Load Switches With Slew Rate Control
 - Up to 300-mA Output Current With Voltage Drop Less than 1.5 % of Nominal Input Voltage
 - $R_{DS(ON)} < 96 \text{ m}\Omega$ at Input Voltage of 1.8 V
- 5-V Fixed Output Voltage LDO (LDO5)
 - Power Supply for Gate Drivers of SMPS and for LDOA1
 - Automatic Switch to External 5-V Buck for Higher Efficiency
- Built-in Flexibility and Configurability
 - 6 GPI Pins Configurable to Enable or Sleep Mode of Any Selected Rails
 - 4 GPO Pins Configurable to Power Good of Any Selected Rails
 - Open-Drain Interrupt Output Pin
- I²C Interface (Device Address 0x5E) Supports Standard Mode (100 kHz), Fast Mode (400 kHz), and Fast Mode Plus (1 MHz)
- 64-Pin, Single-Row, 0.4-mm Pitch QFN Package

1.2 Applications

- NVDC or non-NVDC Power System Architectures
- 2 or 3 Series-Cell Li-Ion Battery-Powered Products
- Tablet, Ultrabook, and Notebook Computers
- Mobile PCs and Mobile Internet Devices
- Personal Medical Products
- Residential Gateway
- POS Terminals

1.3 Description

The TPS65086xx is a single-chip solution power-management IC designed specifically for the latest Intel processors, FPGAs, and any other mobile processors targeted for tablets, ultrabooks, notebooks, embedded computers with NVDC or non-NVDC power architectures, using 2S or 3S Li-Ion battery packs. The high-frequency voltage regulators use small inductors and capacitors to achieve a small solution size. The I²C interface allows simple control either by an embedded controller (EC) or by an SoC. The PMIC comes in a 8 × 8 single-row QFN package with thermal pad for good thermal dissipation and ease of board routing.

Device Information

PART NUMBER	PACKAGE	BODY SIZE
TPS65086xx	RSK (64)	8.00 mm × 8.00 mm



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCT PREVIEW Information. Product in design phase of development. Subject to change or discontinuance without notice.

1.4 Functional Block Diagram

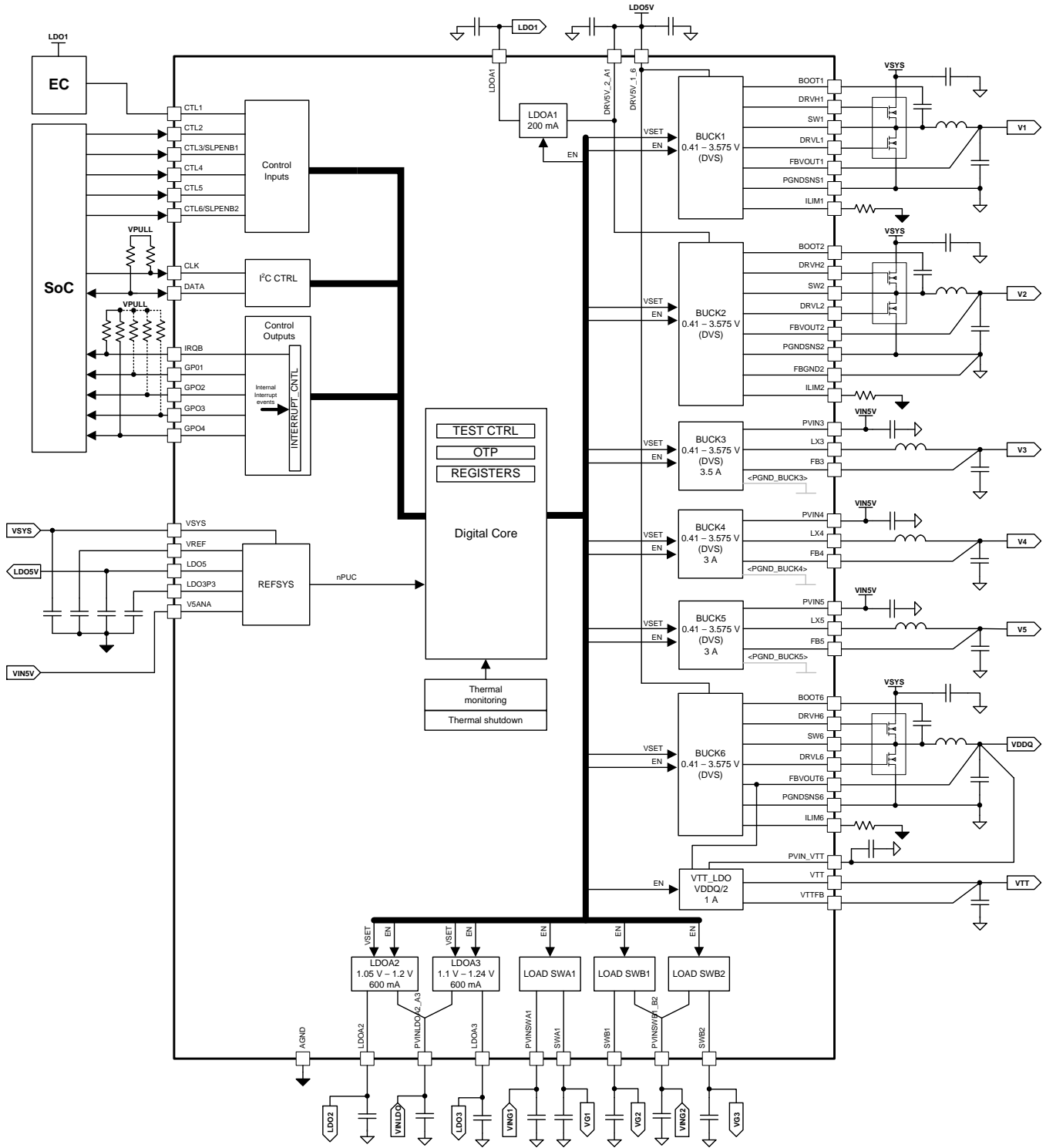


Figure 1-1. PMIC Functional Block Diagram

PRODUCT PREVIEW

2 Revision History

DATE	REVISION	NOTES
March 2015	*	Initial Release

PRODUCT PREVIEW

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS650860A0RSKR	PREVIEW			68		TBD	Call TI	Call TI	-40 to 85		
TPS650860A0RSKT	PREVIEW			68		TBD	Call TI	Call TI	-40 to 85		

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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