TEXAS INSTRUMENTS

TPS62671, TPS62672, TPS62674
TPS62675, TPS626751, TPS626765, TPS62679

SLVS952F – APRIL 2010 – REVISED JUNE 2014

# TPS6267x 500-mA/650-mA, 6-MHz High-Efficiency Step-Down Converter in Low Profile Chip Scale Packaging (Height < 0.4mm)

## 1 Features

- 92% Efficiency at 6MHz Operation
- 17µA Quiescent Current
- Wide $V_{IN}$ Range From 2.3V to 4.8V
- 6MHz Regulated Frequency Operation
- Spread Spectrum, PWM Frequency Dithering
- *Best in Class* Load and Line Transient
- ±2% Total DC Voltage Accuracy
- Low Ripple Light-Load PFM Mode
- ≥35dB $V_{IN}$ PSRR (1kHz to 10kHz)
- Simple Logic Enable Inputs
- Supports External Clock Presence Detect Enable Input
- Three Surface-Mount External Components Required (One 0603 MLCC Inductor, Two 0402 Ceramic Capacitors)
- Complete Sub 0.33-mm Component Profile Solution
- Total Solution Size <10 $mm^2$
- Available in a 6-Pin NanoFree™ (CSP) Ultra-Thin Packaging, 0.4mm Max. Height

## 2 Applications

- Cell Phones, Smart-Phones
- CMOS Camera Module, Optical Data Module
- Digital TV, WLAN, GPS and Bluetooth™ Applications
- Embedded Power Supply

## 3 Description

The TPS6267x devices are high-frequency synchronous step-down dc-dc converters optimized for small battery-powered applications. Intended for low-power applications, the TPS6267x supports up to 650-mA load current and allows the use of low cost chip inductor and capacitors.

With a wide input voltage range of 2.3V to 4.8V, the device supports applications powered by Li-Ion batteries with extended voltage range. Different fixed voltage output versions are available from 1.05V to 2.1V. The TPS6267x operates at a regulated 6-MHz switching frequency and enters the power-save mode operation at light load currents to maintain high efficiency over the entire load current range.

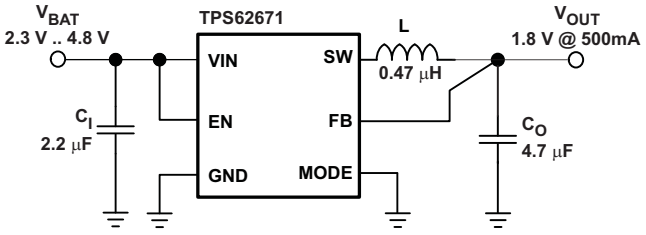
The PFM mode extends the battery life by reducing the quiescent current to 17µA (typ) during light load operation. For noise-sensitive applications, the device has PWM spread spectrum capability providing a lower noise regulated output, as well as low noise at the input. These features, combined with high PSRR and AC load regulation performance, make this device suitable to replace a linear regulator to obtain better power conversion efficiency.

**Device Information(1)**

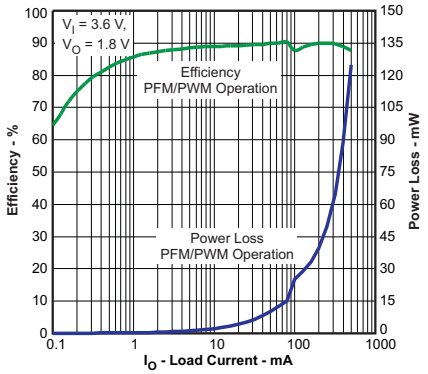
| PART NUMBER | PACKAGE | BODY SIZE (NOM) |
|---|---|---|
| TPS62671, TPS62672, TPS62674, TPS62675, TPS626751, TPS626765 | DSBGA (6) | 1.22mm x 0.85mm |
| TPS62679 | PicoStar (6) | 1.22mm x 0.85mm |

(1) For all available packages, see the orderable addendum at the end of the datasheet.

## 4 Simplified Schematic




**Efficiency vs Output Current**



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## 5 Revision History

**Changes from Revision E (April 2010) to Revision F** — **Page**

- Added Device Information table and included device TPS626765 ... 1
- Deleted the Ordering Information table and replaced with the Device Comparison Table; Ordering Info is in the POA ... 4
- Changed "Terminal" to "Pin" in 3 places ... 4
- Changed the notes in the Handling Ratings table and added values in the MIN column ... 5
- Added column in Thermal Information table for the TPS60679 device and changed "TERMINALS" to "PINS" ... 5
- Added TIMING row to the Electrical Characteristics table ... 8
- Changed formatting of Typical Characteristics section to 6 graphs per page. ... 9
- Added the 3rd-party products disclaimer ... 28
- Changed the location of References from Applications to Related Documentation ... 28

**Changes from Revision D (July 2011) to Revision E** — **Page**

- Added device TPS626751 to Ordering Info table. ... 4
- Added Preview devices TPS62673, TPS62676 to Ordering Info table. ... 4

**Changes from Revision C (April 2011) to Revision D** — **Page**

- Changed from "600-mA" to "650-mA" in document title ... 1
- Changed description text from "600-mA" to "650-mA" load current. ... 1
- Changed $I_O$ specification for TPS62675 from "600 mA" MAX to "650 mA " ... 5
- Changed $V_{OUT}$ specification Condition statement from "600 mA" to "650 mA" for TPS62675 ... 8

**Changes from Revision B (January 2011) to Revision C** — **Page**

- Changed devices TPS62671 and TPS62675 to Production status in Ordering Info table. ... 4
- Added copyright attribution for spectrum illustrations ... 16

**Changes from Revision A (November 2010) to Revision B** **Page**

- Changed device TPS62679 to Production status, and changed TPS62671 to Product Preview status in the Ordering Info table. ..... 4

**Changes from Original (April 2010) to Revision A** **Page**

- Changed Figure 3 image in Typical Char. graphs ..... 9
- Changed Figure 45 image in the Typical Char. graphs ..... 11
- Changed Figure 40 image in the Typical Char. graphs ..... 24

## 6 Device Comparison Table

| PART NUMBER | OUTPUT VOLTAGE | DEVICE SPECIFIC FEATURE | PACKAGE MARKING |
|---|---|---|---|
| TPS62671YFD | 1.8V | PWM Spread Spectrum Modulation (SSM) | NZ |
| TPS62672YFD | 1.5V | PWM Spread Spectrum Modulation (SSM) | OA |
| TPS62674YFD | 1.26V | PWM SSM, PWM Operation Only, Output Discharge | PN |
| TPS62675YFD | 1.2V | PWM Spread Spectrum Modulation (SSM) | OB |
| TPS626751YFD | 1.2V | PWM SSM, Output Discharge | E3 |
| TPS626765YFD | 1.05V | PWM SSM, Output Discharge | EH |
| TPS62679ZYFM | 1.26V | PWM SSM, Extended Start-Up Time, Output Discharge | - |

## 7 Pin Configuration and Functions


**Pin Functions**

| PIN | | I/O | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| FB | C1 | I | Output feedback sense input. Connect FB to the converter's output. |
| VIN | A2 | I | Power supply input. |
| SW | B1 | I/O | This is the switch pin of the converter and is connected to the drain of the internal Power MOSFETs. |
| EN | B2 | I | This is the enable pin of the device. Connecting this pin to ground forces the device into shutdown mode. Pulling this pin to $V_I$ enables the device. If an external clock (4MHz to 27MHz) is detected the device will automatically power up. This pin must not be left floating and must be terminated. |
| MODE | A1 | I | This is the mode selection pin of the device. This pin must not be left floating and must be terminated.<br>MODE = LOW: The device is operating in regulated frequency pulse width modulation mode (PWM) at high-load currents and in pulse frequency modulation mode (PFM) at light load currents.<br>MODE = HIGH: Low-noise mode enabled, regulated frequency PWM operation forced. |
| GND | C2 | – | Ground pin. |

# 8 Specifications

## 8.1 Absolute Maximum Ratings(1)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| Input Voltage | Voltage at VIN(2), SW(3) | –0.3 | 6 | V |
| | Voltage at FB(3) | –0.3 | 3.6 | V |
| | Voltage at EN, MODE (3) | –0.3 | $V_I$ + 0.3 | V |
| $T_A$ | Operating temperature range(4) | –40 | 85 | °C |
| $T_J$ | Operating junction temperature | | 150 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Operation above 4.8V input voltage for extended periods may affect device reliability.
(3) All voltage values are with respect to network ground terminal.
(4) In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature ($T_{A(max)}$) is dependent on the maximum operating junction temperature ($T_{J(max)}$), the maximum power dissipation of the device in the application ($P_{D(max)}$), and the junction-to-ambient thermal resistance of the part/package in the application ($\theta_{JA}$), as given by the following equation: $T_{A(max)} = T_{J(max)} - (\theta_{JA} \times P_{D(max)})$. To achieve optimum performance, it is recommended to operate the device with a maximum junction temperature of 105°C.

## 8.2 Handling Ratings

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| Tstg | Storage temperature range | –65 | 150 | °C |
| $V_{ESD}$ | Human Body Model (HBM) ESD stress voltage(1) | –2 | 2 | kV |
| | Charge device model (CDM) ESD stress voltage(2) | –1 | 1 | kV |
| | Machine Model (MM) ESD Stress Voltage(3) | –200 | 200 | V |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.
(3) The machine model is a 200pF capacitor discharged directly into ech pin.

## 8.3 Recommended Operating Conditions

| | | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_I$ | Input voltage range | | 2.3 | | 4.8(1) | V |
| $I_O$ | Output current range | TPS62671, TPS62672, TPS62674, TPS62679 | 0 | | 500 | mA |
| | | TPS62675, TPS626751, TPS626765 | 0 | | 650 | mA |
| L | Inductance | | 0.3 | | 1.8 | µH |
| $C_O$ | Output capacitance (PFM/PWM operation) | | 0.8 | 2.5 | 10 | µF |
| | Output capacitance (PWM operation) | | 0.8 | 2.5 | 10 | µF |
| $T_A$ | Ambient temperature | | –40 | | +85 | °C |
| $T_J$ | Operating junction temperature | | –40 | | +125 | °C |

(1) Operation above 4.8V input voltage for extended periods may affect device reliability.

## 8.4 Thermal Information

| THERMAL METRIC(1) | | TPS60679 | TPS6267X | UNIT |
|---|---|---|---|---|
| | | YFM (6 PINS) | YFD (6 PINS) | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | | 125 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | | - | |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | | 53 | |
| $\psi_{JT}$ | Junction-to-top characterization parameter | | - | |
| $\psi_{JB}$ | Junction-to-board characterization parameter | | - | |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | | - | |

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

## 8.5 Electrical Characteristics

Minimum and maximum values are at $V_I$ = 2.3V to 5.5V, $V_O$ = 1.8V, EN = 1.8V, AUTO mode and $T_A$ = –40°C to 85°C; Circuit of Parameter Measurement Information section (unless otherwise noted). Typical values are at $V_I$ = 3.6V, $V_O$ = 1.8V, EN = 1.8V, AUTO mode and $T_A$ = 25°C (unless otherwise noted).

| PARAMETER | | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| **SUPPLY CURRENT** | | | | | | | |
| $I_Q$ | Operating quiescent current | TPS62671<br>TPS62672<br>TPS62675<br>TPS62679<br>TPS626751<br>TPS626765 | $I_O$ = 0mA. Device not switching | | 17 | 40 | µA |
| | | TPS62671<br>TPS626751<br>TPS626765 | $I_O$ = 0mA, PWM mode | | 5.5 | | mA |
| | | TPS62674<br>TPS62679 | $I_O$ = 0mA, PWM mode | | 5.0 | | mA |
| $I_{(SD)}$ | Shutdown current | | EN = GND | | 0.2 | 1 | µA |
| UVLO | Undervoltage lockout threshold | | | | 2.05 | 2.1 | V |
| **ENABLE, MODE** | | | | | | | |
| $V_{IH}$ | High-level input voltage | TPS62671<br>TPS62672<br>TPS62675<br>TPS626751<br>TPS626765 | | 1.0 | | | V |
| $V_{IL}$ | Low-level input voltage | | | | | 0.4 | V |
| $I_{lkg}$ | Input leakage current | | Input connected to GND or VIN | | 0.01 | 1.5 | µA |
| $V_{IH}$ | High-level input voltage (ENABLE) | TPS62674<br>TPS62679 | | 1.26 | | | V |
| | High-level input voltage (MODE) | | | 1.0 | | | V |
| $V_{IL}$ | Low-level input voltage (ENABLE) | | | | | 0.54 | V |
| | Low-level input voltage (MODE) | TPS62679 | | | | 0.4 | V |
| $I_{lkg}$ | Input leakage current | TPS62674<br>TPS62679 | Input connected to GND or VIN | | 0.01 | 1.5 | µA |
| $C_{IN}$ | Input capacitance (ENABLE) | | | | 5 | | pF |
| EXTCLK | Clock presence detect frequency | TPS62674<br>TPS62679 | | 4 | | 27 | MHz |
| | Clock presence detect duty cycle | | | 40% | | 60% | |

## Electrical Characteristics (continued)

Minimum and maximum values are at $V_I$ = 2.3V to 5.5V, $V_O$ = 1.8V, EN = 1.8V, AUTO mode and $T_A$ = –40°C to 85°C; Circuit of Parameter Measurement Information section (unless otherwise noted). Typical values are at $V_I$ = 3.6V, $V_O$ = 1.8V, EN = 1.8V, AUTO mode and $T_A$ = 25°C (unless otherwise noted).

| PARAMETER | | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| **POWER SWITCH** | | | | | | | | |
| $r_{DS(on)}$ | P-channel MOSFET on resistance | | $V_I = V_{(GS)}$ = 3.6V. PWM mode | | | 170 | | mΩ |
| | | | $V_I = V_{(GS)}$ = 2.5V. PWM mode | | | 230 | | mΩ |
| $I_{lkg}$ | P-channel leakage current, PMOS | | $V_{(DS)}$ = 5.5V, -40°C ≤ $T_J$ ≤ 85°C | | | | 1 | µA |
| $r_{DS(on)}$ | N-channel MOSFET on resistance | | $V_I = V_{(GS)}$ = 3.6V. PWM mode | | | 120 | | mΩ |
| | | | $V_I = V_{(GS)}$ = 2.5V. PWM mode | | | 180 | | mΩ |
| $I_{lkg}$ | N-channel leakage current, NMOS | | $V_{(DS)}$ = 5.5V, -40°C ≤ $T_J$ ≤ 85°C | | | | 2 | µA |
| $r_{DIS}$ | Discharge resistor for power-down sequence | | TPS62674, TPS626751, TPS626765, TPS62679 | | | 70 | 150 | Ω |
| | P-MOS current limit | | 2.3V ≤ $V_I$ ≤ 4.8V. Open loop | TPS62671<br>TPS62672<br>TPS62674<br>TPS62679 | 900 | 1000 | 1150 | mA |
| | | | 2.3V ≤ $V_I$ ≤ 4.8V. Open loop | TPS62675<br>TPS626751<br>TPS626765 | 1000 | 1100 | 1250 | mA |
| | Input current limit under short-circuit conditions | | $V_O$ shorted to ground | | | 12 | | mA |
| | Thermal shutdown | | | | | 140 | | °C |
| | Thermal shutdown hysteresis | | | | | 10 | | °C |
| **OSCILLATOR** | | | | | | | | |
| $f_{SW}$ | Oscillator center frequency | TPS62671<br>TPS62672<br>TPS62675<br>TPS626751<br>TPS626765 | $I_O$ = 0mA. PWM operation | | 5.4 | 6 | 6.6 | MHz |
| | Oscillator center frequency | TPS62674<br>TPS62679 | $I_O$ = 0mA. PWM operation | | 4.9 | 5.45 | 6.0 | MHz |

## Electrical Characteristics (continued)

Minimum and maximum values are at $V_I$ = 2.3V to 5.5V, $V_O$ = 1.8V, EN = 1.8V, AUTO mode and $T_A$ = –40°C to 85°C; Circuit of Parameter Measurement Information section (unless otherwise noted). Typical values are at $V_I$ = 3.6V, $V_O$ = 1.8V, EN = 1.8V, AUTO mode and $T_A$ = 25°C (unless otherwise noted).

| PARAMETER | | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| **OUTPUT** | | | | | | | |
| $V_{OUT}$ | Regulated DC output voltage | TPS62671 TPS62672 TPS62679 | 2.3V ≤ $V_I$ ≤ 4.8V, 0mA ≤ $I_O$ ≤ 500 mA PFM/PWM operation | 0.98×$V_{NOM}$ | $V_{NOM}$ | 1.03×$V_{NOM}$ | V |
| | | | 2.3V ≤ $V_I$ ≤ 5.5V, 0mA ≤ $I_O$ ≤ 500 mA PFM/PWM operation | 0.98×$V_{NOM}$ | $V_{NOM}$ | 1.04×$V_{NOM}$ | V |
| | | | 2.3V ≤ $V_I$ ≤ 5.5V, 0mA ≤ $I_O$ ≤ 500 mA PWM operation | 0.98×$V_{NOM}$ | $V_{NOM}$ | 1.02×$V_{NOM}$ | V |
| | | TPS62674 | 2.3V ≤ $V_I$ ≤ 5.5V, 0mA ≤ $I_O$ ≤ 500 mA PWM operation | 0.98×$V_{NOM}$ | $V_{NOM}$ | 1.02×$V_{NOM}$ | V |
| | | TPS62675 TPS626751 TPS626765 | 2.3V ≤ $V_I$ ≤ 4.8V, 0mA ≤ $I_O$ ≤ 650 mA PFM/PWM operation | 0.98×$V_{NOM}$ | $V_{NOM}$ | 1.03×$V_{NOM}$ | V |
| | | | 2.3V ≤ $V_I$ ≤ 5.5V, 0mA ≤ $I_O$ ≤ 650 mA PWM operation | 0.98×$V_{NOM}$ | $V_{NOM}$ | 1.02×$V_{NOM}$ | V |
| | Line regulation | | $V_I$ = $V_O$ + 0.5V (min 2.3V) to 5.5V, $I_O$ = 200 mA | | 0.23 | | %/V |
| | Load regulation | | $I_O$ = 0mA to 500 mA. PWM operation | | –0.00045 | | %/mA |
| | Feedback input resistance | | | | 480 | | kΩ |
| $\Delta V_O$ | Power-save mode ripple voltage | TPS62671 | $I_O$ = 1mA, $V_O$ = 1.8 V | | 14 | | $mV_{PP}$ |
| | | TPS62675 TPS626751 TPS626765 TPS62679 | $I_O$ = 1mA, $V_O$ = 1.2 V | | 16 | | $mV_{PP}$ |
| **TIMING** | | | | | | | |
| | Start-up time | TPS62671 | $I_O$ = 0mA, Time from active EN to $V_O$ | | 130 | | µs |
| | | TPS62674 TPS626751 TPS626765 | $I_O$ = 0mA, Time from EXTCLK clock active to $V_O$ | | 125 | | µs |
| | | TPS62679 | $I_O$ = 0mA, Time from EXTCLK clock active to $V_O$ L = 1µH DCR = 240mΩ 0603 (TY CKP1608S1R0) $C_O$ = 2.2µF 4V 0402 (TY AMK105BJ225MP) | | 430 | | µs |
| | Shutdown time | TPS62674 TPS62679 | $I_O$ = 0mA, Time from EXTCLK clock inactive to $V_O$ down $C_O$ = 4.7µF 6.3V 0402 (Murata GRM155R60J475M) | | 1.2 | | ms |
| | | | $I_O$ = 0mA, Time from EXTCLK clock inactive to $V_O$ down L = 1µH DCR = 240mΩ 0603 (TY CKP1608S1R0) $C_O$ = 2.2µF 4V 0402 (TY AMK105BJ225MP) | | 600 | | µs |

## 8.6 Typical Characteristics

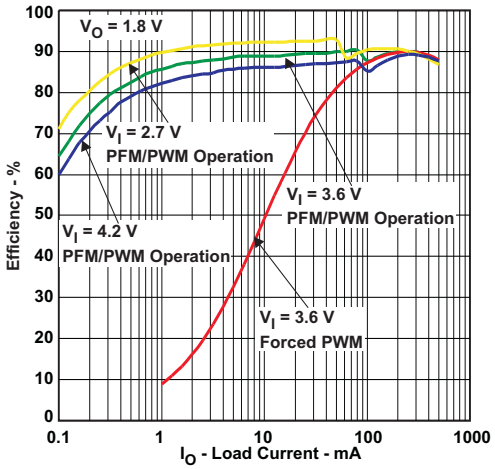



Figure 1. Efficiency vs Load Current

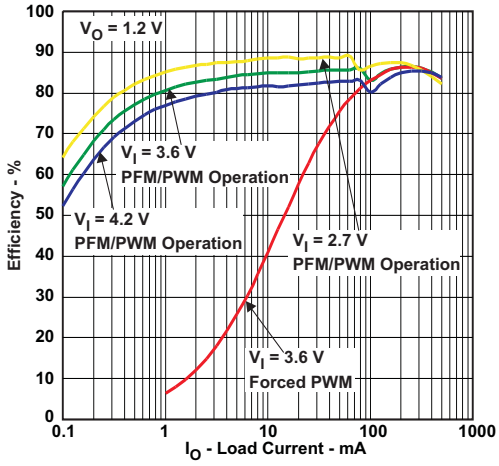



Figure 2. Efficiency vs Load Current

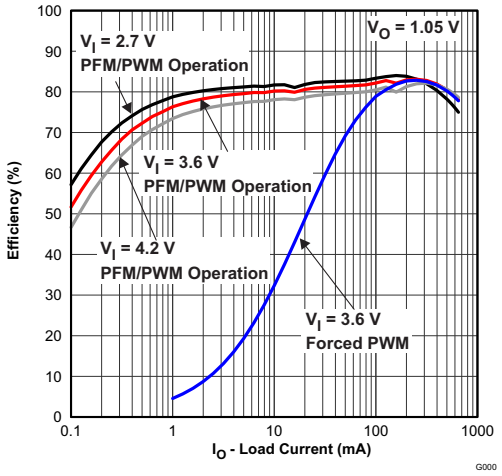



Figure 3. Efficiency vs Load Current

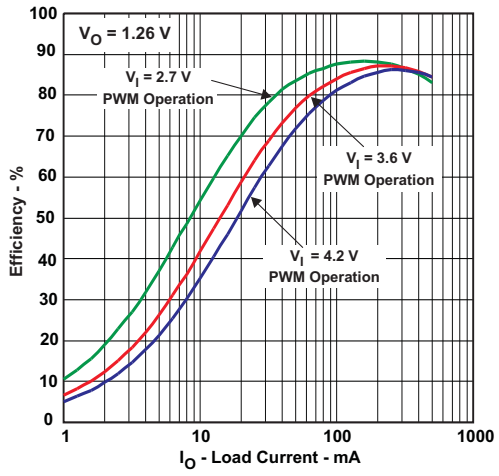



Figure 4. Efficiency vs Load Current

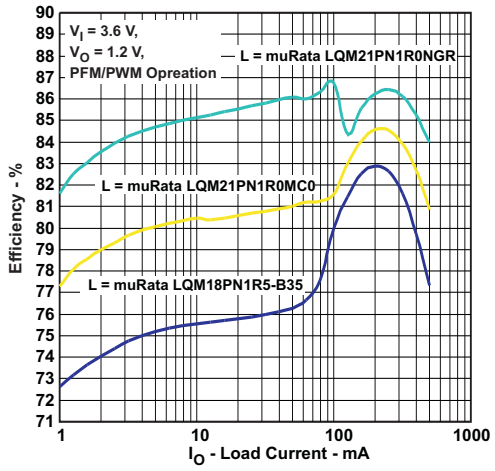



Figure 5. Efficiency vs Load Current

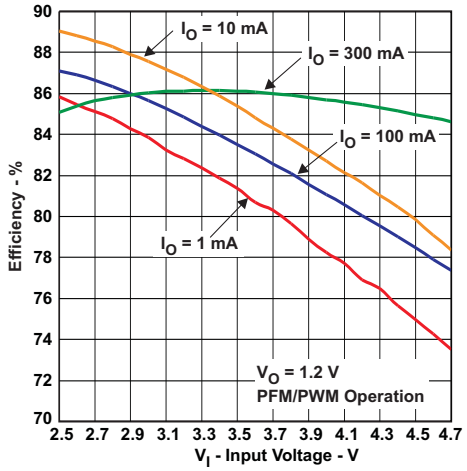



Figure 6. Efficiency vs Input Voltage

## Typical Characteristics (continued)

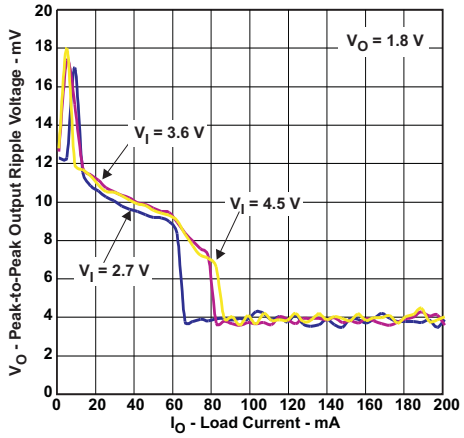



**Figure 7. Peak-To-Peak Output Ripple Voltage vs Load Current**

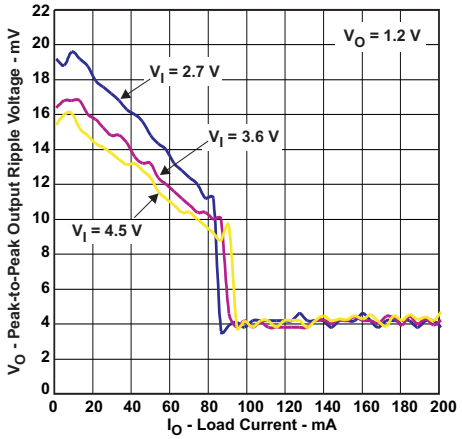



**Figure 8. Peak-To-Peak Output Ripple Voltage vs Load Current**

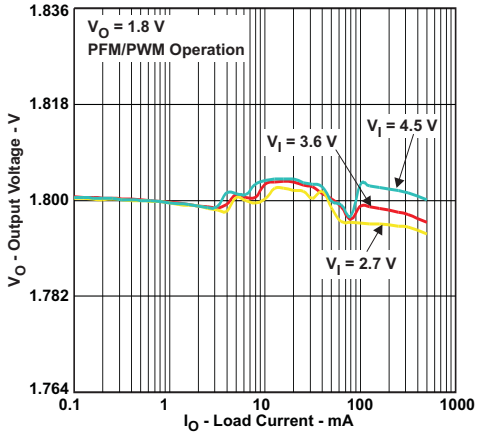



**Figure 9. DC Output Voltage vs Load Current**

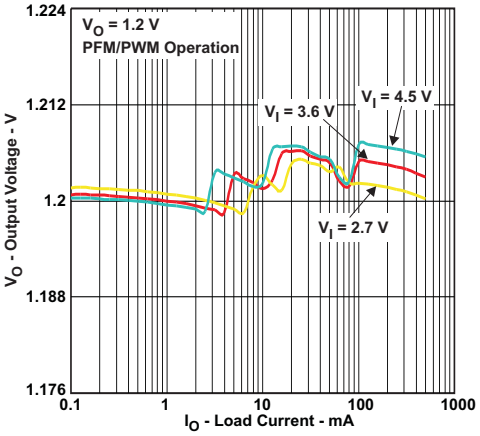



**Figure 10. DC Output Voltage vs Load Current**

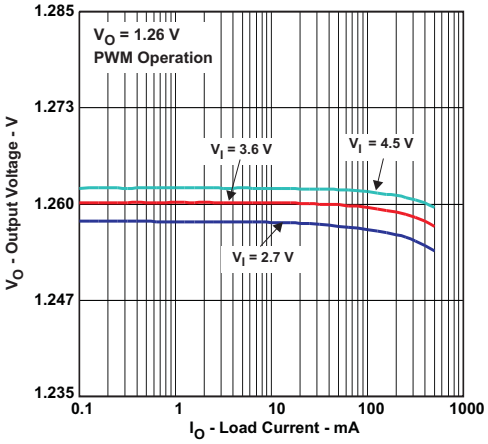



**Figure 11. DC Output Voltage vs Load Current**

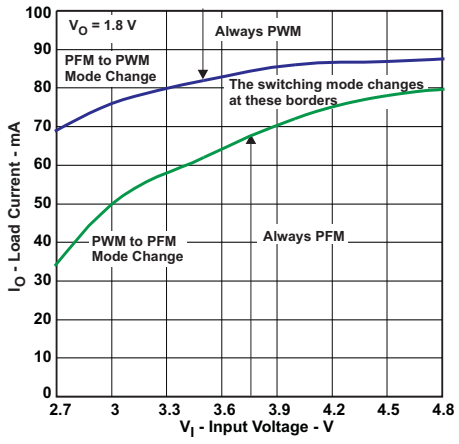



**Figure 12. PFM/PWM Boundaries**

## Typical Characteristics (continued)

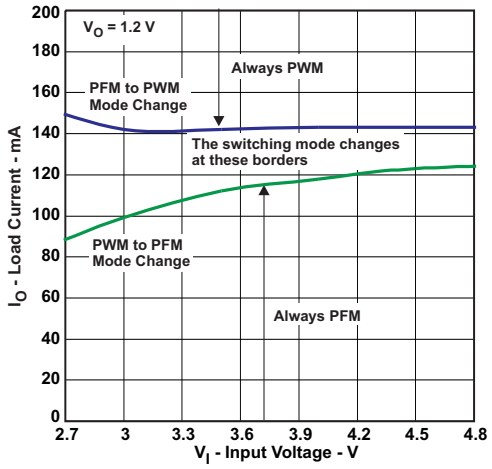



**Figure 13. PFM/PWM Boundaries**

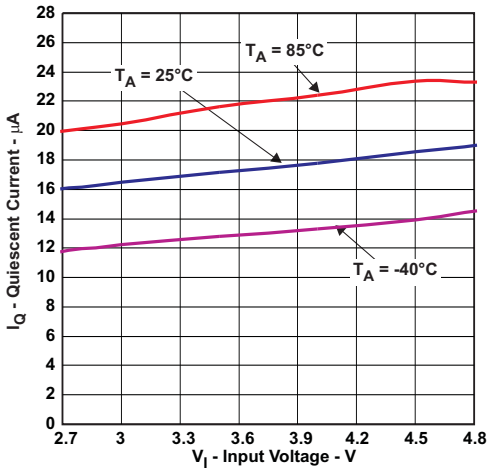



**Figure 14. Quiescent Current vs Input Voltage**

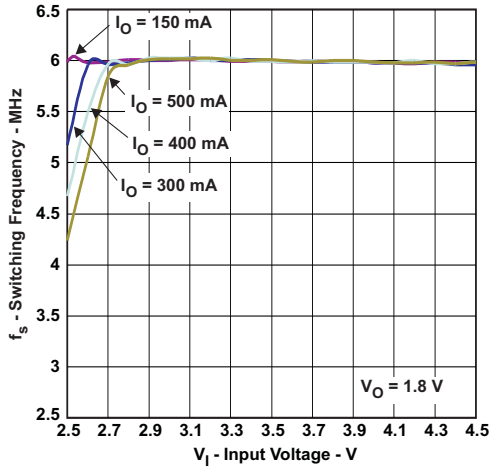



**Figure 15. PWM Switching Frequency vs Input Voltage**

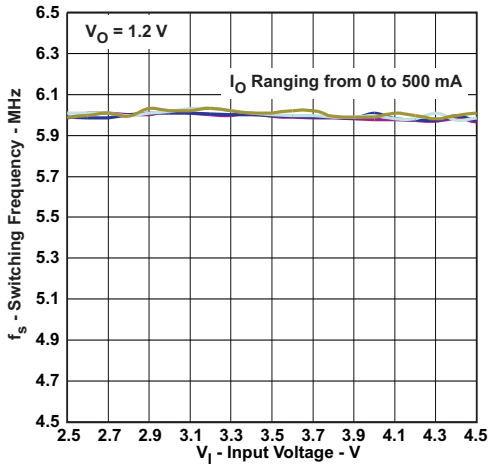



**Figure 16. PWM Switching Frequency vs Input Voltage**

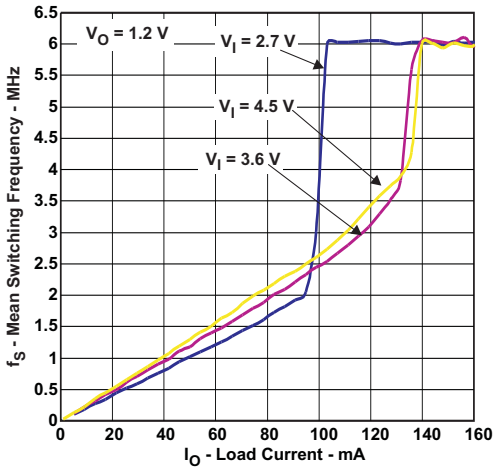



**Figure 17. PFM Switching Frequency vs Input Voltage**

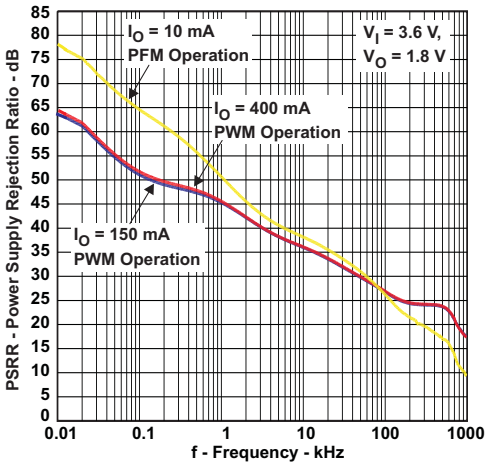



**Figure 18. PSRR vs Frequency**

## Typical Characteristics (continued)

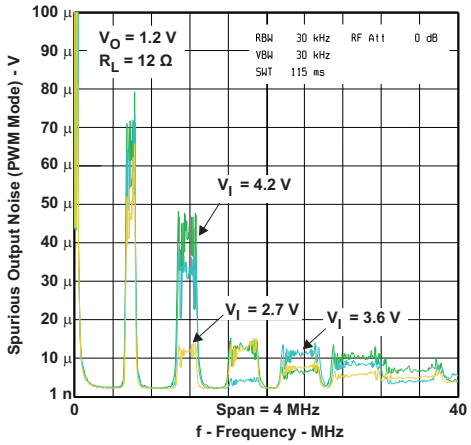



**Figure 19. Spurious Output Noise (PWM Mode) vs Frequency**

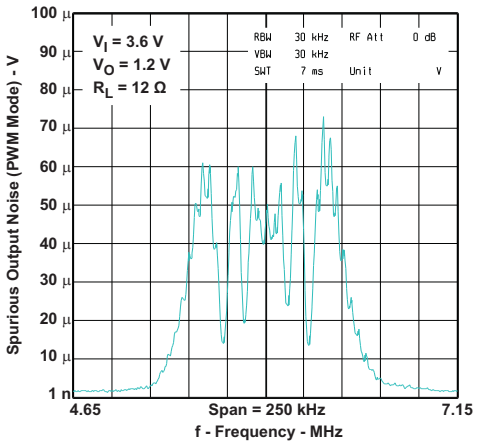



**Figure 20. Spurious Output Noise (PWM Mode) vs Frequency**

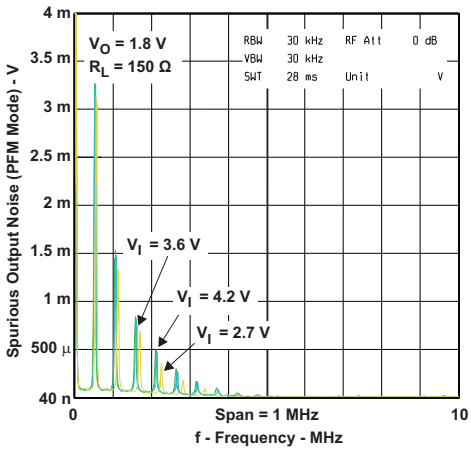



**Figure 21.**

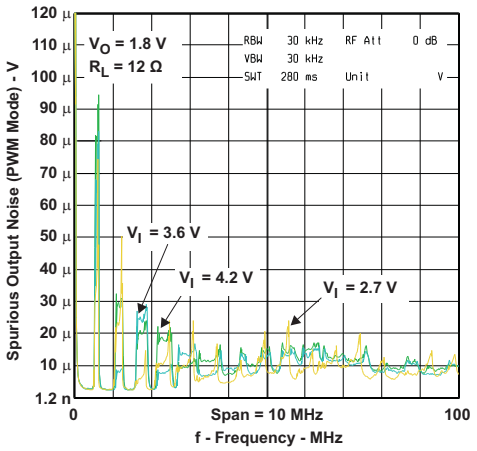



**Figure 22.**

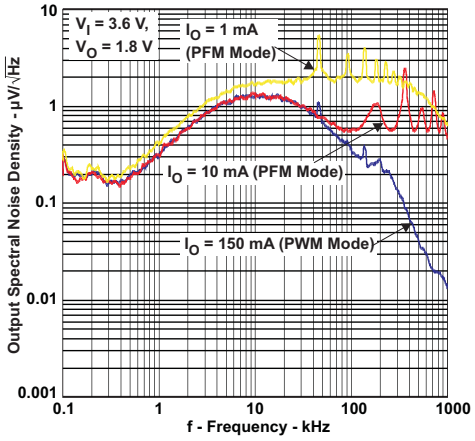



**Figure 23. Output Spectral Noise Density vs Frequency**

# 9 Parameter Measurement Information

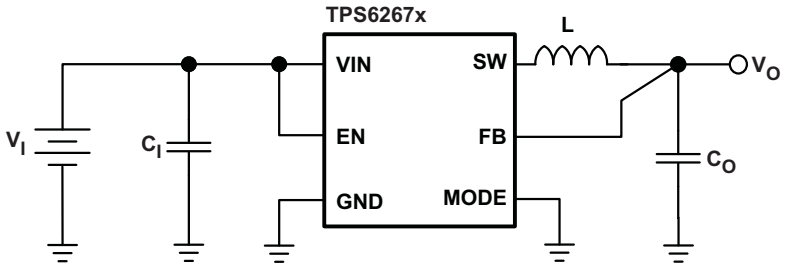



**Figure 24. Measurement Setup**

List of components:

- L = MURATA LQM21PN1R0NGR
- $C_I$ = MURATA GRM155R60J225ME15 (2.2µF, 6.3V, 0402, X5R)
- $C_O$ = MURATA GRM155R60J475M (4.7µF, 6.3V, 0402, X5R)

# 10 Detailed Description

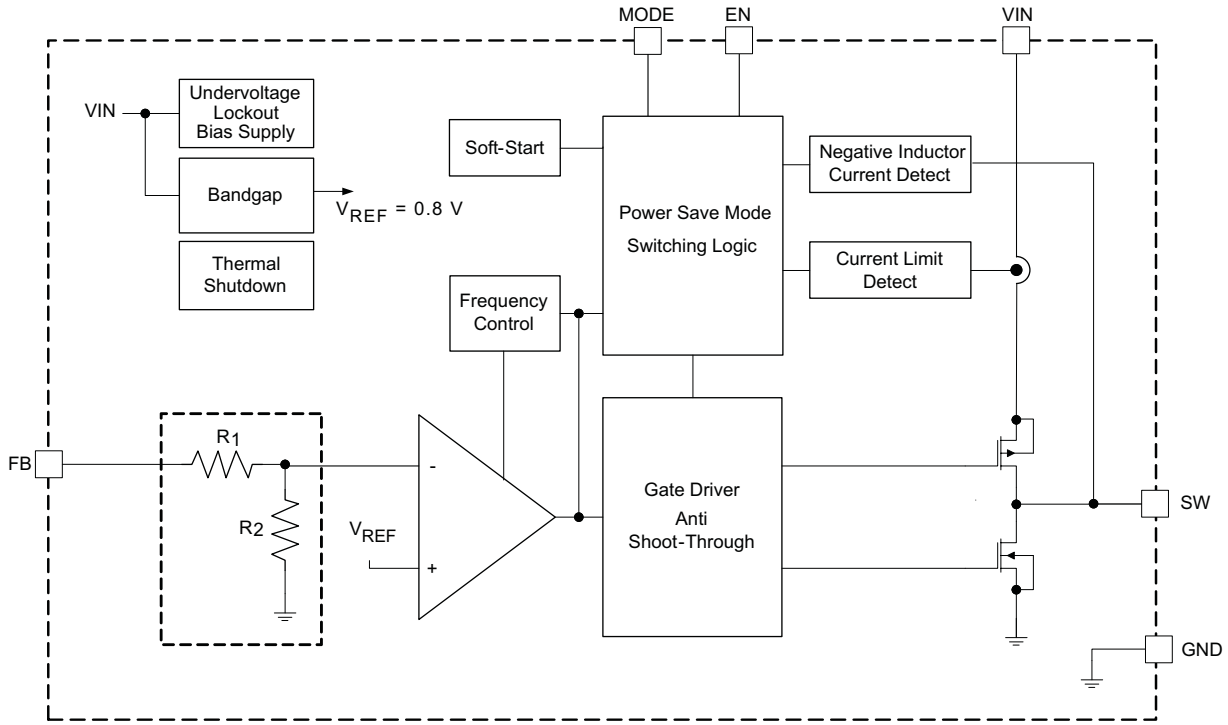
## 10.1 Overview

The TPS6267x synchronous step-down converters typically operate at a regulated 6-MHz frequency pulse width modulation (PWM) at moderate to heavy load currents. At light load currents, the TPS6267x converters operate in power-save mode with pulse frequency modulation (PFM). The converters use a unique frequency locked ring oscillating modulator to achieve *best-in-class* load and line response and allow the use of tiny inductors and small ceramic input and output capacitors. At the beginning of each switching cycle, the P-channel MOSFET switch is turned on and the inductor current ramps up rising the output voltage until the main comparator trips, then the control logic turns off the switch.

One key advantage of the non-linear architecture is that there is no traditional feed-back loop. The loop response to change in $V_O$ is essentially instantaneous, which explains the transient response. The absence of a traditional, high-gain compensated linear loop means that the TPS6267x is inherently stable over a range of L and $C_O$. Although this type of operation normally results in a switching frequency that varies with input voltage and load current, an internal frequency lock loop (FLL) holds the switching frequency constant over a large range of operating conditions. Combined with *best in class* load and line transient response characteristics, the low quiescent current of the device (ca. 17µA) allows to maintain high efficiency at light load, while preserving fast transient response for applications requiring tight output regulation.

Using the YFD package allows for a low profile solution size (0.4mm max height, including external components). The recommended external components are stated within the application information. The maximum output current is 500/650mA when these specific low profile external components are used.

## 10.2 Functional Block Diagram



## 10.3 Feature Description

### 10.3.1 Switching Frequency

The magnitude of the internal ramp, which is generated from the duty cycle, reduces for duty cycles either set of 50%. Thus, there is less overdrive on the main comparator inputs which tends to slow the conversion down. The intrinsic maximum operating frequency of the converter is about 10MHz to 12MHz, which is controlled to circa. 6MHz by a frequency locked loop.

When high or low duty cycles are encountered, the loop runs out of range and the conversion frequency falls below 6MHz. The tendency is for the converter to operate more towards a "constant inductor peak current" rather than a "constant frequency". In addition to this behavior which is observed at high duty cycles, it is also noted at low duty cycles.

When the converter is required to operate towards the 6MHz nominal at extreme duty cycles, the application can be assisted by decreasing the ratio of inductance (L) to the output capacitor's equivalent serial inductance (ESL). This increases the *ESL step* seen at the main comparator's feed-back input thus decreasing its propagation delay, hence increasing the switching frequency.

### 10.3.2 Power Save Mode

If the load current decreases, the converter will enter Power Save Mode operation automatically (does not apply for TPS62674). During power-save mode the converter operates in discontinuous current (DCM) single-pulse PFM mode, which produces low output ripple compared with other PFM architectures.

When in power-save mode, the converter resumes its operation when the output voltage trips below the nominal voltage. It ramps up the output voltage with a minimum of one pulse and goes into power-save mode when the inductor current has returned to a zero steady state. The PFM on-time varies inversely proportional to the input voltage and proportional to the output voltage giving the regulated switching frequency when in steady-state.

PFM mode is left and PWM operation is entered as the output current can no longer be supported in PFM mode. As a consequence, the DC output voltage is typically positioned ca. 0.5% above the nominal output voltage and the transition between PFM and PWM is seamless.

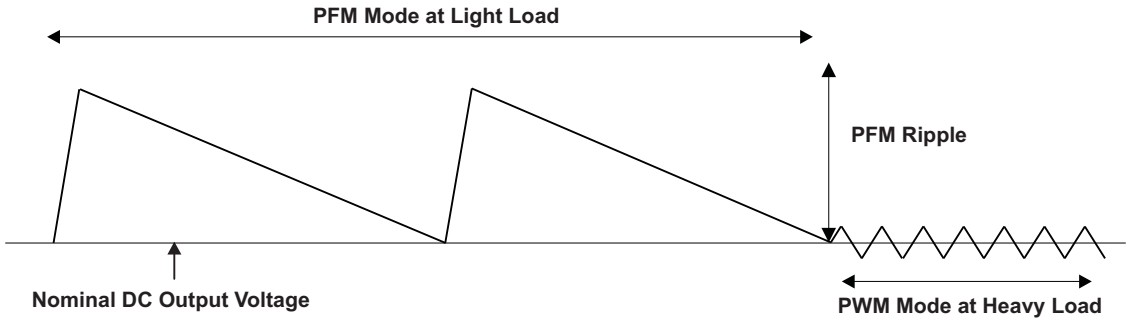



**Figure 25. Operation in PFM Mode and Transfer to PWM Mode**

### 10.3.3 Mode Selection

The MODE pin allows to select the operating mode of the device. Connecting this pin to GND enables the automatic PWM and power-save mode operation. The converter operates in regulated frequency PWM mode at moderate to heavy loads and in the PFM mode during light loads, which maintains high efficiency over a wide load current range.

Pulling the MODE pin high forces the converter to operate in the PWM mode even at light load currents. The advantage is that the converter modulates its switching frequency according to a spread spectrum PWM modulation technique allowing simple filtering of the switching harmonics in noise-sensitive applications. In this mode, the efficiency is lower compared to the power-save mode during light loads. Notice that the TPS62674 device only permits PWM operation and required the MODE input to be tied high.

For additional flexibility, it is possible to switch from power-save mode to PWM mode during operation. This allows efficient power management by adjusting the operation of the converter to the specific system requirements.

## Feature Description (continued)

### 10.3.4 Spread Spectrum, PWM Frequency Dithering

The goal is to spread out the emitted RF energy over a larger frequency range so that the resulting EMI is similar to white noise. The end result is a spectrum that is continuous and lower in peak amplitude, making it easier to comply with electromagnetic interference (EMI) standards and with the power supply ripple requirements in cellular and non-cellular wireless applications. Radio receivers are typically susceptible to narrowband noise that is focused on specific frequencies.

Switching regulators can be particularly troublesome in applications where electromagnetic interference (EMI) is a concern. Switching regulators operate on a cycle-by-cycle basis to transfer power to an output. In most cases, the frequency of operation is either fixed or regulated, based on the output load. This method of conversion creates large components of noise at the frequency of operation (fundamental) and multiples of the operating frequency (harmonics).

The spread spectrum architecture varies the switching frequency by ca. ±10% of the nominal switching frequency thereby significantly reducing the peak radiated and conducting noise on both the input and output supplies. The frequency dithering scheme is modulated with a triangle profile and a modulation frequency $f_m$.

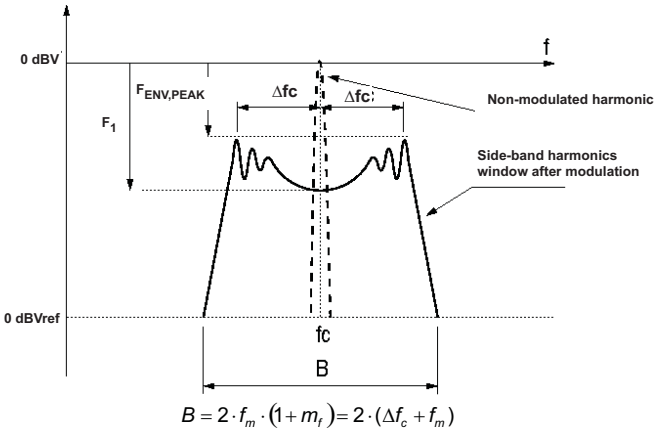



**Figure 26. Spectrum of a Frequency Modulated Sin. Wave with Sinusoidal Variation in Time**

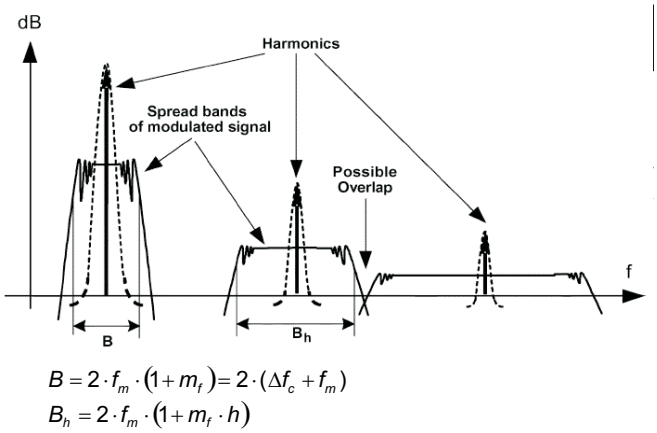



**Figure 27. Spread Bands of Harmonics in Modulated Square Signals** (1)

The above figures show that after modulation the sideband harmonic is attenuated compared to the non-modulated harmonic, and the harmonic energy is spread into a certain frequency band. The higher the modulation index (*mf*) the larger the attenuation.

$$m_f = \frac{\delta \times f_c}{f_m} \tag{1}$$

With:

$f_c$ is the carrier frequency

$f_m$ is the modulating frequency (approx. 0.008*$f_c$)

$\delta$ is the modulation ratio (approx 0.1)

$$\delta = \frac{\Delta f_c}{f_c} \tag{2}$$

The maximum switching frequency $f_c$ is limited by the process and finally the parameter modulation ratio (δ), together with $f_m$ , which is the side-band harmonics bandwidth around the carrier frequency $f_c$. The bandwidth of a frequency modulated waveform is approximately given by the Carson's rule and can be summarized as:

$$B = 2 \times f_m \times (1 + m_f) = 2 \times (\Delta f_c + f_m) \tag{3}$$

(1) Spectrum illustrations and formulae (Figure 26 and Figure 27) copyright IEEE TRANSACTIONS ON ELECTROMAGNETIC COMPATIBILITY, VOL. 47, NO.3, AUGUST 2005. See *References* section for full citation.

## Feature Description (continued)

$f_m$ < RBW: The receiver is not able to distinguish individual side-band harmonics, so, several harmonics are added in the input filter and the measured value is higher than expected in theoretical calculations.

$f_m$ > RBW: The receiver is able to properly measure each individual side-band harmonic separately, so the measurements match with the theoretical calculations.

### 10.3.5 Short-Circuit Protection

The TPS6267x integrates a P-channel MOSFET current limit to protect the device against heavy load or short circuits. When the current in the P-channel MOSFET reaches its current limit, the P-channel MOSFET is turned off and the N-channel MOSFET is turned on. The regulator continues to limit the current on a cycle-by-cycle basis.

As soon as the output voltage falls below ca. 0.4V, the converter current limit is reduced to half of the nominal value. Because the short-circuit protection is enabled during start-up, the device does not deliver more than half of its nominal current limit until the output voltage exceeds approximately 0.5V. This needs to be considered when a load acting as a current sink is connected to the output of the converter.

### 10.3.6 Thermal Shutdown

As soon as the junction temperature, $T_J$, exceeds typically 140°C, the device goes into thermal shutdown. In this mode, the P- and N-channel MOSFETs are turned off. The device continues its operation when the junction temperature again falls below typically 130°C.

## 10.4 Device Functional Modes

### 10.4.1 Soft Start

The TPS6267x has an internal soft-start circuit that limits the inrush current during start-up. This limits input voltage drops when a battery or a high-impedance power source is connected to the input of the converter.

The soft-start system progressively increases the on-time from a minimum pulse-width of 35ns as a function of the output voltage. This mode of operation continues for c.a. 100µs after enable. Should the output voltage not have reached its target value by this time, such as in the case of heavy load, the soft-start transitions to a second mode of operation.

The converter then operates in a current limit mode, specifically the P-MOS current limit is set to half the nominal limit, and the N-channel MOSFET remains on until the inductor current has reset. After a further 100 µs, the device ramps up to the full current limit operation if the output voltage has risen above 0.5V (approximately). Therefore, the start-up time mainly depends on the output capacitor and load current.

### 10.4.2 Enable

The TPS6267x device starts operation when EN is set high and starts up with the soft start as previously described. For proper operation, the EN pin must be terminated and must not be left floating.

Pulling the EN pin Low, forces the device into shutdown with a shutdown quiescent current of typically 0.1µA. In this mode, the P and N-channel MOSFETs are turned off, the internal resistor feedback divider is disconnected, and the entire internal-control circuitry is switched off.

When an external clock signal (EXTCLK), 4MHz to 27MHz, is applied to the TPS62674 or TPS62679, the DC/DC converter powers-up automatically within approx. 120µs (TPS62674) or 450µs (TPS62679). When the external clock signal is stopped, the DC/DC converter is powered down and the output capacitor is discharged actively.

### 10.4.3 Active Output Discharge

The TPS62674, TPS626751, TPS626765 and TPS62679 actively discharge the output capacitor when turned off. The integrated discharge resistor has a typical resistance of 70 Ω. The required time to discharge the output capacitor at the output node depends on load current and the output capacitance value.

## Device Functional Modes (continued)

### 10.4.4 Undervoltage Lockout

The undervoltage lockout circuit prevents the device from misoperation at low input voltages. It prevents the converter from turning on the switch or rectifier MOSFET under undefined conditions. The TPS6267x device have a UVLO threshold set to 2.05V (typical). Fully functional operation is permitted down to 2.1V input voltage.

# 11 Application and Implementation

## 11.1 Application Information

TPS6267x are high frequency step-down converters. They can convert from a 2.3V to 4.8V input source to various fixed output voltages, providing up to 500mA. Needing a minimum amount of external components, the design procedure is easy to do and usually done by choosing input and output capacitor as well as an appropriate inductor which is described in the sections below.

## 11.2 Typical Applications

### 11.2.1 TPS6267x Point-Of-Load Supply

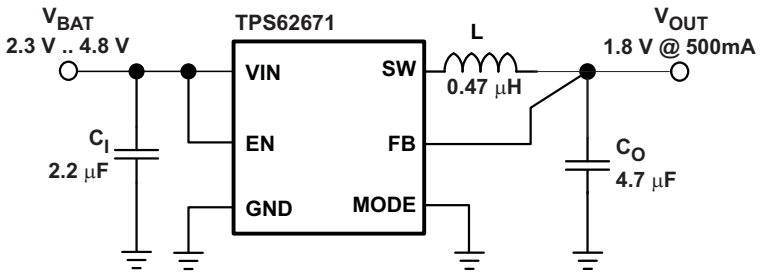



**Figure 28. 1.8V/0.5A Power Supply Using TPS62671**

#### *11.2.1.1 Design Requirements*

The TPS6267x devices are optimized to work with the external components as shown in Figure 28, providing stable operation for the input voltage and load current range up to 500mA. Connecting the MODE pin to GND provides PWM/PFM operation.

#### *11.2.1.2 Detailed Design Procedure*

##### 11.2.1.2.1 Inductor Selection

The TPS6267x series of step-down converters have been optimized to operate with an effective inductance value in the range of 0.3µH to 1.8µH and with output capacitors in the range of 2.2µF to 4.7µF. The internal compensation is optimized to operate with an output filter of L = 0.47µH and $C_O$ = 2.2µF. Larger or smaller inductor values can be used to optimize the performance of the device for specific operation conditions. For more details, see the *CHECKING LOOP STABILITY* section.

The inductor value affects its peak-to-peak ripple current, the PWM-to-PFM transition point, the output voltage ripple and the efficiency. The selected inductor has to be rated for its dc resistance and saturation current. The inductor ripple current ($\Delta I_L$) decreases with higher inductance and increases with higher $V_I$ or $V_O$.

$$\Delta I_L = \frac{V_O}{V_I} \times \frac{V_I - V_O}{L \times f_{SW}} \qquad \Delta I_{L(MAX)} = I_{O(MAX)} + \frac{\Delta I_L}{2} \tag{4}$$

With:

$f_{SW}$ = switching frequency (6 MHz typical)

L = inductor value

$\Delta I_L$ = peak-to-peak inductor ripple current

$I_{L(MAX)}$ = maximum inductor current

In high-frequency converter applications, the efficiency is essentially affected by the inductor AC resistance (i.e. quality factor) and to a smaller extent by the inductor DCR value. To achieve high efficiency operation, care should be taken in selecting inductors featuring a quality factor above 25 at the switching frequency. Increasing the inductor value produces lower RMS currents, but degrades transient response. For a given physical inductor size, increased inductance usually results in an inductor with lower saturation current.

The total losses of the coil consist of both the losses in the DC resistance, $R_{(DC)}$, and the following frequency-dependent components:

## Typical Applications (continued)

- The losses in the core material (magnetic hysteresis loss, especially at high switching frequencies)
- Additional losses in the conductor from the skin effect (current displacement at high frequencies)
- Magnetic field losses of the neighboring windings (proximity effect)
- Radiation losses

The following inductor series from different suppliers have been used with the TPS6267x converters.

**Table 1. List of Inductors(1)**

| MANUFACTURER | SERIES | DIMENSIONS (in mm) |
|---|---|---|
| MURATA | LQM21PN1R0NGR | 2.0 x 1.2 x 1.0 max. height |
| | LQM21PNR47MC0 | 2.0 x 1.2 x 0.55 max. height |
| | LQM21PN1R0MC0 | 2.0 x 1.2 x 0.55 max. height |
| | LQM18PN1R5-B35 | 1.6 x 0.8 x 0.4 max. height |
| | LQM18PN1R5-A62 | 1.6 x 0.8 x 0.33 max. height |
| PANASONIC | ELGTEAR82NA | 2.0 x 1.2 x 1.0 max. height |
| SEMCO | CIG21L1R0MNE | 2.0 x 1.2 x 1.0 max. height |
| TAIYO YUDEN | BRC1608T1R0M6, BRC1608TR50M6 | 1.6 x 0.8 x 1.0 max. height |
| | CKP1608L1R5M | 1.6 x 0.8 x 0.55 max. height |
| | CKP1608U1R5M | 1.6 x 0.8 x 0.4 max. height |
| | CKP1608S1R0M, CKP1608S1R5M | 1.6 x 0.8 x 0.33 max. height |
| | NM2012NR82, NM2012N1R0 | 2.0 x 1.2 x 1.0 max. height |
| TDK | MLP2012SR82T | 2.0 x 1.2 x 0.6 max. height |
| TOKO | MDT2012-CR1R0A | 2.0 x 1.2 x 1.0 max. height |

(1) See *Third-Party Products Disclaimer*

#### 11.2.1.2.2 Output Capacitor Selection

The advanced fast-response voltage mode control scheme of the TPS6267x allows the use of tiny ceramic capacitors. Ceramic capacitors with low ESR values have the lowest output voltage ripple and are recommended. For best performance, the device should be operated with a minimum effective output capacitance of 0.8µF. The output capacitor requires either an X7R or X5R dielectric. Y5V and Z5U dielectric capacitors, aside from their wide variation in capacitance over temperature, become resistive at high frequencies.

At nominal load current, the device operates in PWM mode and the overall output voltage ripple is the sum of the voltage step caused by the output capacitor ESL and the ripple current flowing through the output capacitor impedance.

At light loads, the output capacitor limits the output ripple voltage and provides holdup during large load transitions. A 2.2µF or 4.7µF ceramic capacitor typically provides sufficient bulk capacitance to stabilize the output during large load transitions. The typical output voltage ripple is 1% of the nominal output voltage $V_O$.

For best operation (i.e. optimum efficiency over the entire load current range, proper PFM/PWM auto transition), the TPS6267x requires a minimum output ripple voltage in PFM mode. The typical output voltage ripple is ca. 1% of the nominal output voltage $V_O$. The PFM pulses are time controlled resulting in a PFM output voltage ripple and PFM frequency that depends (first order) on the capacitance seen at the converter's output.

#### 11.2.1.2.3 Input Capacitor Selection

Because of the nature of the buck converter having a pulsating input current, a low ESR input capacitor is required to prevent large voltage transients that can cause misbehavior of the device or interferences with other circuits in the system. For most applications, a 1 or 2.2-µF capacitor is sufficient. If the application exhibits a noisy or erratic switching frequency, the remedy will probably be found by experimenting with the value of the input capacitor.

Take care when using only ceramic input capacitors. When a ceramic capacitor is used at the input and the power is being supplied through long wires, such as from a wall adapter, a load step at the output can induce ringing at the VIN pin. This ringing can couple to the output and be mistaken as loop instability or could even damage the part. Additional "bulk" capacitance (electrolytic or tantalum) should in this circumstance be placed between $C_I$ and the power source lead to reduce ringing than can occur between the inductance of the power source leads and $C_I$.

#### 11.2.1.2.4 Checking Loop Stability

The first step of circuit and stability evaluation is to look from a steady-state perspective at the following signals:

- Switching node, SW
- Inductor current, $I_L$
- Output ripple voltage, $V_{O(AC)}$

These are the basic signals that need to be measured when evaluating a switching converter. When the switching waveform shows large duty cycle jitter or the output voltage or inductor current shows oscillations, the regulation loop may be unstable. This is often a result of board layout and/or L-C combination.

As a next step in the evaluation of the regulation loop, the load transient response is tested. The time between the application of the load transient and the turn on of the P-channel MOSFET, the output capacitor must supply all of the current required by the load. $V_O$ immediately shifts by an amount equal to $\Delta I_{(LOAD)}$ x ESR, where ESR is the effective series resistance of $C_O$. $\Delta I_{(LOAD)}$ begins to charge or discharge $C_O$ generating a feedback error signal used by the regulator to return $V_O$ to its steady-state value. The results are most easily interpreted when the device operates in PWM mode.

During this recovery time, $V_O$ can be monitored for settling time, overshoot or ringing that helps judge the converter's stability. Without any ringing, the loop has usually more than 45° of phase margin.

Because the damping factor of the circuitry is directly related to several resistive parameters (e.g., MOSFET $r_{DS(on)}$) that are temperature dependant, the loop stability analysis has to be done over the input voltage range, load current range, and temperature range.

### 11.2.1.3 Application Curves

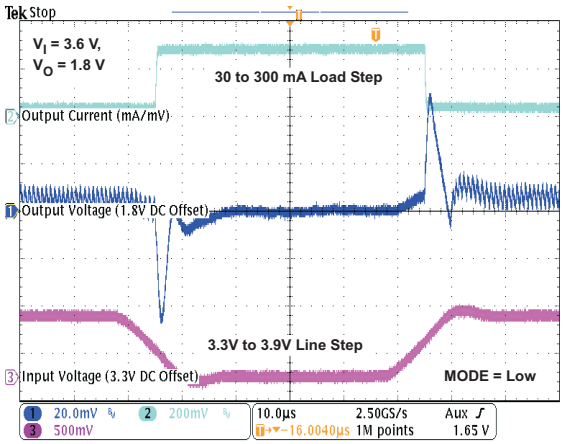



**Figure 29. Combined Line/Load Transient Response**

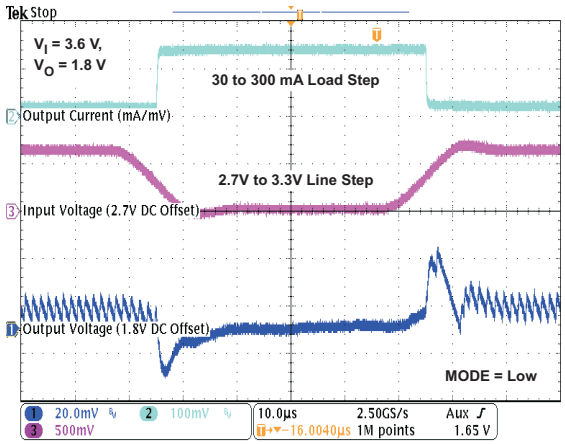



**Figure 30. Combined Line/Load Transient Response**

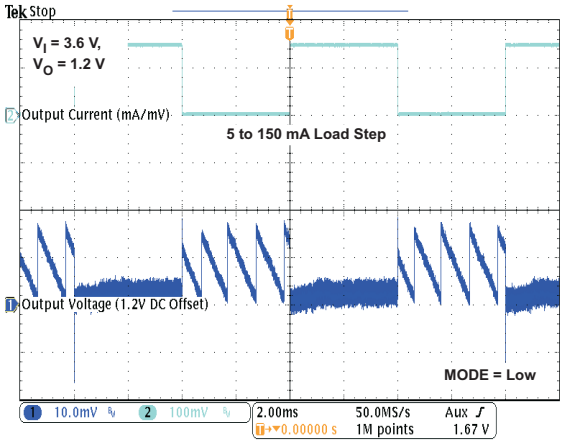



**Figure 31. Load Transient Response in PFM/PWM Operation**

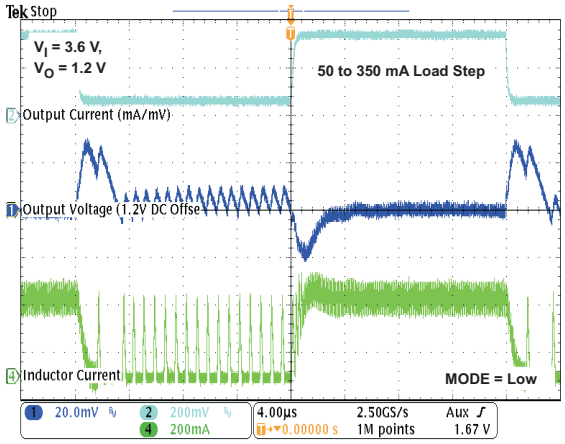



**Figure 32. Load Transient Response in PFM/PWM Operation**

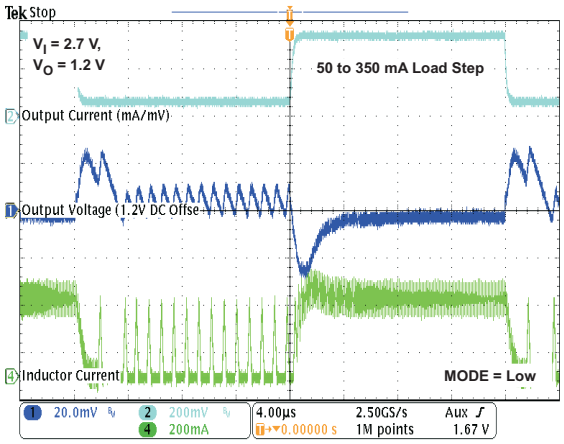



**Figure 33. Load Transient Response in PFM/PWM Operation**

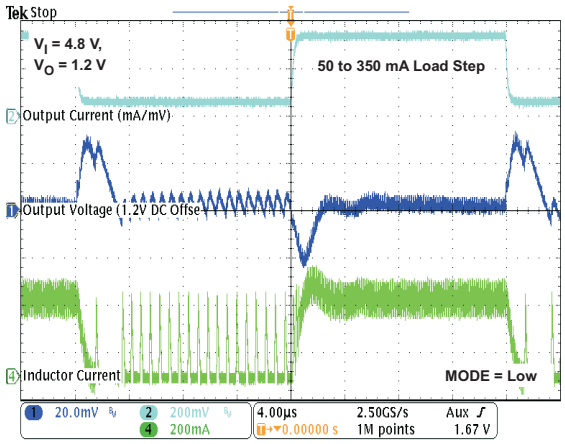



**Figure 34. Load Transient Response in PFM/PWM Operation**

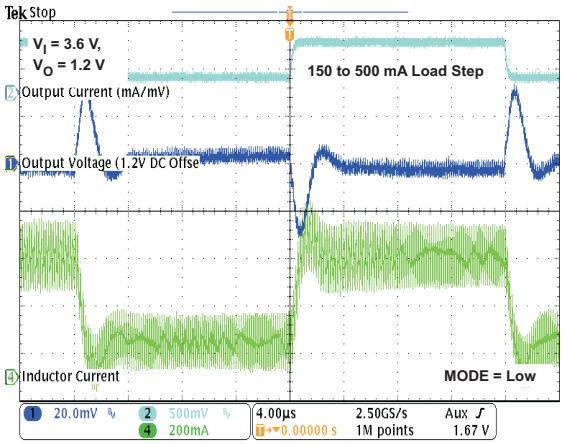



**Figure 35. Load Transient Response in PWM/PWM Operation**

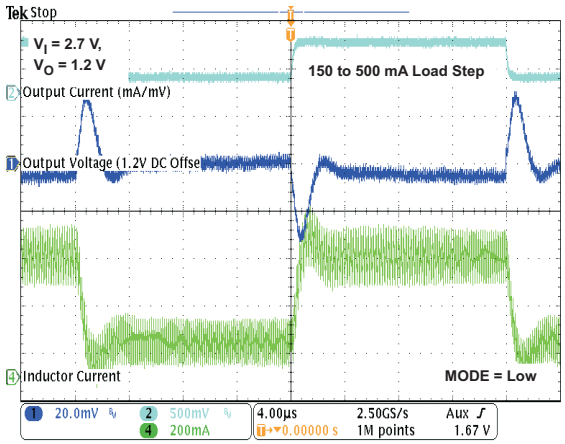



**Figure 36. Load Transient Response in PWM/PWM Operation**

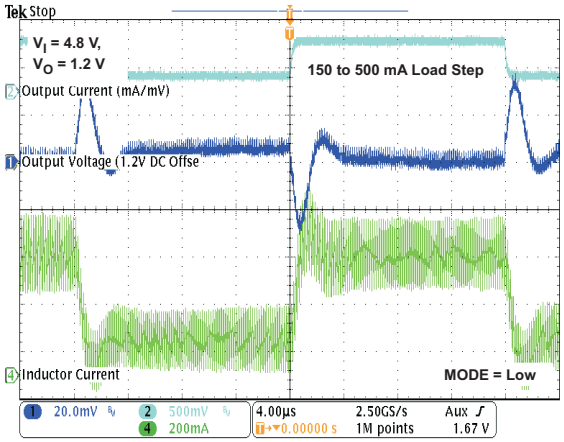



**Figure 37. Load Transient Response in PWM/PWM Operation**

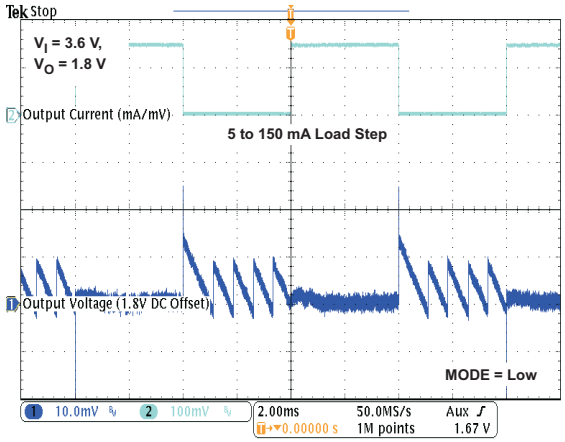



**Figure 38. Load Transient Response in PFM/PWM Operation**

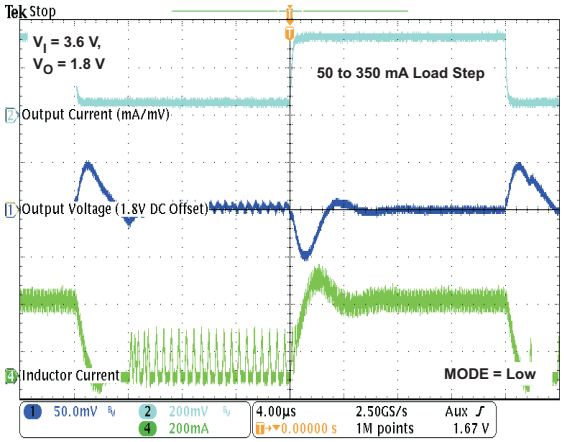



**Figure 39. Load Transient Response in PFM/PWM Operation**

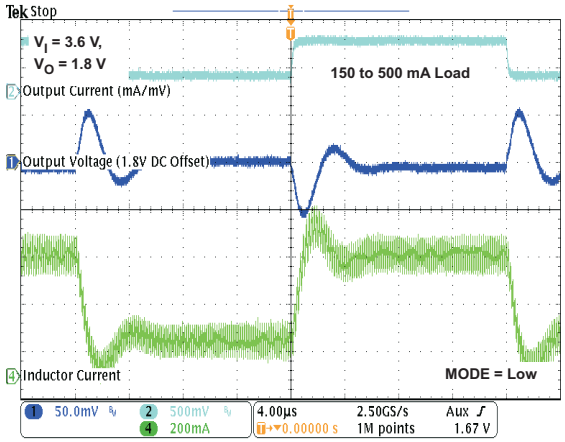



**Figure 40. Load Transient Response in PWM/PWM Operation**

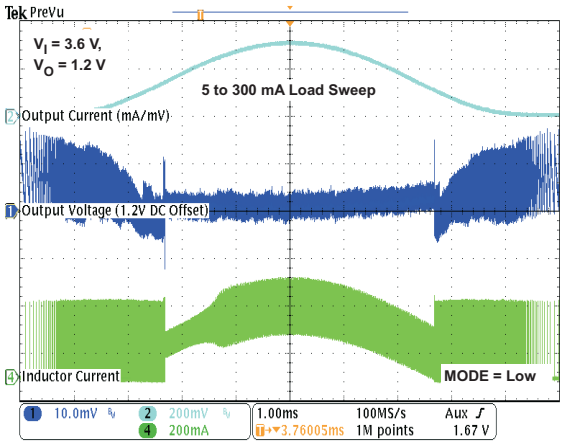



**Figure 41. AC Load Transient Response**

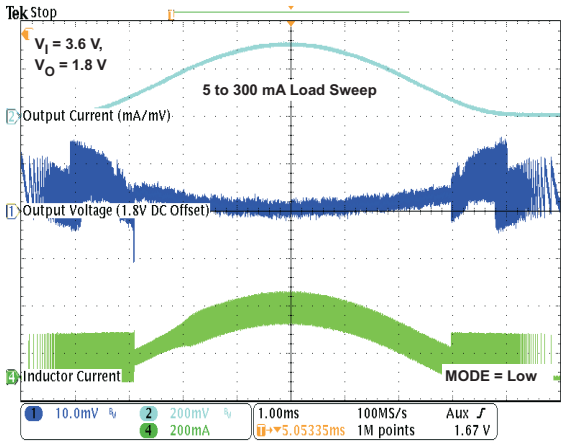



**Figure 42. AC Load Transient Response**

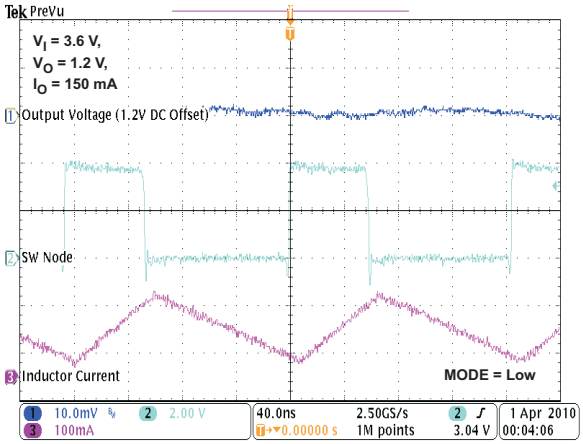



**Figure 43. Typical PWM Mode Operation**

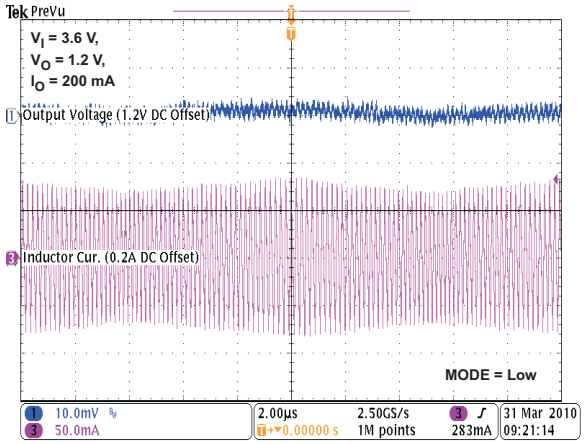



**Figure 44. PWM Mode Operation - SSFM Modulation**

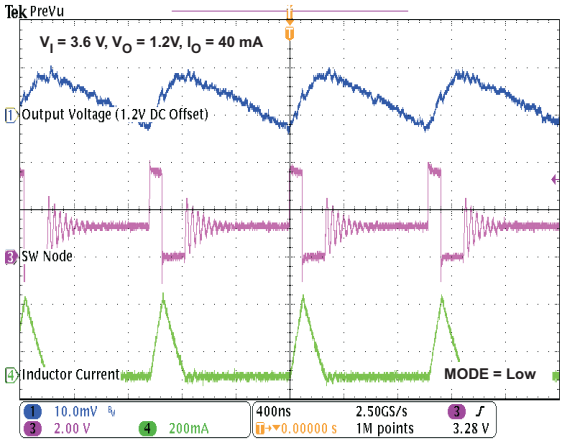



**Figure 45. Typical Power Save Mode Operation**

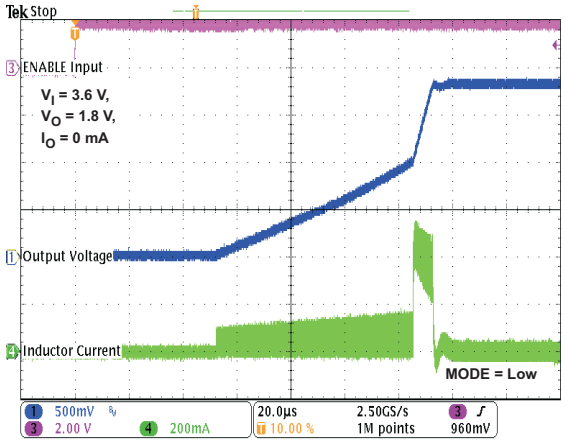



**Figure 46. Start-Up**

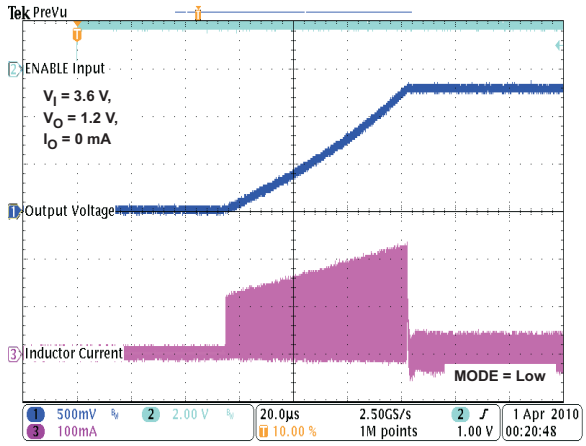



**Figure 47. Start-Up**

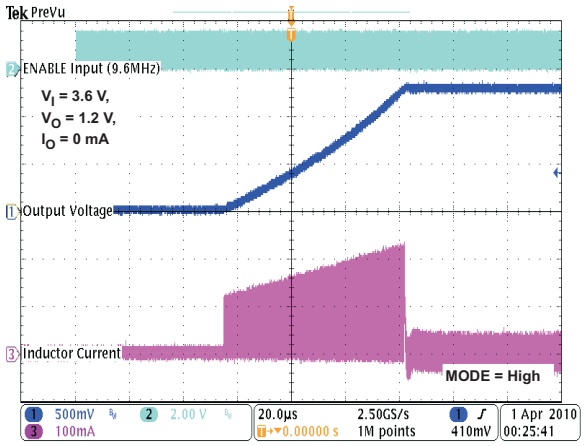



**Figure 48. Start-Up (RF Clock)**

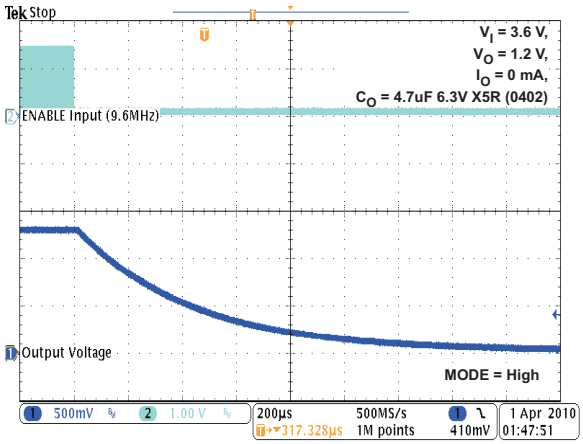



**Figure 49. Shut-Down (RF Clock)**

### 11.2.2 1.26V CMOS Sensor Embedded Power Solution — Featuring Sub 0.4mm Profile

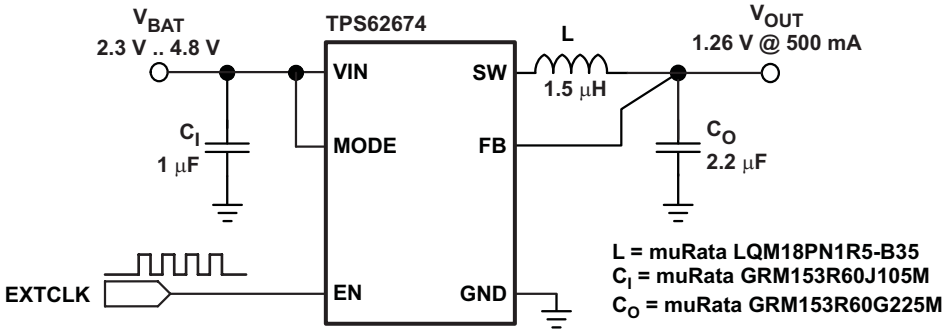



**Figure 50. 1.26V CMOS Sensor Embedded Power Solution — Featuring Sub 0.4mm Profile**

#### *11.2.2.1 Design Requirements*

A CMOS sensor power supply providing a voltage of 1.26V is needed. The profile height mustn't exceed 0.4mm and the device is enabled/switched off by external clock signal.

#### *11.2.2.2 Detailed Design Procedure*

See previous *Detailed Design Procedure*. To provide 1.26V, the TPS62674 or TPS62679 can be used. The inductor can be chosen from Table 1, selecting low profile device. Startup and shut down sequence with external clock are shown below.

#### *11.2.2.3 Application Curves*

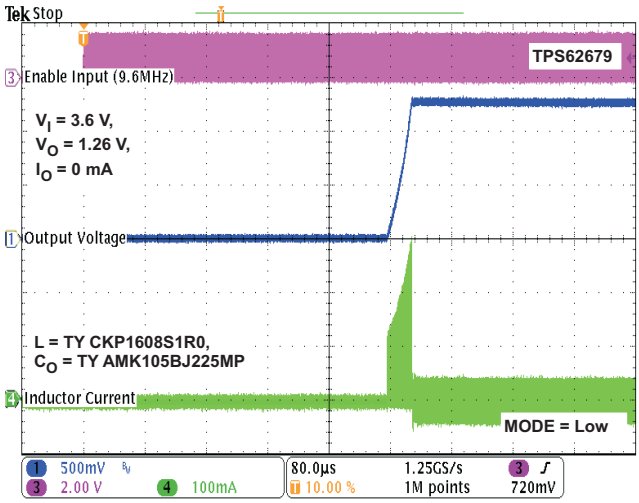



**Figure 51. Start-Up (RF Clock)**

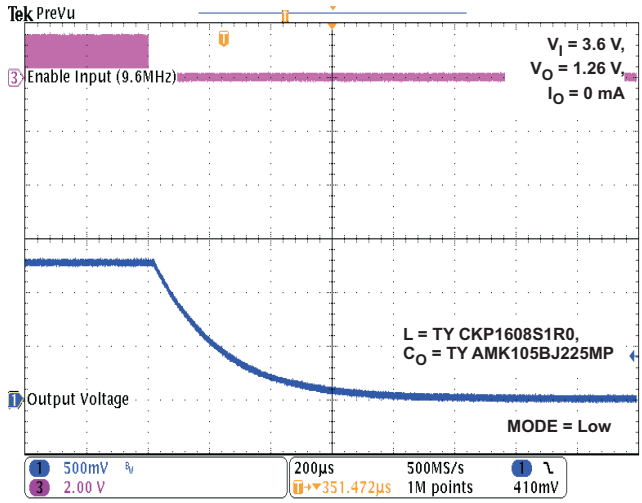



**Figure 52. Shut-Down (RF Clock)**

## 12 Power Supply Recommendations

The power supply of TPS6267X devices needs to have appropriate current rating to support input and output voltage range for the maximum load current.

# 13 Layout

## 13.1 Layout Guidelines

As for all switching power supplies, the layout is an important step in the design. High-speed operation of the TPS6267x devices demand careful attention to PCB layout. Care must be taken in board layout to get the specified performance. If the layout is not carefully done, the regulator could show poor line and/or load regulation, stability and switching frequency issues as well as EMI problems. It is critical to provide a low inductance, impedance ground path. Therefore, use wide and short traces for the main current paths.

The ground pins of the dc/dc converter must be strongly connected to the PCB ground (i.e. reference potential across the system). These ground pins serve as the return path for both the control circuitry and the synchronous rectifier. Furthermore, due to its high frequency switching circuitry, it is imperative for the input capacitor to be as close to the SMPS device as possible, and that there is an unbroken ground plane under the TPS6267x and its external passives. Additionally, minimizing the area between the SW pin trace and inductor will limit high frequency radiated energy. The feed-back line should be routed away from noisy components and traces (e.g. SW line).

The output capacitor carries the inductor ripple current. While not as critical as the input capacitor, an unbroken ground connection from this capacitor's ground return to the inductor, input capacitor and SMPS device will reduce the output voltage ripple and it's associated ESL step. This is a critical aspect to achieve best loop and frequency stability.

High frequency currents tend to find their way on the ground plane along a mirror path directly beneath the incident path on the top of the board. If there are slits or cuts in the ground plane due to other traces on that layer, the current will be forced to go around the slits. If high frequency currents are not allowed to flow back through their natural least-area path, excessive voltage will build up and radiated emissions will occur. There should be a group of vias in the surrounding of the dc/dc converter leading directly down to an internal ground plane. To minimize parasitic inductance, the ground plane should be as close as possible to the top plane of the PCB (i.e. onto which the components are located).

## 13.2 Layout Example

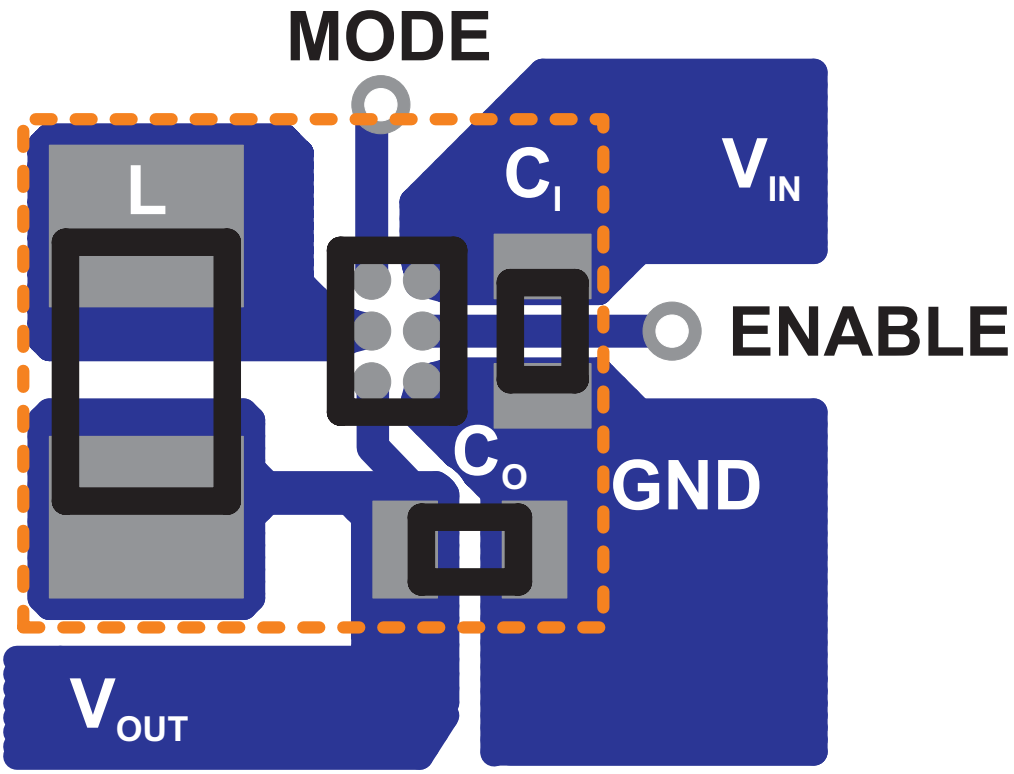



**Figure 53. Suggested Layout (Top)**

# 14 Device and Documentation Support

## 14.1 Device Support

### 14.1.1 Third-Party Products Disclaimer

TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

## 14.2 Documentation Support

### 14.2.1 Related Documentation

#### *14.2.1.1 References*

"EMI Reduction in Switched Power Converters Using Frequency Modulation Techniques", in *IEEE TRANSACTIONS ON ELECTROMAGNETIC COMPATIBILITY, VOL. 4, NO. 3, AUGUST 2005, pp 569-576* by Josep Balcells, Alfonso Santolaria, Antonio Orlandi, David González, Javier Gago.

## 14.3 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

**Table 2. Related Links**

| PARTS | PRODUCT FOLDER | SAMPLE & BUY | TECHNICAL DOCUMENTS | TOOLS & SOFTWARE | SUPPORT & COMMUNITY |
|---|---|---|---|---|---|
| TPS62671 | Click here | Click here | Click here | Click here | Click here |
| TPS62672 | Click here | Click here | Click here | Click here | Click here |
| TPS62674 | Click here | Click here | Click here | Click here | Click here |
| TPS62675 | Click here | Click here | Click here | Click here | Click here |
| TPS626751 | Click here | Click here | Click here | Click here | Click here |
| TPS626765 | Click here | Click here | Click here | Click here | Click here |
| TPS62679 | Click here | Click here | Click here | Click here | Click here |

## 14.4 Trademarks

NanoFree is a trademark of Texas Instruments.
Bluetooth is a trademark of Bluetooth SIG, Inc.

## 14.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## 14.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms and definitions.

## 15 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| TPS62671YFDR | ACTIVE | DSBGA | YFD | 6 | 3000 | Green (RoHS & no Sb/Br) | SNAGCU | Level-1-260C-UNLIM | -40 to 85 | NZ | Samples |
| TPS62671YFDT | ACTIVE | DSBGA | YFD | 6 | 250 | Green (RoHS & no Sb/Br) | SNAGCU | Level-1-260C-UNLIM | -40 to 85 | NZ | Samples |
| TPS62672YFDR | PREVIEW | DSBGA | YFD | 6 | | TBD | Call TI | Call TI | -40 to 85 | | |
| TPS62672YFDT | PREVIEW | DSBGA | YFD | 6 | | TBD | Call TI | Call TI | -40 to 85 | | |
| TPS62674YFDR | ACTIVE | DSBGA | YFD | 6 | 3000 | Green (RoHS & no Sb/Br) | SNAGCU | Level-1-260C-UNLIM | -40 to 85 | PN | Samples |
| TPS62674YFDT | ACTIVE | DSBGA | YFD | 6 | 250 | Green (RoHS & no Sb/Br) | SNAGCU | Level-1-260C-UNLIM | -40 to 85 | PN | Samples |
| TPS626751YFDR | ACTIVE | DSBGA | YFD | 6 | 3000 | Green (RoHS & no Sb/Br) | SNAGCU | Level-1-260C-UNLIM | -40 to 85 | E3 | Samples |
| TPS626751YFDT | ACTIVE | DSBGA | YFD | 6 | 250 | Green (RoHS & no Sb/Br) | SNAGCU | Level-1-260C-UNLIM | -40 to 85 | E3 | Samples |
| TPS62675YFDR | ACTIVE | DSBGA | YFD | 6 | 3000 | Green (RoHS & no Sb/Br) | SNAGCU | Level-1-260C-UNLIM | -40 to 85 | OB | Samples |
| TPS62675YFDT | ACTIVE | DSBGA | YFD | 6 | 250 | Green (RoHS & no Sb/Br) | SNAGCU | Level-1-260C-UNLIM | -40 to 85 | OB | Samples |
| TPS626765YFDR | ACTIVE | DSBGA | YFD | 6 | 3000 | Green (RoHS & no Sb/Br) | SNAGCU | Level-1-260C-UNLIM | -40 to 85 | EH | Samples |
| TPS626765YFDT | ACTIVE | DSBGA | YFD | 6 | 250 | Green (RoHS & no Sb/Br) | SNAGCU | Level-1-260C-UNLIM | -40 to 85 | EH | Samples |
| TPS62679ZYFMR | ACTIVE | DSLGA | YFM | 6 | 3000 | Green (RoHS & no Sb/Br) | Call TI | Level-1-260C-UNLIM | -40 to 85 | | Samples |
| TPS62679ZYFMT | ACTIVE | DSLGA | YFM | 6 | 250 | Green (RoHS & no Sb/Br) | Call TI | Level-1-260C-UNLIM | -40 to 85 | | Samples |

**(1)** The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

**(2)** Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

**(3)** MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

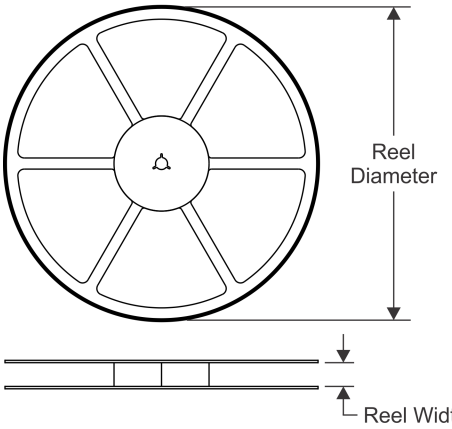
**(4)** There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

**(5)** Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

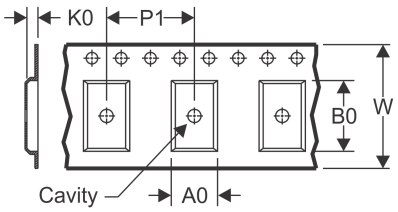
**(6)** Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

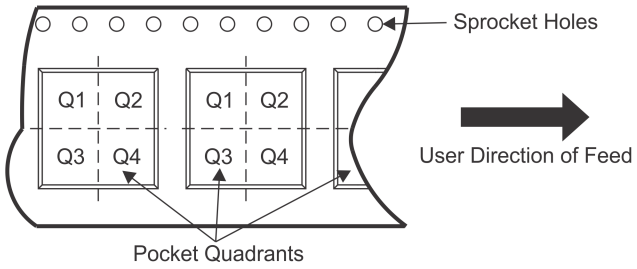



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

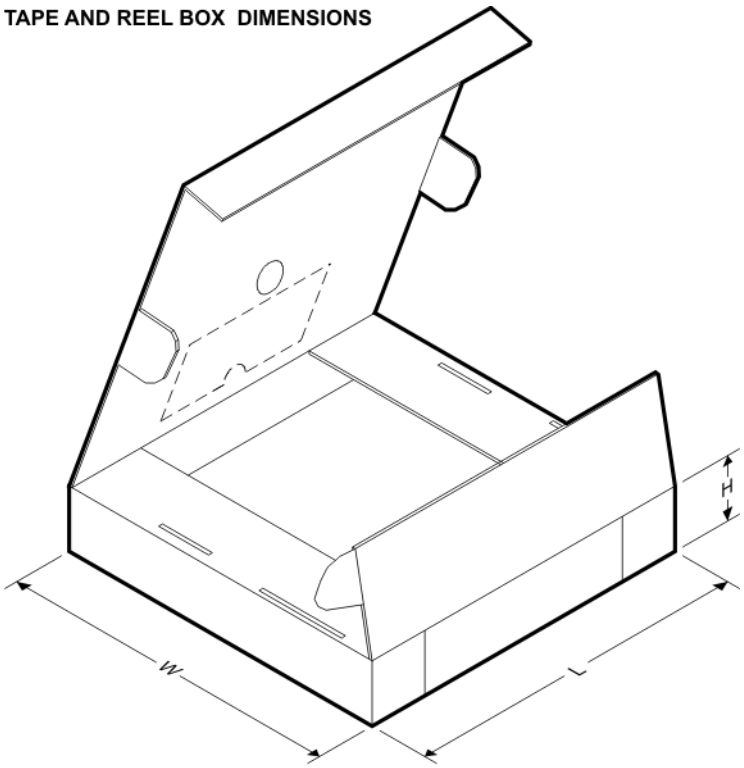
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TPS62671YFDR | DSBGA | YFD | 6 | 3000 | 180.0 | 8.4 | 1.03 | 1.53 | 0.56 | 4.0 | 8.0 | Q1 |
| TPS62671YFDT | DSBGA | YFD | 6 | 250 | 180.0 | 8.4 | 1.03 | 1.53 | 0.56 | 4.0 | 8.0 | Q1 |
| TPS62674YFDR | DSBGA | YFD | 6 | 3000 | 180.0 | 8.4 | 1.03 | 1.53 | 0.56 | 4.0 | 8.0 | Q1 |
| TPS62674YFDT | DSBGA | YFD | 6 | 250 | 180.0 | 8.4 | 1.03 | 1.53 | 0.56 | 4.0 | 8.0 | Q1 |
| TPS626751YFDR | DSBGA | YFD | 6 | 3000 | 180.0 | 8.4 | 1.03 | 1.53 | 0.56 | 4.0 | 8.0 | Q1 |
| TPS626751YFDT | DSBGA | YFD | 6 | 250 | 180.0 | 8.4 | 1.03 | 1.53 | 0.56 | 4.0 | 8.0 | Q1 |
| TPS626765YFDR | DSBGA | YFD | 6 | 3000 | 180.0 | 8.4 | 1.03 | 1.53 | 0.56 | 4.0 | 8.0 | Q1 |
| TPS626765YFDT | DSBGA | YFD | 6 | 250 | 180.0 | 8.4 | 1.03 | 1.53 | 0.56 | 4.0 | 8.0 | Q1 |
| TPS62679ZYFMR | DSLGA | YFM | 6 | 3000 | 180.0 | 8.4 | 1.04 | 1.41 | 0.21 | 2.0 | 8.0 | Q1 |
| TPS62679ZYFMT | DSLGA | YFM | 6 | 250 | 180.0 | 8.4 | 1.04 | 1.41 | 0.21 | 2.0 | 8.0 | Q1 |

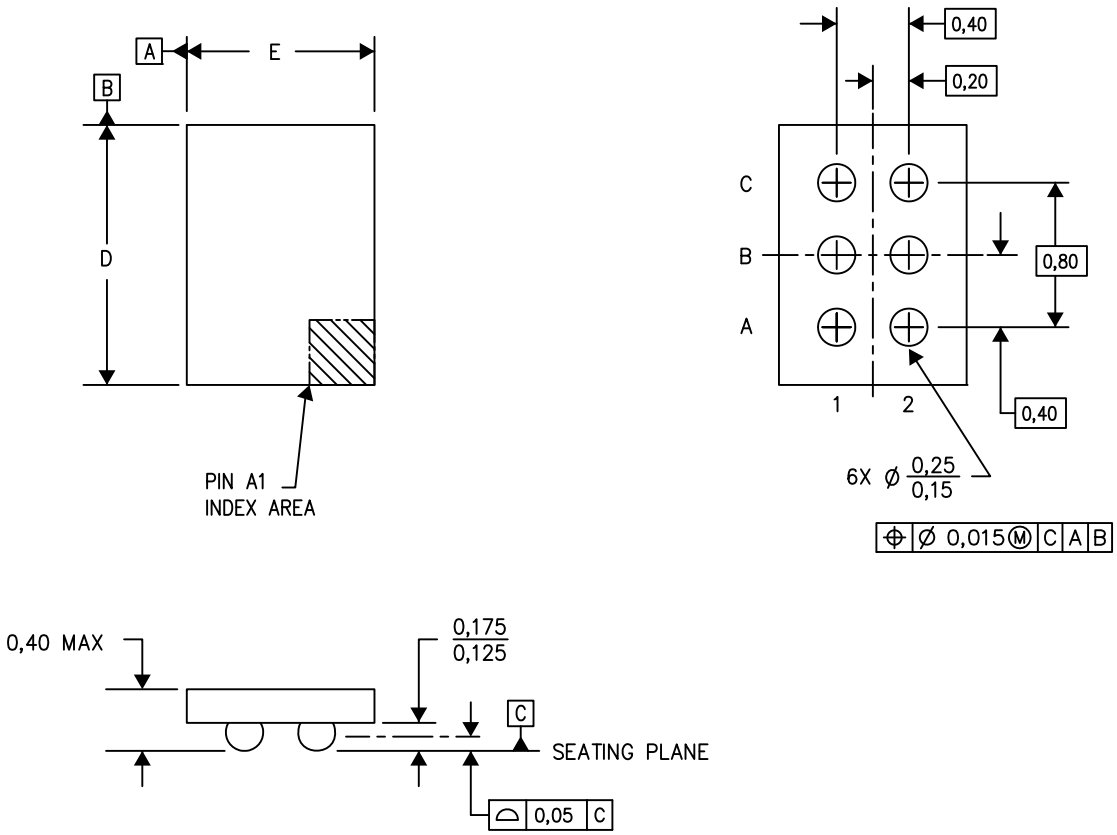
**TAPE AND REEL BOX DIMENSIONS**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| TPS62671YFDR | DSBGA | YFD | 6 | 3000 | 220.0 | 220.0 | 34.0 |
| TPS62671YFDT | DSBGA | YFD | 6 | 250 | 220.0 | 220.0 | 34.0 |
| TPS62674YFDR | DSBGA | YFD | 6 | 3000 | 220.0 | 220.0 | 34.0 |
| TPS62674YFDT | DSBGA | YFD | 6 | 250 | 220.0 | 220.0 | 34.0 |
| TPS626751YFDR | DSBGA | YFD | 6 | 3000 | 220.0 | 220.0 | 34.0 |
| TPS626751YFDT | DSBGA | YFD | 6 | 250 | 220.0 | 220.0 | 34.0 |
| TPS626765YFDR | DSBGA | YFD | 6 | 3000 | 182.0 | 182.0 | 17.0 |
| TPS626765YFDT | DSBGA | YFD | 6 | 250 | 182.0 | 182.0 | 17.0 |
| TPS62679ZYFMR | DSLGA | YFM | 6 | 3000 | 210.0 | 185.0 | 35.0 |
| TPS62679ZYFMT | DSLGA | YFM | 6 | 250 | 210.0 | 185.0 | 35.0 |

YFD (R–XBGA–N6) DIE–SIZE BALL GRID ARRAY




D: Max = 1.33 mm, Min = 1.27 mm

E: Max = 0.956 mm, Min =0.896 mm

4209617–2/F 05/13

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. NanoFree™ package configuration.

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