

TPS61093-Q1 Low Input Boost Converter With Integrated Power Diode and Input/Output Isolation

1 Features

- AEC-Q100 Qualified with the Following Results:
 - Device Temperature Grade 1: -40°C to 125°C Junction Operating Temperature Range
- Input Range: 1.6-V to 6-V
- Integrated Power Diode and Isolation FET
- 20-V Internal Switch FET With 1.1-A Current
- Fixed 1.2-MHz Switching Frequency
- Efficiency at 15-V Output up to 88%
- Overload and Overvoltage Protection
- Programmable Soft Start-up
- Load Discharge Path After IC Shutdown
- 2.5 × 2.5 × 0.8 mm SON Package

2 Applications

- OLED Power Supply
- 3.3-V to 12-V, 5-V to 12-V Boost Converter

3 Description

The TPS61093-Q1 is a 1.2-MHz, fixed-frequency boost converter designed for high integration and high reliability. The IC integrates a 20-V power switch, input/output isolation switch, and power diode. When the output current exceeds the overload limit, the isolation switch of the IC opens up to disconnect the output from the input. This disconnection protects the IC and the input supply. The isolation switch also disconnects the output from the input during shut down to minimize leakage current. When the IC is shutdown, the output capacitor is discharged to a low voltage level by internal diodes. Other protection features include 1.1-A peak overcurrent protection (OCP) at each cycle, output overvoltage protection (OVP), thermal shutdown, and undervoltage lockout (UVLO).

With its 1.6-V minimum input voltage, the IC can be powered by two alkaline batteries, a single Li-ion battery, or 3.3-V and 5-V regulated supply. The output can be boosted up to 17-V. The TPS61093-Q1 is available in 2.5 mm × 2.5 mm SON package with thermal pad.

Device Information⁽¹⁾

| PART NUMBER | PACKAGE | BODY SIZE (NOM) |
|-------------|----------|-------------------|
| TPS61093-Q1 | SON (10) | 2.50 mm x 2.50 mm |

(1) For all available packages, see the orderable addendum at the end of the data sheet.

4 Simplified Schematic

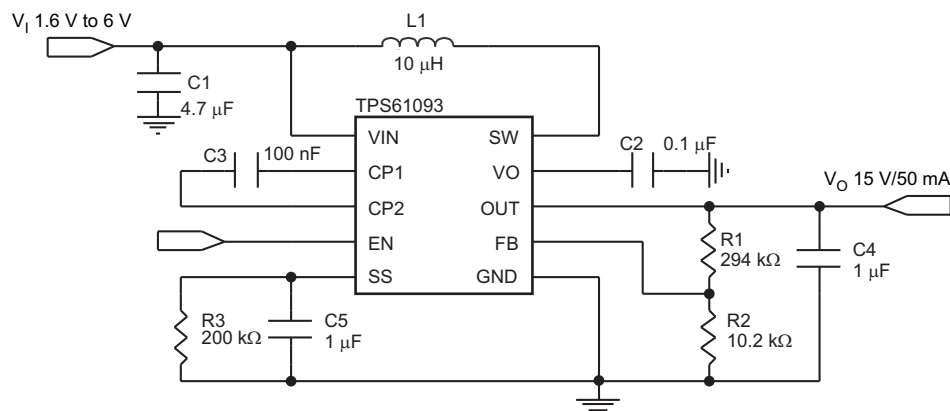


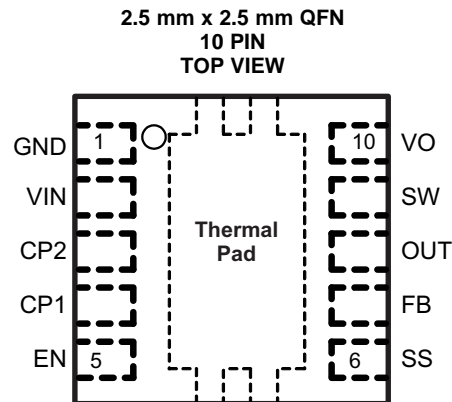
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5 Revision History

| DATE | REVISION | NOTES |
|--------------|----------|-----------------|
| January 2015 | * | Initial Release |

6 Pin Configuration and Functions



Pin Functions

| PIN | | I/O | DESCRIPTION |
|-------------|------|-----|---|
| NAME | NO. | | |
| VIN | 2 | I | IC Supply voltage input. |
| VO | 10 | O | Output of the boost converter. When the output voltage exceeds the over voltage protection (OVP) threshold, the power switch turns off until VO drops below the over voltage protection hysteresis. |
| OUT | 8 | O | Isolation switch is between this pin and VO pin. Connect load to this pin for input/output isolation during IC shutdown. See Without Isolation FET for the tradeoff between isolation and efficiency. |
| GND | 1 | – | Ground of the IC. |
| CP1, CP2 | 3, 4 | | Connect to flying capacitor for internal charge pump. |
| EN | 5 | I | Enable pin (HIGH = enable). When the pin is pulled low for 1 ms, the IC turns off and consumes less than 1- μ A current. |
| SS | 6 | I | Soft start pin. A RC network connecting to the SS pin programs soft start timing. See Start Up |
| FB | 7 | I | Voltage feedback pin for output regulation, 0.5-V regulated voltage. An external resistor divider connected to this pin programs the regulated output voltage. |
| SW | 9 | I | Switching node of the IC where the internal PWM switch operates. |
| Thermal Pad | – | – | It should be soldered to the ground plane. If possible, use thermal via to connect to ground plane for ideal power dissipation. |

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

| | MIN | MAX | UNIT |
|--|------|-----|------|
| Supply voltage on pin VIN ⁽²⁾ | -0.3 | 7 | V |
| Voltage on pins CP2, EN, and SS ⁽²⁾ | -0.3 | 7 | V |
| Voltage on pin CP1 and FB ⁽²⁾ | -0.3 | 3 | V |
| Voltage on pin SW, VO, and OUT ⁽²⁾ | -0.3 | 20 | V |
| Operating Junction Temperature Range | -40 | 150 | °C |
| T _{stg} , Storage temperature range | -55 | 150 | °C |

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values are with respect to network ground terminal.

7.2 ESD Ratings

| | | VALUE | UNIT | |
|--------------------|-------------------------|---|-------------------------------|------|
| V _(ESD) | Electrostatic discharge | Human body model (HBM), per AEC Q100-002 ⁽¹⁾ | ±2000 | |
| | | Charged device model (CDM), per AEC Q100-011 | Corner pins (1, 5, 6, and 10) | ±750 |
| | | | Other pins | ±500 |

- (1) AEC Q100-002 indicates HBM stressing is done in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | | MIN | NOM | MAX | UNIT |
|------------------|--|-----|-----|-----|------|
| V _i | Input voltage range | 1.6 | | 6 | V |
| V _o | Output voltage range at VO pin | | | 17 | V |
| L | Inductor ⁽¹⁾ | 2.2 | 4.7 | 10 | μH |
| C _{in} | Input capacitor | 4.7 | | | μF |
| C _o | Output capacitor at OUT pin ⁽¹⁾ | 1 | | 10 | μF |
| C _{fly} | Flying capacitor at CP1 and CP2 pins | 10 | | | nF |
| T _J | Operating junction temperature | -40 | | 125 | °C |
| T _A | Operating ambient temperature | -40 | | 125 | °C |

- (1) These values are recommended values that have been successfully tested in several applications. Other values may be acceptable in other applications but should be fully tested by the user.

7.4 Thermal Information

| THERMAL METRIC ⁽¹⁾ | | TPS61093-Q1 | UNIT |
|-------------------------------|--|-------------|------|
| | | DSK | |
| | | 10 PINS | |
| R _{θJA} | Junction-to-ambient thermal resistance | 49.2 | °C/W |
| R _{θJC(top)} | Junction-to-case (top) thermal resistance | 63.3 | |
| R _{θJB} | Junction-to-board thermal resistance | 23.4 | |
| Ψ _{JT} | Junction-to-top characterization parameter | 1.1 | |
| Ψ _{JB} | Junction-to-board characterization parameter | 23.0 | |
| R _{θJC(bot)} | Junction-to-case (bottom) thermal resistance | 5.7 | |

- (1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

7.5 Electrical Characteristics

V_{IN} = 3.6 V, EN = V_{IN}, T_A = T_J = -40°C to 125°C, typical values are at T_A = 25°C (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|------------------------------------|--|---------------------------------|------|------|------|------|
| SUPPLY CURRENT | | | | | | |
| V _{IN} | Input voltage range, V _{IN} | | 1.6 | | 6 | V |
| I _Q | Operating quiescent current into V _{IN} | Device PWM switching no load | | 0.9 | 1.5 | mA |
| I _{SD} | Shutdown current | EN = GND, V _{IN} = 6 V | | | 5 | μA |
| UVLO | Undervoltage lockout threshold | V _{IN} falling | | 1.5 | 1.55 | V |
| V _{hys} | Undervoltage lockout hysteresis | | | 50 | | mV |
| ENABLE AND PWM CONTROL | | | | | | |
| V _{ENH} | EN logic high voltage | V _{IN} = 1.6 V to 6 V | 1.2 | | | V |
| V _{ENL} | EN logic low voltage | V _{IN} = 1.6 V to 6 V | | | 0.3 | V |
| R _{EN} | EN pull down resistor | | 400 | 800 | 1600 | kΩ |
| VOLTAGE CONTROL | | | | | | |
| V _{REF} | Voltage feedback regulation voltage | | 0.49 | 0.5 | 0.51 | V |
| I _{FB} | Voltage feedback input bias current | | | | 100 | nA |
| f _S | Oscillator frequency | | 1.0 | 1.2 | 1.4 | MHz |
| D _{max} | Maximum duty cycle | V _{FB} = 0.1 V | 90% | 93% | | |
| POWER SWITCH, ISOLATION FET | | | | | | |
| R _{DS(ON)N} | N-channel MOSFET on-resistance | V _{IN} = 3 V | | 0.25 | 0.4 | Ω |
| R _{DS(ON)iso} | Isolation FET on-resistance | VO = 5 V | | 2.5 | 4 | Ω |
| | | VO = 3.5 V | | 4.5 | | |
| I _{LN_N} | N-channel leakage current | V _{DS} = 20 V | | | 3 | μA |
| I _{LN_iso} | Isolation FET leakage current | V _{DS} = 20 V | | | 1 | μA |
| V _F | Power diode forward voltage | Current = 500 mA | | 0.8 | | V |
| OC, ILIM, OVP SC AND SS | | | | | | |
| I _{LIM} | N-Channel MOSFET current limit | | 0.9 | 1.1 | 1.6 | A |
| V _{ovp} | Over voltage protection threshold | Measured on the VO pin | 18 | 19 | | V |
| V _{ovp_hys} | Over voltage protection hysteresis | | | 0.6 | | V |
| I _{OL} | Over load protection | | 200 | 300 | | mA |
| THERMAL SHUTDOWN | | | | | | |
| T _{shutdown} | Thermal shutdown threshold | | | 150 | | °C |
| T _{hysteresis} | Thermal shutdown hysteresis | | | 15 | | °C |

7.6 Timing Requirements

V_{IN} = 3.6 V, EN = V_{IN}, T_A = T_J = -40°C to 125°C, typical values are at T_A = 25°C (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---------------------|----------------------------|-----------------|-----|-----|-----|------|
| T _{off} | EN pulse width to shutdown | EN high to low | | | 1 | ms |
| T _{min_on} | Minimum on pulse width | | | 65 | | ns |

7.7 Typical Characteristics

Table 1. Table Of Graphs

| Figure 1, L = TOKO #A915_Y-100M, unless otherwise noted | | | FIGURE |
|---|-------------------------|--|-----------|
| η | Efficiency | vs Load current at OUT = 15 V | Figure 1 |
| η | Efficiency | vs Load current at OUT = 10 V | Figure 2 |
| V_{FB} | FB voltage | vs Free-air temperature | Figure 3 |
| V_{FB} | FB voltage | vs Input voltage | Figure 4 |
| I_{LIM} | Switch current limit | vs Free-air temperature | Figure 5 |
| | Line transient response | VIN = 3.3 V to 3.6 V; Load = 50 mA | Figure 10 |
| | Load transient response | VIN = 2.5 V; Load = 10 mA to 50 mA; Cff = 100 pF | Figure 11 |
| | PWM control in CCM | VIN = 3.6 V; Load = 50 mA | Figure 12 |
| | PWM control in DCM | VIN = 3.6 V; Load = 1 mA | Figure 13 |
| | Pulse skip mode | VIN = 4.5 V; OUT = 10 V; No load | Figure 14 |
| | Soft start-up | VIN = 3.6 V; Load = 50 mA | Figure 15 |

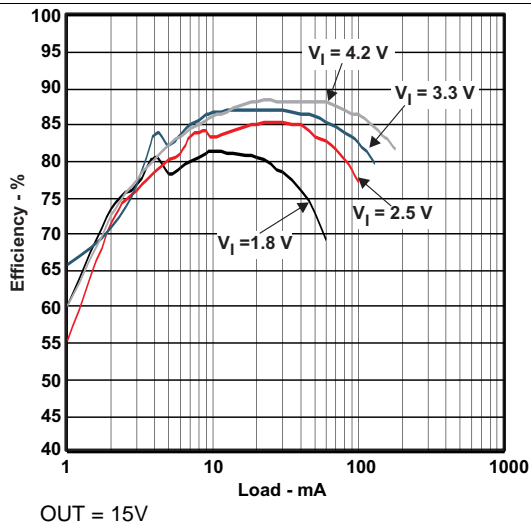


Figure 1. Efficiency vs. Load

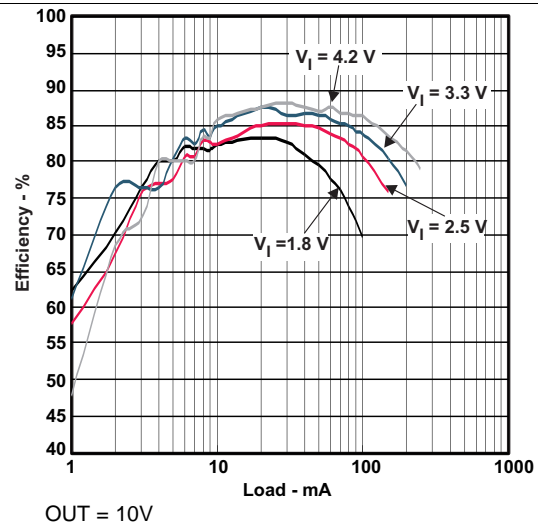


Figure 2. Efficiency vs. Load

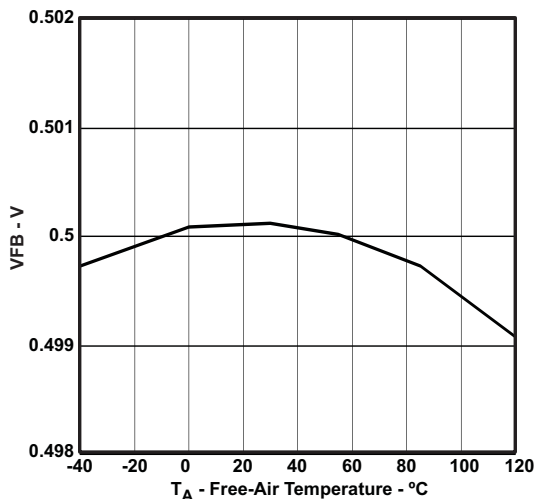


Figure 3. FB Voltage vs. Free-Air Temperature

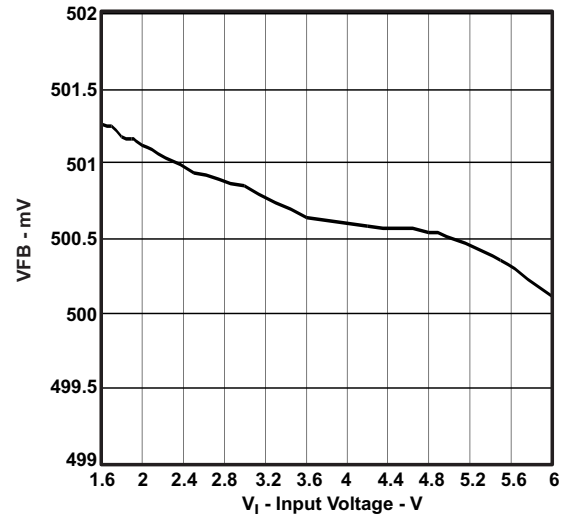


Figure 4. FB Voltage vs. Input Voltage

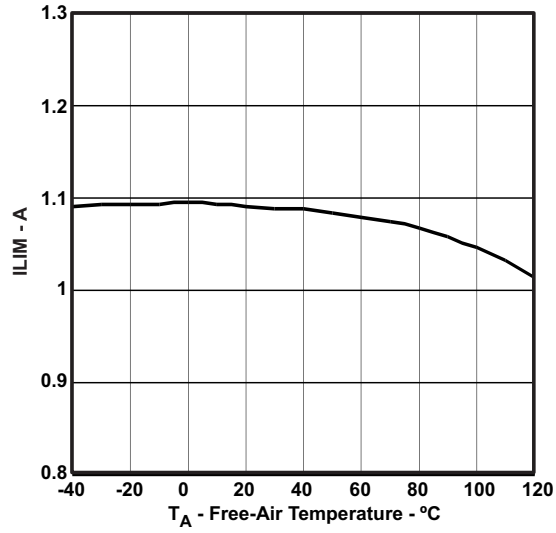


Figure 5. Switch Current Limit vs. Free-Air Temperature

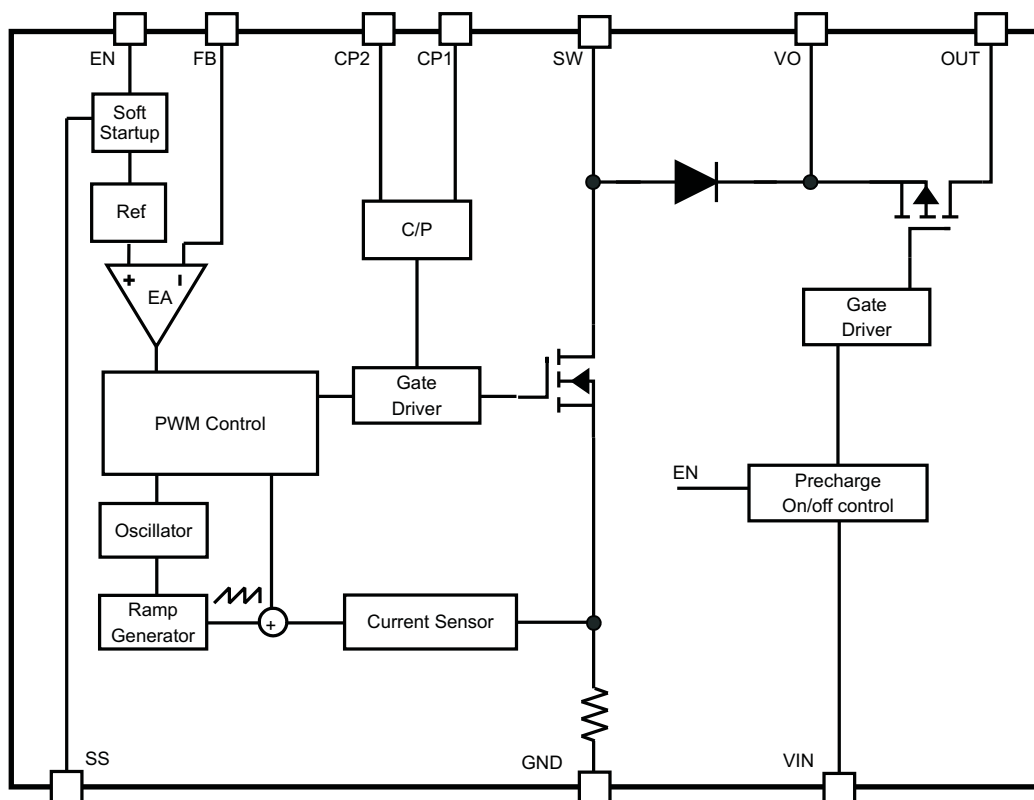
8 Detailed Description

8.1 Overview

The TPS61093-Q1 is a highly integrated boost regulator for up to 17-V output. In addition to the on-chip 1-A PWM switch and power diode, this IC also integrates an output-side isolation switch as shown in the functional block diagram. One common issue with conventional boost regulators is the conduction path from input to output even when the PWM switch is turned off. It creates three problems, which are inrush current during start-up, output leakage current during shutdown, and excessive over load current. In the TPS61093-Q1, the isolation switch turns off under shutdown-mode and over load conditions, thereby opening the current path. However, shorting the VO and OUT pins bypasses the isolation switch and enhances efficiency. Because the isolation switch is on the output side, the IC's VIN pin and power stage input power (up to 10 V) can be separated.

The TPS61093-Q1 adopts current-mode control with constant pulse-width-modulation (PWM) frequency. The switching frequency is fixed at 1.2-MHz typical. PWM operation turns on the PWM switch at the beginning of each switching cycle. The input voltage is applied across the inductor and the inductor current ramps up. In this mode, the output capacitor is discharged by the load current. When the inductor current hits the threshold set by the error amplifier output, the PWM switch is turned off, and the power diode is forward-biased. The inductor transfers its stored energy to replenish the output capacitor. This operation repeats in the next switching cycle. The error amplifier compares the FB-pin voltage with an internal reference, and its output determines the duty cycle of the PWM switching. This closed-loop system requires frequency compensation for stable operation. The device has a built-in compensation circuit that can accommodate a wide range of input and output voltages. To avoid the sub-harmonic oscillation intrinsic to current-mode control, the IC also integrates slope compensation, which adds an artificial slope to the current ramp.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Shutdown And Load Discharge

When the EN pin is pulled low for 1-ms, the IC stops the PWM switch and turns off the isolation switch, providing isolation between input and output. The internal current path consisting of the isolation switch's body diode and several parasitic diodes quickly discharges the output voltage to less than 3.3-V. Afterwards, the voltage is slowly discharged to zero by the leakage current. This protects the IC and the external components from high voltage in shutdown mode.

In shutdown mode, less than 5- μ A of input current is consumed by the IC.

8.3.2 Over Load And Over Voltage Protection

If the over load current passing through the isolation switch is above the over load limit (I_{OL}) for 3- μ s (typ), the TPS61093-Q1 is switched off until the fault is cleared and the EN pin toggles. The function only is triggered 52-ms after the IC is enabled.

To prevent the PWM switch and the output capacitor from exceeding maximum voltage ratings, an over voltage protection circuit turns off the boost switch as soon as the output voltage at the VO pin exceeds the OVP threshold. Simultaneously, the IC opens the isolation switch. The regulator resumes PWM switching after the VO pin voltage falls 0.6-V below the threshold.

8.3.3 Under Voltage Lockout (UVLO)

An under voltage lockout prevents improper operation of the device for input voltages below 1.55-V. When the input voltage is below the under voltage threshold, the entire device, including the PWM and isolation switches, remains off.

8.3.4 Thermal Shutdown

An internal thermal shutdown turns off the isolation and PWM switches when the typical junction temperature of 150°C is exceeded. The thermal shutdown has a hysteresis of 15°C, typical.

8.4 Device Functional Modes

The converter operates in continuous conduction mode (CCM) as soon as the input current increases above half the ripple current in the inductor, for lower load currents it switches into discontinuous conduction mode (DCM). If the load is further reduced, the part starts to skip pulses to maintain the output voltage.

9 Application and Implementation

9.1 Application Information

The following section provides a step-by-step design approach for configuring the TPS61093-Q1 as a voltage regulating boost converter, as shown in [Figure 6](#).

9.2 Typical Applications

9.2.1 15V Output Boost Converter

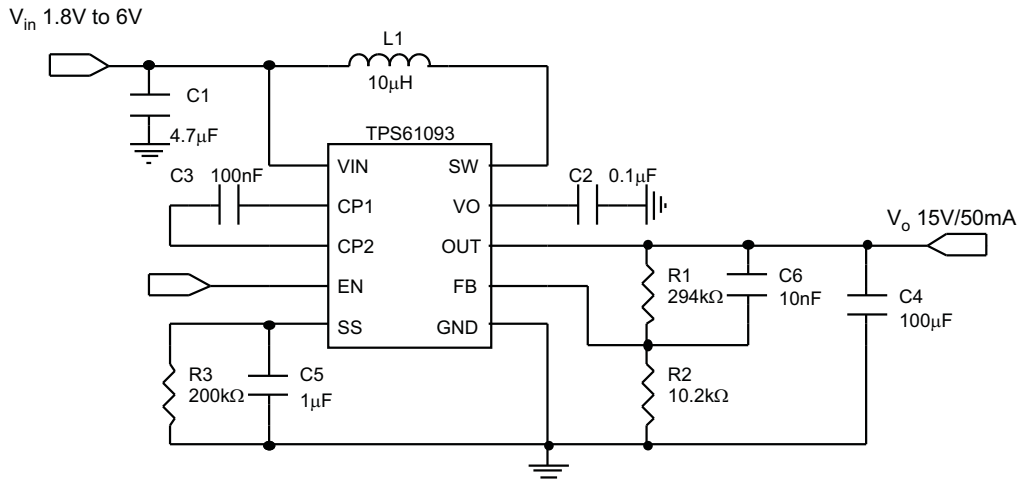


Figure 6. 15V Boost Converter with 100µF Output Capacitor

9.2.1.1 Design Requirements

Table 2. Design Parameters

| PARAMETERS | VALUES |
|---------------------|---------|
| Input voltage | 4.2 V |
| Output voltage | 15 V |
| Operating frequency | 1.2 MHz |

9.2.1.2 Detailed Design Procedure

9.2.1.2.1 Output Program

To program the output voltage, select the values of R1 and R2 (see Figure 7) according to Equation 1.

$$V_{out} = 0.5 V \times \left(\frac{R1}{R2} + 1 \right)$$

$$R1 = R2 \times \left(\frac{V_{out}}{0.5 V} - 1 \right) \tag{1}$$

A recommended value for R2 is approximately 10-kΩ which sets the current in the resistor divider chain to 0.5V/10kΩ = 50-μA. The output voltage tolerance depends on the VFB accuracy and the resistor divider.

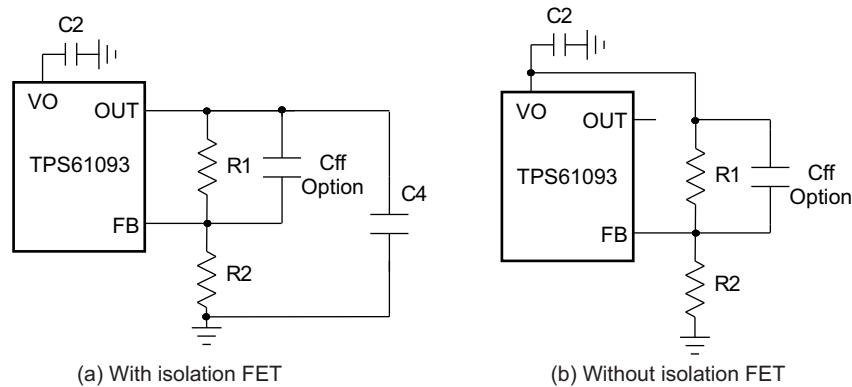


Figure 7. Resistor Divider to Program Output Voltage

9.2.1.2.2 Without Isolation FET

The efficiency of the TPS61093-Q1 can be improved by connecting the load to the VO pin instead of the OUT pin. The power loss in the isolation FET is then negligible, as shown in Figure 8. The tradeoffs when bypassing the isolation FET are:

- Leakage path between input and output causes the output to be a diode drop below the input voltage when the IC is in shutdown
- No overload circuit protection

When the load is connected to the VO pin, the output capacitor on the VO pin should be above 1-μF.

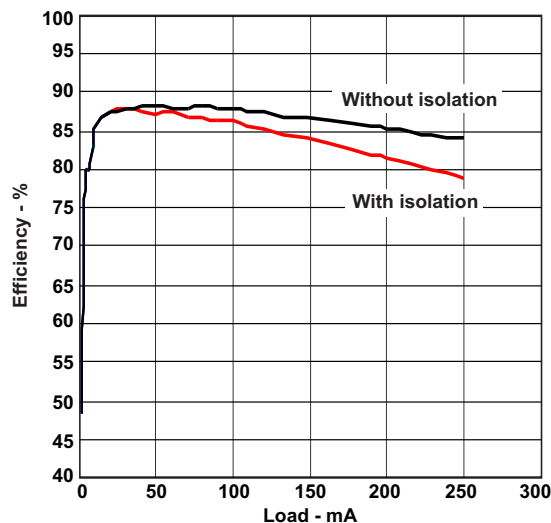


Figure 8. Efficiency vs. Load

9.2.1.2.3 Start Up

The TPS61093-Q1 turns on the isolation FET and PWM switch when the EN pin is pulled high. During the soft start period, the R and C network on the SS pin is charged by an internal bias current of 5- μ A (typ). The RC network sets the reference voltage ramp up slope. Since the output voltage follows the reference voltage via the FB pin, the output voltage rise time follows the SS pin voltage until the SS pin voltage reaches 0.5-V. The soft start time is given by [Equation 2](#).

$$t_{SS} = \frac{0.5 \text{ V} \times C5}{5 \mu\text{A}}$$

where

- C5 is the capacitor connected to the SS pin (2)

When the EN pin is pulled low to switch the IC off, the SS pin voltage is discharged to zero by the resistor R3. The discharge period depends on the RC time constant. Note that if the SS pin voltage is not discharged to zero before the IC is enabled again, the soft start circuit may not slow the output voltage startup and may not reduce the startup inrush current.

9.2.1.2.4 Switch Duty Cycle

The maximum switch duty cycle (D) of the TPS61093-Q1 is 90% (minimum). The duty cycle of a boost converter under continuous conduction mode (CCM) is given by:

$$D = \frac{V_{out} + 0.8 \text{ V} - V_{in}}{V_{out} + 0.8 \text{ V}} \quad (3)$$

The duty cycle must be lower than the specification in the application; otherwise the output voltage cannot be regulated.

The TPS61093-Q1 has a minimum ON pulse width once the PWM switch is turned on. As the output current drops, the device enters discontinuous conduction mode (DCM). If the output current drops extremely low, causing the ON time to be reduced to the minimum ON time, the TPS61093-Q1 enters pulse-skipping mode. In this mode, the device keeps the power switch off for several switching cycles to keep the output voltage in regulation. See [Figure 14](#). The output current when the IC enters skipping mode is calculated with [Equation 4](#).

$$I_{out_skip} = \frac{V_{in}^2 \times T_{min_on}^2 \times f_{SW}}{2 \times (V_{out} + 0.8 \text{ V} - V_{in}) \times L}$$

where

- T_{min_on} = Minimum ON pulse width specification (typically 65-ns);
- L = Selected inductor value;
- f_{SW} = Converter switching frequency (typically 1.2-MHz) (4)

9.2.1.2.5 Inductor Selection

Because the selection of the inductor affects steady state operation, transient behavior, and loop stability, the inductor is the most important component in power regulator design. There are three important inductor specifications, inductor value, saturation current, and dc resistance. Considering inductor value alone is not enough.

The saturation current of the inductor should be higher than the peak switch current as calculated in [Equation 5](#).

$$I_{L_peak} = I_{L_DC} + \frac{\Delta I_L}{2}$$

$$I_{L_DC} = \frac{V_{out} \times I_{out}}{V_{in} \times \eta}$$

$$\Delta I_L = \frac{1}{L \times f_{sw} \times \left(\frac{1}{V_{out} + 0.8 V - V_{IN}} + \frac{1}{V_{IN}} \right)}$$

where

- I_{L_peak} = Peak switch current
- I_{L_DC} = Inductor average current
- ΔI_L = Inductor peak to peak current
- η = Estimated converter efficiency

(5)

Normally, it is advisable to work with an inductor peak-to-peak current of less than 30% of the average inductor current. A smaller ripple from a larger valued inductor reduces the magnetic hysteresis losses in the inductor and EMI. But in the same way, load transient response time is increased. Also, the inductor value should not be outside the 2.2- μ H to 10- μ H range in the recommended operating conditions table. Otherwise, the internal slope compensation and loop compensation components are unable to maintain small signal control loop stability over the entire load range. [Table 3](#) lists the recommended inductor for the TPS61093-Q1.

Table 3. Recommended Inductors for the TPS61093-Q1

| Part Number | L (μ H) | DCR Max (m Ω) | Saturation Current (A) | Size (LxWxH mm) | Vendor |
|---------------|--------------|-----------------------|------------------------|-----------------|-----------|
| #A915_Y-4R7M | 4.7 | 45 | 1.5 | 5.2x5.2x3.0 | Toko |
| #A915_Y-100M | 10 | 90 | 1.09 | 5.2x5.2x3.0 | Toko |
| VLS4012-4R7M | 4.7 | 132 | 1.1 | 4.0x4.0x1.2 | TDK |
| VLS4012-100M | 10 | 240 | 0.82 | 4.0x4.0x1.2 | TDK |
| CDRH3D23/HP | 10 | 198 | 1.02 | 4.0x4.0x2.5 | Sumida |
| LPS5030-103ML | 10 | 127 | 1.4 | 5.0x5.0x3.0 | Coilcraft |

9.2.1.2.6 Input And Output Capacitor Selection

The output capacitor is mainly selected to meet the requirements for output ripple and loop stability. This ripple voltage is related to the capacitor's capacitance and its equivalent series resistance (ESR). Assuming a ceramic capacitor with zero ESR, the minimum capacitance needed for a given ripple can be calculated by:

$$C_{out} = \frac{D \times I_{out}}{F_s \times V_{ripple}}$$

where

- V_{ripple} = peak to peak output ripple

(6)

The ESR impact on the output ripple must be considered if tantalum or electrolytic capacitors are used.

Care must be taken when evaluating a ceramic capacitor's derating under dc bias, aging, and ac signal. For example, larger form factor capacitors (in 1206 size) have their self resonant frequencies in the range of the switching frequency. So the effective capacitance is significantly lower. The dc bias can also significantly reduce capacitance. A ceramic capacitor can lose as much as 50% of its capacitance at its rated voltage. Therefore, always leave margin on the voltage rating to ensure adequate capacitance at the required output voltage.

A 4.7- μF (minimum) input capacitor is recommended. The output requires a capacitor in the range of 1 μF to 10 μF . The output capacitor affects the small signal control loop stability of the boost regulator. If the output capacitor is below the range, the boost regulator can potentially become unstable.

The popular vendors for high value ceramic capacitors are:

- TDK (<http://www.component.tdk.com/components.php>)
- Murata (<http://www.murata.com/cap/index.html>)

9.2.1.2.7 Small Signal Stability

The TPS61093-Q1 integrates slope compensation and the RC compensation network for the internal error amplifier. Most applications will be control loop stable if the recommended inductor and input/output capacitors are used. For those few applications that require components outside the recommended values, the internal error amplifier's gain and phase are presented in [Figure 9](#).

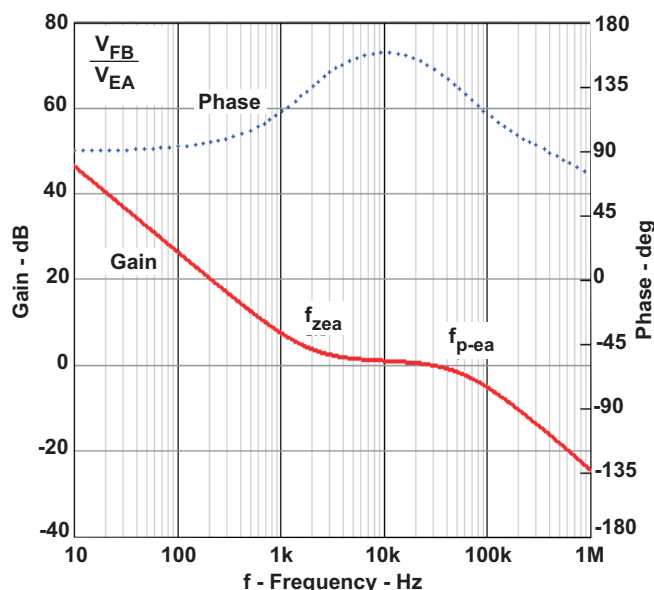


Figure 9. Bode Plot of Error Amplifier Gain and Phase

The RC compensation network generates a pole $f_{p\text{-ea}}$ of 57-kHz and a zero $f_{z\text{-ea}}$ of 1.9-kHz, shown in [Figure 9](#). Use [Equation 7](#) to calculate the output pole, f_p , of the boost converter. If $f_p \ll f_{z\text{-ea}}$. due to a large capacitor beyond 10 μF , for example, a feed forward capacitor on the resistor divider, as shown in [Figure 9](#), is necessary to generate an additional zero $f_{z\text{-f}}$ to improve the loop phase margin and improve the load transient response. The low frequency pole $f_{p\text{-f}}$ and zero $f_{z\text{-f}}$ generated by the feed forward capacitor are given by [Equation 8](#) and [Equation 9](#):

$$f_p = \frac{1}{\pi \times R_o \times C_o} \quad (\text{a}) \quad (7)$$

$$f_{p\text{-f}} = \frac{1}{2\pi \times R2 \times C_{ff}} \quad (\text{b}) \quad (8)$$

$$f_{z\text{-f}} = \frac{1}{2\pi \times R1 \times C_{ff}} \quad (\text{c})$$

where

- C_{ff} = the feed-forward capacitor (9)

For example, in the typical application circuitry (see [Figure 7](#)), the output pole f_p is approximately 1-kHz. When the output capacitor is increased to 100- μF , then the f_p is reduced to 10-Hz. Therefore, a feed-forward capacitor of 10-nF compensates for the low frequency pole.

A feed forward capacitor that sets f_{z-f} near 10-kHz improves the load transient response in most applications, as shown in Figure 11.

9.2.1.3 Application Curves

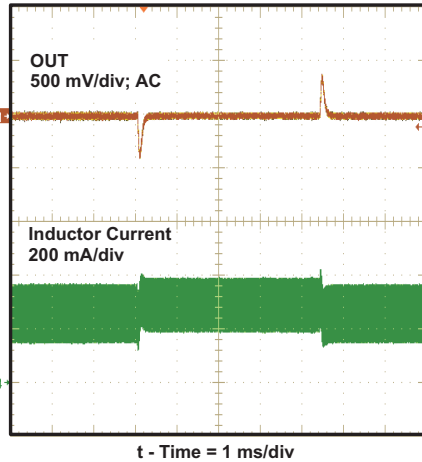


Figure 10. 3.3V to 3.6V Line Transient Response

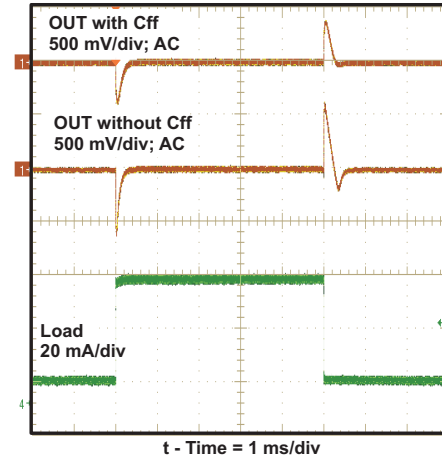


Figure 11. 10mA to 50mA Load Transient Response

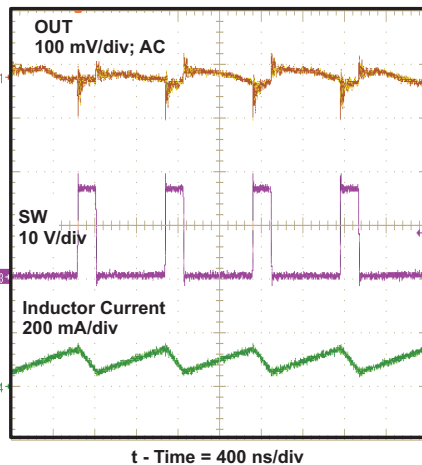


Figure 12. PWM Control in CCM

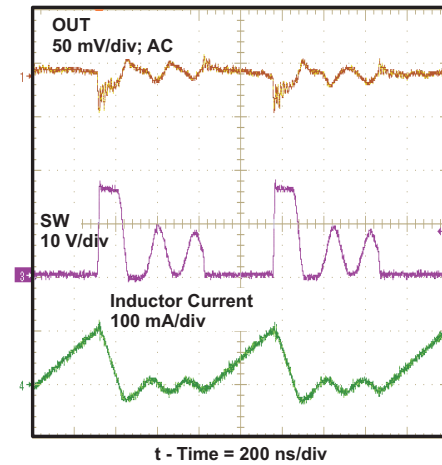


Figure 13. PWM Control in DCM

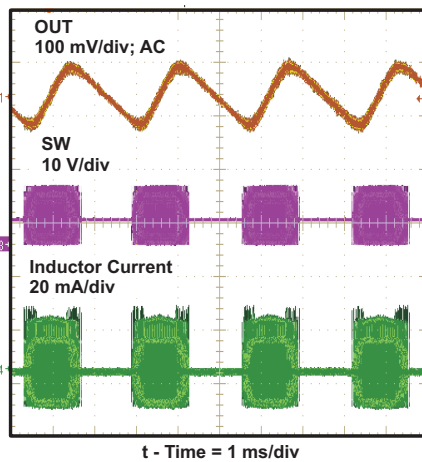


Figure 14. Pulse Skip Mode at Light Load

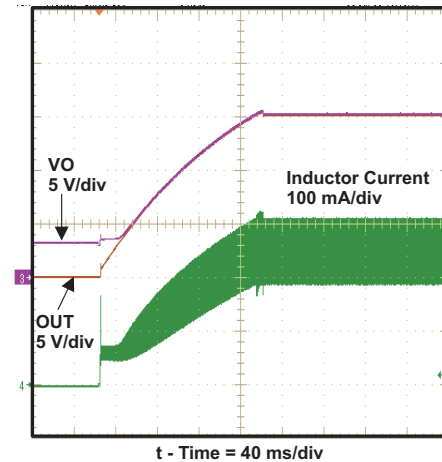
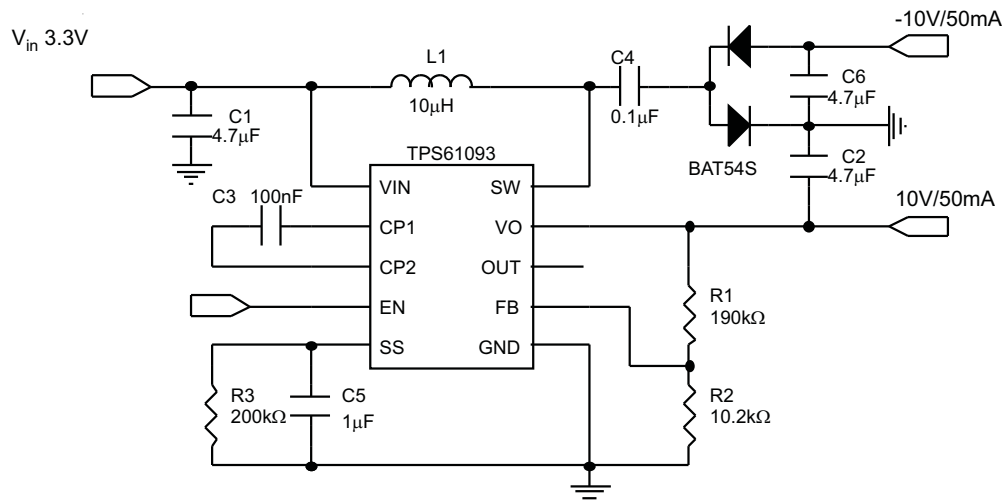


Figure 15. Soft Start-Up

9.2.2 10 V, -10 V Dual Output Boost Converter



9.2.2.1 Design Requirements

Table 4. Design Parameters

| PARAMETERS | VALUES |
|---------------------|------------|
| Input voltage | 3.3 V |
| Output voltage | 10 V/-10 V |
| Operating frequency | 1.2 MHz |

9.2.2.2 Detailed Design Procedure

Refer to [Detailed Design Procedure](#) for the 15V Output Boost Converter.

9.2.2.3 Application Curves

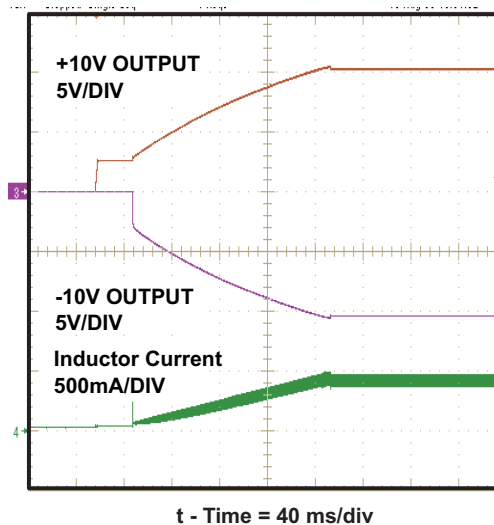


Figure 16. Soft Startup Waveform, 10 V, -10 V Dual Output Boost Converter

10 Power Supply Recommendations

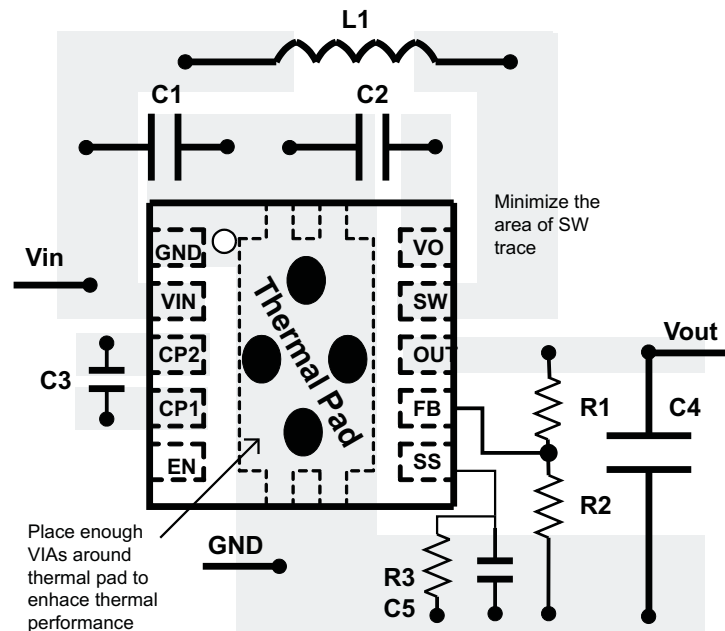
The device is designed to operate from an input voltage supply range between 1.6 V to 6 V. The input power supply's output current needs to be rated according to the supply voltage, output voltage and output current of the TPS61093-Q1.

11 Layout

11.1 Layout Guidelines

As for all switching power supplies, especially those running at high switching frequency and high currents, layout is an important design step. If layout is not carefully done, the regulator could suffer from instability as well as noise problems. To maximize efficiency, switch rise and fall times are very fast. To prevent radiation of high frequency noise (e.g., EMI), proper layout of the high frequency switching path is essential. Minimize the length and area of all traces connected to the SW pin and always use a ground plane under the switching regulator to minimize interplane coupling. The high current path including the switch and output capacitor contains nanosecond rise and fall times and should be kept as short as possible. The input capacitor needs not only to be close to the VIN pin, but also to the GND pin in order to reduce input supply ripple.

11.2 Layout Example



11.3 Thermal Considerations

The maximum IC junction temperature should be restricted to 125°C under normal operating conditions. This restriction limits the power dissipation of the TPS61093-Q1. Calculate the maximum allowable dissipation, $P_{D(max)}$, and keep the actual dissipation less than or equal to $P_{D(max)}$. The maximum-power-dissipation limit is determined using the following equation:

$$P_{D(max)} = \frac{125^{\circ}\text{C} - T_A}{R_{\theta JA}}$$

where

- T_A is the maximum ambient temperature for the application
- $R_{\theta JA}$ is the thermal resistance junction-toambient given in Power Dissipation Table (10)

The TPS61093-Q1 comes in a thermally enhanced SON package. This package includes a thermal pad that improves the thermal capabilities of the package. The $R_{\theta JA}$ of the SON package greatly depends on the PCB layout and thermal pad connection. The thermal pad must be soldered to the analog ground on the PCB. Using thermal vias underneath the thermal pad.

12 Device and Documentation Support

12.1 Trademarks

All trademarks are the property of their respective owners.

12.2 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.3 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|--------------------|------|----------------|----------------------------|-------------------------|----------------------|--------------|-------------------------|---------|
| TPS61093QDSKRQ1 | ACTIVE | SON | DSK | 10 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 093Q | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF TPS61093-Q1 :

- Catalog: [TPS61093](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-----------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| TPS61093QDSKRQ1 | SON | DSK | 10 | 3000 | 180.0 | 8.4 | 2.8 | 2.8 | 1.0 | 4.0 | 8.0 | Q2 |

TAPE AND REEL BOX DIMENSIONS

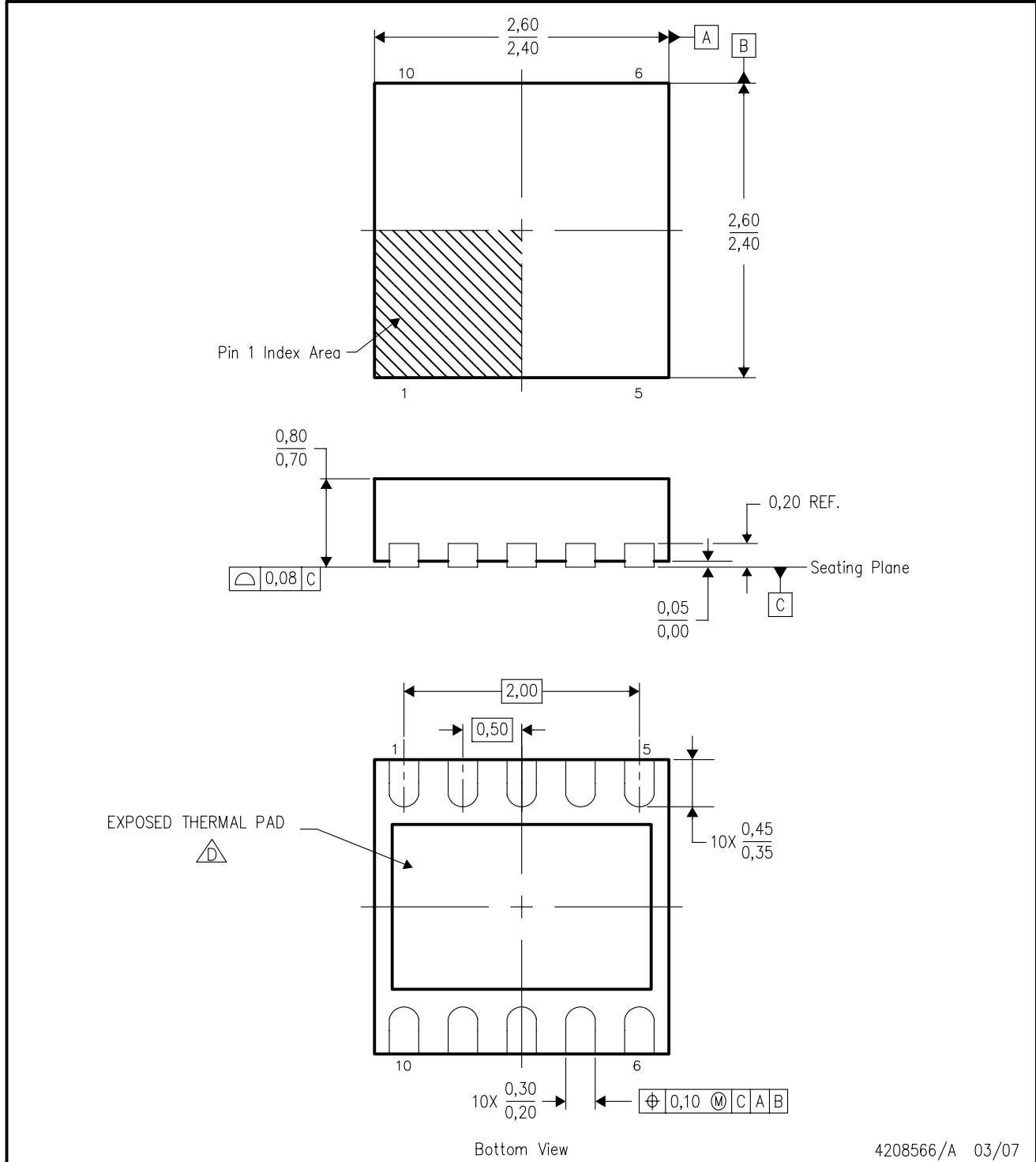


*All dimensions are nominal


| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|-----------------|--------------|-----------------|------|------|-------------|------------|-------------|
| TPS61093QDSKRQ1 | SON | DSK | 10 | 3000 | 210.0 | 185.0 | 35.0 |

DSK (S-PDSO-N10)

PLASTIC QUAD FLATPACK



4208566/A 03/07

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Small Outline No-Lead (SON) package configuration.
 -  D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.

THERMAL PAD MECHANICAL DATA

DSK (R-PWSON-N10)

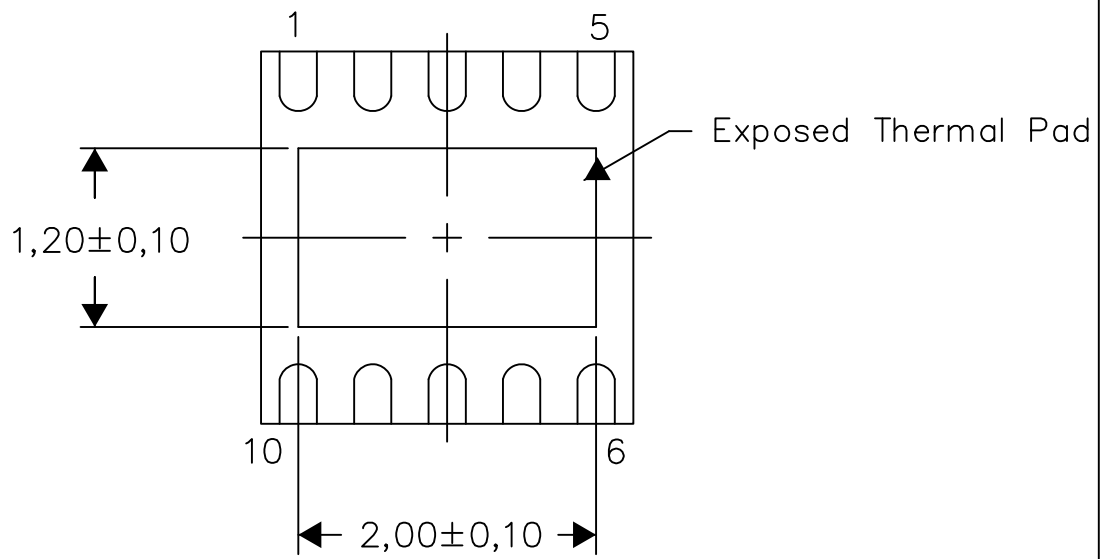
PLASTIC SMALL OUTLINE NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

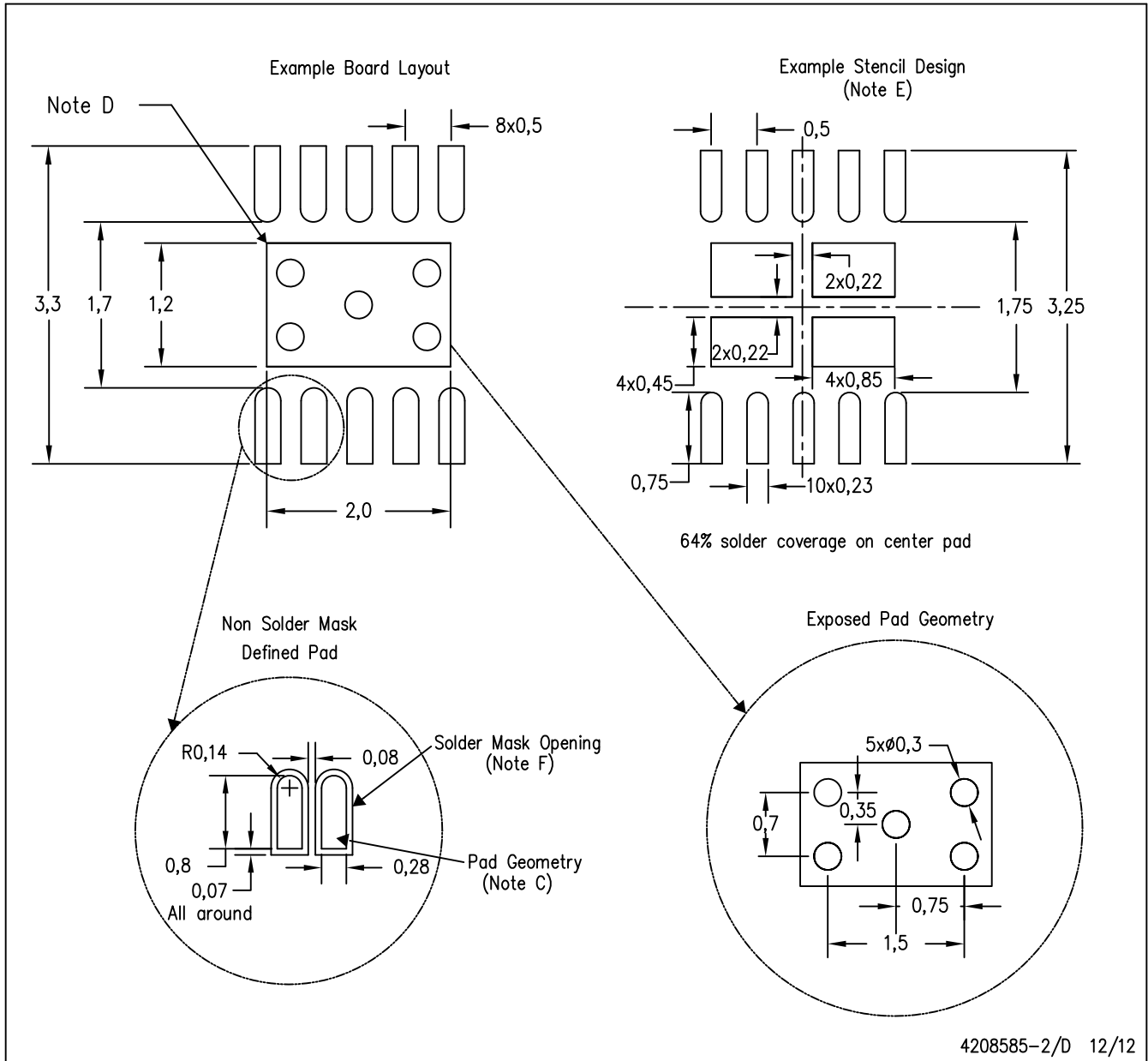
Exposed Thermal Pad Dimensions

4208579-2/E 12/12

NOTE: All linear dimensions are in millimeters

DSK (R-PWSON-N10)

PLASTIC SMALL OUTLINE NO-LEAD



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-SM-782 is recommended for alternate designs.
 - This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <<http://www.ti.com>>.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
 - Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

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