TP5335

P-Channel Enhancement-Mode Vertical DMOS FET

Features

- High Input Impedance and High Gain
- Low Power Drive Requirement
- Ease of Paralleling
- Low C_{ISS} and Fast Switching Speeds
- Excellent Thermal Stability
- Integral Source-Drain Diode
- Free from Secondary Breakdown

Applications

- Logic-Level Interfaces (Ideal for TTL and CMOS)
- Solid-State Relays
- Analog Switches
- Power Management
- Telecommunication Switches

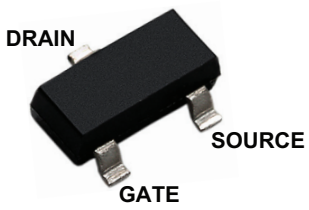
General Description

The TP5335 is a low-threshold, Enhancement-mode (normally-off) transistor that utilizes an advanced vertical DMOS structure and a well-proven silicon gate manufacturing process. This combination produces a device with the power handling capabilities of bipolar transistors and the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, this device is free from thermal runaway and thermally induced secondary breakdown.

Microchip's vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Package Type

3-lead SOT-23
(Top view)



See Table 2-1 for pin information.

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1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings†

Drain-to-Source Voltage ..... BV_{DSS}
Drain-to-Gate Voltage ..... BV_{DGS}
Gate-to-Source Voltage ..... ±20V
Junction Temperature, T_J ..... –55°C to +150°C
Storage Temperature, T_S ..... –55°C to +150°C

† Notice: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS – COMMERCIAL

Electrical Specifications: $T_A = T_J = 25°C$ unless otherwise specified. All DC parameters are 100% tested at 25°C unless otherwise stated. (Pulse test: 300 µs pulse, 2% duty cycle.)

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
Drain-to-Source Breakdown Voltage	BV_{DSS}	–350	—	—	V	V_{GS} = 0V, I_D = –100 µA
Gate Threshold Voltage	$V_{GS(th)}$	–1	—	–2.4	V	V_{DS} = V_{GS}, I_D = –1 mA
Change in $V_{GS(th)}$ with Temperature	$\Delta V_{GS(th)}$	—	—	4.5	mV/°C	V_{DS} = V_{GS}, I_D = –1 mA (**Note 1**)
Gate Body Leakage	I_{GSS}	—	—	–100	nA	V_{GS} = ±20V, V_{DS} = 0V
Zero-Gate Voltage Drain Current	I_{DSS}	—	—	–10	µA	V_{DS} = Maximum rating, V_{GS} = 0V
		—	—	–1	mA	V_{DS} = Maximum rating, V_{GS} = 0V, T_A = 125°C (**Note 1**)
On-State Drain Current	$I_{D(ON)}$	–200	—	—	mA	V_{GS} = –4.5V, V_{DS} = –25V
		–400	—	—	mA	V_{GS} = –10V, V_{DS} = –25V
Static Drain-to-Source On-State Resistance	$R_{DS(ON)}$	—	—	75	Ω	V_{GS} = –4.5V, I_D = –150 mA
		—	—	30	Ω	V_{GS} = –10V, I_D = –200 mA
Change in $R_{DS(ON)}$ with Temperature	$\Delta_{RDS(ON)}$	—	—	1.7	%/°C	V_{GS} = –10V, I_D = –200 mA (**Note 1**)

Note 1: Specification is obtained by characterization and is not 100% tested.

DC ELECTRICAL CHARACTERISTICS – AUTOMOTIVE

Electrical Specifications: $T_A = T_J$ = (–55°C, 25°C, or 150°C) unless otherwise specified. All DC parameters are 100% tested at all three temperatures unless otherwise stated. (Pulse test: 300 µs pulse, 2% duty cycle.)

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
Drain-to-Source Breakdown Voltage	BV_{DSS}	**–350**	—	—	V	V_{GS} = 0V, I_D = –100 µA
Gate Threshold Voltage	$V_{GS(th)}$	–1	—	**–2.4**	V	V_{DS} = V_{GS}, I_D = –1 mA
Change in $V_{GS(th)}$ with Temperature	$\Delta V_{GS(th)}$	—	3.3	—	mV/°C	V_{DS} = V_{GS}, I_D = –1 mA (**Note 1**)
Gate Body Leakage	I_{GSS}	—	—	–100	nA	V_{GS} = ±20V, V_{DS} = 0V
		—	—	**–220**	nA	V_{GS} = ±20V, V_{DS} = 0V, T_A = 150°C

Note 1: Specification is obtained by characterization and is not 100% tested.

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DC ELECTRICAL CHARACTERISTICS – AUTOMOTIVE (CONTINUED)

Electrical Specifications: $T_A = T_J$ = (–55°C, 25°C, or 150°C) unless otherwise specified. All DC parameters are 100% tested at all three temperatures unless otherwise stated. (Pulse test: 300 µs pulse, 2% duty cycle.)

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
Zero-Gate Voltage Drain Current	I_{DSS}	—	—	**–10**	µA	V_{DS} = Maximum rating, V_{GS} = 0V
		—	—	**–1**	mA	V_{DS} = Maximum rating, V_{GS} = 0V, T_A = 150°C
On-State Drain Current	$I_{D(ON)}$	**–200**	—	—	mA	V_{GS} = –4.5V, V_{DS} = –25V
		–400	—	—	mA	V_{GS} = –10V, V_{DS} = –25V
		–375	—	—	mA	V_{GS} = –10V, V_{DS} = –25V, T_A = 150°C
Static Drain-to-Source On-State Resistance	$R_{DS(ON)}$	—	—	**75**	Ω	V_{GS} = –4.5V, I_D = –150 mA
		—	—	30	Ω	V_{GS} = –10V, I_D = –200 mA
		—	—	**70**	Ω	V_{GS} = –10V, I_D = –200 mA, T_A = 150°C
Change in $R_{DS(ON)}$ with Temperature	$\Delta_{RDS(ON)}$	—	1	—	%/°C	V_{GS} = –10V, I_D = –200 mA (**Note 1**)

Note 1: Specification is obtained by characterization and is not 100% tested.

AC ELECTRICAL CHARACTERISTICS – COMMERCIAL

Electrical Specifications: $T_A = T_J$ = 25°C unless otherwise specified. Specification is obtained by characterization and is not 100% tested.

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
Forward Transconductance	G_{FS}	125	—	—	mmho	V_{DS} = –25V, I_D = –200 mA
Input Capacitance	C_{ISS}	—	—	110	pF	V_{GS} = 0V, V_{DS} = –25V, f = 1 MHz
Common Source Output Capacitance	C_{OSS}	—	—	60	pF	
Reverse Transfer Capacitance	C_{RSS}	—	—	22	pF	
Turn-On Delay Time	$t_{d(ON)}$	—	—	20	ns	V_{DD} = –25V, I_D = –150 mA, R_{GEN} = 25Ω
Rise Time	t_r	—	—	15	ns	
Turn-Off Delay Time	$t_{d(OFF)}$	—	—	25	ns	
Fall Time	t_f	—	—	25	ns	
DIODE PARAMETER						
Diode Forward Voltage Drop	V_{SD}	—	—	–1.8	V	V_{GS} = 0V, I_{SD} = –200 mA (**Note 1**)
Reverse Recovery Time	t_{rr}	—	800	—	ns	V_{GS} = 0V, I_{SD} = –200 mA

Note 1: All DC parameters are 100% tested at 25°C unless otherwise stated.(Pulse test: 300 µs pulse, 2% duty cycle.)

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AC ELECTRICAL CHARACTERISTICS – AUTOMOTIVE

Electrical Specifications: $T_A = T_J = 25°C$ unless otherwise specified. Specification is obtained by characterization and is not 100% tested.

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
Forward Transconductance	G_{FS}	—	285	—	mmho	V_{DS} = –25V, I_D = –200 mA
Input Capacitance	C_{ISS}	—	80	—	pF	V_{GS} = 0V, V_{DS} = –25V, f = 1 MHz
Common Source Output Capacitance	C_{OSS}	—	12	—	pF	
Reverse Transfer Capacitance	C_{RSS}	—	2	—	pF	
Turn-On Delay Time	$t_{d(ON)}$	—	7.6	—	ns	V_{DD} = –25V, I_D = –150 mA, R_{GEN} = 25Ω
Rise Time	t_r	—	3	—	ns	
Turn-Off Delay Time	$t_{d(OFF)}$	—	19	—	ns	
Fall Time	t_f	—	10	—	ns	
DIODE PARAMETER						
Diode Forward Voltage Drop	V_{SD}	—	—	**–1.8**	V	V_{GS} = 0V, I_{SD} = –200 mA (**Note 1**)
Reverse Recovery Time	t_{rr}	—	450	—	ns	V_{GS} = 0V, I_{SD} = –200 mA

Note 1: 100% Production Tested at $T_A = T_J$ = (–55°C, 25°C, and 150°C).

TEMPERATURE SPECIFICATIONS

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
TEMPERATURE RANGE						
Operating Junction Temperature	T_J	–55	—	+150	°C	
Storage Temperature	T_S	–55	—	+150	°C	
PACKAGE THERMAL RESISTANCE						
3-lead SOT-23	θ_{JA}	—	203	—	°C/W	

THERMAL CHARACTERISTICS

Package	I_D (Note 1) (Continuous) (mA)	I_D (Pulsed) (mA)	Power Dissipation at T_A = 25°C (W)	I_{DR} (Note 1) (mA)	I_{DRM} (mA)
3-lead SOT-23	–85	–400	0.36	–85	–400

Note 1: I_D (continuous) is limited by maximum T_J.

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2.0 PIN DESCRIPTION

Table 2-1 shows the description of pins in TP5335 SOT-23. Refer to **Package Type** for the location of pins.

TABLE 2-1: PIN FUNCTION TABLE

Pin Number	Pin Name	Description
1	Gate	Gate
2	Source	Source
3	Drain	Drain

3.0 FUNCTIONAL DESCRIPTION

Figure 3-1 illustrates the switching waveforms and test circuit for TP5335.

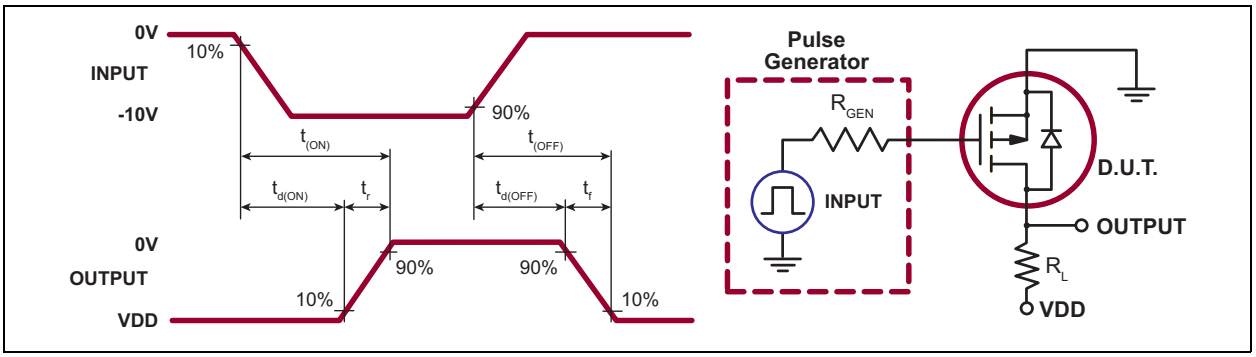

FIGURE 3-1: *Switching Waveforms and Test Circuit.*

TABLE 3-1: PRODUCT SUMMARY

BV_{DSS}/BV_{DGS} (V)	$R_{DS(ON)}$ (Maximum) (Ω)	$V_{GS(th)}$ (Maximum) (V)
–350	30	–2.4

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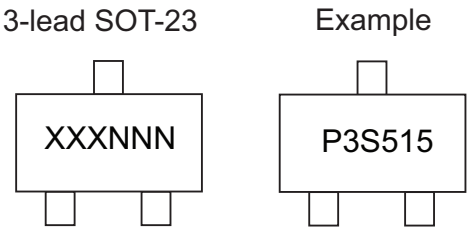
4.0 PACKAGING INFORMATION

4.1 Package Marking Information

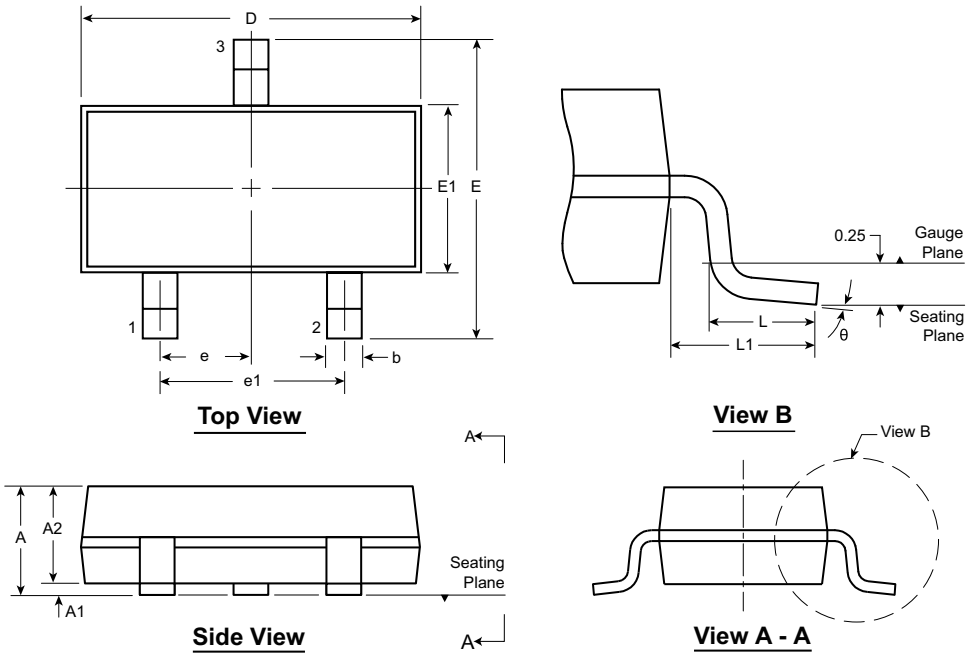


Legend:	XX...X	Product Code or Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for product code or customer-specific information. Package may or not include the corporate logo.

3-Lead TO-236AB (SOT-23) Package Outline (K1/T)

2.90x1.30mm body, 1.12mm height (max), 1.90mm pitch



Note: For the most current package drawings, see the Microchip Packaging Specification at www.microchip.com/packaging.

Symbol		A	A1	A2	b	D	E	E1	e	e1	L	L1	θ
Dimension (mm)	MIN	0.89	0.01	0.88	0.30	2.80	2.10	1.20	0.95 BSC	1.90 BSC	0.20†	0.54 REF	0°
	NOM	-	-	0.95	-	2.90	-	1.30			0.50		-
	MAX	1.12	0.10	1.02	0.50	3.04	2.64	1.40			0.60		8°

JEDEC Registration TO-236, Variation AB, Issue H, Jan. 1999.
† This dimension differs from the JEDEC drawing.
Drawings not to scale.

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APPENDIX A: REVISION HISTORY

Revision A (December 2018)

- Converted Supertex Doc# DSFP-TP5335 to Microchip DS20005704A
- Made minor text changes throughout the document

Revision B (February 2020)

- Revised the order of pins in the Pin Function Table
- Revised the Electrical Specifications and included notes in the DC Electrical Characteristics and AC Electrical Characteristics tables
- Made minor text changes throughout the document

Revision C (June 2020)

- Added automotive specifications to the Electrical Characteristics section
- Added automotive specifications to the Product Identification System section
- Made minor text changes throughout the document

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

PART NO.	XX	-	X	-	X	-	X
Device	Package Options		Environmental		Media Type		Option

Device:	TP5335	=	P-Channel Enhancement-Mode Vertical DMOS FET
Package:	K1	=	3-lead SOT-23
Environmental:	G	=	Lead (Pb)-free/RoHS-compliant Package
Media Type:	(blank)	=	3000/Reel for a K1 Package
Option:	VAO	=	Automotive Grade

Example:

a) TP5335K1-G:	P-Channel Enhancement-Mode Vertical DMOS FET, 3-lead SOT-23, 3000/Reel
b) TP5335K1-G-VAO:	P-Channel Enhancement-Mode Vertical DMOS FET, Automotive Grade, 3-lead SOT-23, 3000/Reel

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