MICROPOWER SUPPLY VOLTAGE SUPERVISORS

Check for Samples: TLC7701-EP, TLC7705-EP, TLC7733-EP

FEATURES

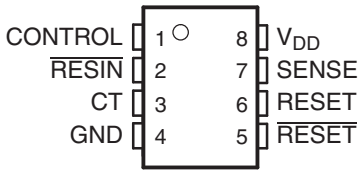
- **Power-On Reset Generator**
- **Automatic Reset Generation After Voltage Drop**
- **Precision Voltage Sensor**
- **Temperature-Compensated Voltage Reference**
- **Programmable Delay Time by External Capacitor**
- **Supply Voltage Range . . . 2 V to 6 V**
- **Defined RESET Output from $V_{DD} \geq 1$ V**
- **Power-Down Control Support for Static RAM With Battery Backup**
- **Maximum Supply Current of 16 mA**
- **Power Saving Totem-Pole Outputs**

SUPPORTS DEFENSE, AEROSPACE, AND MEDICAL APPLICATIONS

- **Controlled Baseline**
- **One Assembly/Test Site**
- **One Fabrication Site**
- **Available in Extended (–40°C/125°C and –55°C/125°C), Temperature Ranges**(1)
- **Extended Product Life Cycle**
- **Extended Product-Change Notification**
- **Product Traceability**

(1) Additional temperature ranges available - contact factory

D OR PW PACKAGE
(TOP VIEW)



DESCRIPTION

The TLC77xx family of micropower supply voltage supervisors provide reset control, primarily in microcomputer and microprocessor systems.

During power-on, RESET is asserted when V_{DD} reaches 1 V. After minimum V_{DD} (≥ 2 V) is established, the circuit monitors SENSE voltage and keeps the reset outputs active as long as SENSE voltage ($V_{I(SENSE)}$) remains below the threshold voltage. An internal timer delays return of the output to the inactive state to ensure proper system reset. The delay time (t_d) is determined by an external capacitor:

$$t_d = 2.1 \times 10^4 \times C_T \quad (1)$$

Where

C_T is in farads

t_d is in seconds

Except for the TLC7701, which can be customized with two external resistors, each supervisor has a fixed sense threshold voltage set by an internal voltage divider. When SENSE voltage drops below the threshold voltage, the outputs become active and stay in that state until SENSE voltage returns above threshold voltage and the delay time (t_d) has expired.

In addition to the power-on reset and undervoltage-supervisor function, the TLC77xx adds power-down control support for static RAM. When CONTROL is tied to GND, RESET will act as active high. The voltage monitor contains additional logic intended for control of static memories with battery backup during power failure. By driving the chip select ($\overline{CS}$) of the memory circuit with the RESET output of the TLC77xx and with the CONTROL driven by the memory bank select signal ($\overline{CSH1}$) of the microprocessor (see Figure 11), the memory circuit is automatically disabled during a power loss. (In this application the TLC77xx power has to be supplied by the battery.)

ORDERING INFORMATION

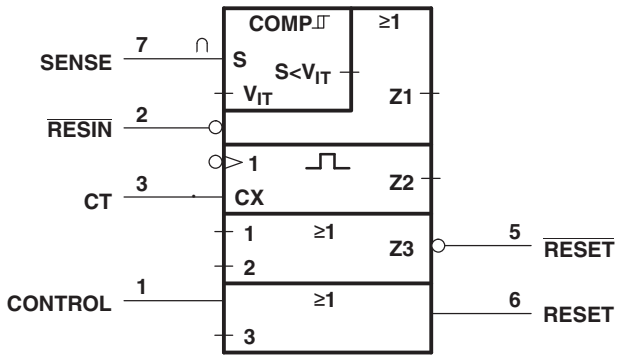
T_A	PACKAGE(1)		ORDERABLE PART NUMBER	TOP-SIDE MARKING	VID NUMBER
-40°C to 125°C	TSSOP - PW	Tape and reel	TLC7701QPWREP	7701QE	V62/04604 - 01XE
			TLC7705QPWREP	7705QE	V62/04604 - 02XE
			TLC7733QPWREP	7733QE	V62/04604 - 03XE
-55°C to 125°C	TSSOP - PW	Tape and reel	TLC7701MPWREP	7701ME	V62/04604 - 04XE
			TLC7733MPWREP	7733ME	V62/04604 - 06XE
	SOIC - D	Tape and reel	TLC7701MDREP	7701ME	V62/04604 - 04YE

(1) The PW package is only available left-end taped and reeled (indicated by the R suffix on the device type; e.g., TLC7701QPWREP).

Table 1. FUNCTION TABLE

CONTROL	RESIN	$V_{I(SENSE)} > V_{IT+}$	RESET	$\overline{RESET}$
L	L	False	H	L
L	L	True	H	L
L	H	False	H	L
L	H	True	L(1)	H(1)
H	L	False	H	L
H	L	True	H	L
H	H	False	H	L
H	H	True	H	H(1)

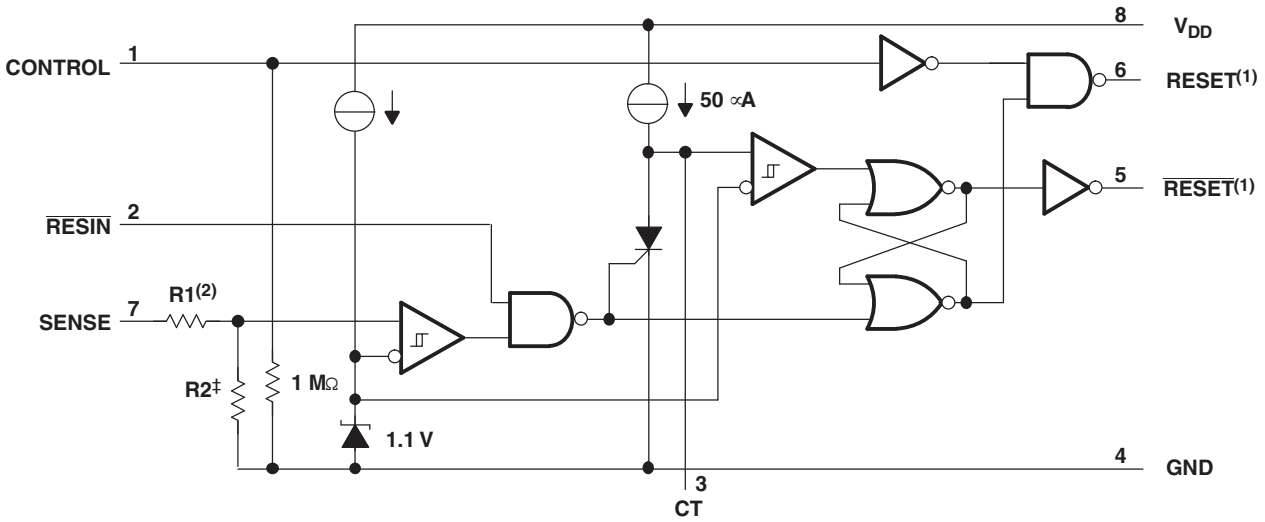
(1) RESET and $\overline{RESET}$ states shown are valid for $t > t_d$.



(1) This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Figure 1. Logic Symbol

FUNCTIONAL BLOCK DIAGRAM

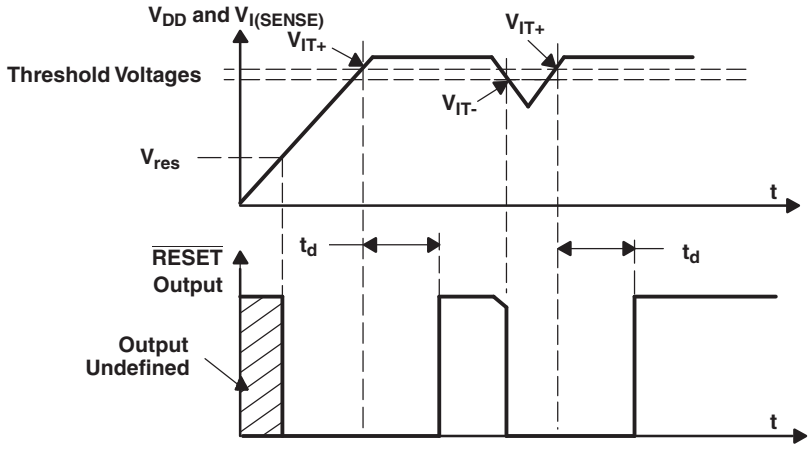


(1) Outputs are totem-pole configuration. External pullup or pulldown resistors are not required.

(2) Nominal values:

	R1 (Typ)	R2 (Typ)
TLC7701	0	∞
TLC7705	910 kΩ	290 kΩ
TLC7733	750 kΩ	450 kΩ

TIMING DIAGRAM



ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)

			VALUE	UNIT
V_{DD}	Supply voltage(2)		7	V
	Input voltage range, CONTROL, RESIN, SENSE (2)		-0.3 to 7	V
I_{OL}	Maximum low output current		10	mA
I_{OH}	Maximum high output current		10	mA
I_{IK}	Input clamp current, (V_I < 0 or V_I > V_{DD})		±10	mA
I_{OK}	Output clamp current, (V_O < 0 or V_O > V_{DD})		±10	mA
T_A	Operating free-air temperature range	TL77xxQ	-40 to 125	°C
		TL77xxM	-55 to 125	
T_{stg}	Storage temperature range		-65 to 150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to GND.

THERMAL INFORMATION

THERMAL METRIC(1)		TLC77xx-EP D 8 PINS	TLC77xx-EP PW 8 PINS	UNITS
θ_{JA}	Junction-to-ambient thermal resistance	97.1	168	°C/W
θ_{JC}	Junction-to-case thermal resistance	39.4	38.9	
θ_{JB}	Junction-to-board thermal resistance	-	96.6	
ψ_{JT}	Junction-to-top characterization parameter	-	1.5	
ψ_{JB}	Junction-to-board characterization parameter	-	94.7	

(1) For more information about traditional and new thermal metrics, see the IC Package Thermal Metrics application report, SPRA953.

RECOMMENDED OPERATING CONDITIONS(1)

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{DD}	Supply voltage		2		6	V
V_I	Input voltage		0		V_{DD}	V
V_{IH}	High-level input voltage at $\overline{\text{RESIN}}$ and CONTROL(2)		0.7×V_{DD}			V
V_{IL}	Low-level input voltage at $\overline{\text{RESIN}}$ and CONTROL				0.2×V_{DD}	V
I_{OH}	High-level output current, V_{DD} ≥ 2.7 V				-2	mA
I_{OL}	Low-level output current, V_{DD} ≥ 2.7 V				2	mA
Δt/ΔV	Input transition rise and fall rate at $\overline{\text{RESIN}}$ and CONTROL				100	ns/V
T_A	Operating free-air temperature range	Q temperature range	-40		125	°C
		M temperature range	-55		125	

(1) Long-term high-temperature storage and/or extended use at maximum recommended operating conditions may result in a reduction of overall device life. See http://www.ti.com/ep_quality for additional information on enhanced plastic packaging.
(2) To ensure a low supply current, V_{IL} should be kept <0.3 V and V_{IH} > -0.3 V.

ELECTRICAL CHARACTERISTICS

over recommended operating conditions(1) (unless otherwise noted)

PARAMETER			TEST CONDITIONS	T_A = -40°C to 125°C			T_A = -55°C to 125°C			UNIT
				MIN	TYP(2)	MAX	MIN	TYP(2)	MAX	
V_{OH}	High-level output voltage	I_{OH} = - 20 µA	V_{DD} = 2 V	1.8			1.8			V
			V_{DD} = 2.7 V	2.5			2.5			
			V_{DD} = 4.5 V	4.3			4.3			
		I_{OH} = - 20 mA	V_{DD} = 4.5 V	3.7			3.7			
V_{OL}	Low-level output voltage	I_{OH} = - 20 µA	V_{DD} = 2 V			0.2			0.2	V
			V_{DD} = 2.7 V			0.2			0.2	
			V_{DD} = 4.5 V			0.2			0.2	
		I_{OH} = - 20 mA	V_{DD} = 4.5 V			0.5			0.5	
V_{IT-}	Negative-going input threshold voltage, SENSE(3)	TLC7701	V_{DD} = 2 V to 6 V	1.04	1.1	1.16				V
		TLC7705		4.43	4.5	4.63				
		TLC7733		2.855	2.93	3.03	2.8	2.93	3.03	
V_{hys}	Hysteresis voltage, SENSE	TLC7701	V_{DD} = 2 V to 6 V		30					mV
		TLC7705			70					
		TLC7733			70			70		
V_{res}	Power-up reset voltage(4)		I_{OL} = 20 µA			1			1	V
I_I	Input current	$\overline{RESIN}$	V_I = 0 V to V_{DD}			2			2	µA
		CONTROL	V_I = V_{DD}		7	15		7	15	
		SENSE	V_I = 5 V		5	10		5	10	
		SENSE, TLC7701 only	V_I = 5 V			2				
I_{DD}	Supply current		$\overline{RESIN}$ = V_{DD}, SENSE = V_{DD} ≥ V_{ITmax} + 0.2 V CONTROL = 0 V, Outputs open		9	16		9	18	µA
$I_{DD(d)}$	Supply current during t_d		V_{DD} = 5 V, V_{CT} = 0 , $\overline{RESIN}$ = V_{DD}, SENSE = V_{DD} CONTROL = 0 V, Outputs open		120	150		120	150	µA
C_I	Input capacitance, SENSE		V_I = 0 V to V_{DD}		50			50		pF

(1) All characteristics are measured with C_T = 0.1 µF.
(2) Typical values apply at T_A = 25°C.
(3) To ensure best stability of the threshold voltage, a bypass capacitor (ceramic, 0.1 µF) should be connected near the supply terminals.
(4) The lowest supply voltage at which $\overline{RESET}$ becomes active. The symbol V_{res} is not currently listed within EIA or JEDEC standards for semiconductor symbology. Rise time of VDD ≥ 15 ms/V.

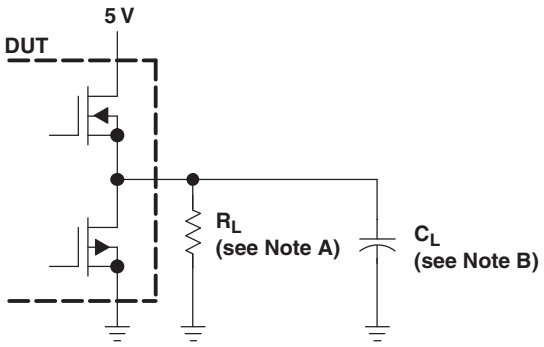
SWITCHING CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER		MEASURED		TEST CONDITIONS	T_A = -40°C to 125°C			T_A = -55°C to 125°C			UNIT
		FROM (INPUT)	TO (OUTPUT)		MIN	TYP	MAX	MIN	TYP	MAX	
t_d	Delay time			$\overline{RESIN}$ = 0.7 × V_{DD}, CONTROL = 0.2 × $V_{DD,CT}$ = 100 nF, T_A = Full range, See timing diagram	1.1	2.1	4.2		2.1		ms
t_{PLH}	Propagation delay time, low-to-high level output	SENSE	$\overline{RESET}$	V_{IH} = V_{IT+max} + 0.2 V, V_{IL} = V_{IT-min} - 0.2 V, $\overline{RESIN}$ = 0.7 × $V_{DD,CONTROL}$ = 0.2 × V_{DD}, C_T = NC(1)			20			20	µs
t_{PLH}	Propagation delay time, high-to-low level output						5			5	
t_{PLH}	Propagation delay time, low-to-high level output		RESET				5			5	
t_{PLH}	Propagation delay time, high-to-low level output						20			20	
t_{PLH}	Propagation delay time, low-to-high level output	$\overline{RESIN}$	$\overline{RESET}$	V_{IH} = 0.7 × V_{DD}, V_{IL} = 0.2 × $V_{DD,SENSE}$ = V_{IT+max} + 0.2 V, CONTROL = 0.2 × V_{DD}, C_T = NC(1)			20			20	µs
t_{PLH}	Propagation delay time, high-to-low level output						60			60	ns
t_{PLH}	Propagation delay time, low-to-high level output		RESET				65			65	
t_{PLH}	Propagation delay time, high-to-low level output						20			20	µs
t_{PLH}	Propagation delay time, low-to-high level output	CONTROL	RESET	V_{IH} = 0.7 × V_{DD}, V_{IL} = 0.2 × $V_{DD,SENSE}$ = V_{IT+max} + 0.2 V, $\overline{RESIN}$ = 0.7 × V_{DD}, C_T = NC(1)			58			58	ns
t_{PLH}	Propagation delay time, high-to-low level output						58			58	ns
	Low-level minimum pulse duration to switch RESET and $\overline{RESET}$	SENSE		V_{IH} = V_{IT+max} + 0.2 V, V_{IL} = V_{IT-min} - 0.2 V	3			4			µs
		$\overline{RESIN}$		V_{IL} = 0.2 × V_{DD}, V_{IH} = 0.7 × V_{DD}	1			1			
t_r	Rise time		RESET and $\overline{RESET}$	10% to 90%		8			8		ns/V
t_f	Fall time			90% to 10%		4			4		

(1) NC = No capacitor, and includes up to 100-pF probe and jig capacitance.

PARAMETER MEASUREMENT INFORMATION



A. For switching characteristics, R_L = 2 kΩ

B. C_L = 50 pF includes jig and probe capacitance

Figure 2. RESET AND $\overline{\text{RESET}}$ Output Configurations

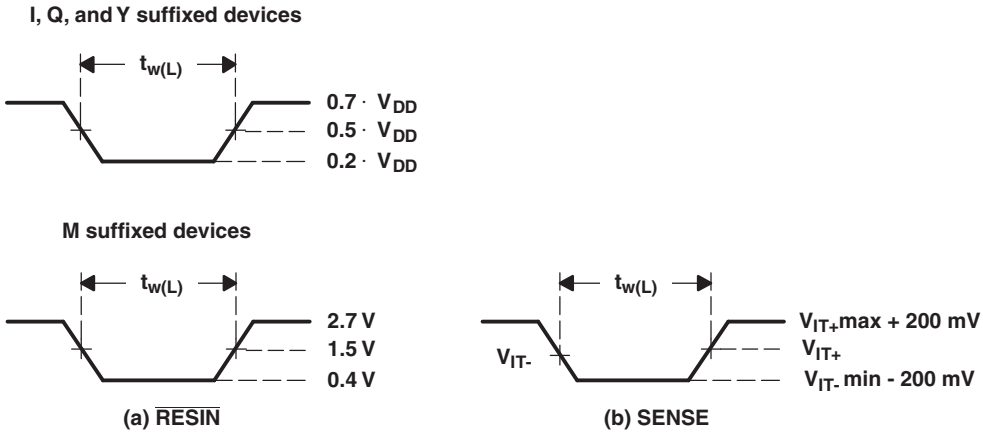


Figure 3. Input Pulse Definition Waveforms

TYPICAL CHARACTERISTICS

NORMALIZED INPUT THRESHOLD VOLTAGE vs TEMPERATURE

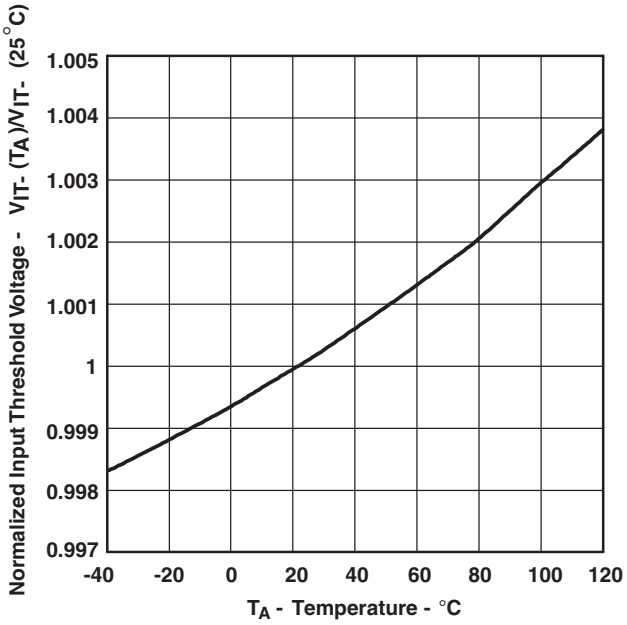


Figure 4.

SUPPLY CURRENT vs SUPPLY VOLTAGE

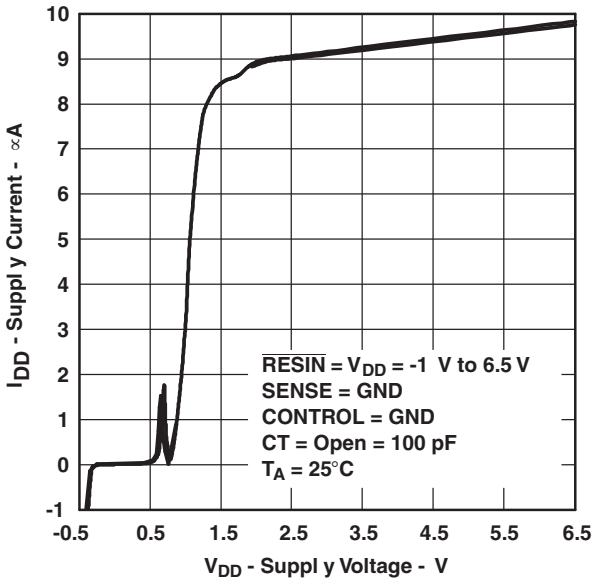


Figure 5.

HIGH-LEVEL OUTPUT VOLTAGE vs HIGH-LEVEL OUTPUT CURRENT

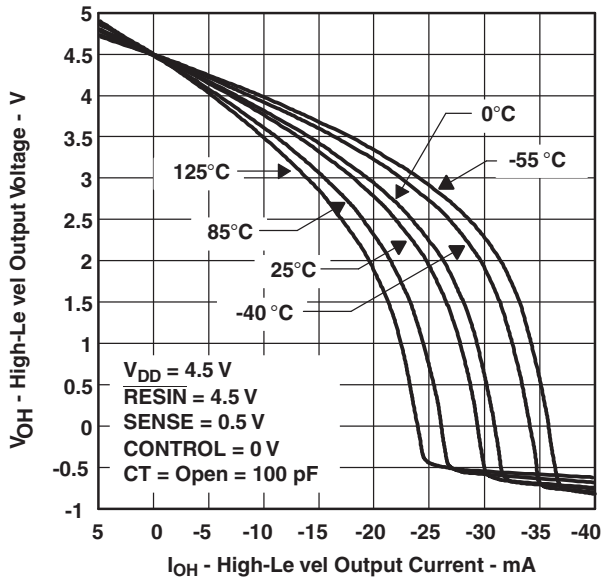


Figure 6.

LOW-LEVEL OUTPUT VOLTAGE vs LOW-LEVEL OUTPUT CURRENT

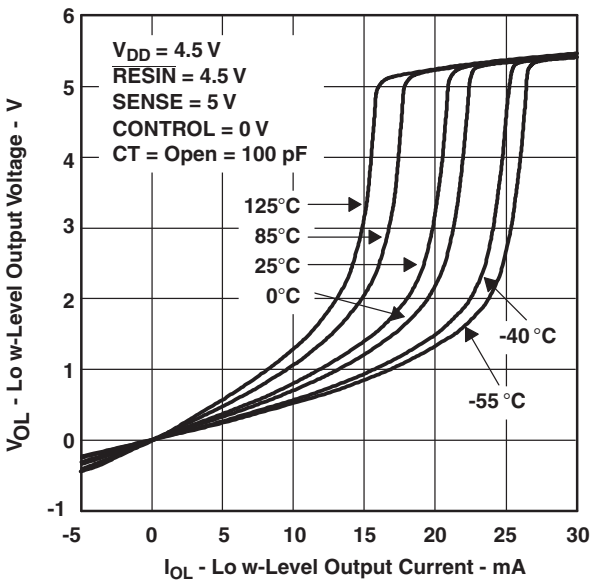


Figure 7.

TYPICAL CHARACTERISTICS (continued)

INPUT CURRENT vs INPUT VOLTAGE AT SENSE

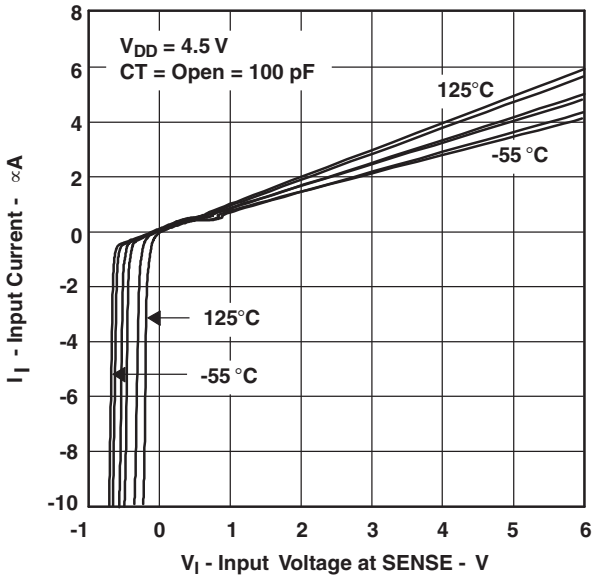


Figure 8.

MINIMUM PULSE DURATION AT SENSE vs SENSE THRESHOLD OVERDRIVE

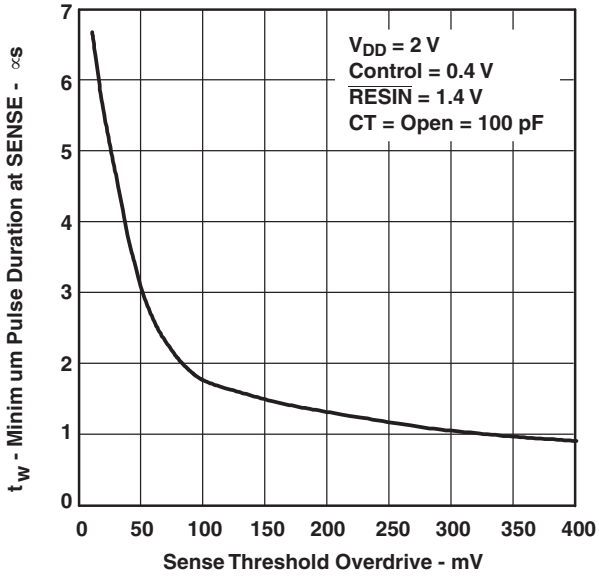


Figure 9.

APPLICATION INFORMATION

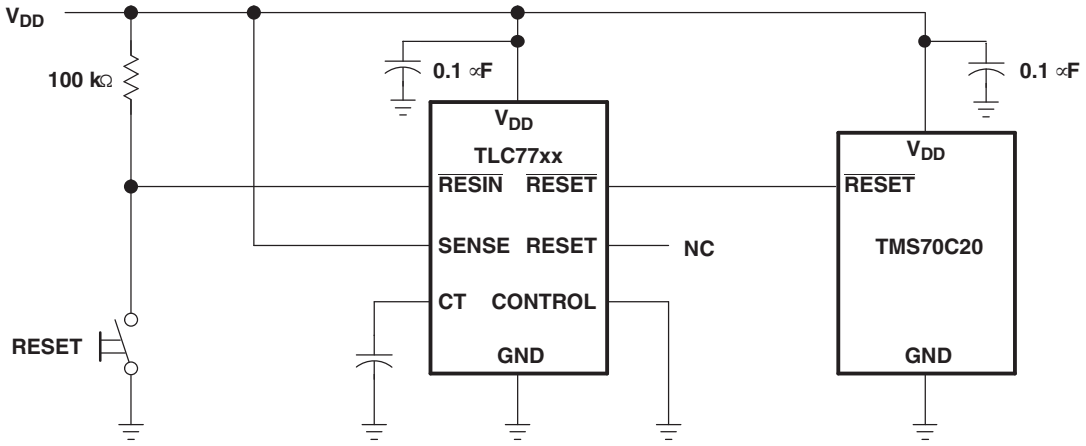


Figure 10. Reset Controller in a Microcomputer System

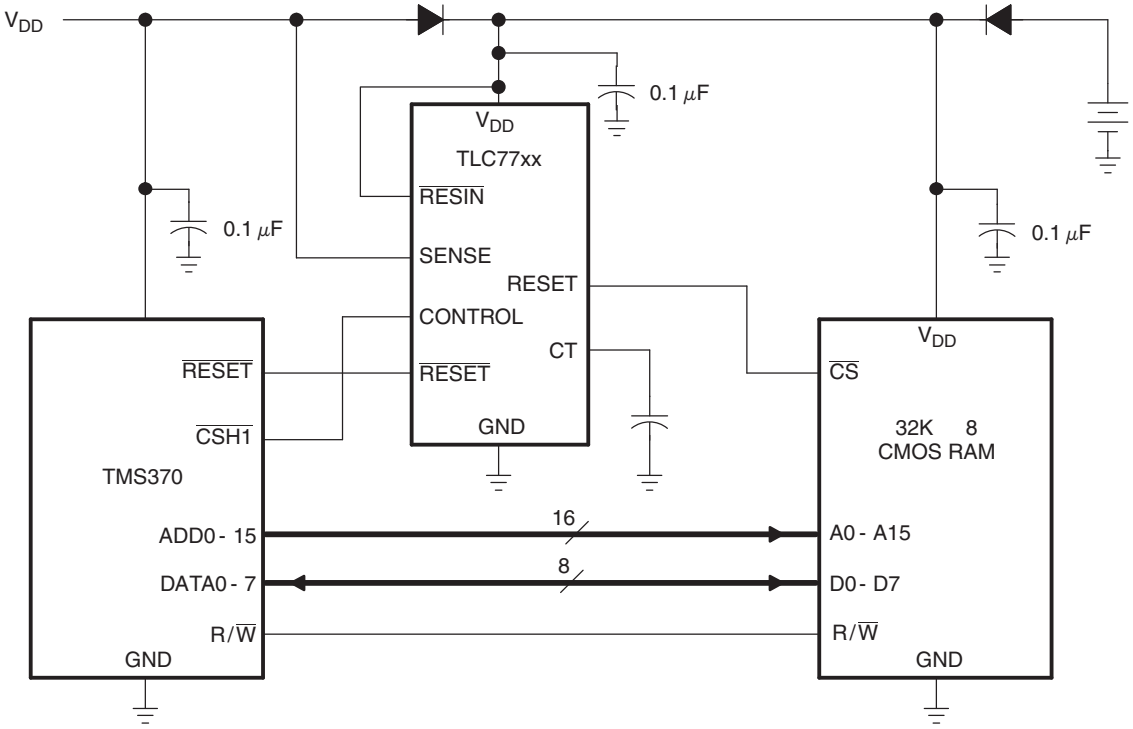


Figure 11. Data Retention During Power Down Using Static CMOS RAMs

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLC7701MDREP	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	7701ME	Samples
TLC7701MPWREP	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	7701ME	Samples
TLC7701MPWREPG4	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	7701ME	Samples
TLC7701QPWREP	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	7701QE	Samples
TLC7705QPWREP	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	7705QE	Samples
TLC7733MPWREP	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	7733ME	Samples
TLC7733QPWREP	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	7733QE	Samples
V62/04604-01XE	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	7701QE	Samples
V62/04604-02XE	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	7705QE	Samples
V62/04604-03XE	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	7733QE	Samples
V62/04604-04XE	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	7701ME	Samples
V62/04604-04YE	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	7701ME	Samples
V62/04604-06XE	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	7733ME	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF TLC7701-EP, TLC7705-EP, TLC7733-EP :

- Catalog: TLC7701, TLC7705, TLC7733
- Automotive: TLC7701-Q1, TLC7705-Q1, TLC7733-Q1
- Military: TLC7705M, TLC7733M

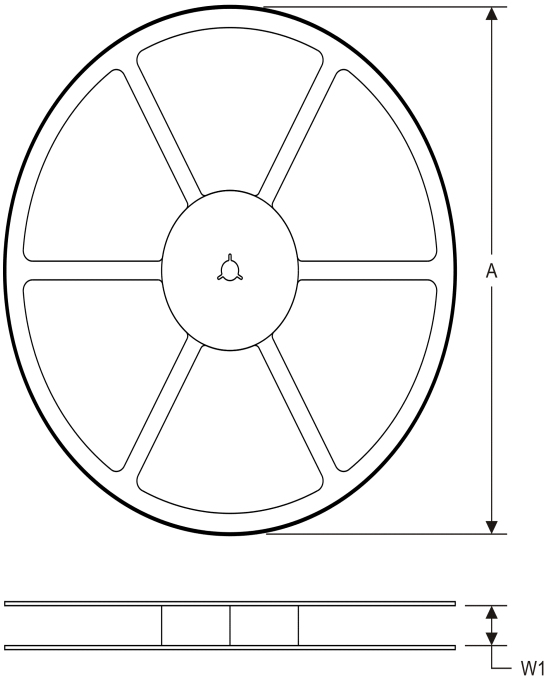
NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

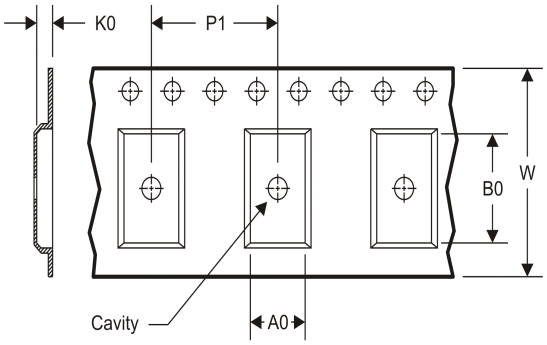
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



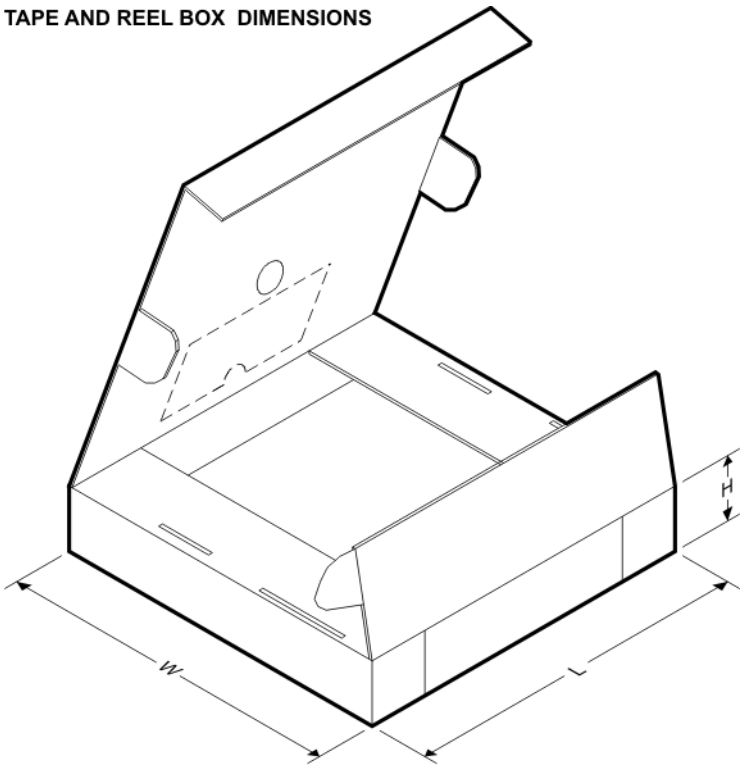
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLC7701MDREP	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLC7701MPWREP	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
TLC7701QPWREP	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
TLC7705QPWREP	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
TLC7733MPWREP	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
TLC7733QPWREP	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

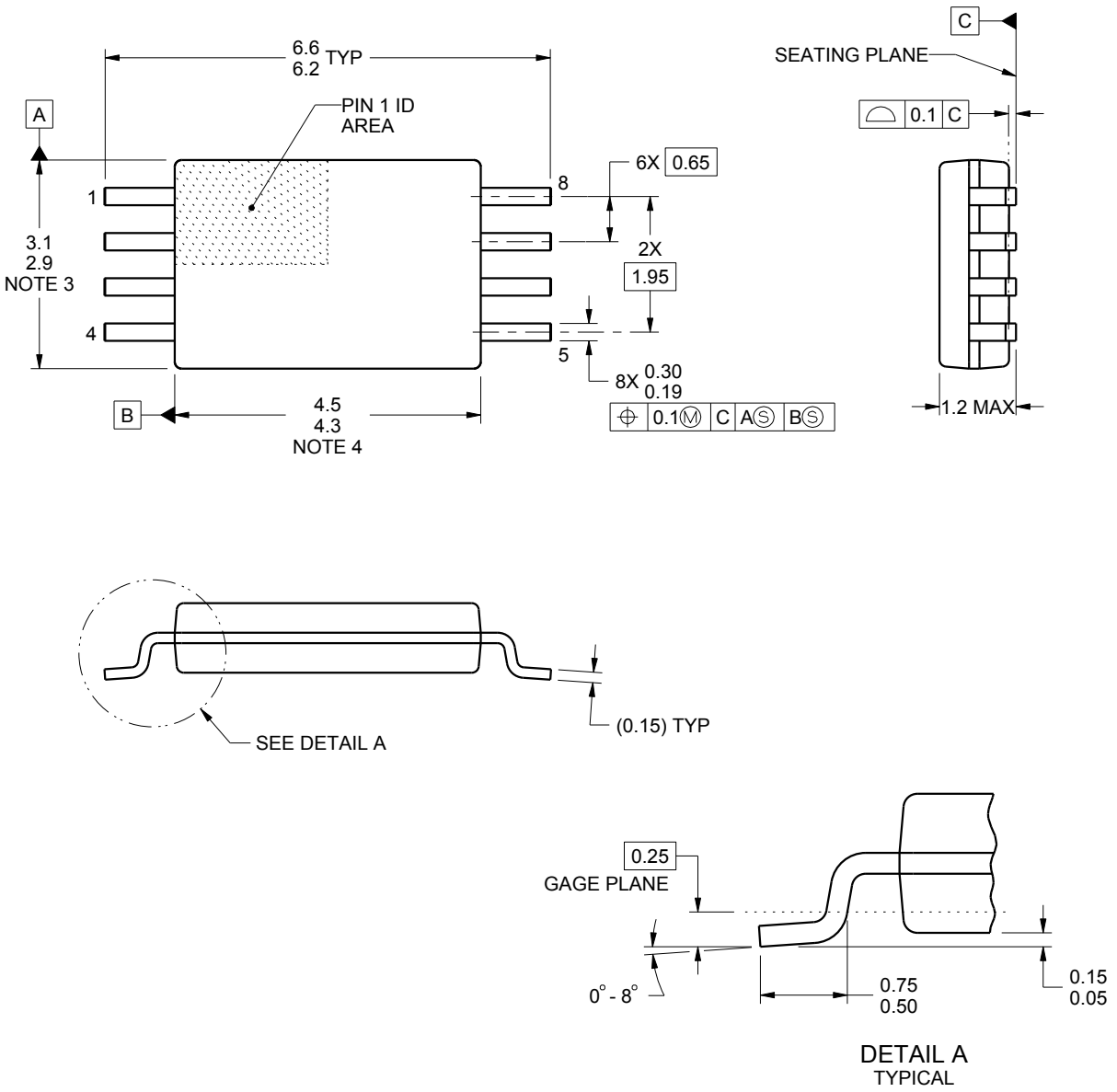
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLC7701MDREP	SOIC	D	8	2500	367.0	367.0	35.0
TLC7701MPWREP	TSSOP	PW	8	2000	367.0	367.0	35.0
TLC7701QPWREP	TSSOP	PW	8	2000	367.0	367.0	35.0
TLC7705QPWREP	TSSOP	PW	8	2000	367.0	367.0	35.0
TLC7733MPWREP	TSSOP	PW	8	2000	367.0	367.0	35.0
TLC7733QPWREP	TSSOP	PW	8	2000	367.0	367.0	35.0

PACKAGE OUTLINE

PW0008A

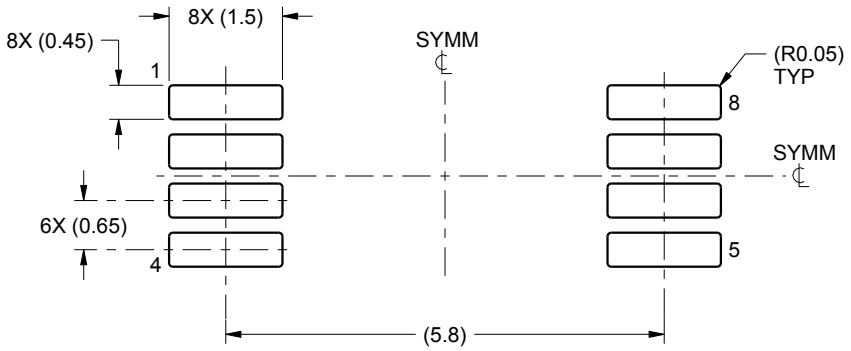
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

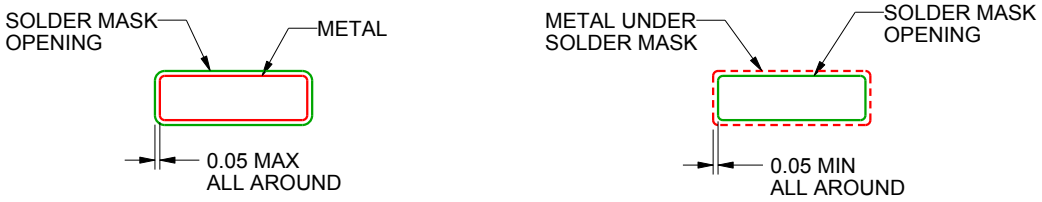


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153, variation AA.



LAND PATTERN EXAMPLE
SCALE:10X



SOLDER MASK DETAILS
NOT TO SCALE

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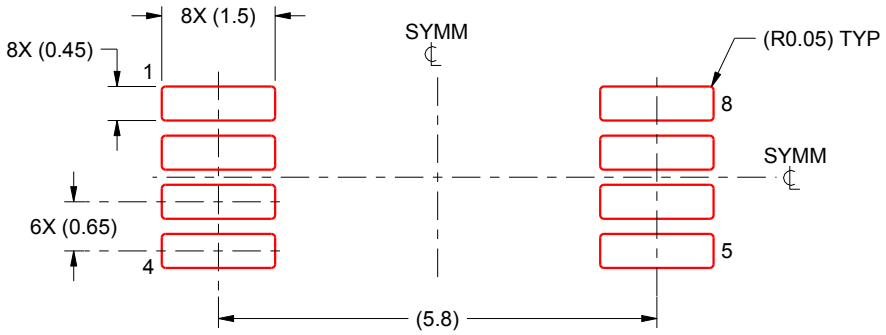
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

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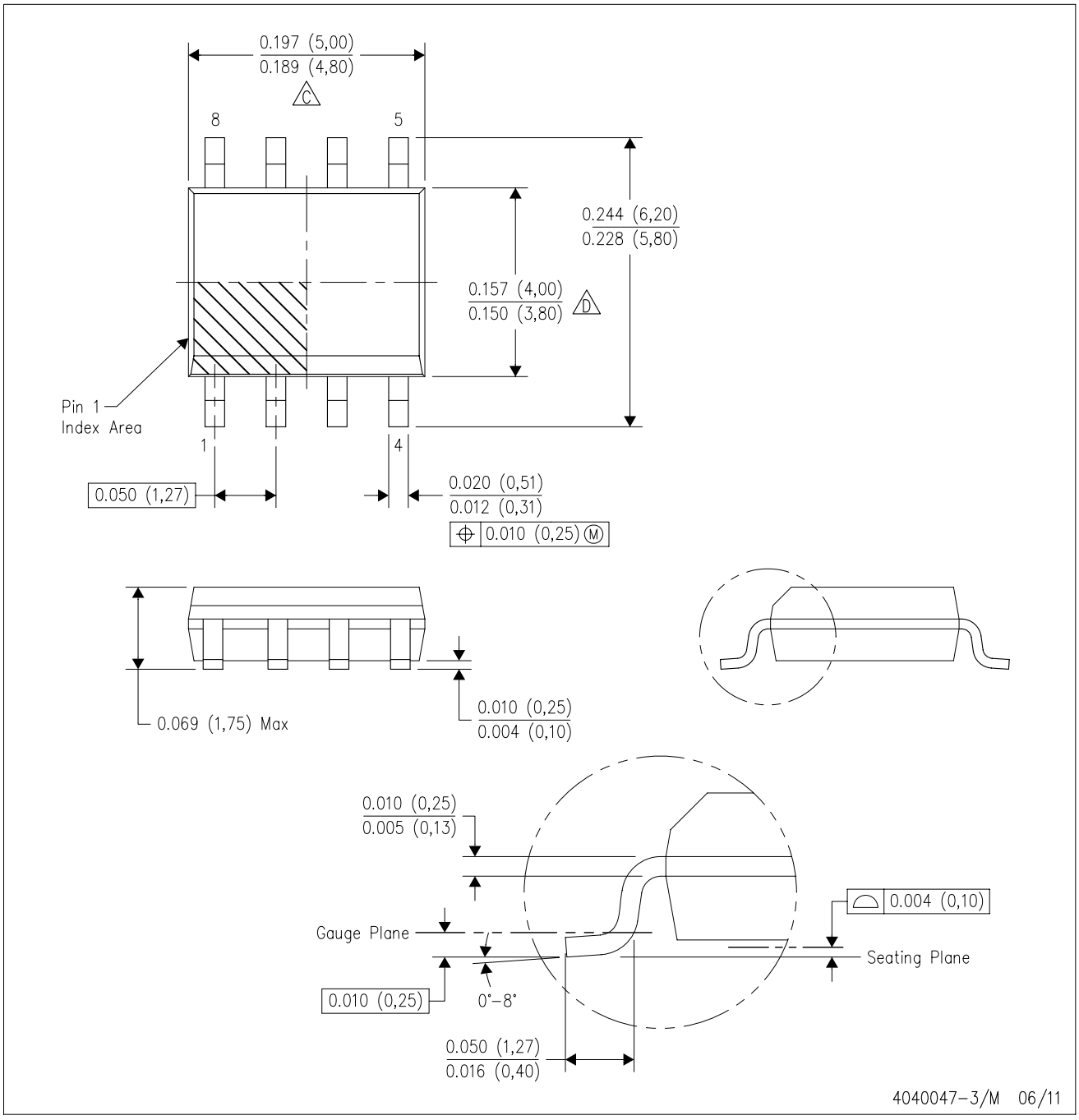
NOTES: (continued)

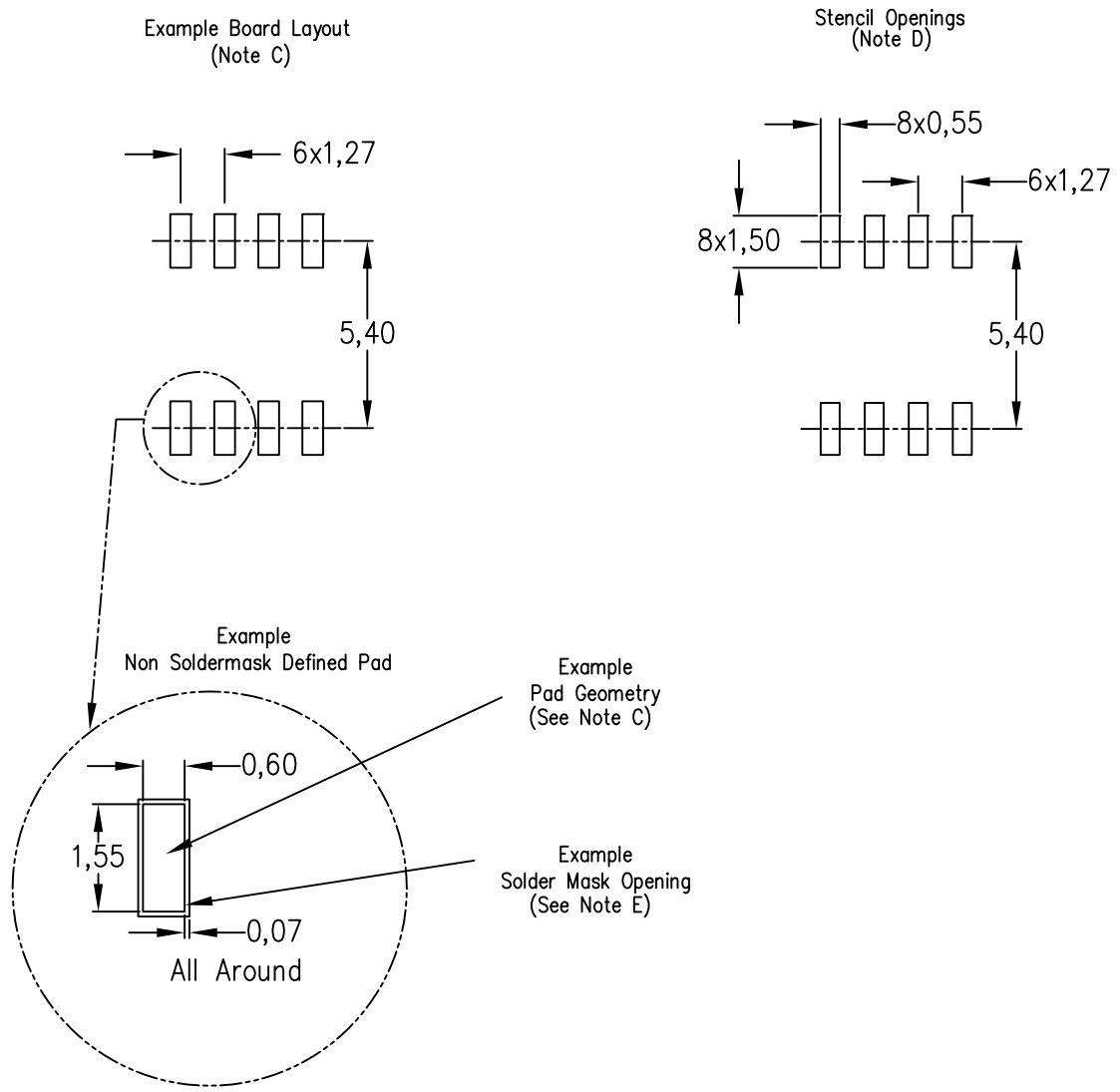
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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