

TOSHIBA BIPOLAR LINEAR INTEGRATED CIRCUIT SILICON MONOLITHIC

TA8435H

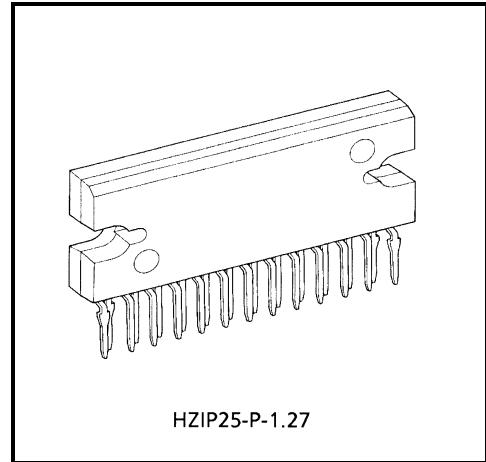
PWM CHOPPER TYPE BIPOLAR STEPPING MOTOR DRIVER.

The TA8435H is PWM chopper type sinusoidal micro step bipolar stepping motor driver.

Sinusoidal micro step operation is accomplished only a clock signal inputting by means of built-in hard ware.

FEATURES

- 1 chip bipolar sinusoidal micro step stepping motor driver.
- Output current up to 1.5 A (AVE.) and 2.5 A (PEAK).
- PWM chopper type.
- Structured by high voltage Bi-CMOS process technology.
- Forward and reverse rotation are available.
- 2, 1-2, W1-2, 2W1-2 phase 1 or 2 clock drives are selectable.
- Package : HZIP25-P
- Input Pull-up Resistor equipped with $\overline{\text{RESET}}$ Terminal: R = 100 k Ω (Typ.)
- Output Monitor available with $\overline{\text{MO}}$ $I_{O(\overline{\text{MO}})} = \pm 2 \text{ mA (MAX.)}$
- Reset and Enable are available with $\overline{\text{RESET}}$ and $\overline{\text{ENABLE}}$.

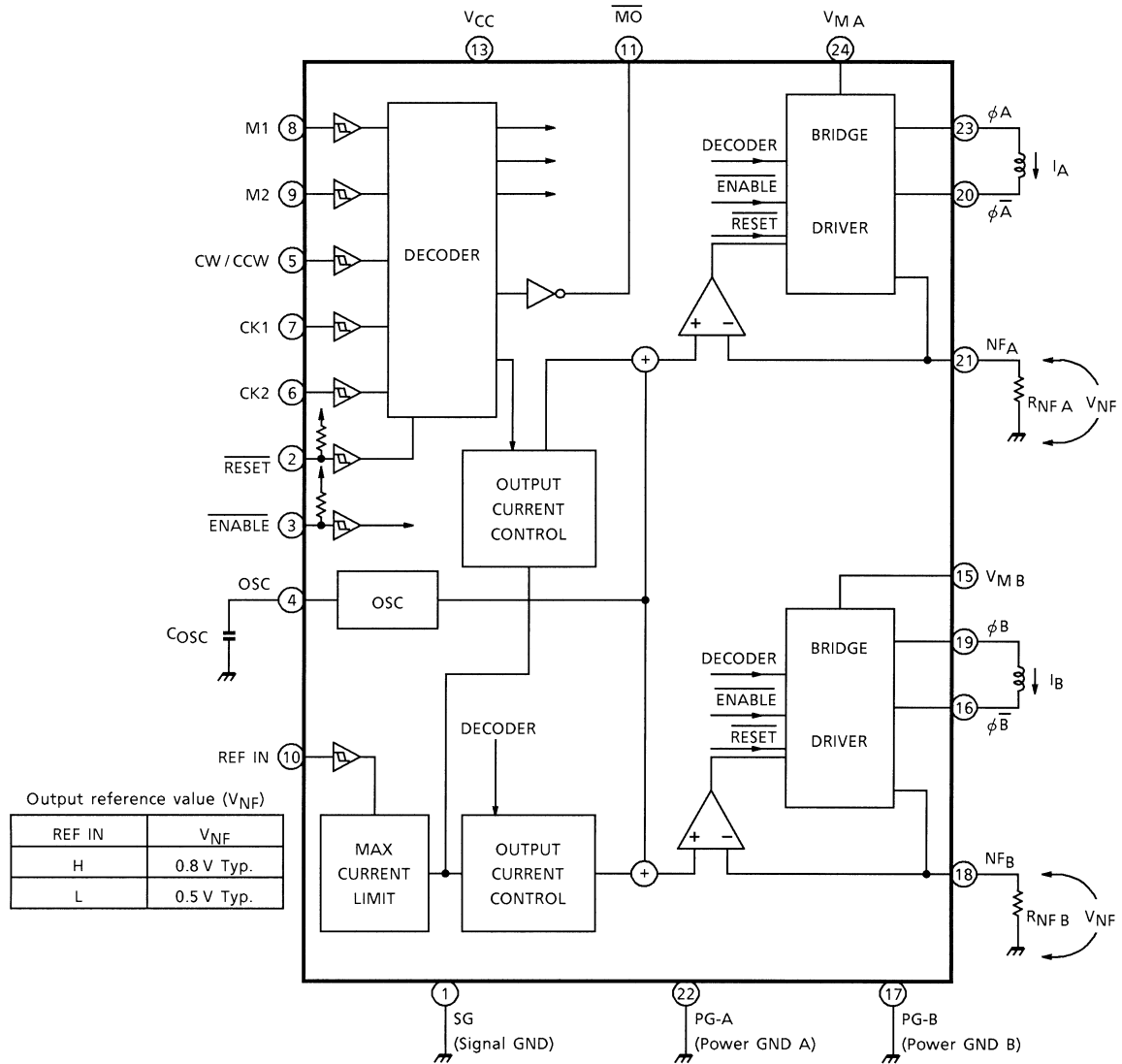


Weight: 9.86 g (Typ.)

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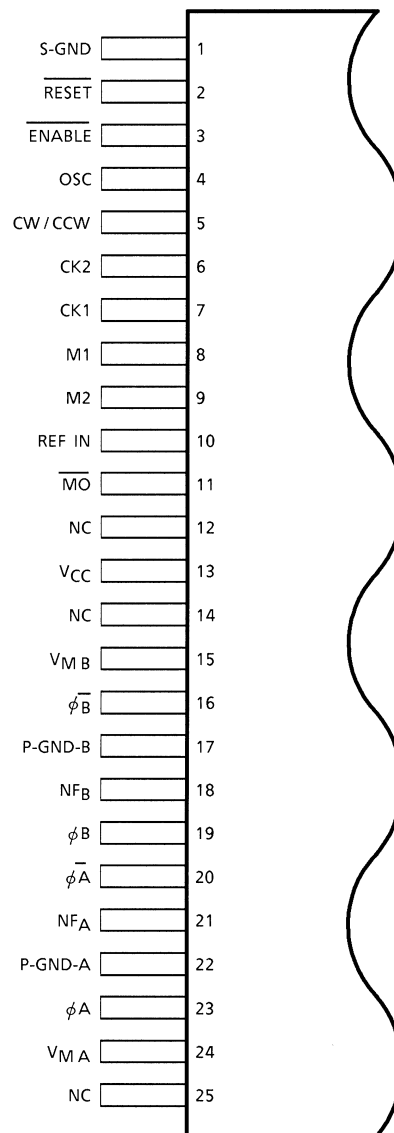
BLOCK DIAGRAM



Pull-up resistance : 100 k Ω (Typ.)

Pin 12、14、25 : Non connection

PIN CONNECTION (Top view)

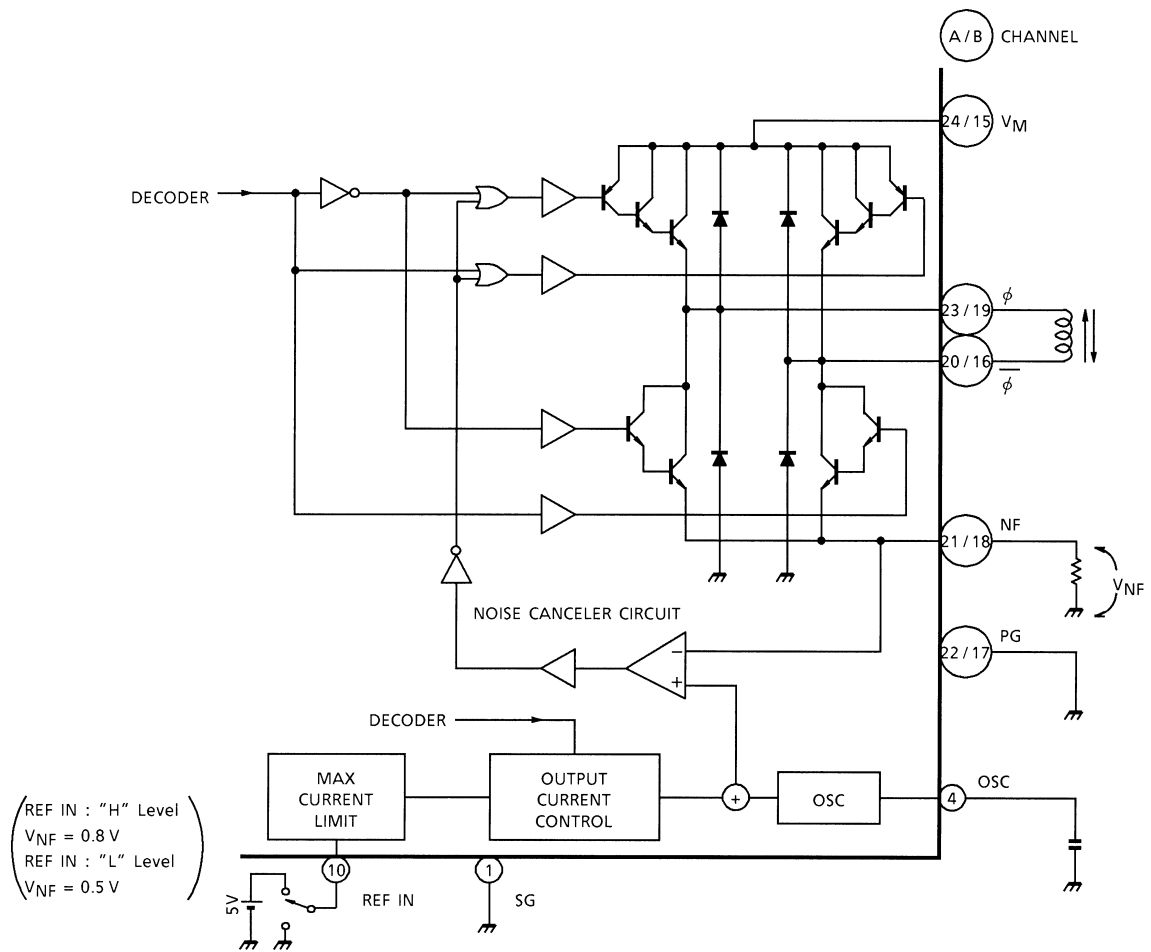


Note: NC : No connection

PIN FUNCTION

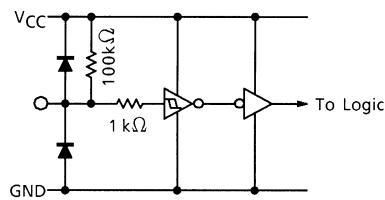
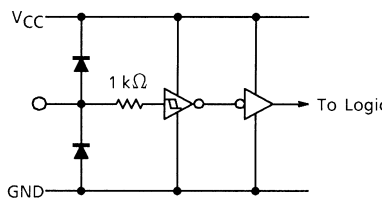
PIN No	SYMBOL	FUNCTIONAL DESCRIPTION
1	SG	Signal GND.
2	$\overline{\text{RESET}}$	L : RESET.
3	$\overline{\text{ENABLE}}$	L : ENABLE, H: OFF.
4	OSC	Chopping oscillation is determined by the external capacitor.
5	CW / CCW	Forward / Reverse switching terminal.
6	CK2	Clock input terminal.
7	CK1	Clock input terminal.
8	M1	Excitation control input
9	M2	Excitation control input
10	REF IN	V_{NF} control input
11	$\overline{\text{MO}}$	Monitor output
12	NC	No connection.
13	V_{CC}	Voltage supply for logic.
14	NC	No connection.
15	V_{MB}	Output power supply terminal.
16	$\phi \overline{\text{B}}$	Output $\phi \overline{\text{B}}$
17	PG-B	Power GND.
18	NF_{B}	B-ch output current detection terminal.
19	ϕB	Output ϕB
20	$\phi \overline{\text{A}}$	Output $\phi \overline{\text{A}}$
21	NF_{A}	A-ch output current detection terminal.
22	PG-A	Power GND
23	ϕA	Output ϕA
24	V_{MA}	Output power supply terminal.
25	NC	No connection.

OUTPUT CIRCUIT

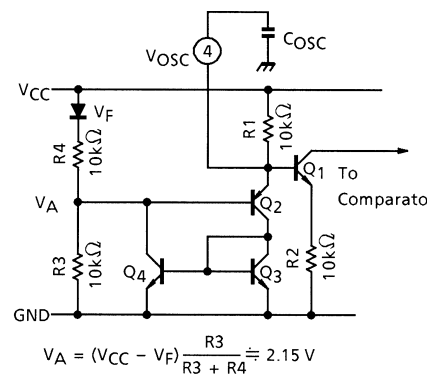


INPUT CIRCUIT

- CK1, CK2, CW / CCW, M1, M2, REF IN: Terminals
- $\overline{\text{RESET}}$, $\overline{\text{ENABLE}}$: Terminals
- OSC: Terminal



100 kΩ of Pull-up Resistor is equipped.



OSC FREQUENCY CALCULATION

Sawtooth OSC circuit consists of Q₁ through Q₄ and R₁ through R₄.

Q₂ is turned “off” when V_{OSC} is less than the voltage of 2.5 V + V_{BE} Q₂ approximately equal to 2.85 V.

V_{OSC} is increased by C_{OSC} charging through R₁.

Q₃ and Q₄ are turned “on” when V_{OSC} becomes 2.85 V (Higher level.)

Lower level of V (4) pin is equal to V_{BE} Q₂ + V_{SAT} Q₄ approximately equal to 1.4 V.

V_{OSC} is calculated by following equation.

$$V_{OSC} = 5 \cdot \left[1 - \exp\left(-\frac{1}{C_{OSC} \cdot R_1}\right) \right] \dots\dots\dots (1)$$

Assuming that V_{OSC} = 1.4 V (t = t₁) and = 2.85 V (t = t₂)

C_{OSC} is external capacitance connected to pin (4) and R₁ is on-chip 10 kΩ resistor.

Therefore, OSC frequency is calculated as follows.

$$t_1 = -C_{OSC} R_1 \cdot \ln \left(1 - \frac{1.4}{5} \right) \dots\dots\dots (2)$$

$$t_2 = -C_{OSC} R_1 \cdot \ln \left(1 - \frac{2.85}{5} \right) \dots\dots\dots (3)$$

$$f_{OSC} = \frac{1}{t_2 - t_1} = \frac{1}{C_{OSC} \left(R_1 \cdot \ln \left(1 - \frac{1.4}{5} \right) - R_1 \cdot \ln \left(1 - \frac{2.85}{5} \right) \right)}$$

$$= \frac{1}{5.15 \cdot C_{OSC}} \text{ (kHz) (C}_{OSC} : \mu\text{F)}$$

ENABLE AND RESET FUNCTION AND \overline{MO} SIGNAL

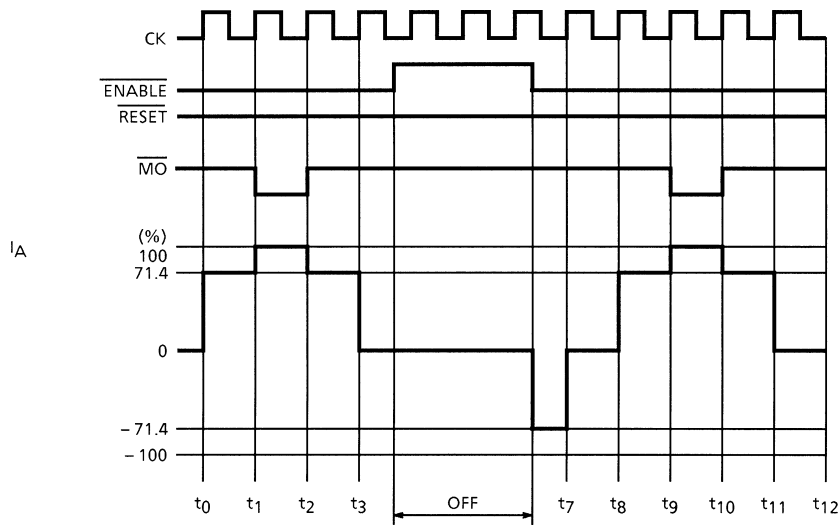


Fig.1 1-2 Phase drive mode (M1: H, M2: L)

\overline{ENABLE} Signal disables only Output Signal.

Internal logic functions are proceeded by CK signal without regard to \overline{ENABLE} signal.

Therefore, Output Current is initiated from the proceeded timing point of internal logic circuit after release of disable mode.

Fig.1 shows the \overline{ENABLE} functions, when the system is selected in 1-2 Phase drive mode.

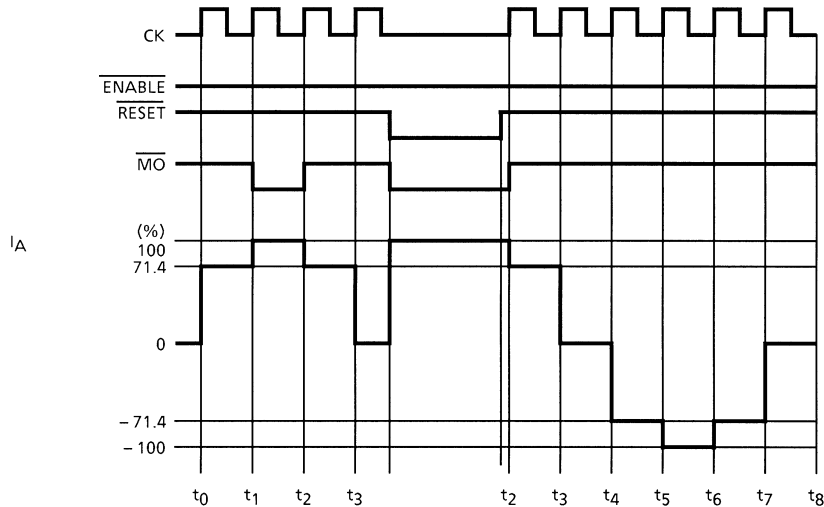


Fig.2 1-2 Phase drive mode (M1: H, M2: L)

Low level active of \overline{RESET} Signal offs not only the Outputs but also stops internal CK functions and \overline{MO} to low.

Outputs are initiated from the initial point after release of \overline{RESET} (High) as shown in Fig.2.

\overline{MO} (Monitor Output) Signals can be used as rotation and initial signal for stable rotation checking.

FUNCTION

INPUT					MODE
CK1	CK2	CW / CCW	RESET	ENABLE	
	H	L	H	L	CW
	L	L	H	L	INHIBIT (Note)
H		L	H	L	CCW
L		L	H	L	INHIBIT (Note)
	H	H	H	L	CCW
	L	H	H	L	INHIBIT (Note)
H		H	H	L	CW
L		H	H	L	INHIBIT (Note)
X	X	X	L	L	RESET
X	X	X	X	H	Z

INITIAL MODE

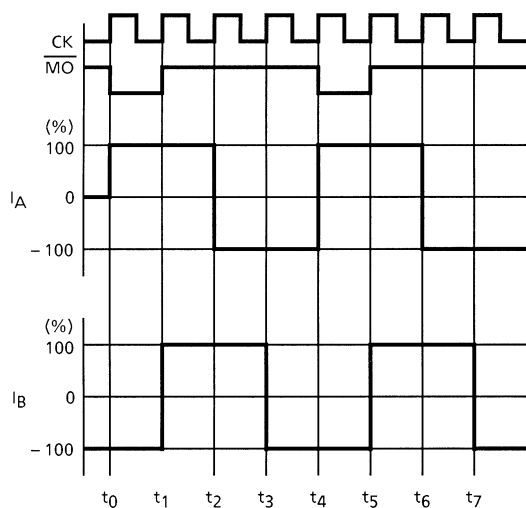
EXCITATION MODE	A PHASE CURRENT	B PHASE CURRENT
2 Phase	100%	-100%
1-2 Phase	100%	0%
W1-2 Phase	100%	0%
2W1-2 Phase	100%	0%

Z: High impedance

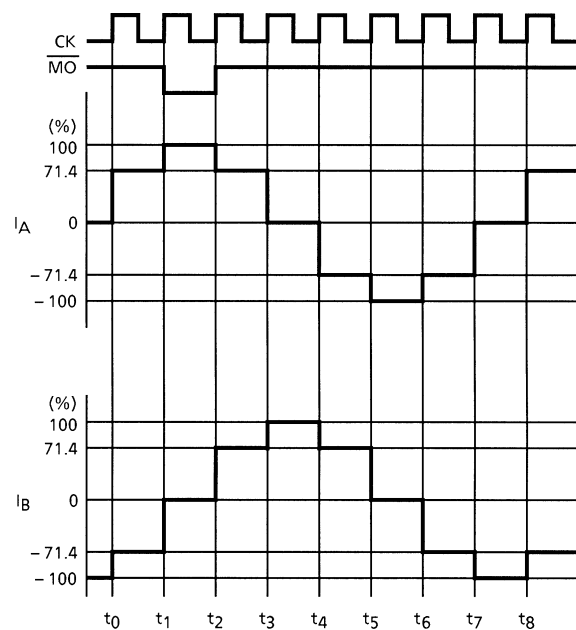
X: Don't Care

INPUT		MODE (EXCITATION)
M1	M2	
L	L	2 Phase
H	L	1-2 Phase
L	H	W1-2 Phase
H	H	2W1-2 Phase

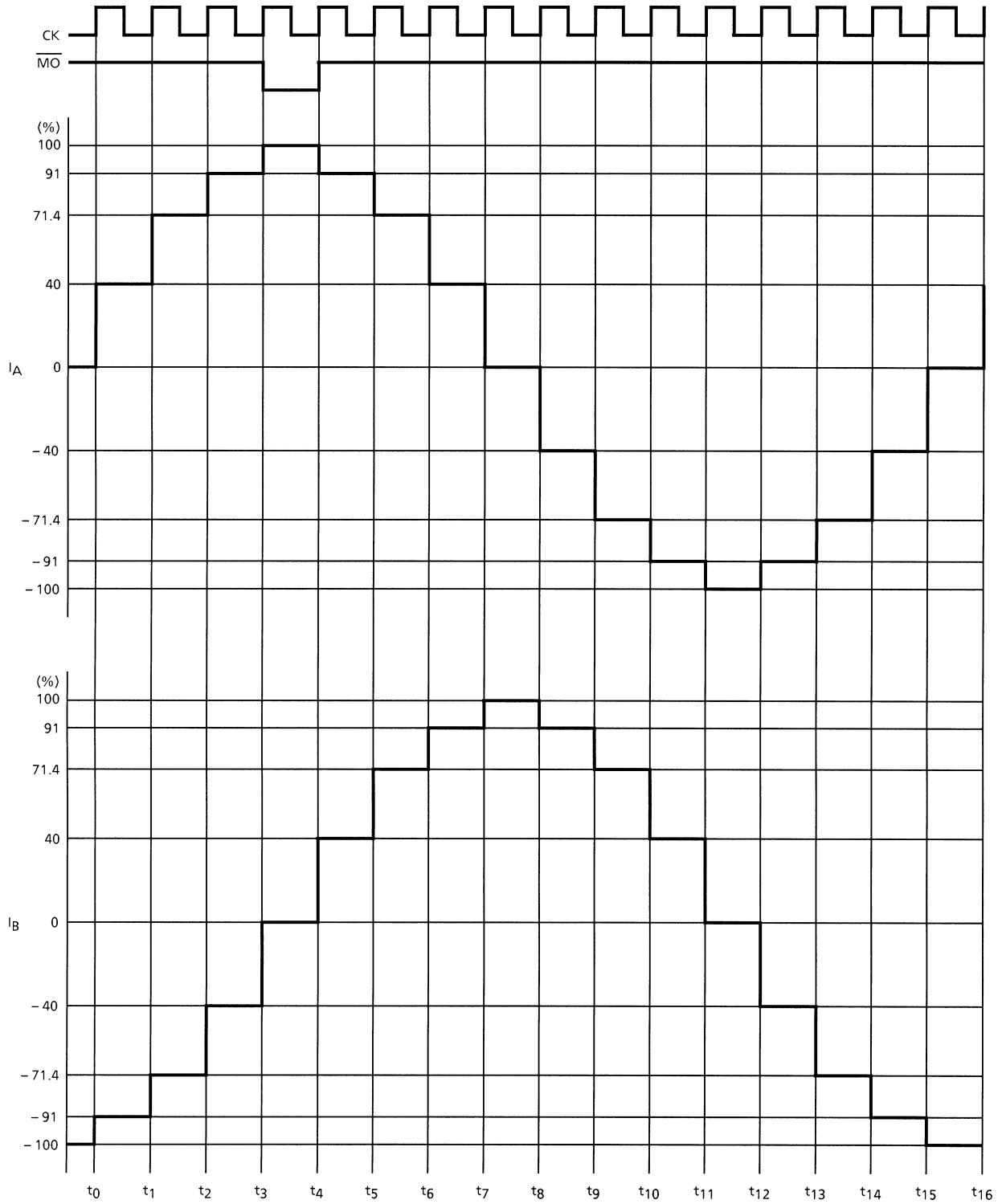
2 PHASE EXCITATION (M1 : L, M2 : L, CW MODE)



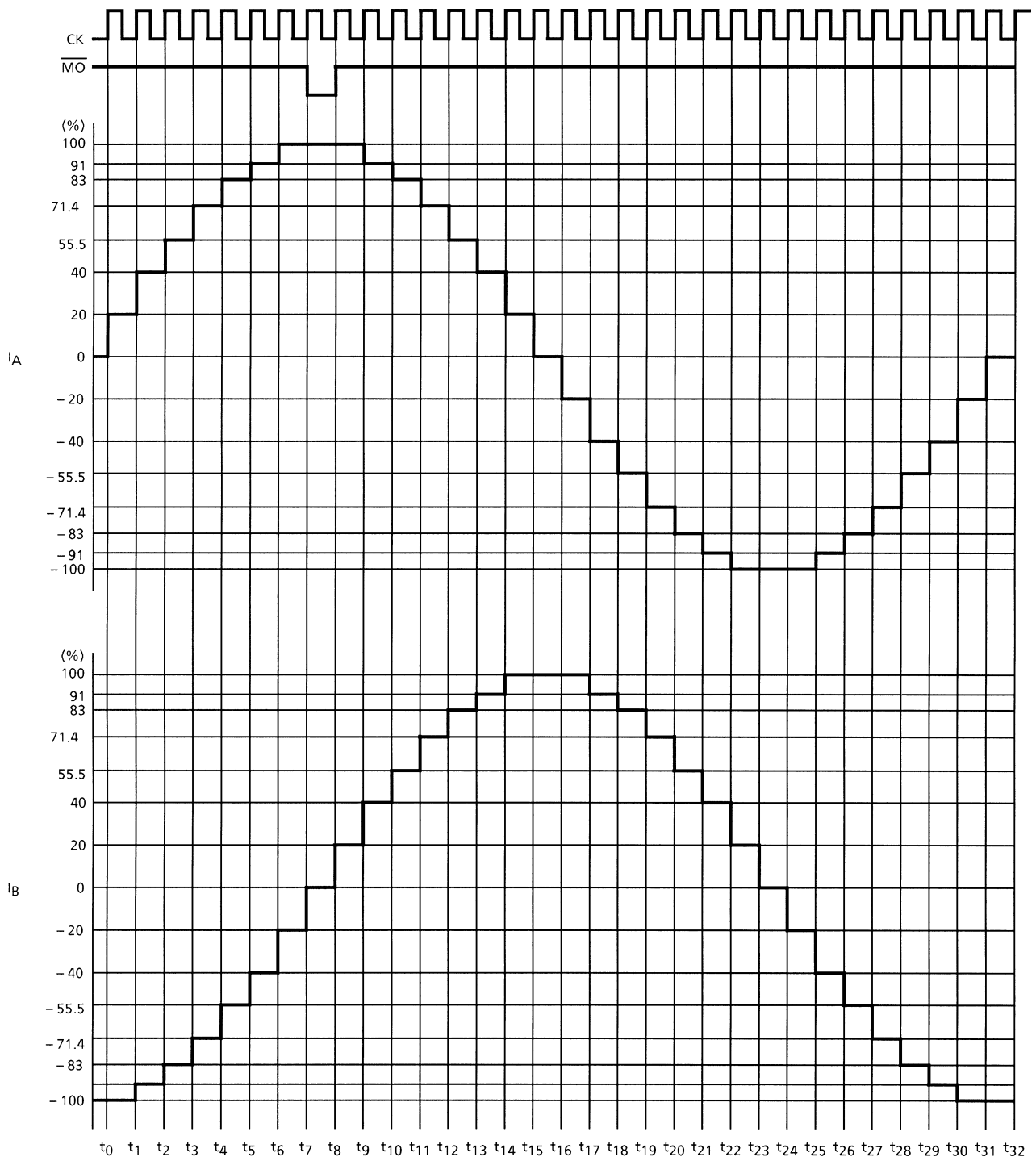
1-2 PHASE EXCITATION (M1 : H, M2 : L, CW MODE)



W1-2 PHASE EXCITATION (M1 : L, M2 : H, CW MODE)



2W1-2 PHASE EXCITATION (M1 : H, M2 : H, CW MODE)



MAXIMUM RATINGS (Ta = 25°C)

CHARACTERISTIC		SYMBOL	RATING	UNIT
Supply Voltage		V _{CC}	5.5	V
Output Voltage		V _M	40	V
Output Current	PEAK	I _{O (PEAK)}	2.5	A
	AVE	I _{O (AVE.)}	1.5	
\overline{MO} Output Current		I _{O (\overline{MO})}	±2	mA
Input Voltage		V _{IN}	~V _{CC}	V
Power Dissipation		P _D	5 (Note 1)	W
			43 (Note 2)	
Operating Temperature		T _{opr}	-40~85	°C
Storage Temperature		T _{stg}	-55~150	°C
Feed Back Voltage		V _{NF}	1.0	V

Note 1: No heat sink

Note 2: T_c = 85°C

RECOMMENDED OPERATING CONDITIONS (Ta = -20~75°C)

CHARACTERISTIC	SYMBOL	TEST CONDITION	MIN	TYP.	MAX	UNIT
Supply Voltage	V _{CC}	—	4.5	5.0	5.5	V
Output Voltage	V _M	—	21.6	24	26.4	V
Output Current	I _{OUT}	—	—	—	1.5	A
Input Voltage	V _{IN}	—	—	—	V _{CC}	V
Clock Frequency	f _{CK}	—	—	—	5	kHz
OSC Frequency	f _{OSC}	—	15	—	80	kHz

ELECTRICAL CHARACTERISTICS (Ta = 25°C, VCC = 5 V, VM = 24 V)

CHARACTERISTIC		SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN	TYP.	MAX	UNIT	
Input Voltage	High	$V_{IN(H)}$	1	M1, M2, CW / CCW, REF IN \overline{ENABLE} , CK1, CK2 RESET	3.5	—	$V_{CC} + 0.4$	V	
	Low	$V_{IN(L)}$			GND - 0.4	—	1.5		
Input Hysteresis Voltage		V_H			—	600	—	mV	
Input Current		$I_{IN-1(H)}$	1	M1, M2, REF IN, $V_{IN} = 5.0$ V	—	—	100	nA	
		$I_{IN-1(L)}$		\overline{RESET} , \overline{ENABLE} , $V_{IN} = 0$ V INTERNAL PULL-UP RESISTOR	10	50	100	μ A	
		$I_{IN-2(L)}$		SOURCE TYPE, $V_{IN} = 0$ V	—	—	100	nA	
Quiescent Current VCC Terminal		I_{CC1}	1	Output Open, $\overline{RESET} : H$ $\overline{ENABLE} : L$ (2, 1-2 Phase excitation)	—	10	18	mA	
		I_{CC2}		Output Open, $\overline{RESET} : H$ $\overline{ENABLE} : L$ (W1-2, 2W1-2 Phase excitation)	—	10	18		
		I_{CC3}		$\overline{RESET} : L$, $\overline{ENABLE} : H$	—	5	—		
		I_{CC4}		$\overline{RESET} : H$, $\overline{ENABLE} : H$	—	5	—		
Comparator Reference Voltage	High	$V_{NF(H)}$	3	REF IN H Output Open	(Note)	0.72	0.8	0.88	V
	Low	$V_{NF(L)}$		REF IN L Output Open		0.45	0.5	0.55	
Output Differential		ΔV_O	—	B / A, $C_{OSC} = 0.0033 \mu F$, $R_{NF} = 0.8 \Omega$	-10	—	10	%	
$V_{NF(H)} - V_{NF(L)}$		ΔV_{NF}	—	$V_{NF(L)} / V_{NF(H)}$ $C_{OSC} = 0.0033 \mu F$, $R_{NF} = 0.8 \Omega$	56	63	70	%	
NF Terminal Current		I_{NF}	—	SOURCE TYPE	—	170	—	μ A	
Maximum OSC Frequency		$f_{OSC(MAX.)}$	—	—	100	—	—	kHz	
Minimum OSC Frequency		$f_{OSC(MIN.)}$	—	—	—	—	10	kHz	
OSC Frequency		f_{OSC}	—	$C_{OSC} = 0.0033 \mu F$	25	44	62	kHz	
Minimum Clock Pulse Width		$t_W(CK)$	—	—	—	1.0	—	μs	
Output Voltage	$V_{OH(MO)}$	—	—	$I_{OH} = -40 \mu A$	4.5	4.9	V_{CC}	V	
	$V_{OL(MO)}$			$I_{OL} = 40 \mu A$	GND	0.1	0.5		

Note: 2 Phase excitation, $R_{NF} = 0.7 \Omega$, $C_{OSC} = 0.0033 \mu F$

OUTPUT BLOCK

CHARACTERISTIC				SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN	TYP.	MAX	UNIT		
Output Saturation Voltage	Upper Side		$V_{SAT U1}$	4	$I_{OUT} = 1.5 A$	—	2.1	2.8	V			
	Lower Side		$V_{SAT L1}$			—	1.3	2.0				
	Upper Side		$V_{SAT U2}$		$I_{OUT} = 0.8 A$	—	1.8	2.2				
	Lower Side		$V_{SAT L2}$			—	1.1	1.5				
	Upper Side		$V_{SAT U3}$		$I_{OUT} = 2.5 A$ Pulse width 30 ms	—	2.5	3.0				
	Lower Side		$V_{SAT L3}$			—	1.8	2.2				
Diode Forward Voltage	Upper Side		$V_F U1$	5	$I_{OUT} = 1.5 A$	—	2.0	3.0	V			
	Lower Side		$V_F L1$			—	1.5	2.1				
	Upper Side		$V_F U2$		$I_{OUT} = 2.5 A$ Pulse width 30 ms	—	2.5	3.3				
	Lower Side		$V_F L2$			—	1.8	2.5				
Output Dark Current (A + B Channels)				I_{M1}	2	ENABLE : "H" Level, Output Open RESET : "L" Level	—	—	50	μA		
				I_{M2}		ENABLE : "L" Level Output Open RESET : "H" Level	—	8	15	mA		
A-B Chopping Current (Note)	2W1-2 ϕ	W1-2 ϕ	1-2 ϕ	VECTOR	—	$\theta = 0$	REF IN : H $R_{NF} = 0.8 \Omega$ $C_{OSC} = 0.0033 \mu F$	—	100	—	%	
	2W1-2 ϕ	—	—			$\theta = 1 / 8$		—	100	—		
	2W1-2 ϕ	W1-2 ϕ	—			$\theta = 2 / 8$		86	91	96		
	2W1-2 ϕ	—	—			$\theta = 3 / 8$		78	83	88		
	2W1-2 ϕ	W1-2 ϕ	1-2 ϕ			$\theta = 4 / 8$		66.4	71.4	76.4		
	2W1-2 ϕ	—	—			$\theta = 5 / 8$		50.5	55.5	60.5		
	2W1-2 ϕ	W1-2 ϕ	—			$\theta = 6 / 8$		35	40	45		
	2W1-2 ϕ	—	—			$\theta = 7 / 8$		15	20	25		
	2 Phase Excitation Mode VECTOR					—		—	—	100		—

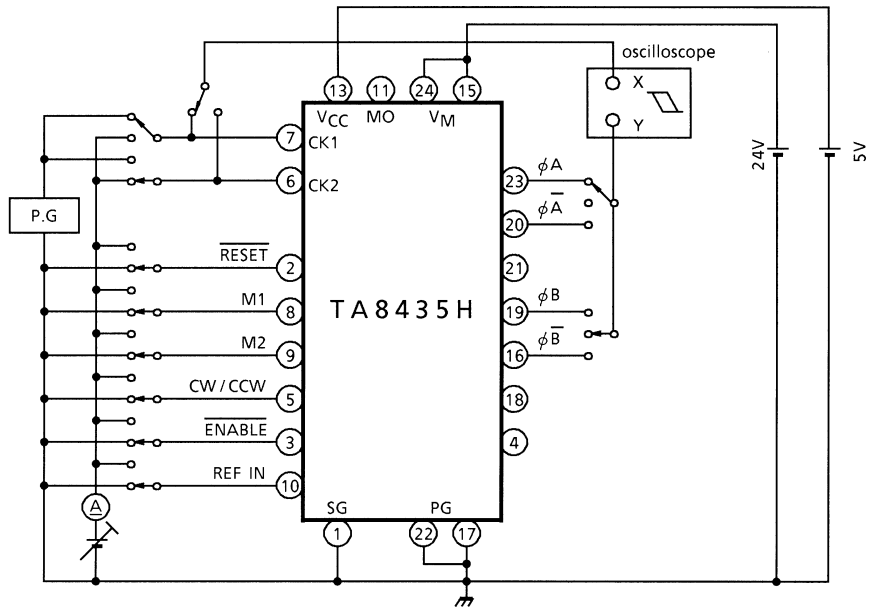
Note: Maximum current ($\theta = 0$): 100%
 2W1-2 ϕ : 2W1, 2 phase excitation mode
 W1-2 ϕ : W1, 2 phase excitation mode
 1-2 ϕ : 1, 2 phase excitation mode

CHARACTERISTIC			SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN	TYP.	MAX	UNIT		
A-B Chopping Current (Note)	2W1-2φ	W1-2φ	1-2φ	VECTOR	—	REF IN : H R _{NF} = 0.8 Ω C _{OSC} = 0.0033 μF	θ = 0	—	100	—	%
	2W1-2φ	—	—				θ = 1 / 8	—	100	—	
	2W1-2φ	W1-2φ	—				θ = 2 / 8	86	91	96	
	2W1-2φ	—	—				θ = 3 / 8	78	83	88	
	2W1-2φ	W1-2φ	1-2φ				θ = 4 / 8	66.4	71.4	76.4	
	2W1-2φ	—	—				θ = 5 / 8	50.5	55.5	60.5	
	2W1-2φ	W1-2φ	—				θ = 6 / 8	35	40	45	
	2W1-2φ	—	—				θ = 7 / 8	15	20	25	
	2 Phase Excitation Mode VECTOR							—	—	100	
Feed Back Voltage Step			ΔV _{NF}	—	REF IN : H R _{NF} = 0.8 Ω C _{OSC} = 0.0033 μF	Δθ = 0 / 8 - 1 / 8	—	0	—	mV	
						Δθ = 1 / 8 - 2 / 8	32	72	112		
						Δθ = 2 / 8 - 3 / 8	24	64	104		
						Δθ = 3 / 8 - 4 / 8	53	93	133		
						Δθ = 4 / 8 - 5 / 8	87	127	167		
						Δθ = 5 / 8 - 6 / 8	84	124	164		
						Δθ = 6 / 8 - 7 / 8	120	160	200		
Output T _r Switching Characteristics			t _r	7	R _L = 2 Ω, V _{NF} = 0 V, C _L = 15 pF	CK~Output	—	0.3	—	μs	
			t _f				—	2.2	—		
			t _{pLH}			OSC~Output	—	1.5	—		
			t _{pHL}				—	2.7	—		
			t _{pLH}			RESET ~Output	—	5.4	—		
			t _{pHL}				—	6.3	—		
			t _{pLH}			ENABLE ~Output	—	2.0	—		
			t _{pHL}				—	2.5	—		
			t _{pLH}				—	5.0	—		
t _{pHL}	—	6.0	—								
Output Leakage Current	Upper Side	I _{OH}	6	V _M = 30 V	—	—	50	μA			
	Lower Side	I _{OL}			—	—	50				

Note: Maximum current (θ = 0): 100%
 2W1-2φ: 2W1, 2 phase excitation mode
 W1-2φ : W1, 2 phase excitation mode
 1-2φ : 1, 2 phase excitation mode

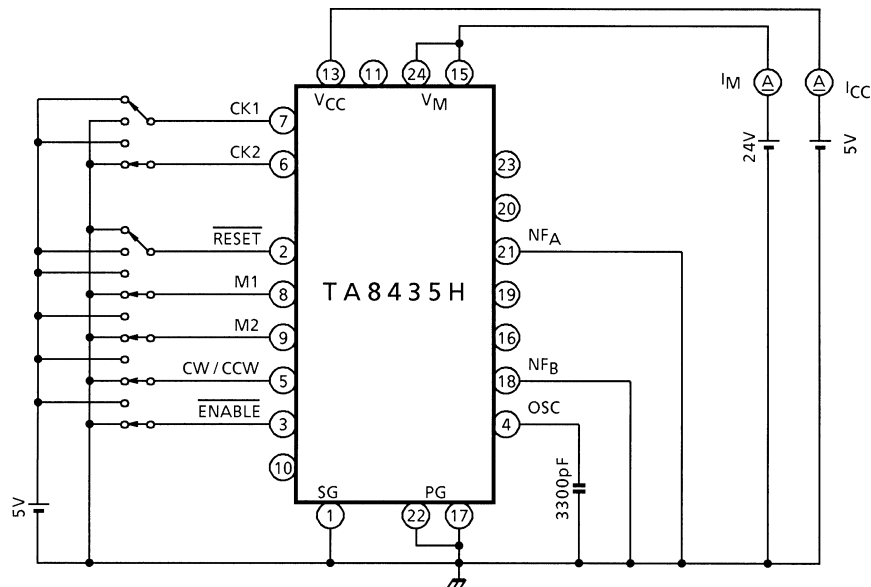
TEST CIRCUIT 1

V_{IN} (H), (L), I_{IN} (H), (L)



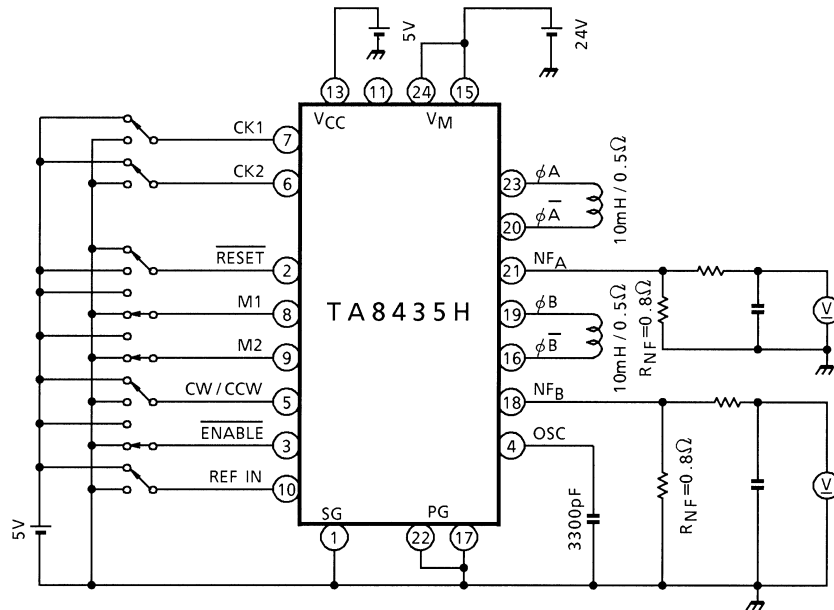
TEST CIRCUIT 2

I_{CC} , I_M



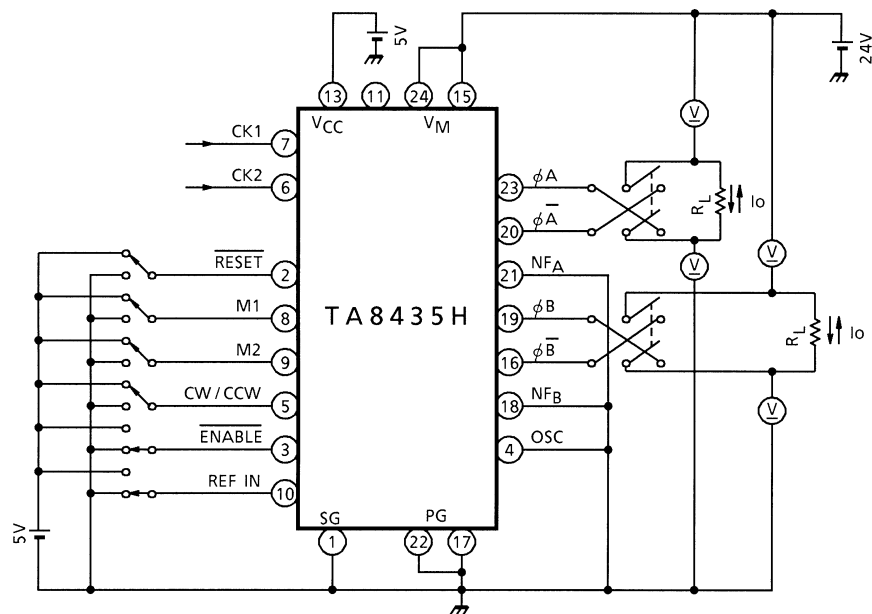
TEST CIRCUIT 3

$V_{NF(H)}, (L)$



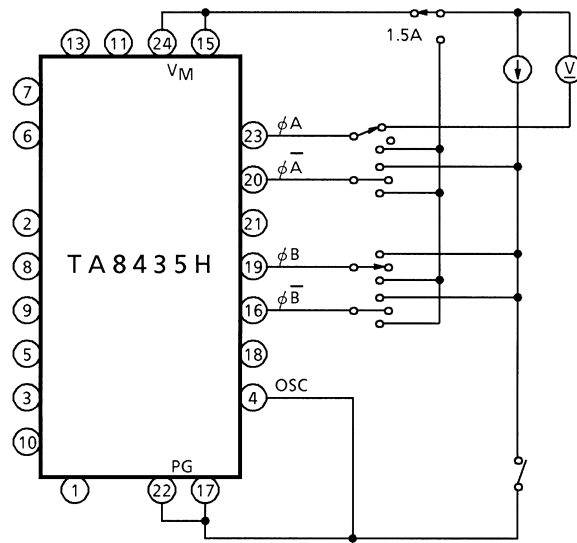
TEST CIRCUIT 4

$V_{CE(SAT)}$ UPPER SIDE, LOWER SIDE

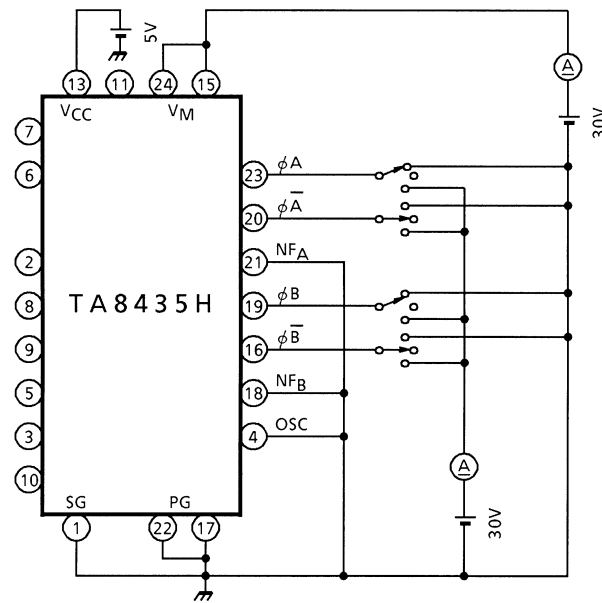


Note: Calibrate I_o to 1.5 A / 0.8 A by R_L

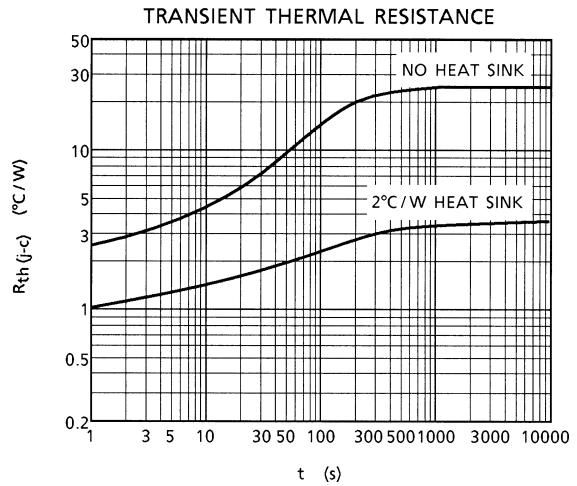
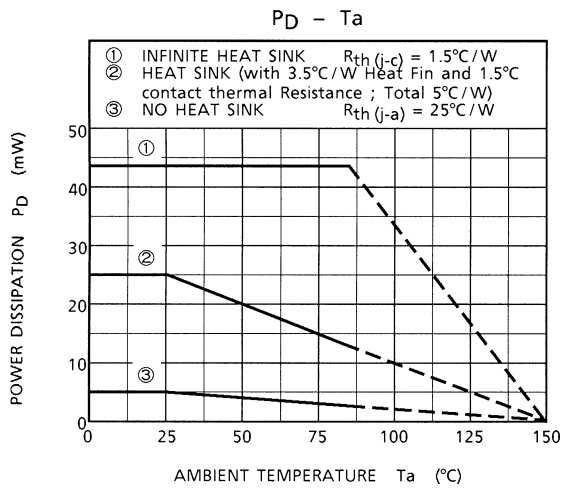
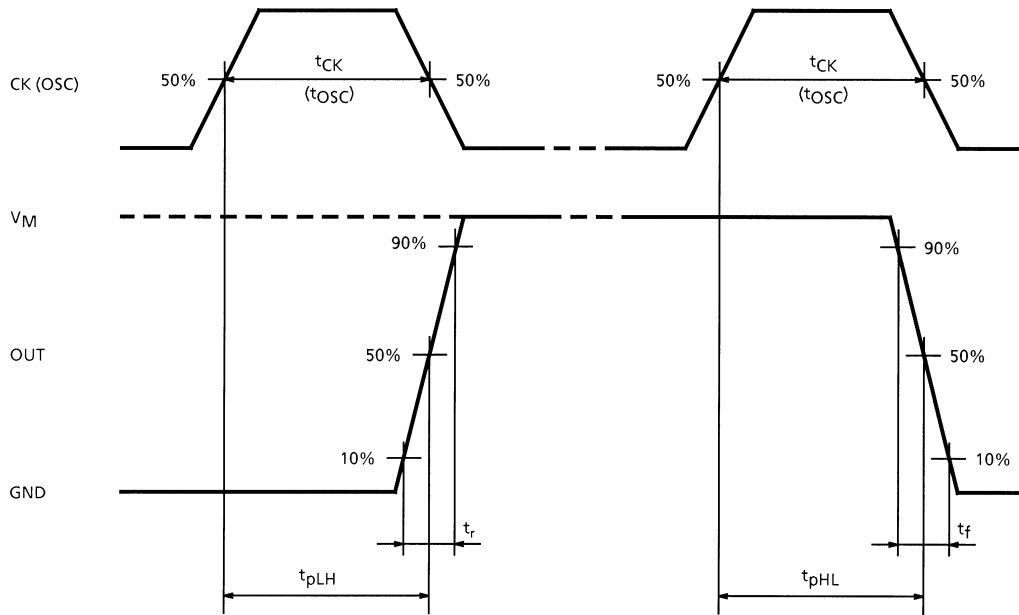
TEST CIRCUIT 5
 V_{FU} , V_{FL}



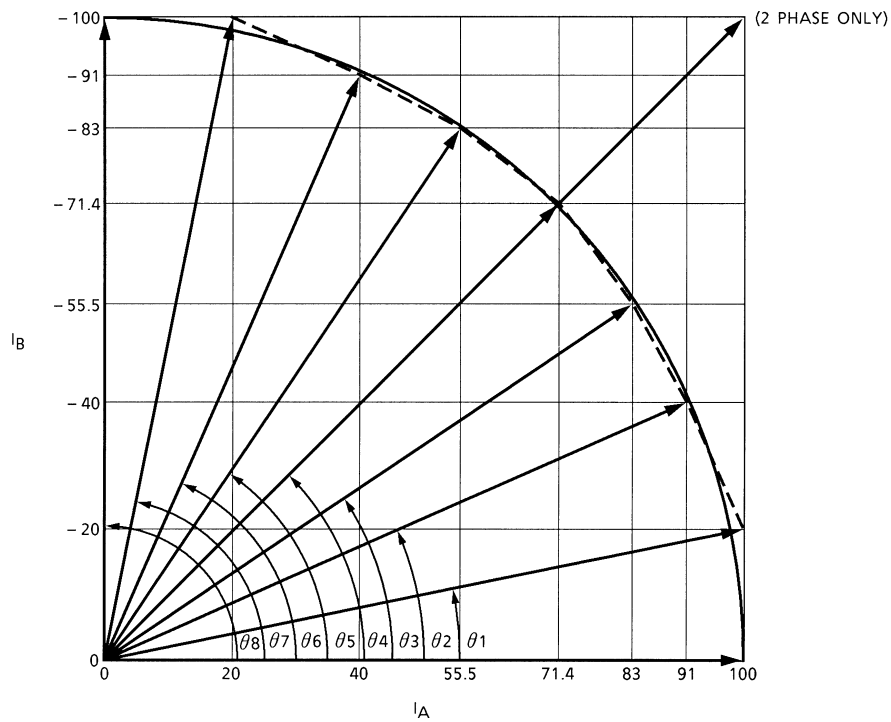
TEST CIRCUIT 6
 I_{OH} , I_{OL}



AC ELECTRICAL CHARACTERISTICS, MEASUREMENT WAVE CK (OSC)-OUT

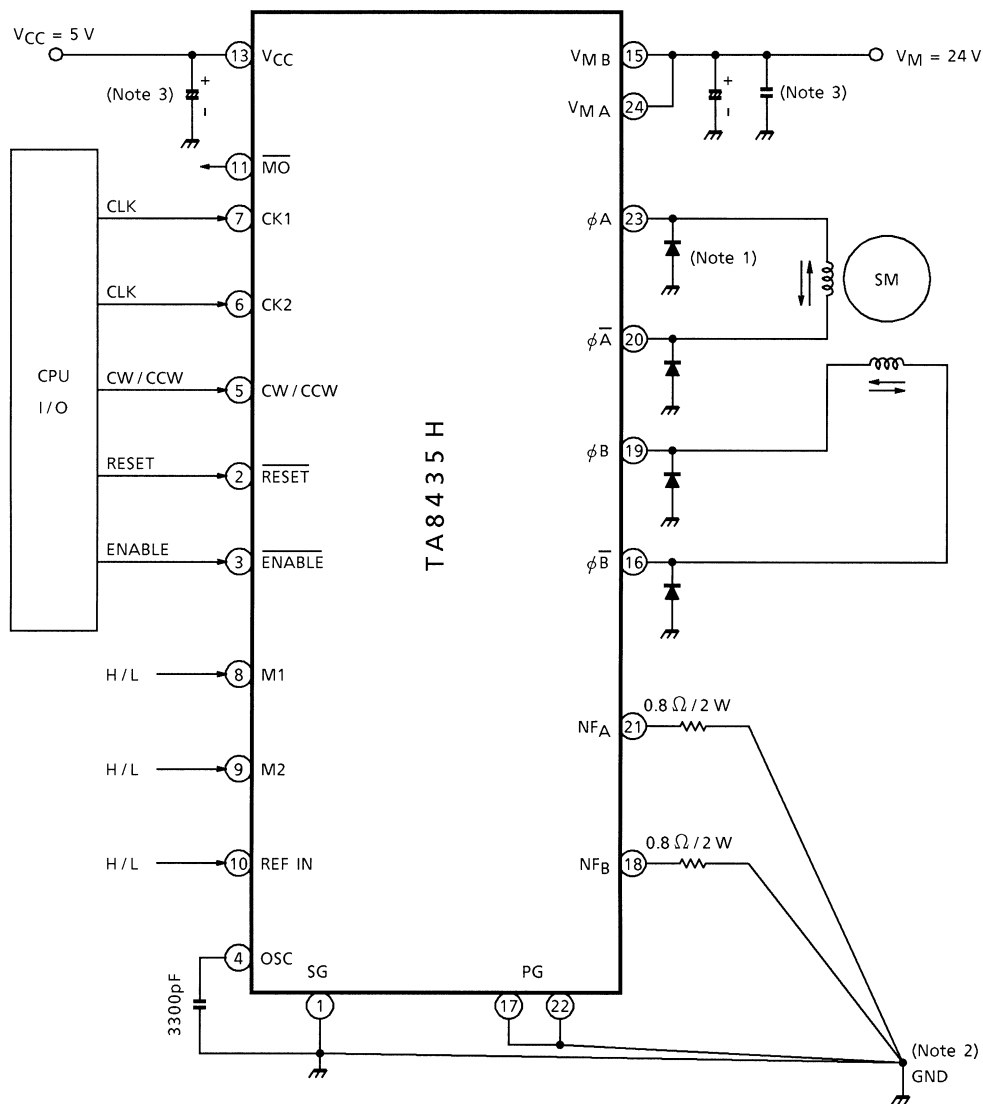


OUTPUT CURRENT VECTOR ORBIT (Normalize to 90° for each one step)



θ	ROTATION ANGLE		VECTOR LENGTH		
	IDEAL	TA8435H	IDEAL	TA8435H	
θ_0	0°	0°	100	100.00	—
θ_1	11.25°	11.31°	100	101.98	—
θ_2	22.5°	23.73°	100	99.40	—
θ_3	33.75°	33.77°	100	99.85	—
θ_4	45°	45°	100	100.97	141.42
θ_5	56.25°	56.23°	100	99.85	—
θ_6	67.5°	66.27°	100	99.40	—
θ_7	78.75°	78.69°	100	101.98	—
θ_8	90°	90°	100	100.00	—
				1-2 / W1-2 / 2W1-2 Phase	2 Phase

APPLICATION CIRCUIT



Note 1: Schottky diode (3GWJ42) to be connected additionally between each output (pin 16 / 19 / 20 / 23) and GND for preventing Punch-Through Current

Note 2: GND pattern to be laid out at one point in order to prevent common impedance.

Note 3: Capacitor for noise suppression to be connected between the Power Supply (V_{CC} , V_M) and GND to stabilize the operation.

Note 4: Utmost care is necessary in the design of the output line, V_M and GND line since IC may be destroyed due to short-circuit between outputs, air contamination fault, or fault by improper grounding.

When using TA8435H

0. Introduction

The TA8435H controls PWM to set the stepping motor winding current to constant current. The device is a micro-step driver IC used to efficiently drive the stepping motor at low vibration.

1. About micro-step drive

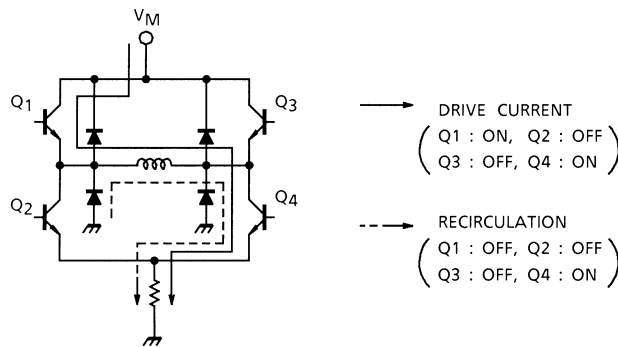
The TA8435H drives a stepping motor in micro steps with a maximum resolution of 1 / 8 of the 2-phase stepping angle (in 2W1-2 phase mode).

In micro steps, A-phase and B-phase current levels are set inside the IC so that the composite vector size and the rotation angle are even. Just inputting clock signals rotates the stepping motor in micro steps.

2. About PWM control and output current setting

(1) Output current path (PWM control)

The TA8435H controls PWM by turning the upper power transistor on / off.
In such a case, current flows as shown in the figure below.



(2) Setting of output current by REF-IN input and current detection resistor

The motor current (maximum current for micro-step drive) I_O is set as shown in the following equation, using REF-IN input and the external current detection resistor RNF.

$$I_O = V_{REF} / R_{NF}$$

where,

$$\text{REF - IN} = \text{High}, \quad V_{REF} = 0.8 \text{ V}$$

$$\text{REF - IN} = \text{Low}, \quad V_{REF} = 0.5 \text{ V}$$

3. Logic control

(1) Clock input for rotation direction control

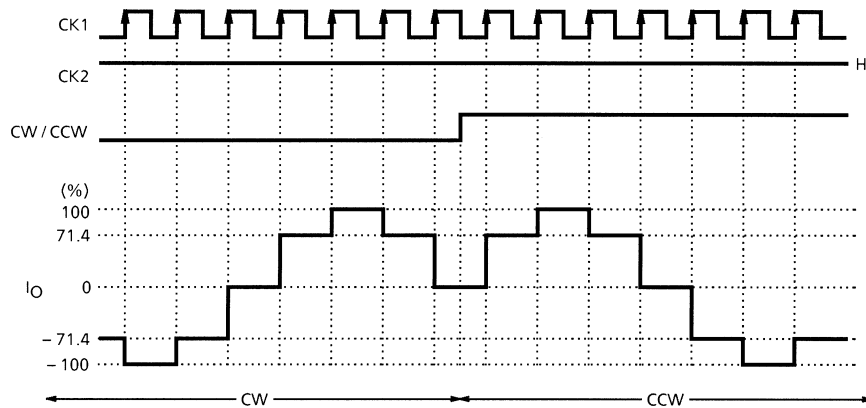
To switch rotation between forward and reverse, there are two clock input types: 1-clock input and 2-clock input.

(a) 1-clock input

Uses either clock pin CK1 or CK2.

Switches rotation between forward or reverse using the CW or CCW signal.

<Input signal example: 1-2 phase mode>

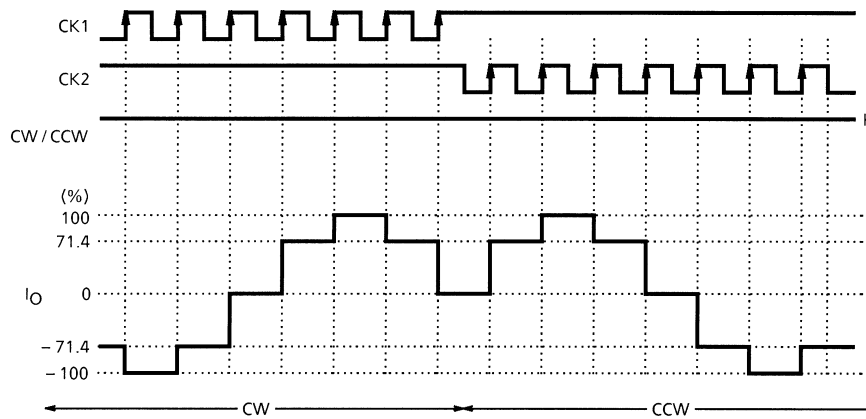


(b) 2-clock input

Uses both clock pins CK1 and CK2.

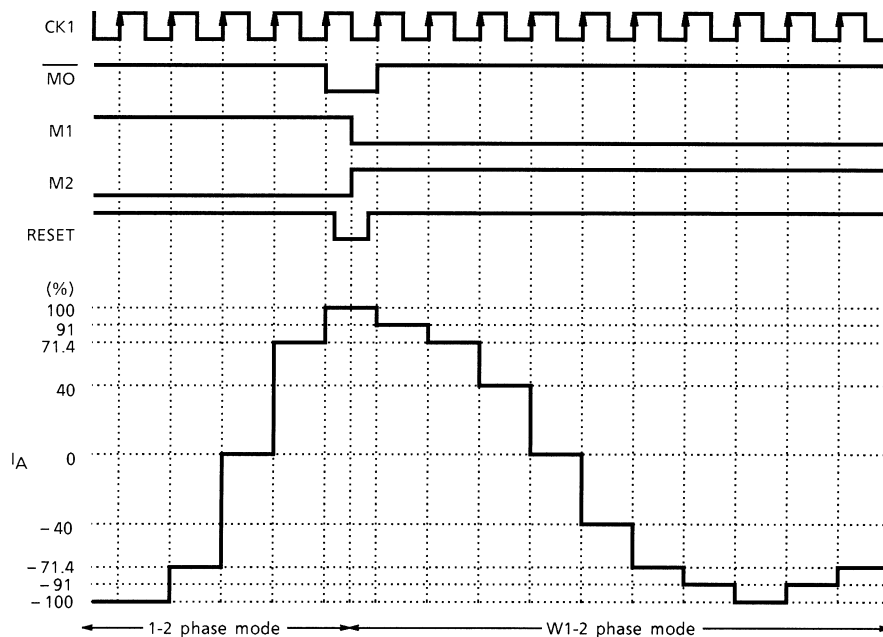
Switching between CK1 and CK2 controls forward / reverse rotation.

<Input signal example: 1-2 phase mode>



- (2) Mode setting
Setting M1 and M2 selects one of the following modes: 2-phase, 1-2 phase, W1-2 phase, and 2W1-2 phase modes.
- (3) Monitor (\overline{MO}) output
Supports the monitor output used to monitor the current waveform location.
For 2-phase mode, \overline{MO} output is Low at the timing of A-phase current = 100% and B-phase current = -100%.
For 1-2 phase, W1-2 phase, or 2W1-2 phase mode, \overline{MO} output is Low at the timing of A-phase current = 100% and B-phase current = 0%.
- (4) Reset pin
Supports reset input used to reset the internal counter.
Setting RESET to Low resets the internal counter, forcing the output current to the same value as that when the \overline{MO} output is Low.
- (5) Phase mode switching
To avoid the step changing during motor rotation, current must not fluctuate at phase mode switching. Pay attention to the following points.
 - (a) When switching between 2-phase and other phase modes, current fluctuates.
 - (b) When switching between phase modes other than 2-phase, current can be switched without fluctuation at the timing of \overline{MO} output = Low.
However, when switching as follows, set RESET to Low beforehand:
From 1-2 phase to W1-2 phase or 2W1-2 phase mode
From W1-2 phase to 2W1-2 phase mode

<Example of Input Signal>



4. About PWM oscillation frequency (external capacitor setting)

An external capacitor connected to the OSC pin is used to internally generate a sawtooth waveform. PWM is controlled using this frequency. Toshiba recommend 3300 pF for the capacitance by taking variation between ICs into consideration.

5. About external Schottky diode

A parasitic diode is created on the lower side of the output. When PWM is controlled, current flows to the parasitic diode. This current results in a punch-through current and micro-step waveform fluctuation. Therefore, make sure to externally connect a Schottky barrier diode. The external diode can reduce heat generated in the IC.

6. Power dissipation

The IC power dissipation is determined by the following equation (In a case where shottky diode is connected between Output pin and GND):

$$P = V_{CC} \times I_{CC} + V_M \times I_M + I_O (t_{ON} \times V_{SAT-U} + V_{SAT-L})$$
$$t_{ON} = T_{ON} / T_S \text{ (PWM control ON duty)}$$

The higher the ambient temperature, the smaller the power dissipation. Check the PD-Ta curve and design heat dissipation with a sufficient margin.

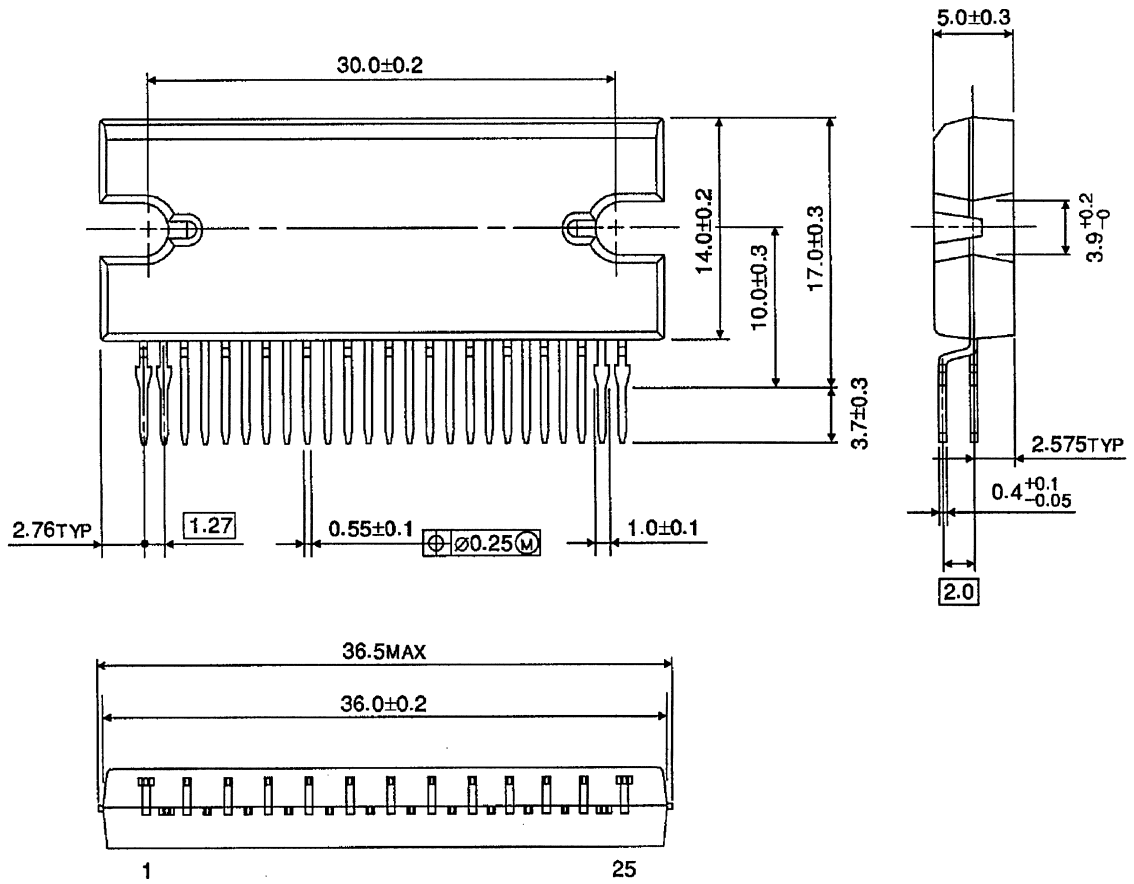
7. About heatsink fin processing

The IC fin (rear) is electrically connected to the rear of the chip. When current flows to the fin, the IC malfunctions. If there is any possibility of a voltage being generated between the IC GND and the fin, either ground the fin or insulate it.

OUTLINE DRAWING

HZIP25-P-1.27

Unit: mm



Weight: 9.86 g (Typ.)