# SY89838U

## Precision 1:8 LVDS Clock Fanout Buffer with 2:1 Runt Pulse Eliminator Input MUX (Precision Edge®)

### Features

- Selects between Two Clocks, and Provides 8 Precision, Low Skew LVDS Output Copies
- 2:1 MUX Input Provides a Glitch-free, Stable LVDS Output
- Guaranteed AC Performance Overtemperature and Supply Voltage:
  - Wide Operating Frequency: 1 kHz to >1.5 GHz
  - <150 ps $t_r/t_f$
  - <40 ps Output-to-Output Skew
- Unique Patent-pending Input Isolation Design Minimizes Crosstalk
- Fail-safe Input Prevents Oscillation
- Ultra-low Jitter Design:
  - 150 $fs_{RMS}$ Phase Jitter
  - <0.7 $ps_{RMS}$ MUX Crosstalk Induced Jitter
- Unique Patent-pending Input Termination and VT Pin Accepts DC- and AC-coupled Inputs (CML, PECL, LVDS)
- 350 mV LVDS Output Swing
- Power Supply 2.5V ±5%
- –40°C to +85°C Industrial Temperature Range
- Available in 32-lead (5 mm × 5 mm) VQFN Package

### Applications

- Redundant Clock Switchover
- Failsafe Clock Protection

### Markets

- LAN/WAN
- Enterprise Servers
- ATE
- Test and Measurements

### General Description

The SY89838U is a low jitter, low skew, high-speed 1:8 fanout buffer with a unique, 2:1 differential input multiplexer (MUX) optimized for redundant source switchover applications. Unlike standard multiplexers, the SY89838U's unique 2:1 Runt Pulse Eliminator (RPE) MUX prevents any short cycles or "runt" pulses during switchover.

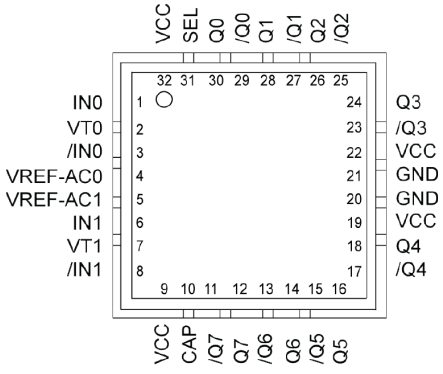
In addition, a unique fail-safe input protection prevents metastable conditions when the selected input clock fails to a DC voltage (between the pins of the differential input drops below 200 mV). The SY89838U distributes clock frequencies from 1 kHz to 1.5 GHz, guaranteed, over temperature and voltage.

The differential input includes Microchip's unique, 3-lead input termination architecture that allows customers to interface to any differential signal (AC- or DC-coupled) as small as 200 mV (400 $Mv_{PP}$) without any level shifting or termination resistor networks in the signal path. The outputs are 350 mV compatible LVDS with fast rise/fall times guaranteed to be less than 150 ps.

The SY89838U operates from a 2.5V ±5% supply and is guaranteed over the full industrial temperature range of –40°C to +85°C. For applications that require 800 mV LVPECL outputs, consider the SY89837U. The SY89838U is part of Microchip's high-speed, Precision Edge® product line.

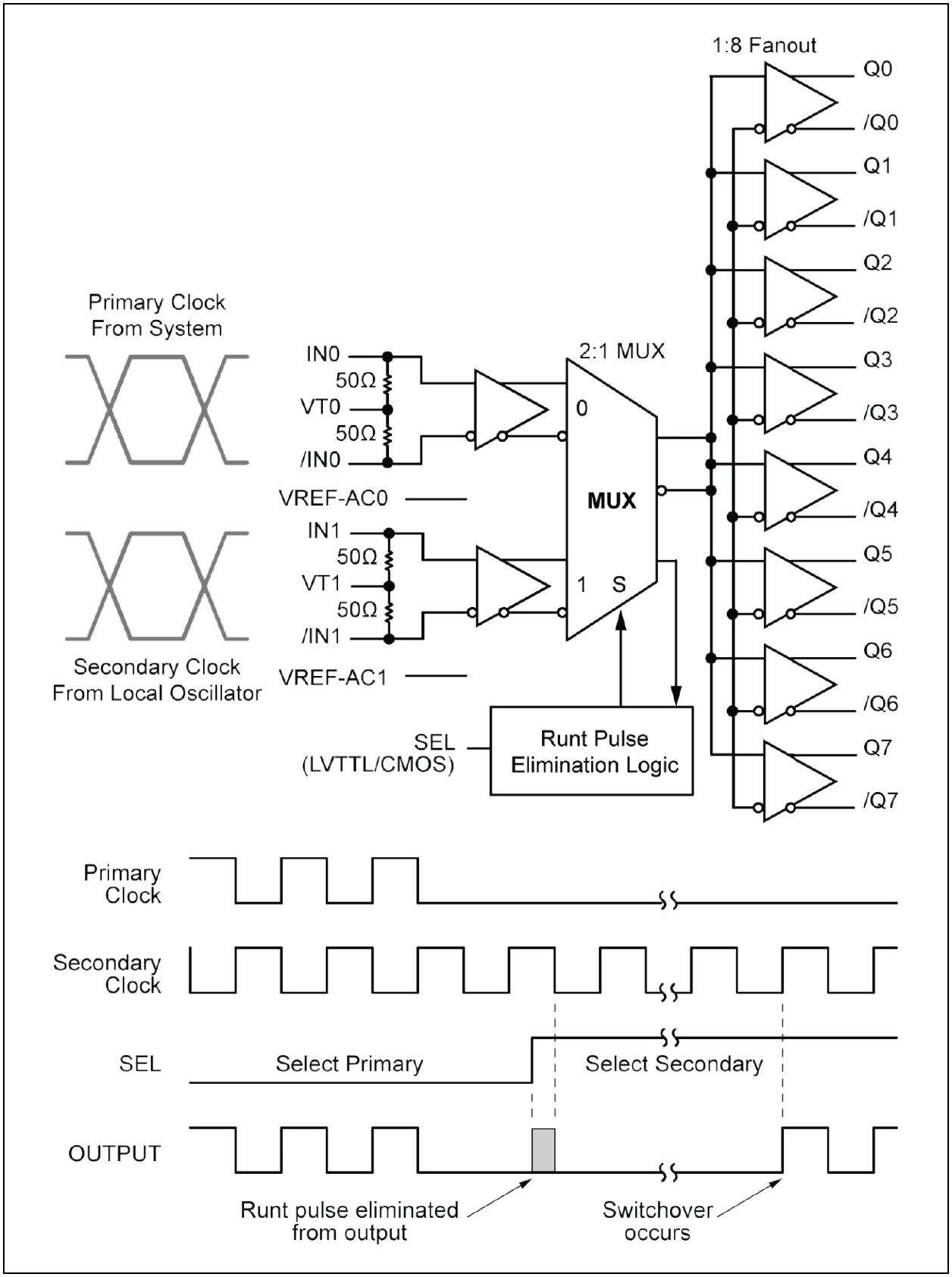
### Package Type

**SY89838U**
32-Lead VQFN




**32-Pin QFN**

### Typical Application



# 1.0 |ELECTRICAL CHARACTERISTICS

## Absolute Maximum Ratings†

Supply Voltage ($V_{CC}$) ..... –0.5V to +4.0V
Input Voltage ($V_{IN}$) ..... –0.5V to $V_{CC}$
Input Current ($V_T$), Source or sink current on IN, /IN ..... ±50 mA
Termination Current, Source or sink current on $V_T$ ..... ±100 mA
$V_{REF-AC}$ source or sink current ..... ±2 mA

## Operating Ratings††

Supply Voltage ($V_{CC}$) ..... +2.375V to +2.625V

**† Notice:** Permanent device damage may occur if absolute maximum ratings are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**†† Notice:** The data sheet limits are not guaranteed if the device is operated beyond the operating ratings.

**TABLE 1-1: DC ELECTRICAL CHARACTERISTICS**

| All values applicable for when $T_A$ = –40°C to +85°C unless otherwise stated. (Note 1) | | | | | | |
|---|---|---|---|---|---|---|
| **Parameter** | **Symbol** | **Min.** | **Typ.** | **Max.** | **Units** | **Conditions** |
| Power Supply Voltage | $V_{CC}$ | 2.375 | 2.5 | 2.625 | V | — |
| Power Supply Current | $I_{CC}$ | — | 250 | 350 | mA | No load, max. $V_{CC}$ |
| Input Resistance (IN-to-VT) | $R_{IN}$ | 45 | 50 | 55 | Ω | — |
| Differential Input Resistance (IN-to-/IN) | $R_{DIFF\_IN}$ | 90 | 100 | 110 | Ω | — |
| Input High Voltage (IN, /IN) | $V_{IH}$ | 1.2 | — | $V_{CC}$ | V | — |
| Input Low Voltage (IN, /IN) | $V_{IL}$ | 0 | — | $V_{IH}$ – 0.2 | V | — |
| Input Voltage Swing (IN, /IN) | $V_{IN}$ | 0.2 | — | $V_{CC}$ | V | See Figure 6-1 and Note 2 |
| Differential Input Voltage Swing \|IN-/IN\| | $V_{DIFF\_IN}$ | 0.4 | — | — | V | See Figure 6-2 |
| Input Voltage Threshold that Triggers FSI | $V_{IN\_FSI}$ | — | 30 | 100 | mV | — |
| IN-to-VT (IN, /IN) | $V_{T\_IN}$ | — | — | 1.8 | V | — |
| Output Reference Voltage | $V_{REF-AC}$ | $V_{CC}$ – 1.3 | $V_{CC}$ – 1.2 | $V_{CC}$ – 1.1 | V | — |

**Note 1:** The circuit is designed to meet the DC specifications shown in this table after thermal equilibrium has been established.

**2:** $V_{IN}$ (max) is specified when VT pin is floating.

**TABLE 1-2: LVDS OUTPUTS DC ELECTRICAL CHARACTERISTICS**

| $V_{CC}$ = 2.5V ±5%; $T_A$ = –40°C to +85°C; $R_L$ = 100Ω across output pair, or equivalent, unless otherwise stated. (Note 1) | | | | | | |
|---|---|---|---|---|---|---|
| **Parameter** | **Symbol** | **Min.** | **Typ.** | **Max.** | **Units** | **Conditions** |
| Output Voltage Swing (Q, /Q) | $V_{OUT}$ | 250 | 325 | — | mV | See Figure 6-1 and Figure 9-1 |
| Output Output Voltage Swing \|Q - /Q\| | $V_{DIFF-OUT}$ | 500 | 650 | — | mV | See Figure 6-2 |
| Output Common Mode Voltage | $V_{OCM}$ | 1.125 | — | 1.275 | V | See Figure 9-2 |
| Change in Common Mode Voltage | $\Delta V_{OCM}$ | –50 | — | +50 | mV | See Figure 9-2 |

**Note 1:** High-frequency AC-parameters are guaranteed by design and characterization.

**TABLE 1-3: LVTTL/CMOS DC ELECTRICAL CHARACTERISTICS**

| $V_{CC}$ = 2.5V ±5%; $T_A$ = –40°C to +85°C, unless otherwise stated. (Note 1) | | | | | | |
|---|---|---|---|---|---|---|
| **Parameter** | **Symbol** | **Min.** | **Typ.** | **Max.** | **Units** | **Conditions** |
| Input HIGH Voltage | $V_{IH}$ | 2.0 | — | — | V | — |
| Input LOW Voltage | $V_{IL}$ | — | — | 0.8 | V | — |
| Input HIGH Current | $I_{IH}$ | –125 | — | 30 | µA | — |
| Input LOW Current | $I_{IL}$ | –300 | — | — | µA | — |

**Note 1:** High-frequency AC-parameters are guaranteed by design and characterization.

**TABLE 1-4: AC ELECTRICAL CHARACTERISTICS**

| $V_{CC}$ = 2.5V ±5%; $T_A$ = –40°C to + 85°C, RPE enabled, Input $t_r/t_f$ ≤ 600 ps (20% to 80%), $R_L$ = 100Ω, unless otherwise noted. (Note 1) | | | | | | |
|---|---|---|---|---|---|---|
| **Parameter** | **Symbol** | **Min.** | **Typ.** | **Max.** | **Units** | **Conditions** |
| Maximum Operating Frequency | $f_{MAX}$ | 1.5 | 2.0 | | GHz | RPE enabled |
| Differential Propagation Delay, IN-to-Q | $t_{pd}$ | 500 | 700 | 950 | ps | $V_{IN}$ ≥ 250 mV, see Note 2 |
| Differential Propagation Delay, SEL-to-Q | | | | 17 | cycles | RPE enabled—see Timing Diagram |
| Differential Propagation Delay, SEL-to-Q | | | | 1000 | ps | RPE disabled ($V_{IN}$ = $V_{CC}$/2) |
| Differential Propagation Delay Temperature Coefficient | $t_{pd\_tempco}$ | | 115 | | fs/°C | — |
| Output-to-output Skew | $t_{SKEW}$ | | 20 | 40 | ps | See Note 3 |
| Part-to-part Skew | | | | 200 | ps | See Note 4 |
| RMS Phase Jitter | $t_{JITTER}$ | | 150 | | fs | Output = 622 MHz, Integration Range 12 kHz–20 MHz. |
| Crosstalk-induced Jitter | | | | 0.7 | $ps_{RMS}$ | See Note 5 |
| Output Rise/Fall Time (20% to 80%) | $t_r$, $t_f$ | 40 | 80 | 150 | ps | At full output swing |

**Note 1:** High-frequency AC-parameters are guaranteed by design and characterization.

**2:** Propagation delay is a function of rise and fall time at IN. See “Typical Operating Characteristics” for more details.

**3:** Output-to-output skew is measured between two different outputs under identical transitions.

**4:** Part-to-part skew is defined for two parts with identical power supply voltages at the same temperature and with no skew of the edges at the respective inputs.

**5:** Crosstalk is measured at the output while applying two similar differential clock frequencies that are asynchronous with respect to each other at the inputs.

**TABLE 1-5: TEMPERATURE SPECIFICATIONS**

| **Parameter** | **Symbol** | **Min.** | **Typ.** | **Max.** | **Units** | **Conditions** |
|---|---|---|---|---|---|---|
| **Temperature Range** | | | | | | |
| Operating Temperature | $T_A$ | –40 | — | +85 | °C | — |
| Lead Temperature | $T_{LEAD}$ | — | +260 | — | °C | Soldering, 20 sec. |
| Storage Temperature | $T_S$ | –65 | — | +150 | °C | — |
| **Package Thermal Resistance** (Note 1) | | | | | | |
| 32-Lead VQFN, Still Air | $\theta_{JA}$ | — | +35 | — | °C/W | — |
| 32-Lead VQFN, Junction-to-Board | $\Psi_{JB}$ | — | +16 | — | °C/W | — |

**Note 1:** Package thermal resistance assumes the exposed pad is soldered (or equivalent) to the device’s most negative potential on the PCB. The $\theta_{JA}$ and $\Psi_{JB}$ values are determined for a 4-layer board in still-air, unless otherwise stated.

## 2.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 2-1.

**TABLE 2-1: PIN FUNCTION TABLE**

| Pin Number | Pin Name | Description |
|---|---|---|
| 1, 3, 6, 8 | IN0, /IN0, IN1, /IN1 | **Differential Inputs:** These input pairs are the differential signal inputs to the device. These inputs accept AC or DC-coupled signals as small as 100 mV (200 $mV_{PP}$). Each pin of a pair internally terminates to a VT pin through 50Ω. Please refer to Section 8.0, Input Interface Applications for more details. |
| 2, 7 | VT0, VT1 | **Input Termination Center-Tap:** Each side of the differential input pair terminates to a VT pin. The VT0 and VT1 pins provide a center-tap to a termination network for maximum interface flexibility. See Section 8.0, Input Interface Applications for more details. |
| 31 | SEL | This single-ended TTL/CMOS-compatible input selects the inputs to the multiplexer. Note that this input is internally connected to a 25 kΩ pull-up resistor and will default to a logic HIGH state if left open. Input threshold is VCC/2. |
| 9, 19, 22, 32 | VCC | **Positive Power Supply:** Bypass with 0.1 µF//0.01 µF low ESR capacitors as close to VCC pins as possible. |
| 30, 28, 26, 24, 18, 16, 14, 12, 29, 27, 25, 23, 17, 15, 13, 11 | Q0–Q7, /Q0–/Q7 | **Differential Outputs:** These LVDS output pairs are a logic function of the IN0, IN1, and SEL inputs. Please refer to the truth table below for details. Unused output pairs must be terminated with 100Ω across the pair. |
| 20, 21 | GND, Exposed Pad | **Ground:** Ground pin and exposed pad must be connected to the same ground plane. |
| 10 | CAP | **Power-On Reset (POR) Initialization capacitor.** When using the multiplexer with RPE capability, this pin is tied to a capacitor to VCC. The purpose is to ensure the internal RPE logic starts up in a known state. See “Power-On Rest (POR) Description” section for more details regarding capacitor selection. If this pin is tied directly to VCC, the RPE function will be disabled and the multiplexer will function as a normal multiplexer. The CAP pin should never be left open. |
| 4, 5 | VREF-AC0, VREF-AC1 | **Reference Voltage:** These outputs bias to VCC–1.2V. They are used for AC-coupling inputs (IN, /IN). Connect VREF_AC directly to the VT pin. Bypass with 0.01µF low ESR capacitor to VCC. See “Input Interface Applications” section. Maximum sink/source current is ±1.5mA. |

**TABLE 2-2: TRUTH TABLE**

| Inputs | | | | | Outputs | |
|---|---|---|---|---|---|---|
| **IN0** | **/IN0** | **IN1** | **/IN1** | **SEL** | **Q** | **/Q** |
| 0 | 1 | X | X | 0 | 0 | 1 |
| 1 | 0 | X | X | 0 | 1 | 0 |
| X | X | 0 | 1 | 1 | 0 | 1 |
| X | X | 1 | 0 | 1 | 1 | 0 |

# 3.0 FUNCTIONAL DESCRIPTION

## 3.1 RPE MUX and Fail-Safe Input

The SY89838U is optimized for clock switchover applications where switching from one clock to another clock without runt pulses (short cycles) is required. It features two unique circuits:

### 3.1.1 RUNT-PULSE ELIMINATOR (RPE) CIRCUIT:

The RPE MUX provides a “glitchless” switchover between two clocks and prevents any runt pulses from occurring during the switchover transition. The design of both clock inputs is identical (i.e., the switchover sequence and protection is symmetrical for both input pair, IN0 or IN1. Thus, either input pair may be defined as the primary input). If not required, the RPE function can be permanently disabled to allow the switchover between inputs to occur immediately. If the CAP pin is tied directly to VCC, the RPE function will be disabled and the multiplexer will function as a normal multiplexer.

### 3.1.2 FAIL-SAFE INPUT (FSI) CIRCUIT:

The FSI function provides protection against a selected input pair that drops below the minimum amplitude requirement. If the selected input pair drops sufficiently below the 100 mV minimum single-ended input amplitude limit ($V_{IN}$), or 200 mV differentially ($V_{DIFF\_IN}$), the output will latch to the last valid clock state.

## 3.2 RPE and FSI Functionality

The basic operation of the RPE MUX and FSI functionality is described with the following four example descriptions. All descriptions are related to the true inputs and outputs. The primary (or selected) clock is called CLK1; the secondary (or alternate) clock is called CLK2.

Due to the totally asynchronous relation of the IN and SEL signals and an additional internal protection against metastability, the number of pulses required for the operations described in Example 3-1, Example 3-2, Example 3-3, and Example 3-4 can vary within certain limits. Refer to “Timing Diagrams” for more detailed information.

### EXAMPLE 3-1: TWO NORMAL CLOCKS AND RPE ENABLED

In this case the frequency difference between the two running clocks IN0 and IN1 must not be greater than 1.5:1. For example, if the IN0 clock is 500 MHz, the IN1 clock must be within the range of 334 MHz to 750 MHz.

If the SEL input changes state to select the alternate clock, the switchover from CLK1 to CLK2 will occur in three stages.

1. The output will continue to follow CLK1 for a limited number of pulses.
2. The output will remain LOW for a limited number of pulses of CLK2.
3. The output follows CLK2.

See Figure 3-1.

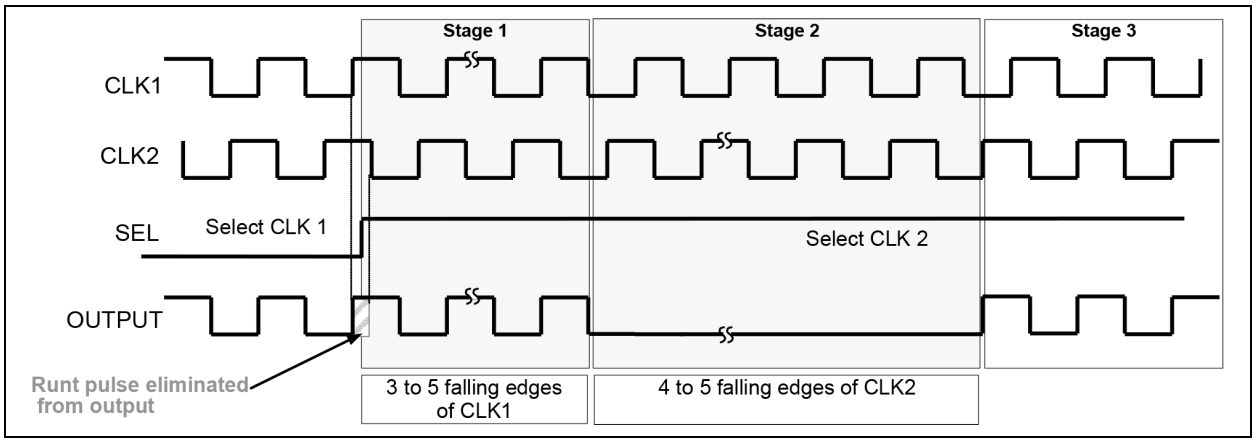



**FIGURE 3-1: CLK1 TO CLK2 SWITCHOVER WHEN SEL INPUT CHANGES TO ALTERNATE CLOCK BETWEEN TWO NORMAL CLOCKS WHERE RPE IS ENABLED AND FREQUENCY DIFFERENCE IS <1.5:1.**

### EXAMPLE 3-2: INPUT CLOCK FAILURE: SWITCHING FROM A SELECTED CLOCK STUCK HIGH TO A VALID CLOCK (RPE ENABLED)

If CLK1 fails HIGH before the RPE MUX selects CLK2 (using the SEL pin), the switchover will occur in three stages.

1. The output will remain HIGH for a limited number of pulses of CLK2.
2. The output will switch to LOW and then remain LOW for a limited number of falling edges of CLK2.
3. The output will follow CLK2.

See Figure 3-2.

### EXAMPLE 3-3: INPUT CLOCK FAILURE: SWITCHING FROM A SELECTED CLOCK STUCK LOW TO A VALID CLOCK (RPE ENABLED)

If CLK1 fails LOW before the RPE MUX selects CLK2 (using the SEL pin), the switchover will occur in two stages.

1. The output will remain LOW for a limited number of falling edges of CLK2.
2. The output will follow CLK2.

See Figure 3-3.

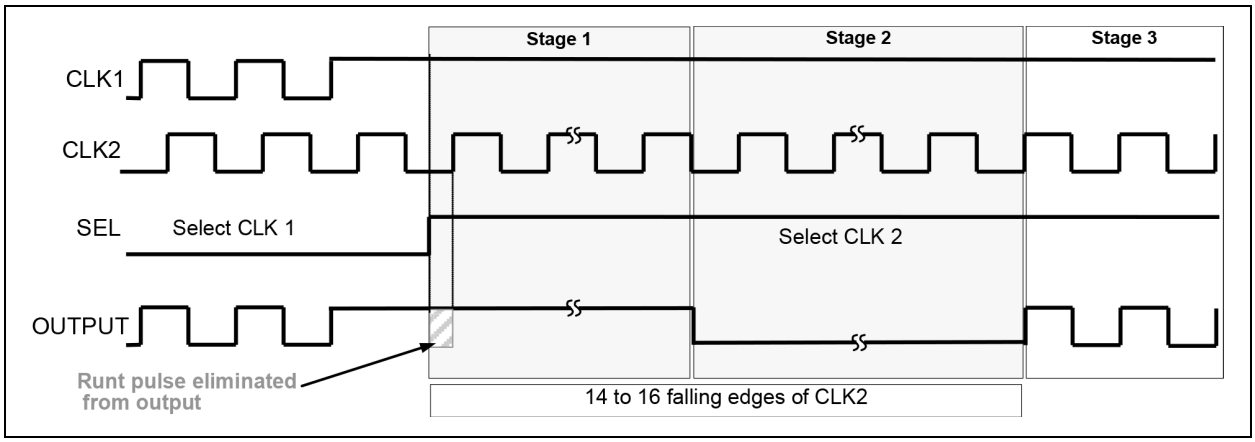



**FIGURE 3-2: SWITCHING FROM A SELECTED CLOCK STUCK HIGH TO A VALID CLOCK (RPE ENABLED).**

**Note:** In Figure 3-2, output shows extended clock cycle during switchover and pulse width for both high and low of this cycle will always be greater than 50% of the CLK2 period.

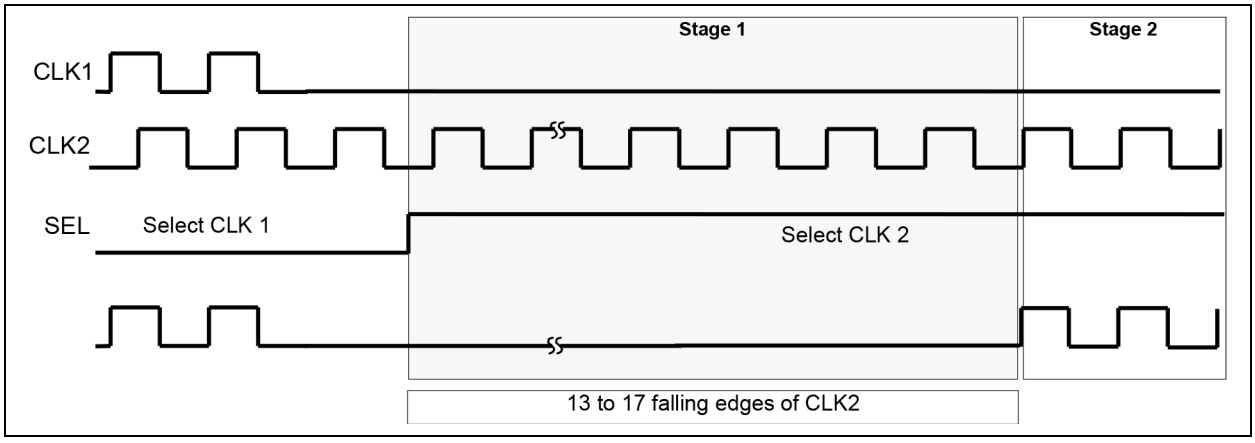



**FIGURE 3-3: SWITCHING FROM A SELECTED CLOCK STUCK LOW TO A VALID CLOCK (RPE ENABLED).**

**EXAMPLE 3-4: INPUT CLOCK FAILURE: SWITCHING FROM THE SELECTED CLOCK INPUT STUCK IN AN UNDETERMINED STATE TO A VALID CLOCK INPUT (RPE ENABLED)**

If CLK1 fails to an undetermined state (e.g., amplitude falls below the 100 mV [$V_{IN}$] minimum single-ended input limit, or 200 mV differentially) before the RPE MUX selects CLK2 (using the SEL pin), the switchover to the valid clock CLK2 will occur either following Example 3-2 or Example 3-3, depending on the last valid state at the CLK1.

If the selected input clock fails to a floating, static, or extremely low signal swing, including 0 mV, the FSI function will eliminate any metastable condition and guarantee a stable output signal. No ringing and no undetermined state will occur at the output under these conditions.

Please note that the FSI function will not prevent duty cycle distortions or runt pulses in case of a slowly deteriorating (but still toggling) input signal. Due to the FSI function, the propagation delay will depend on rise and fall time of the input signal and on its amplitude. Refer to Section 5.0, Typical Characteristics for more detailed information.

See also Figure 3-4.

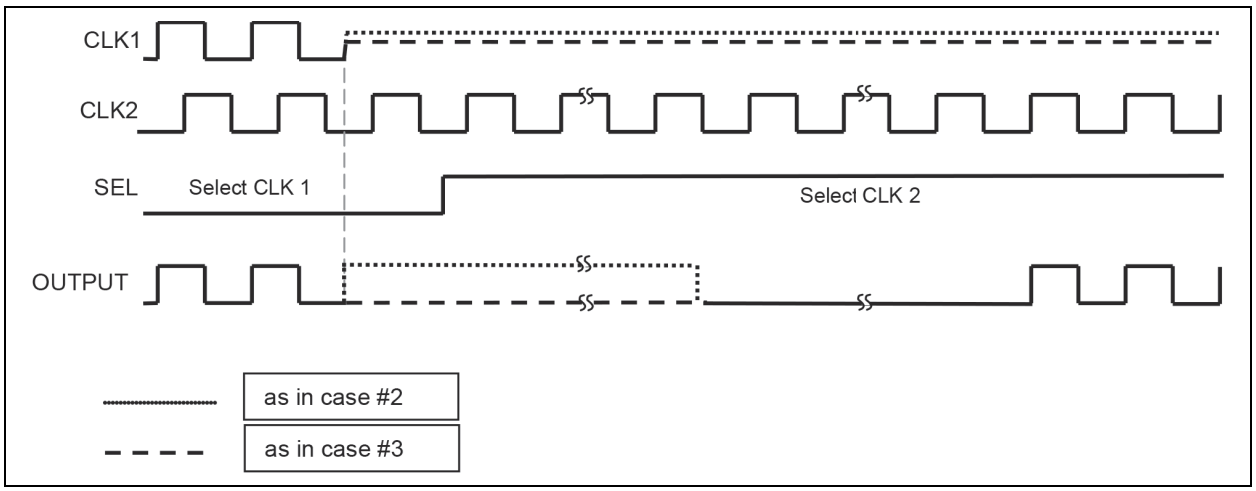



**FIGURE 3-4: SWITCHING FROM THE SELECTED CLOCK INPUT STUCK IN AN UNDETERMINED STATE TO A VALID CLOCK INPUT (RPE ENABLED).**

## 4.0 POWER-ON RESET (POR) DESCRIPTION

The SY89838U includes an internal power-on reset (POR) function to ensure the RPE logic starts-up in a known logic state once the power-supply voltage is stable.

An external capacitor connected between VCC and the CAP pin (pin 10) controls the delay for the power-on reset function.

Calculation of the required capacitor value is based on the time the system power supply needs to power up to a minimum of 2.3V.

The time constant for the internal power-on-reset must be greater than the time required for the power supply to ramp up to a minimum of 2.3V.

Equation 4-1 describes this relationship:

**EQUATION 4-1:**

$$C(\mu F) \geq \frac{t_{dPS}(ms)}{12(ms/\mu F)}$$

As an example, if the time required for the system power supply to power up past 2.3V is 12 ms, the required capacitor value on pin 10 would be as shown in Equation 4-2:

**EQUATION 4-2:**

$$C(\mu F) \geq \frac{12ms}{12(ms/\mu F)}$$
$$C(\mu F) \geq 1\mu F$$

## 5.0 TYPICAL CHARACTERISTICS

$V_{CC}$ = 2.5V; GND = 0V; $V_{IN} \geq 250\ mV_{pk}$, $t_r/t_f \leq 300$ ps, $R_L = 100\Omega$ across output pair; $T_A = 25°C$, unless otherwise stated.

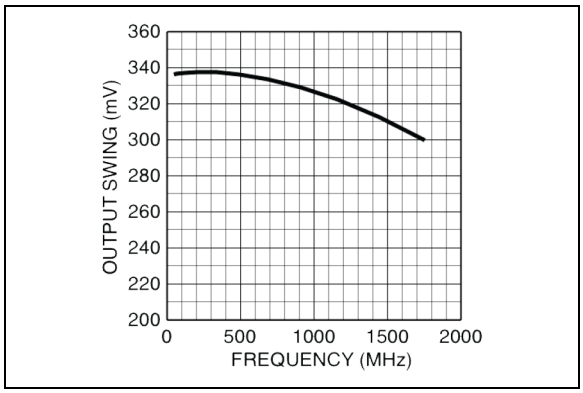



**FIGURE 5-1: OUTPUT SWING VS. FREQUENCY.**

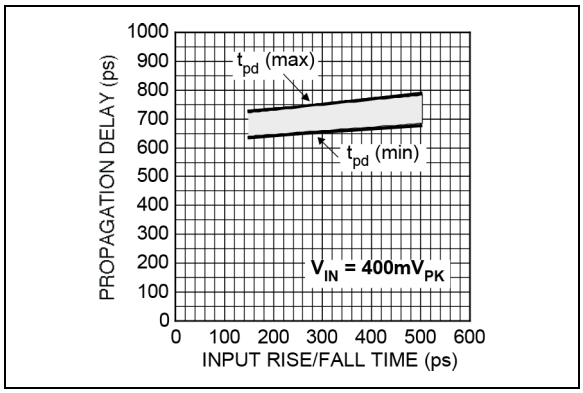



**FIGURE 5-3: PROPAGATION DELAY VARIATION VS. INPUT RISE/FALL TIME ($V_{IN}$ = 400 $MV_{PK}$).**

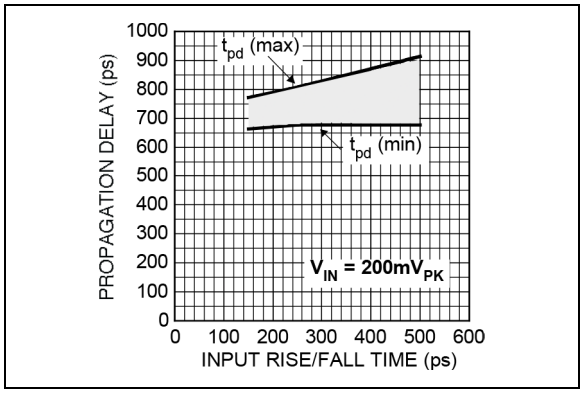



**FIGURE 5-2: PROPAGATION DELAY VARIATION VS. INPUT RISE/FALL TIME ($V_{IN}$ = 200 $MV_{PK}$).**

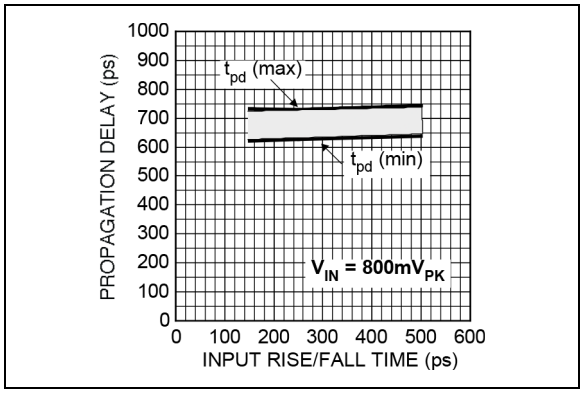



**FIGURE 5-4: PROPAGATION DELAY VARIATION VS. INPUT RISE/FALL TIME ($V_{IN}$ = 800 $MV_{PK}$).**

## 6.0 SINGLE-ENDED AND DIFFERENTIAL SWINGS

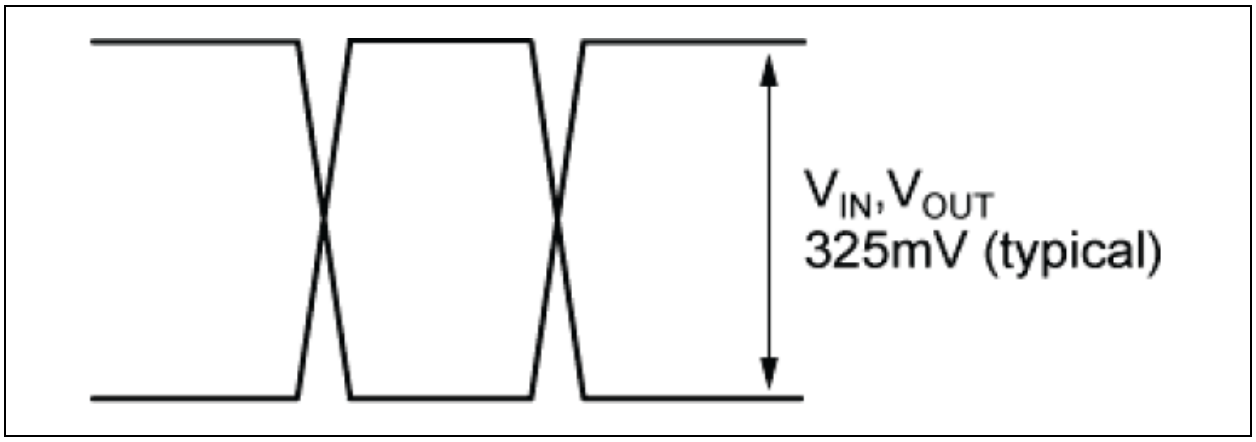



**FIGURE 6-1: SINGLE-ENDED VOLTAGE SWING.**

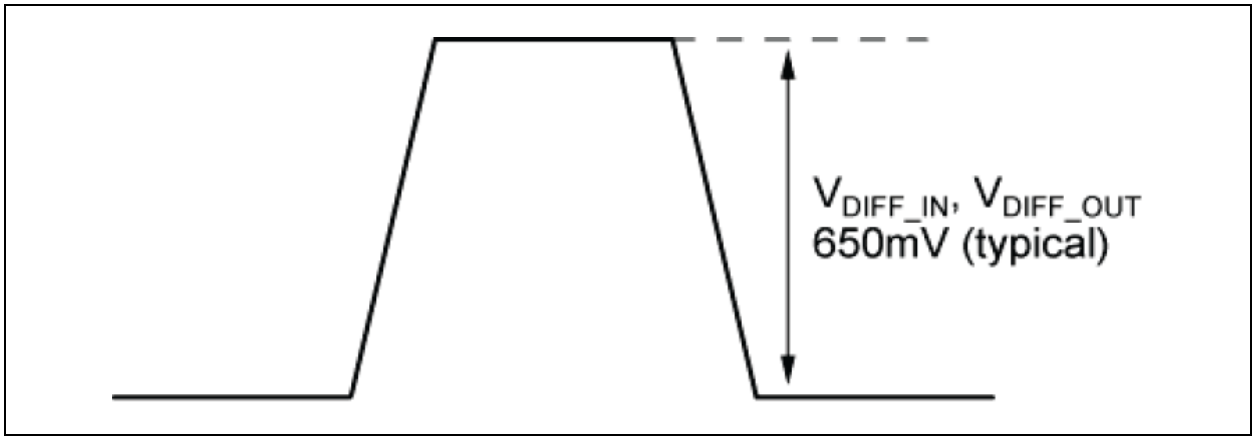



**FIGURE 6-2: DIFFERENTIAL VOLTAGE SWING.**

## 7.0 INPUT STAGE

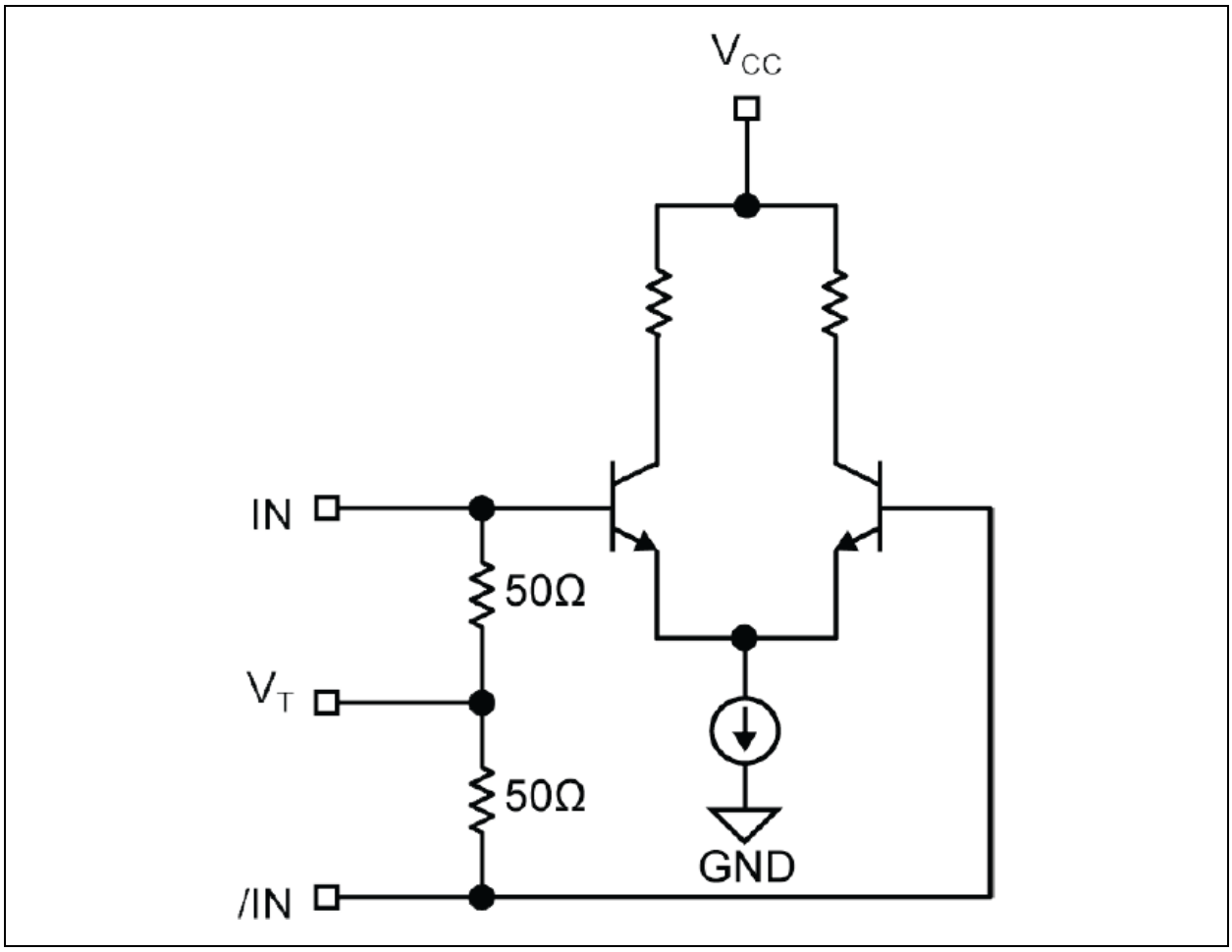



**FIGURE 7-1: SIMPLIFIED DIFFERENTIAL INPUT STAGE.**

## 8.0 INPUT INTERFACE APPLICATIONS

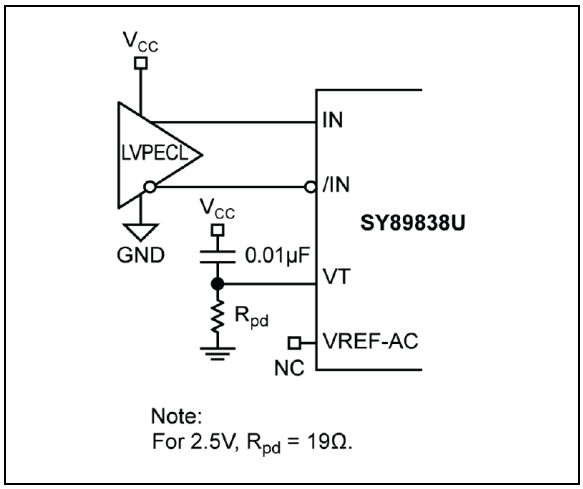



**FIGURE 8-1: DC-COUPLED LVPECL INPUT INTERFACE.**

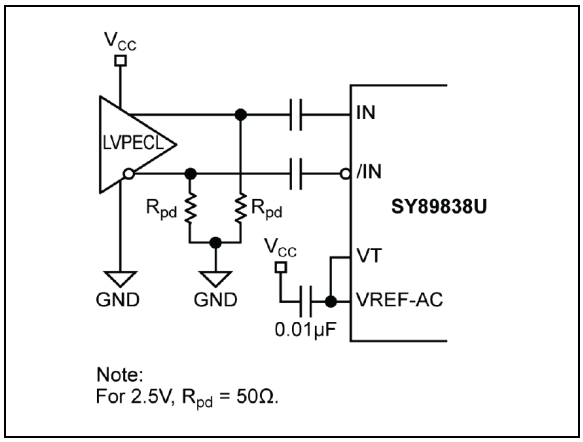



**FIGURE 8-2: AC-COUPLED LVPECL INPUT INTERFACE.**

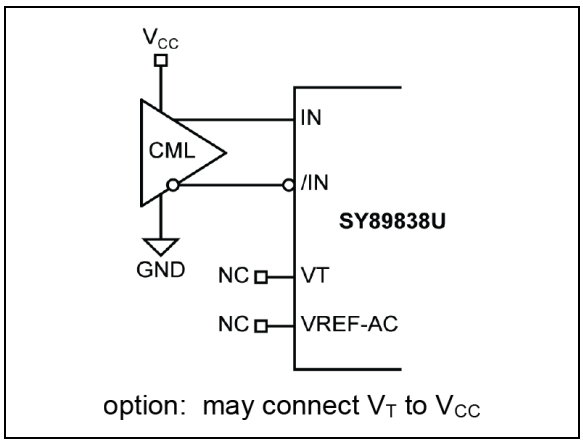



**FIGURE 8-3: DC-COUPLED CML INPUT INTERFACE.**

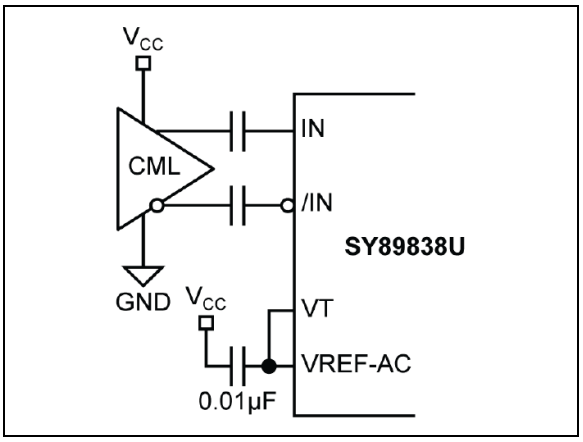



**FIGURE 8-4: AC-COUPLED CML INPUT INTERFACE.**

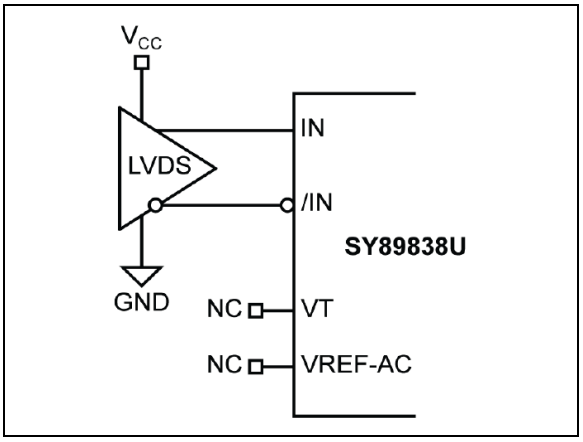



**FIGURE 8-5: DC-COUPLED LVDS INPUT INTERFACE.**

## 9.0 LVDS OUTPUT INTERFACE APPLICATIONS

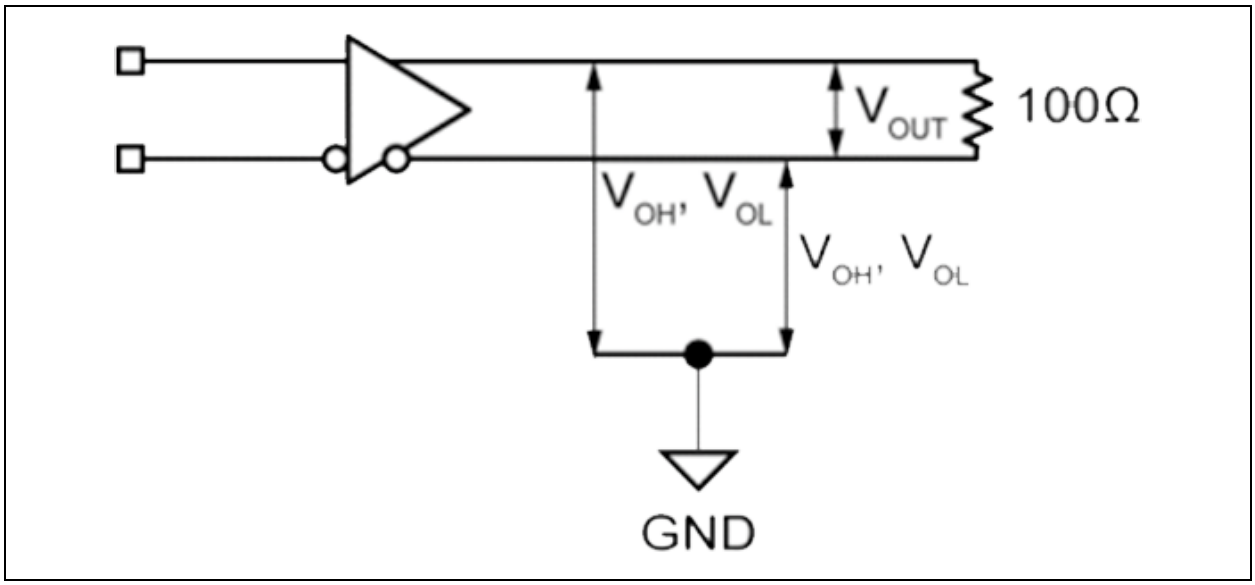



**FIGURE 9-1: LVDS DIFFERENTIAL MEASUREMENT.**

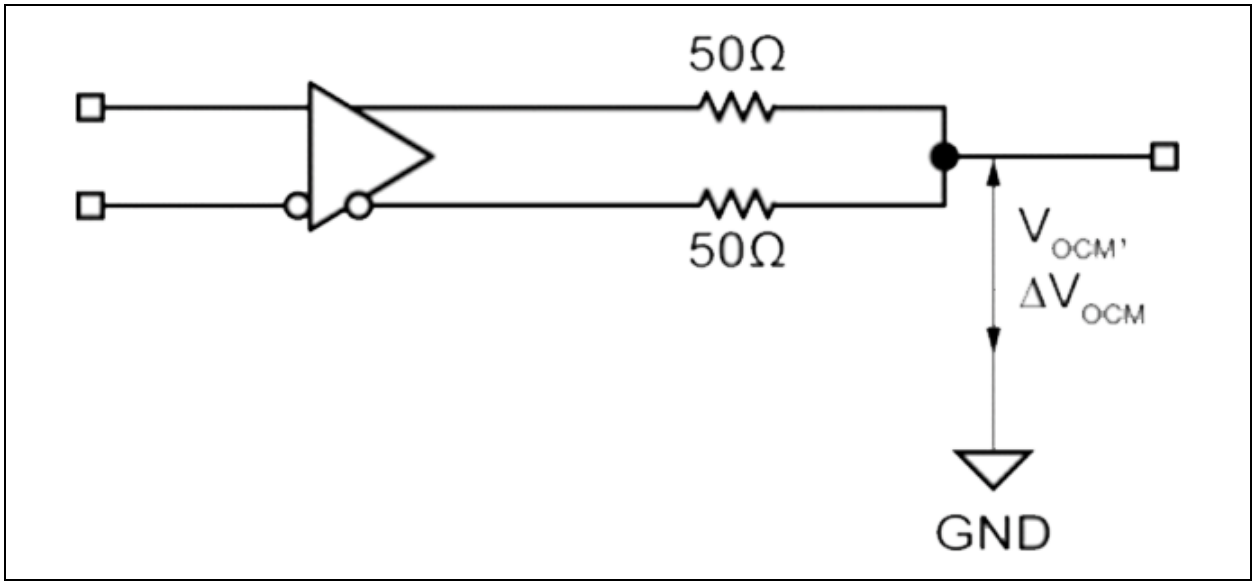
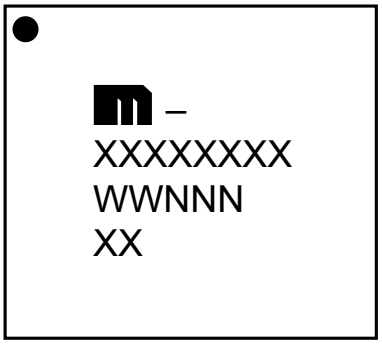



**FIGURE 9-2: LVDS COMMON MODE MEASUREMENT.**

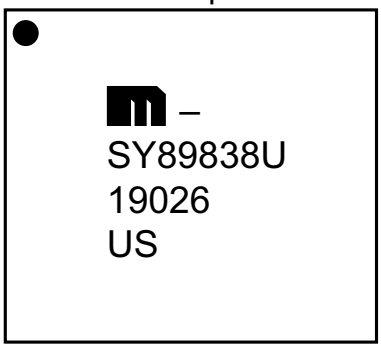
## 10.0 PACKAGING INFORMATION

### 10.1 Package Marking Information

32-Lead VQFN*




Example*



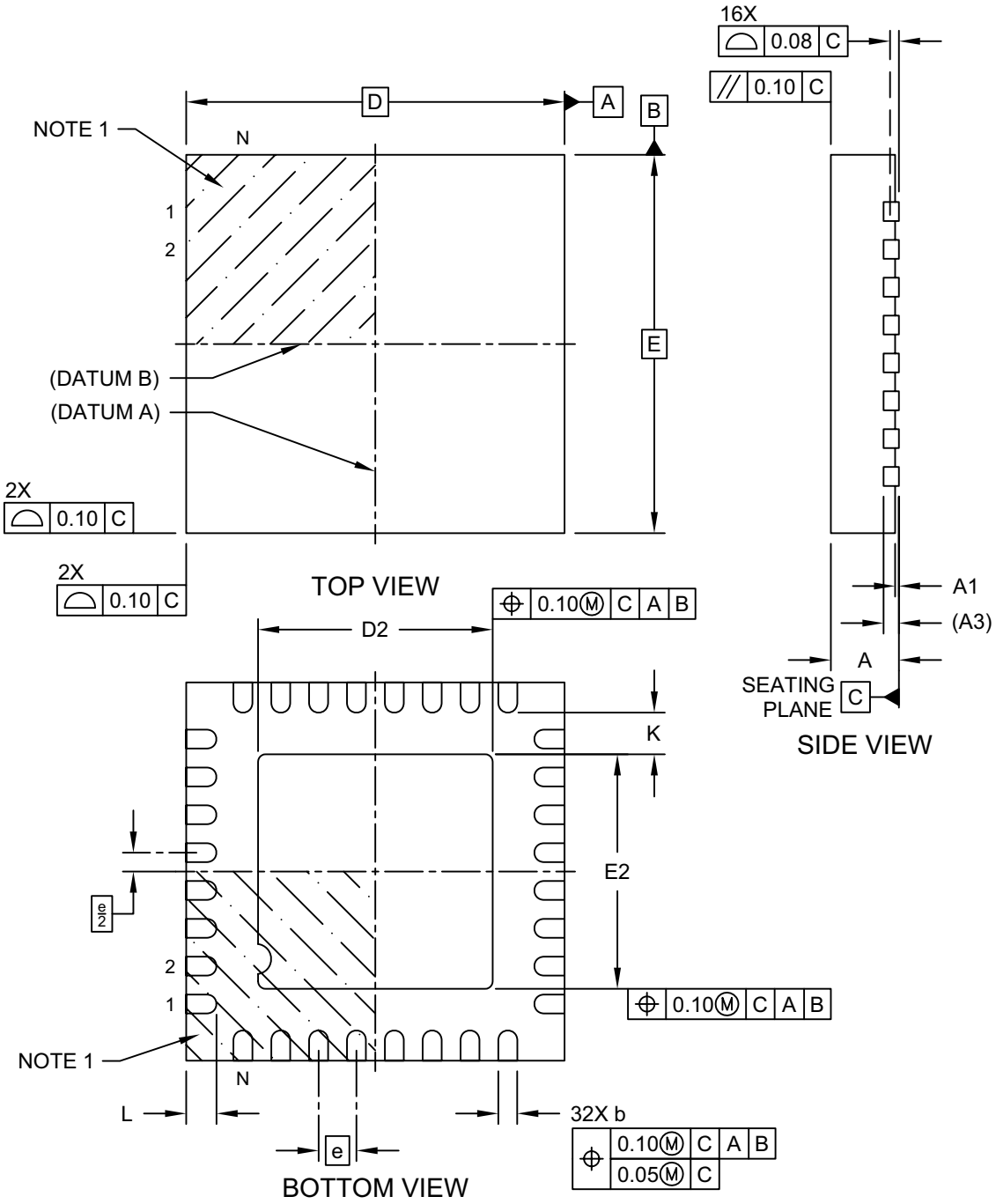

| | | |
|---|---|---|
| **Legend:** | XX...X | Product code or customer-specific information |
| | W | Week code |
| | NNN | Alphanumeric traceability code (week) |
| | * | This package is Pb-free. The Pb-free JEDEC designator can be found on the outer packaging for this package. |
| | ● | Pin one index is identified by a dot |

**Note**: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. Package may or may not include the corporate logo.

Underbar (_) and/or Overbar (¯) symbol may not be to scale.

### 32-Lead 5 mm × 5 mm VQFN [PEA] Package Outline and Recommended Land Pattern

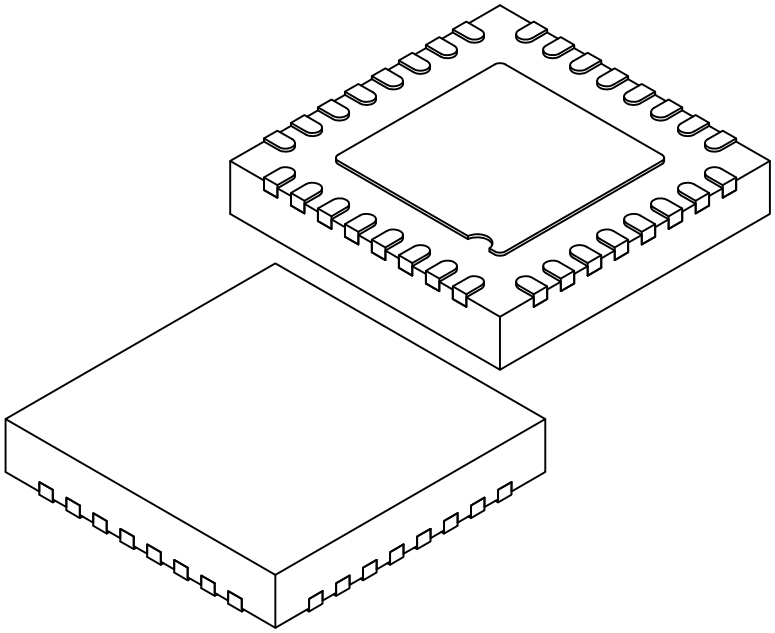
**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




Microchip Technology Drawing C04-1118-PEA Rev A Sheet 1 of 2

### 32-Lead 5 mm × 5 mm VQFN [PEA] Package Outline and Recommended Land Pattern

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Number of Terminals | N | | 32 | |
| Pitch | e | | 0.50 BSC | |
| Overall Height | A | 0.80 | 0.85 | 0.90 |
| Standoff | A1 | 0.00 | 0.02 | 0.05 |
| Terminal Thickness | A3 | | 0.203 REF | |
| Overall Length | D | | 5.00 BSC | |
| Exposed Pad Length | D2 | 3.05 | 3.10 | 3.15 |
| Overall Width | E | | 5.00 BSC | |
| Exposed Pad Width | E2 | 3.05 | 3.10 | 3.15 |
| Terminal Width | b | 0.20 | 0.25 | 0.30 |
| Terminal Length | L | 0.35 | 0.40 | 0.45 |
| Terminal-to-Exposed-Pad | K | 0.20 | - | - |

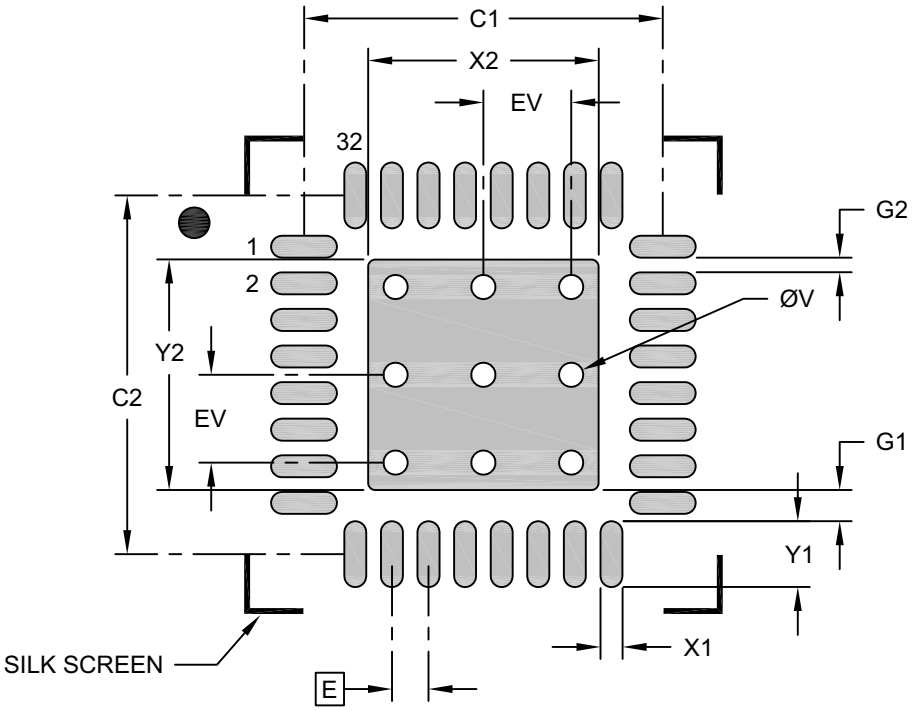
Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-1118-PEA Rev A Sheet 2 of 2

## 32-Lead 5 mm × 5 mm VQFN [PEA] Package Outline and Recommended Land Pattern

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




RECOMMENDED LAND PATTERN

| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Contact Pitch | E | 0.50 BSC | | |
| Optional Center Pad Width | X2 | | | 3.15 |
| Optional Center Pad Length | Y2 | | | 3.15 |
| Contact Pad Spacing | C1 | | 4.90 | |
| Contact Pad Spacing | C2 | | 4.90 | |
| Contact Pad Width (Xnn) | X1 | | | 0.30 |
| Contact Pad Length (Xnn) | Y1 | | | 0.90 |
| Contact Pad to Center Pad (Xnn) | G1 | 0.43 | | |
| Contact Pad to Contact Pad (Xnn) | G2 | 0.20 | | |
| Thermal Via Diameter | V | | 0.33 | |
| Thermal Via Pitch | EV | | 1.20 | |

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-3118-PEA Rev A

**NOTES:**

## APPENDIX A: REVISION HISTORY

### Revision A (May 2024)

- Converted Micrel data sheet for SY89838U to Microchip format as DS20006869A.
- Minor text changes throughout.

**NOTES:**

## PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

| PART NO. | X | X | X | -XX |
|---|---|---|---|---|
| Device | Supply Voltage Range | Package | Temperature Range | Special Processing |

| | | | |
|---|---|---|---|
| **Device:** | SY89838 | = | Precision 1:8 LVDS Clock Fanout Buffer with 2:1 Runt Pulse Eliminator Input MUX (Precision Edge®) |
| **Voltage Option:** | U | = | 2.5V |
| **Package:** | M | = | 32-Lead VQFN |
| **Temperature Range:** | G | = | –40°C to 85°C |
| **Special Processing:** | <blank> | = | 60/Tube |
| | TR | = | 1,000/Reel |

**Examples:**

a) **SY89838UMG**

2.5V, 32-Lead VQFN, –40°C to 85°C, 60/Tube

b) **SY89838UMG-TR**

2.5V, 32-Lead VQFN, –40°C to 85°C, 1,000/Reel

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