SY89311U

2.5V/3.3V/5V 1:2 Differential PECL/LVPECL/ECL Fanout Buffer

Features

- 2.5V, 3.3V, and 5V Power Supply
- Ensured AC Parameters over Temperature
  - f_{MAX} > 3.0 GHz
  - <20 ps Output-to-Output Skew
  - <200 ps t_r/t_f
  - <300 ps Propagation Delay
  - 51 fs_{RMS} Phase Jitter (typical)
- 100K Compatible I/O
- Wide Temperature Range: –40°C to +85°C
- Available in Ultra-Small 8-Lead VDFN (2 mm x 2 mm) Package

General Description

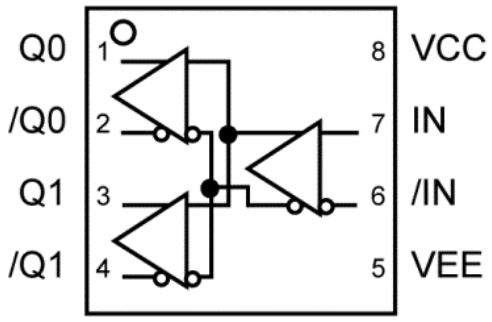
The SY89311U is a precision, high-speed 1:2 differential fanout buffer. Having within-device skews and output transition times significantly improved over the EL11V, the SY89311U is ideally suited for those applications that require excellent AC performance in a small package.

The differential inputs of the SY89311U employ clamping circuitry to maintain stability under open input conditions. If the inputs are left open, the Q outputs will be LOW.

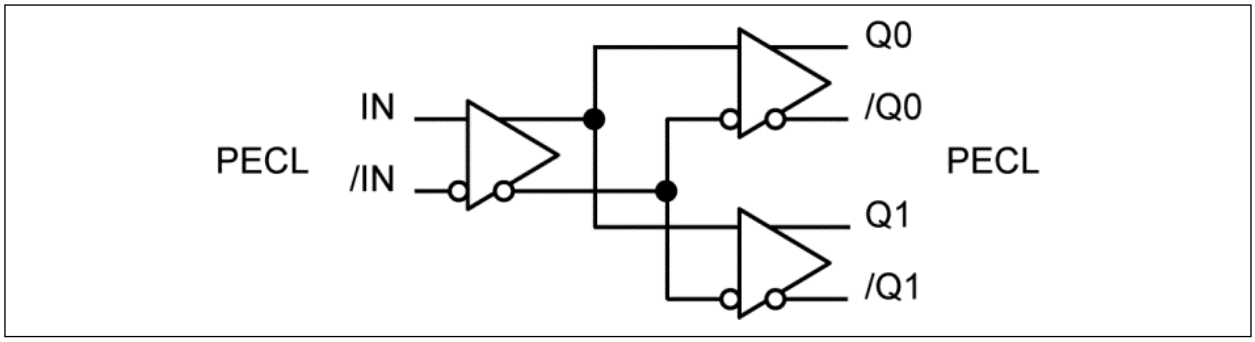
The differential inputs can accept 10/100K ECL/PECL signals (external termination required) and the outputs are 100K ECL/PECL compatible.

Package Type

SY89311U
8-Lead VDFN (M)
(Top View)



Functional Block Diagram



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

Supply Voltage (V_{CC}) ..... –0.5V to +6.0V
Input Voltage (V_{IN}) ..... –0.5V to V_{CC}
LVPECL Continuous Output Current (I_{OUT}) ..... 50 mA
LVPECL Surge Output Current (I_{OUT}) ..... 100 mA
Source or Sink Current on IN, /IN Pin ..... ±50 mA

Operating Ratings ‡

Supply Voltage (V_{CC}-V_{EE}) ..... +2.375V to +2.625V
Supply Voltage (V_{CC}-V_{EE}) ..... +3.0V to +3.6V
Supply Voltage (V_{CC}-V_{EE}) ..... +4.5V to +5.5V

† Notice: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

‡ Notice: The device is not guaranteed to function outside its operating ratings.

DC ELECTRICAL CHARACTERISTICS

T_A = –40°C to +85°C, unless otherwise stated. Note 1

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Power Supply Votlage	V_{CC}	2.375	2.5	2.625	V	LVPECL
		3.0	3.3	3.6	V	LVPECL
		4.5	5.0	5.5	V	PECL
		–5.5	–5.0	–4.5	V	ECL
		–3.6	–3.3	–3.0	V	LVECL
		–2.625	–2.5	–2.375	V	LVECL
Power Supply Current	I_{EE}	—	30	44	mA	Max. V_{CC}, no load
Input High Current	I_{IH}	—	—	150	µA	$V_{IN} = V_{IH}$
Input Low Current (IN)	I_{IL}	0.5	—	—	µA	$V_{IN} = V_{IL}$
Input Low Current (/IN)		–150	—	—	µA	$V_{IN} = V_{IL}$
Input Capacitance	C_{IN}	—	1.0	—	pF	—

Note 1: This circuit is designed to meet the DC specifications shown in the table above after thermal equilibrium has been established.

100K ECL/LVECL DC ELECTRICAL CHARACTERISTICS

V_{CC} = +2.5V ±5% or +3.3V ±10% or +5.0V ±10% and V_{EE} = 0V; V_{CC} = 0V and V_{EE} = –2.5V ±5% or –3.3V ±10% or –5.0V ±10%; R_L = 50Ω to V_{CC} – 2V; T_A = –40°C to +85°C, unless otherwise noted.

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Output High Voltage	V_{OH}	V_{CC} – 1.145	—	V_{CC} – 0.895	V	—
Output Low Voltage	V_{OL}	V_{CC} – 1.945	—	V_{CC} – 1.695	V	—
Input High Voltage	V_{IH}	V_{CC} – 1.225	—	V_{CC} – 0.88	V	—
Input Low Voltage	V_{IL}	V_{CC} – 1.945	—	V_{CC} – 1.625	V	—
Input High Voltage Common Mode Range	V_{IHCMR}	V_{EE} + 1.2	—	V_{CC}	V	Note 1
Input High Current	I_{IH}	—	—	150	µA	V_{IN} = V_{IH}
Input Low Current (IN)	I_{IL}	0.5	—	—	µA	V_{IN} = V_{IL}
Input Low Current (/IN)		–150	—	—	µA	V_{IN} = V_{IL}

Note 1: $V_{IHCMR(MIN)}$ varies 1:1 with V_{EE}. $V_{IHCMR(MAX)}$ varies 1:1 with V_{CC}.

AC ELECTRICAL CHARACTERISTICS

V_{CC} = +2.5V ±5% or +3.3V ±10% or +5.0V ±10% and V_{EE} = 0V; V_{CC} = 0V and V_{EE} = –2.5V ±5% or –3.3V ±10% or –5.0V ±10%; R_L = 50Ω to V_{CC} – 2V; T_A = –40°C to +85°C, unless otherwise noted. Note 1

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Maximum Toggle Frequency	f_{MAX}	3	—	—	GHz	—
Propagation Delay (Differential)	t_{PD}	140	220	300	ps	IN to Q, /Q; V_{CC} = 3.3V/5V
		170	240	360	ps	IN to Q, /Q; V_{CC} = 2.5V
Within-Device Skew	t_{SKEW}	—	5	20	ps	Q, /Q; Note 2
Part-to-Part Skew		—	—	150	ps	V_{CC} = 3.3V/5V, Note 2
		—	—	120	ps	V_{CC} = 2.5V, Note 2
Cycle-to-Cycle Jitter (RMS)	t_{JITTER}	—	—	1	ps_{RMS}	—
Additive Phase Jitter		—	51	—	fs_{RMS}	622 MHz over 12 kHz to 20 MHz
Input Swing	V_{DIFF}	150	800	1200	mV	Note 3
Output Rise/Fall Time (20% to 80%)	t_r/t_f	70	120	200	ps	—

Note 1: Measured with 750 mV input signal, 50% duty cycle. V_{DIFF_OUT} is ≥ 400 mV.

2: Skew is measured between outputs under identical transitions. Duty cycle skew is defined only for differential operation when the delays are measured from the cross point of the inputs to the cross point of the outputs.

3: See Figure 1-1.

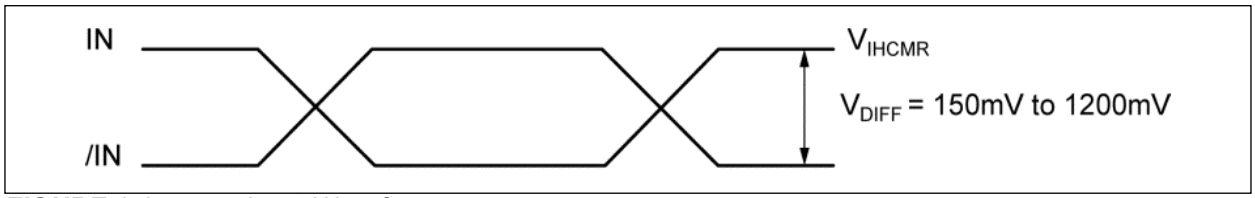


FIGURE 1-1: *Input Waveform.*

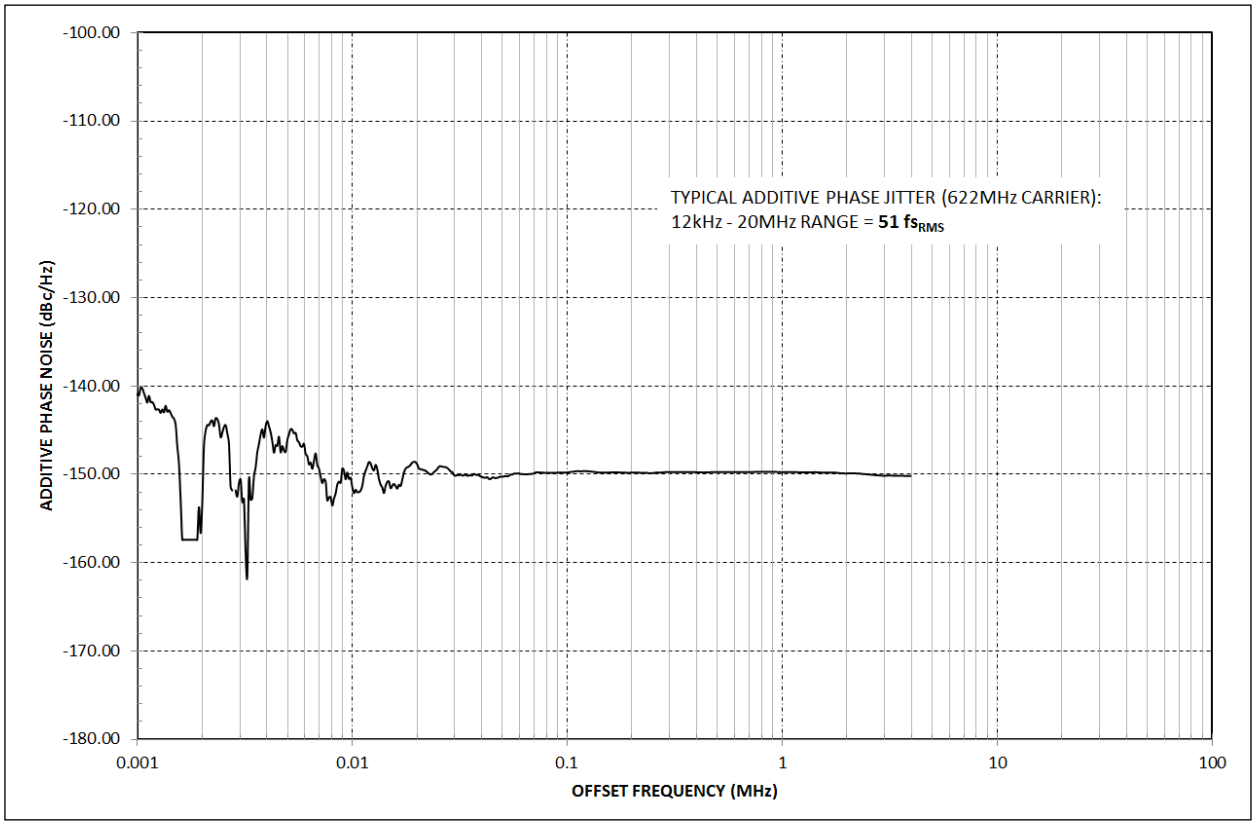
TEMPERATURE SPECIFICATIONS

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Temperature Ranges						
Storage Temperature Range	T_S	–65	—	+150	°C	—
Lead Temperature	T_{LEAD}	—	—	+260	°C	Soldering, 20 sec.
Ambient Temperature Range	T_A	–40	—	+85	°C	—
Package Thermal Resistance (Note 1)						
Thermal Resistance, VDFN 8-Ld	θ_{JA}	—	93	—	°C/W	Still-Air
	θ_{JA}	—	87	—	°C/W	500 lpfm
	θ_{JB}	—	60	—	°C/W	Junction-to-Board

Note 1: Package Thermal Resistance values assume exposed pad is soldered (or equivalent) to the device's most negative potential on the PCB.

Additive Phase Noise Plot

V_{CC} = +3.3V, GND = 0V, R_L = 50Ω to V_{CC} – 2V, T_A = +25°C.



2.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 2-1.

TABLE 2-1: PIN FUNCTION TABLE

Pin Number	Pin Name	Type	Description
1, 2 3, 4	Q0, /Q0 Q1, /Q1	100K Output	Differential PECL/ECL Outputs: Default to LOW if IN inputs are left open. Q1, /Q1 See the LVPECL Output Interface Applications section for recommendations on terminations. Unused output pairs may be left floating without any impact on skew or jitter.
5	VEE, Exposed Pad	Negative Power Supply	Negative Power Supply: VEE and exposed pad must be tied to most negative supply. For PECL/LVPECL, connect to ground.
6	/IN	100K Input	Differential PECL/ECL Input: Internal 75 kΩ pull-up and pull-down resistors. If left floating, pin defaults to $V_{CC}/2$. When not used, this input can be left open. See the Input Interface Application section for single-ended inputs.
7	IN	100K Input	Differential PECL/ECL Input: Internal 75 kΩ pull-down resistor. If left open, pin defaults LOW. Q output will be LOW. Accepts differential 10K and 100K ECL/PECL. See the Input Interface Application section for single-ended inputs.
8	VCC	Positive Power Supply	Positive Power Supply: Bypass with 0.1 µF//0.01 µF low ESR capacitors

3.0 INPUT INTERFACE APPLICATION

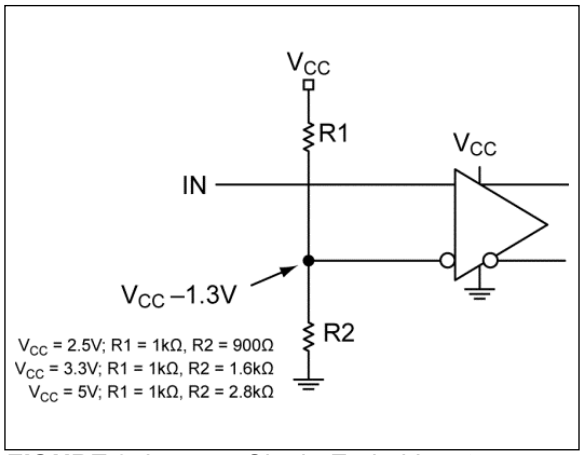


FIGURE 3-1: *Single-Ended Input (Terminating Unused Input).*

4.0 LVPECL OUTPUT INTERFACE APPLICATIONS

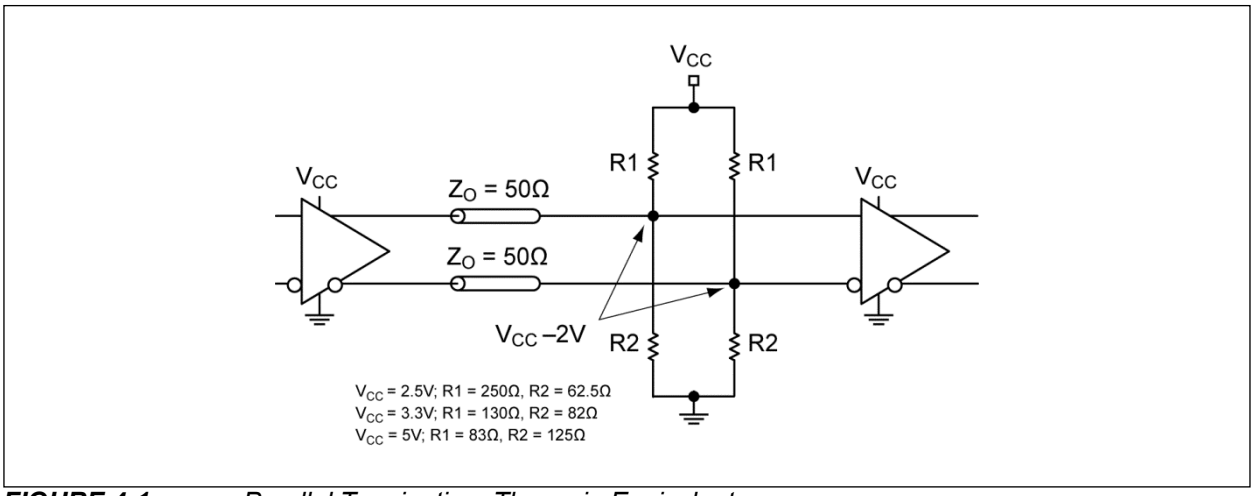


FIGURE 4-1: *Parallel Termination: Thevenin Equivalent.*

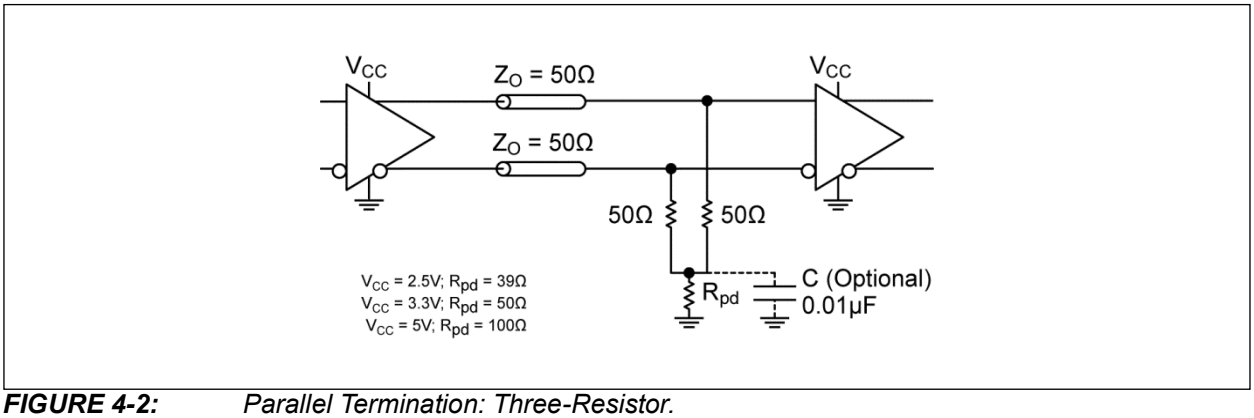


FIGURE 4-2: *Parallel Termination: Three-Resistor.*

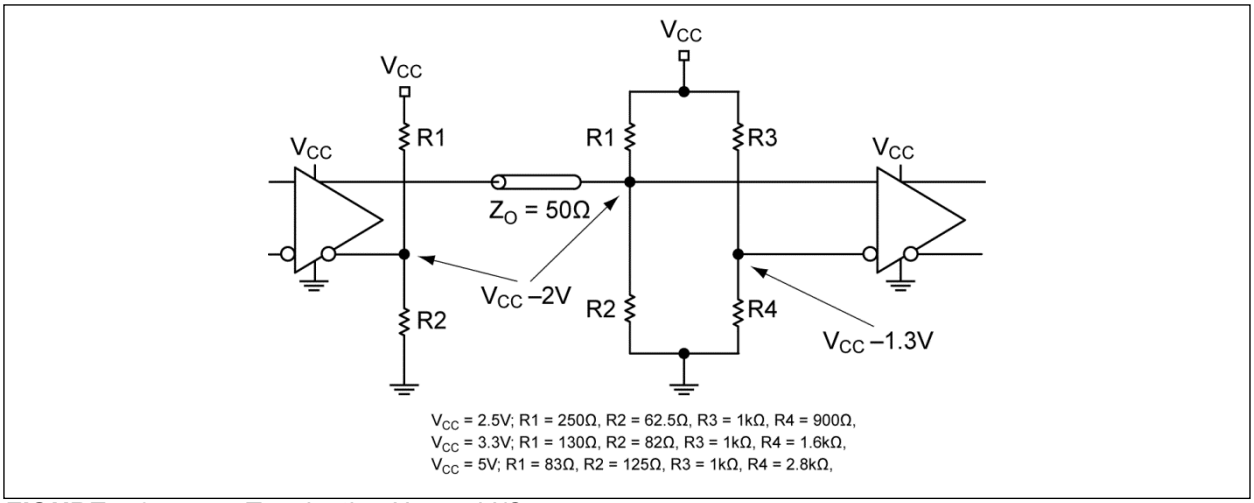
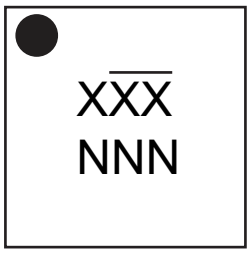


FIGURE 4-3: *Terminating Unused I/O.*

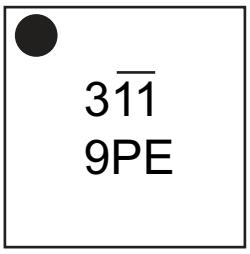
5.0 PACKAGING INFORMATION

5.1 Package Marking Information

8-Lead VDFN*



Example



Legend:	XX...X	Product code or customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.
	●, ▲, ▼	Pin one index is identified by a dot, delta up, or delta down (triangle mark).

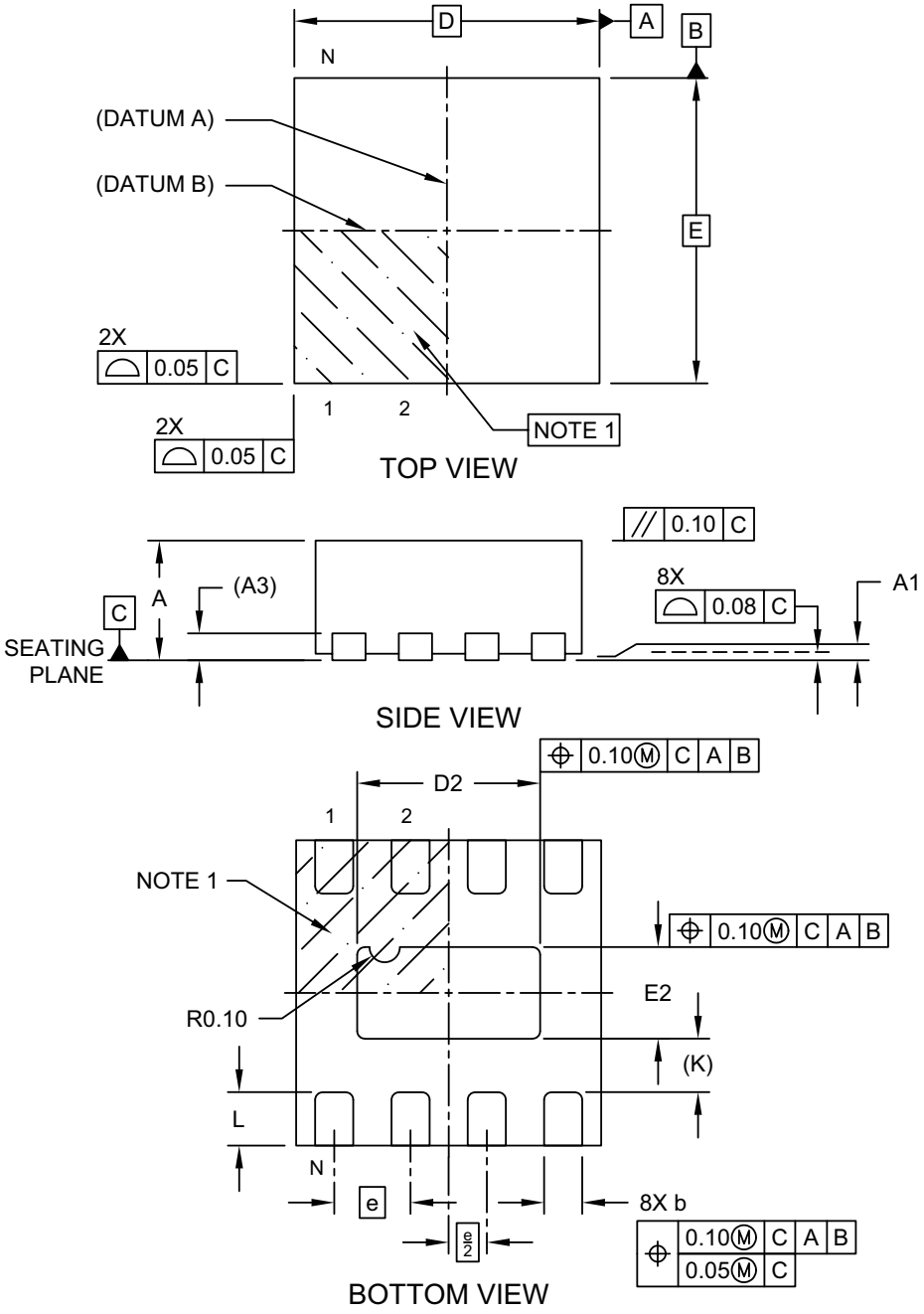
Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. Package may or may not include the corporate logo.

Underbar (_) and/or Overbar (‾) symbol may not be to scale.

Note: If the full seven-character YYWWNNN code cannot fit on the package, the following truncated codes are used based on the available marking space:
6 Characters = YWWNNN; 5 Characters = WWNNN; 4 Characters = WNNN; 3 Characters = NNN;
2 Characters = NN; 1 Character = N

8-Lead Very Thin Plastic Dual Flat, No Lead Package (H2A) - 2x2x0.9 mm Body [VDFN] With 1.20x0.6 mm Exposed Pad

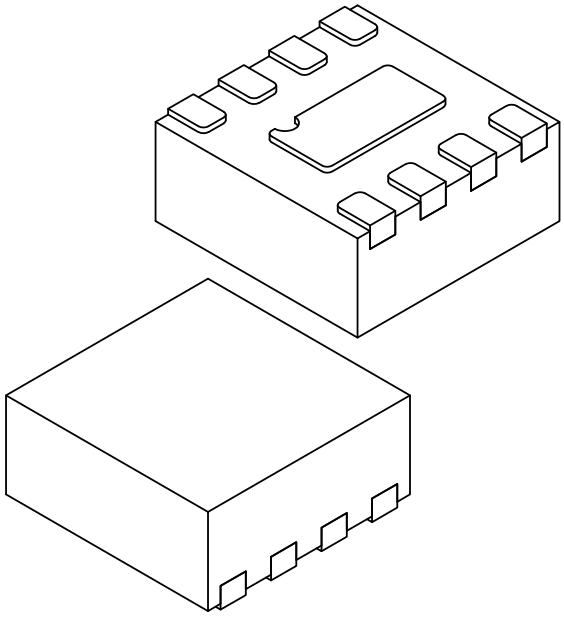
Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-1247 Rev B Sheet 1 of 2

8-Lead Very Thin Plastic Dual Flat, No Lead Package (H2A) - 2x2x.9 mm Body [VDFN] With 1.20x0.6 mm Exposed Pad

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		8	
Pitch	e		0.50 BSC	
Overall Height	A	0.80	0.85	0.90
Standoff	A1	0.00	0.02	0.05
Terminal Thickness	A3		0.203 REF	
Overall Length	D		2.00 BSC	
Exposed Pad Length	D2	1.10	1.20	1.30
Overall Width	E		2.00 BSC	
Exposed Pad Width	E2	0.50	0.60	0.70
Terminal Width	b	0.20	0.25	0.30
Terminal Length	L	0.30	0.35	0.40
Terminal-to-Exposed-Pad	K		0.35 REF	

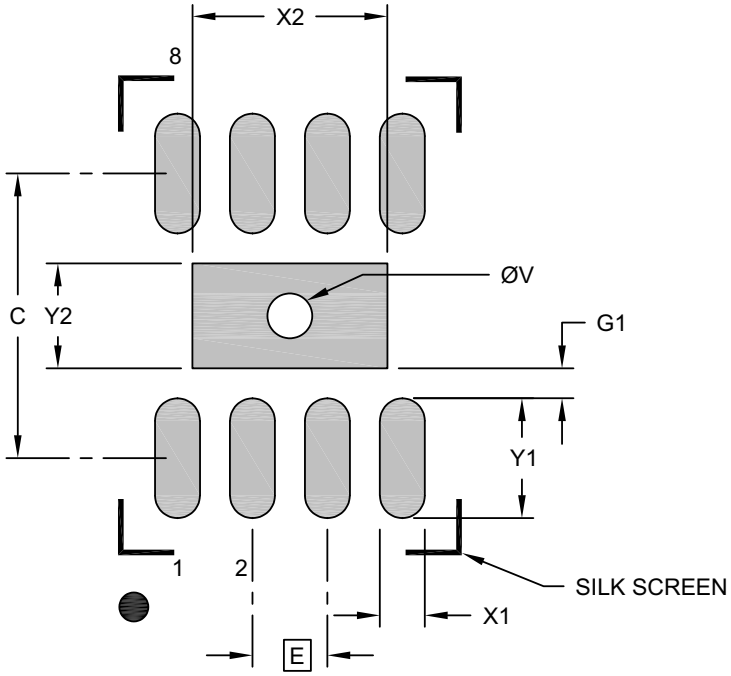
Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-1247 Rev B Sheet 2 of 2

8-Lead Very Thin Plastic Dual Flat, No Lead Package (H2A) - 2x2 mm Body [VDFN] Micrel Legacy Package

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.50 BSC	
Optional Center Pad Width	X2			1.30
Optional Center Pad Length	Y2			0.70
Contact Pad Spacing	C		1.90	
Contact Pad Width (X8)	X1			0.30
Contact Pad Length (X8)	Y1			0.80
Contact Pad to Center Pad (X8)	G1	0.20		
Thermal Via Diameter	V	0.27	0.30	0.33

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-3247 Rev. B

APPENDIX A: REVISION HISTORY

Revision A (December 2023)

- Converted Micrel document SY89311U to Microchip data sheet template DS20006839A.
- Minor text changes throughout.

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

Part No.	X	X	X	[-XX]
Device	Supply Voltage	Package	Temperature Range	Media Type

Device:	SY89311:	2.5V/3.3V/5V 1:2 Differential PECL/LVPECL/ ECL Fanout Buffer	
Supply Voltage:	U	=	2.5V/3.3V/5V
Package:	M	=	8-Lead 2 mm x 2 mm VDFN
Temperature Range:	G	=	–40°C to +85°C
Media Type:	TR	=	1,000/Reel

Examples:

a) SY89311UMG-TR:

SY89311, 2.5V/3.3V/5V Supply Voltage, 8-Lead VDFN, –40°C to +85°C Temperature Range, 1,000/Reel

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

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