

P-Channel 40-V (D-S) MOSFET

PRODUCT SUMMARY

V _{DS} (V)	R _{DS(on)} (Ω)	I _D (A)	Q _g (TYP.)
-40	0.0081 at V _{GS} = -10 V	-50 ^d	60
	0.0117 at V _{GS} = -4.5 V	-48 ^d	

FEATURES

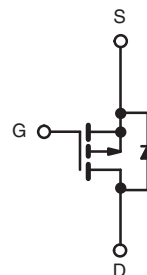
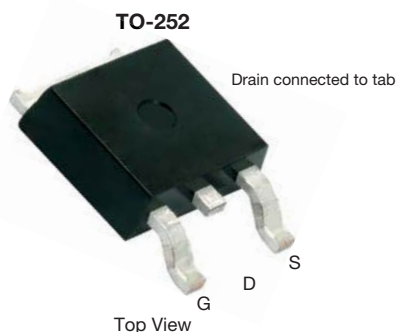
- TrenchFET® power MOSFET
- 100 % R_g and UIS tested
- Material categorization:
for definitions of compliance please see
www.vishay.com/doc?99912



RoHS
COMPLIANT
HALOGEN
FREE

APPLICATIONS

- Power switch
- Load switch in high current applications
- DC/DC converters



P-Channel MOSFET

Ordering Information:

SUD50P04-08-GE3 (lead (Pb)-free and halogen-free)

ABSOLUTE MAXIMUM RATINGS (T_C = 25 °C, unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-Source Voltage	V _{DS}	-40	V
Gate-Source Voltage	V _{GS}	± 20	
Continuous Drain Current (T _J = 150 °C)	I _D	T _C = 25 °C -50 ^d	A
		T _C = 70 °C -50 ^d	
Pulsed Drain Current	I _{DM}	-100	
Avalanche Current	I _{AS}	-46	
Single Avalanche Energy ^a	E _{AS}	106	mJ
Maximum Power Dissipation ^a	P _D	T _C = 25 °C 73.5 ^b	W
		T _A = 25 °C ^c 2.5	
Operating Junction and Storage Temperature Range	T _J , T _{stg}	-55 to +150	°C

THERMAL RESISTANCE RATINGS

PARAMETER	SYMBOL	LIMIT	UNIT
Junction-to-Ambient (PCB Mount) ^c	R _{thJA}	50	°C/W
Junction-to-Case (Drain)	R _{thJC}	1.7	

Notes

- Duty cycle ≤ 1 %.
- See SOA curve for voltage derating.
- When mounted on 1" square PCB (FR-4 material).
- Package limited.



SPECIFICATIONS (T _J = 25 °C, unless otherwise noted)						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static						
Drain-Source Breakdown Voltage	V _{DS}	V _{GS} = 0 V, I _D = -250 μA	-40	-	-	V
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = -250 μA	-1	-	-2.5	
Gate-Body Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ± 20 V	-	-	± 250	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = -40 V, V _{GS} = 0 V	-	-	-1	μA
		V _{DS} = -40 V, V _{GS} = 0 V, T _J = 125 °C	-	-	-50	
		V _{DS} = -40 V, V _{GS} = 0 V, T _J = 150 °C	-	-	-250	
On-State Drain Current ^a	I _{D(on)}	V _{DS} ≤ -10 V, V _{GS} = -10 V	-50	-	-	A
Drain-Source On-State Resistance ^a	R _{DS(on)}	V _{GS} = -10 V, I _D = -22 A	-	0.0067	0.0081	Ω
		V _{GS} = -4.5 V, I _D = -19 A	-	0.0097	0.0117	
Forward Transconductance ^a	g _{fs}	V _{DS} = -15 V, I _D = -22 A	-	45	-	S
Dynamic ^b						
Input Capacitance	C _{iss}	V _{GS} = 0 V, V _{DS} = -20 V, f = 1 MHz	-	5380	-	pF
Output Capacitance	C _{oss}		-	570	-	
Reverse Transfer Capacitance	C _{rss}		-	500	-	
Total Gate Charge ^c	Q _g	V _{DS} = -20 V, V _{GS} = -10 V, I _D = -20 A	-	106	159	nC
		V _{DS} = -20 V, V _{GS} = -4.5 V, I _D = -20 A	-	60	90	
Gate-Source Charge ^c	Q _{gs}		-	22	-	
Gate-Drain Charge ^c	Q _{gd}		-	27	-	
Gate Resistance	R _g	f = 1 MHz	0.4	1.8	3.6	Ω
Turn-On Delay Time ^c	t _{d(on)}	V _{DD} = -20 V, R _L = 2 Ω I _D ≅ -10 A, V _{GEN} = -10 V, R _g = 1 Ω	-	15	23	ns
Rise Time ^c	t _r		-	12	18	
Turn-Off Delay Time ^c	t _{d(off)}		-	70	105	
Fall Time ^c	t _f		-	18	27	
Drain-Source Body Diode Ratings and Characteristics (T _C = 25 °C) ^b						
Continuous Current	I _S		-	-	-50	A
Pulsed Current	I _{SM}		-	-	-100	
Forward Voltage ^a	V _{SD}	I _F = -10 A, V _{GS} = 0 V	-	-0.8	-1.5	V
Reverse Recovery Time	trr	I _F = -10 A, dI/dt = 100 A/μs	-	35	53	ns
Peak Reverse Recovery Current	I _{RM(REC)}		-	-2	-3	A
Reverse Recovery Charge	Q _{rr}		-	33	50	nC

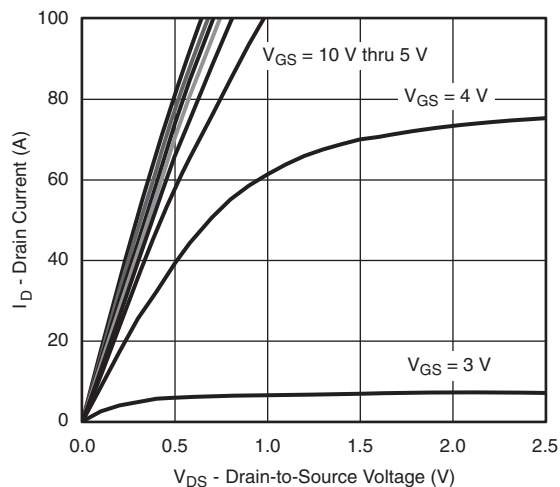
Notes

- a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.
b. Guaranteed by design, not subject to production testing.
c. Independent of operating temperature.

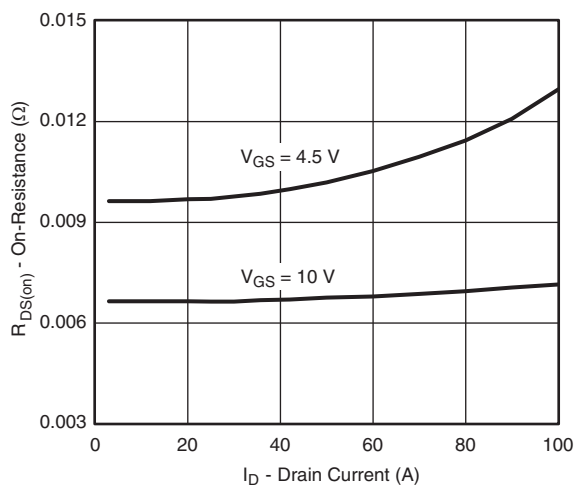
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



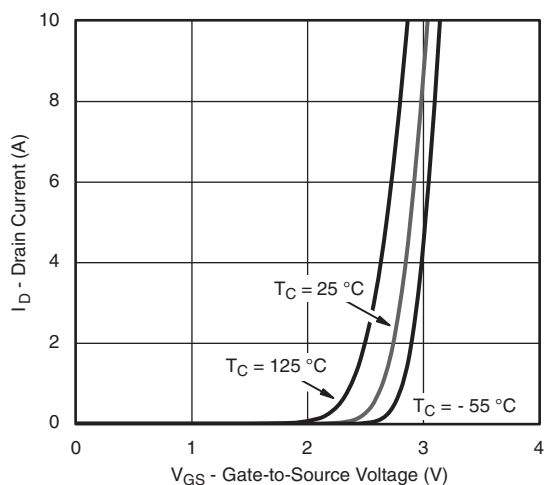
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



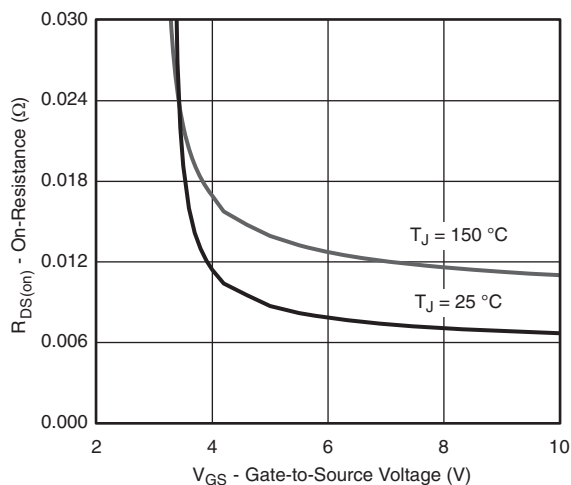
Output Characteristics



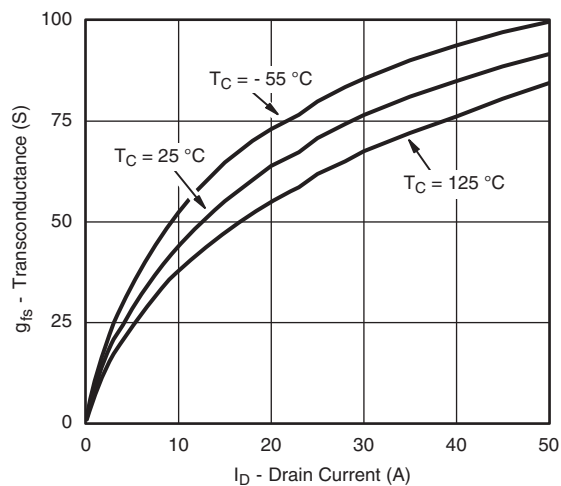
On-Resistance vs. Drain Current



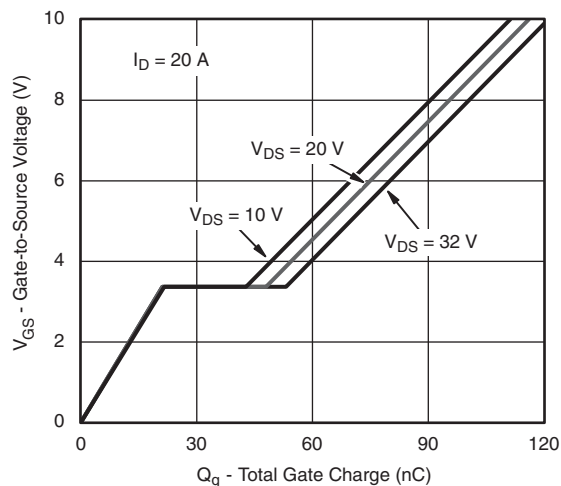
Transfer Characteristics



On-Resistance vs. Gate-to-Source Voltage



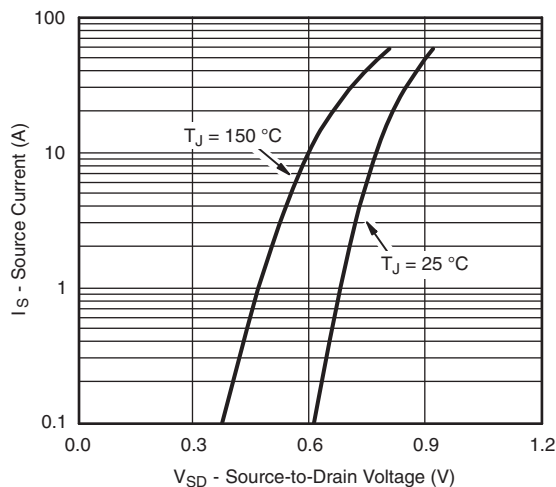
Transconductance



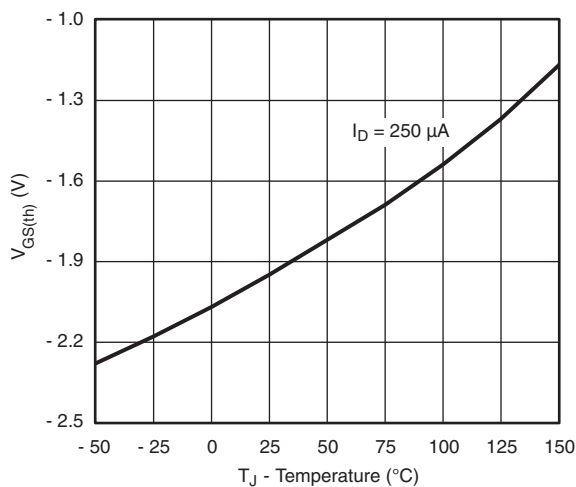
Gate Charge



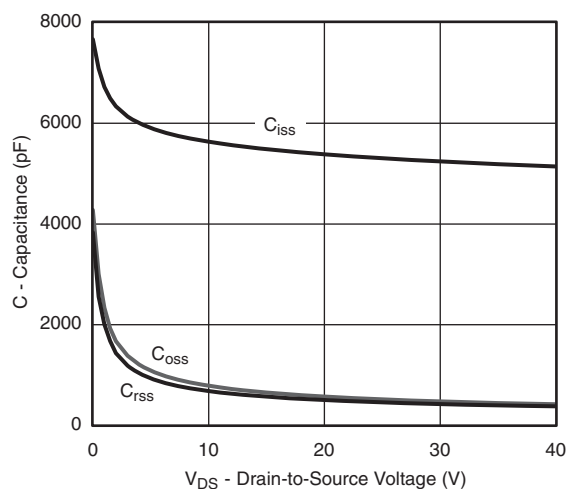
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



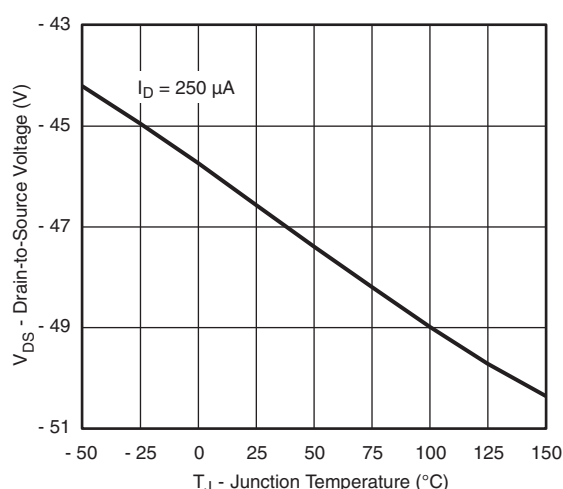
Source-Drain Diode Forward Voltage



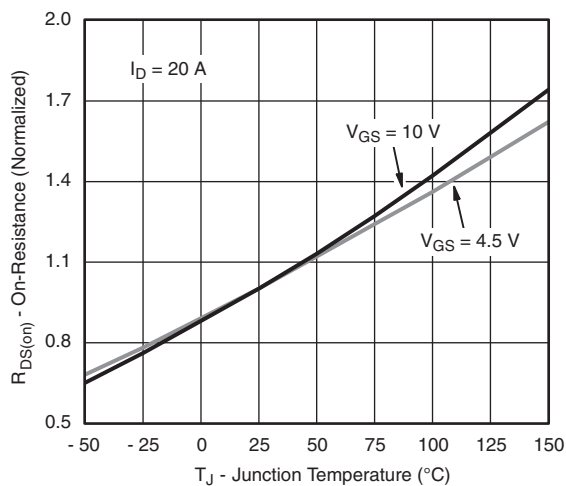
Threshold Voltage



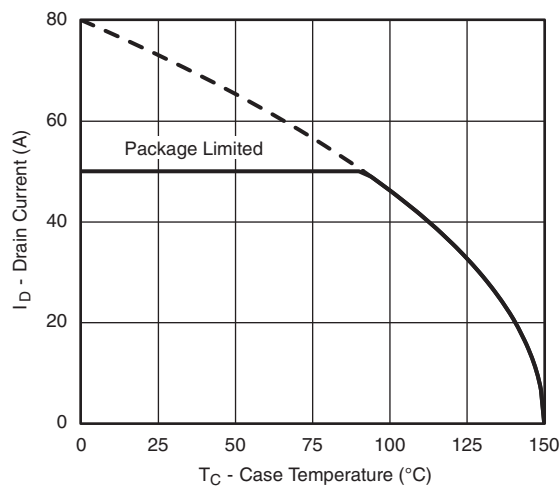
Capacitance



Drain Source Breakdown vs. Junction Temperature



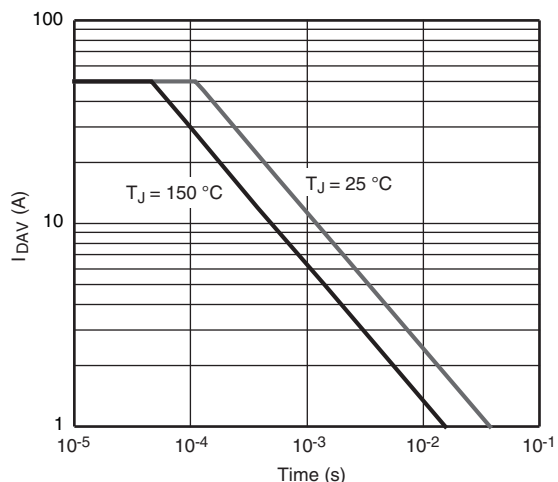
On-Resistance vs. Junction Temperature



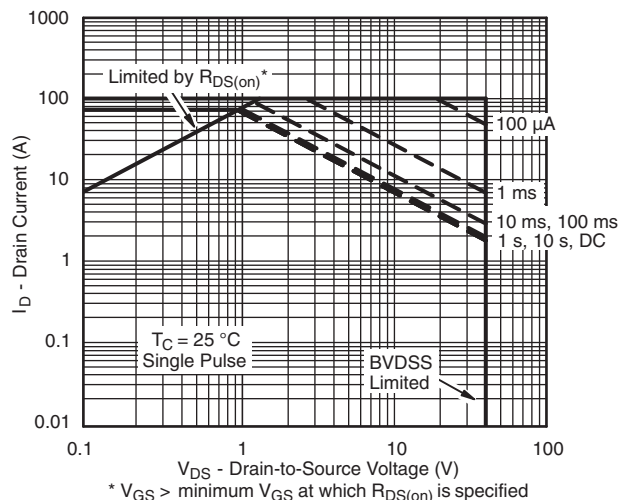
Current Derating



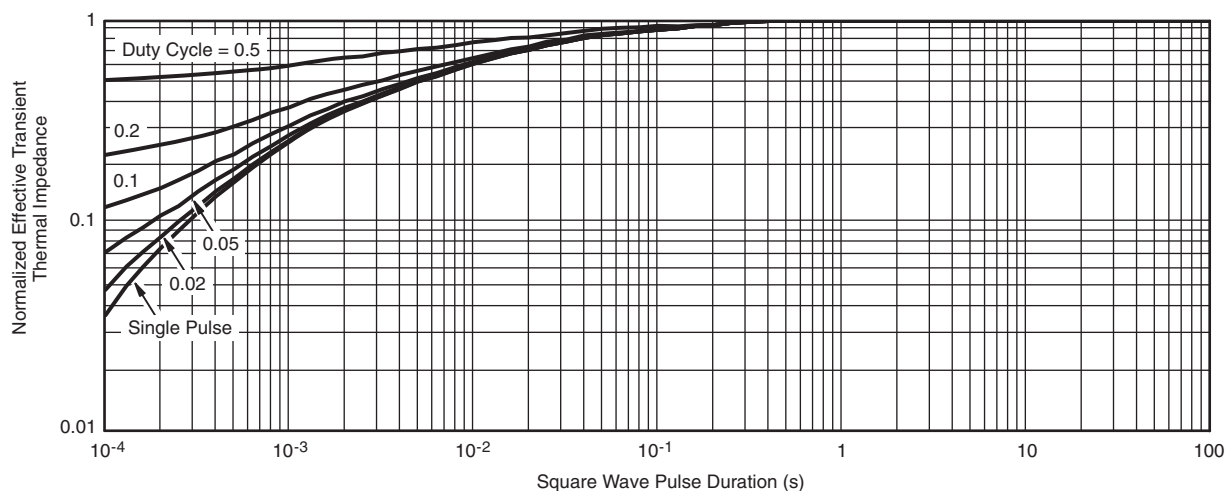
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Single Pulse Avalanche Current Capability vs. Time



Safe Operating Area

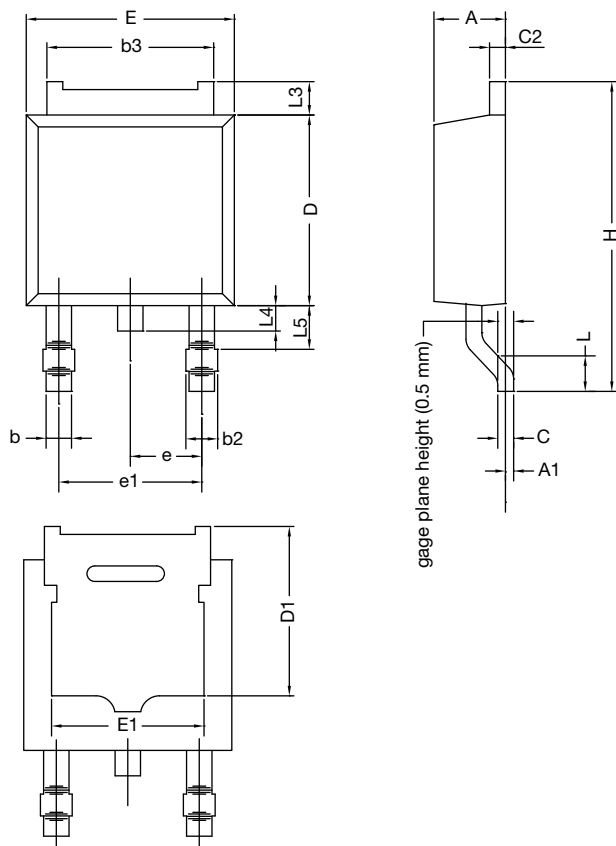


Normalized Thermal Transient Impedance, Junction-to-Case

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?65594.



TO-252AA Case Outline

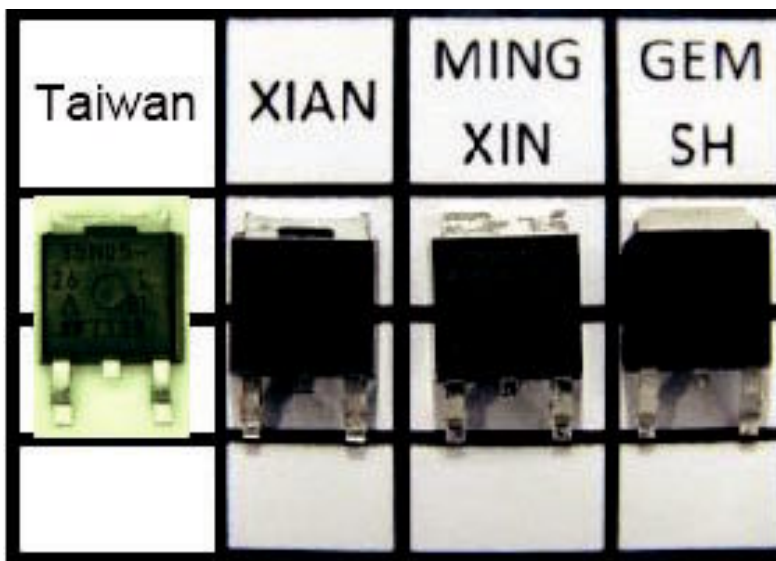


DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	2.18	2.38	0.086	0.094
A1	-	0.127	-	0.005
b	0.64	0.88	0.025	0.035
b2	0.76	1.14	0.030	0.045
b3	4.95	5.46	0.195	0.215
C	0.46	0.61	0.018	0.024
C2	0.46	0.89	0.018	0.035
D	5.97	6.22	0.235	0.245
D1	4.10	-	0.161	-
E	6.35	6.73	0.250	0.265
E1	4.32	-	0.170	-
H	9.40	10.41	0.370	0.410
e	2.28 BSC		0.090 BSC	
e1	4.56 BSC		0.180 BSC	
L	1.40	1.78	0.055	0.070
L3	0.89	1.27	0.035	0.050
L4	-	1.02	-	0.040
L5	1.01	1.52	0.040	0.060

ECN: T13-0359-Rev. O, 03-Jun-13
DWG: 5347

Notes

- Dimension L3 is for reference only.
- Xi'an, Mingxin, and GEM SH actual photo.



RECOMMENDED MINIMUM PADS FOR DPAK (TO-252)



Recommended Minimum Pads
Dimensions in Inches/(mm)

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