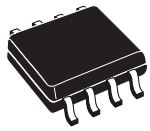
STS10DN3LH5

Dual N-channel 30 V, 0.019 Ω, 10 A, SO-8 STripFET™ V Power MOSFET

Features

Type	V_{DSS}	$R_{DS(on)}$ max	I_D
STS10DN3LH5	30 V	0.021 Ω	10 A

- $R_{DS(on)}$ * Q_g industry benchmark
- Extremely low on-resistance $R_{DS(on)}$
- Very low switching gate charge
- High avalanche ruggedness
- Low gate drive power losses



SO-8

Application

- Switching applications

Description

This STripFET™V Power MOSFET technology is among the latest improvements, which have been especially tailored to achieve very low on-state resistance providing also one of the best-in-class FOM.

Figure 1. Internal schematic diagram

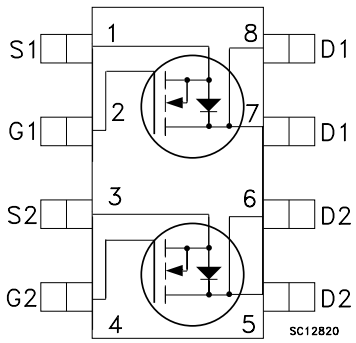


Table 1. Device summary

Order codes	Marking	Package	Packaging
STS10DN3LH5	10DD3L	SO-8	Tape and reel

Contents

1 Electrical ratings 3

2 Electrical characteristics 4

2.1 Electrical characteristics (curves) 6

3 Test circuits 8

4 Package mechanical data 10

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1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage (V_{GS} = 0)	30	V
V_{GS}	Gate-Source voltage	± 22	V
I_D (1)	Drain current (continuous) at T_C = 25 °C	10	A
I_D	Drain current (continuous) at T_C = 100 °C	7	A
I_{DM} (2)	Drain current (pulsed)	40	A
P_{TOT}	Total dissipation at T_C = 25 °C	2.5	W
	Derating factor	0.02	W/°C
E_{AS} (3)	Single pulse avalanche energy	50	mJ
T_J T_{stg}	Operating junction temperature Storage temperature	- 55 to 150	°C

1. Limited by wire bonding
2. Pulse width limited by safe operating area
3. Starting T_J = 25 °C, I_D = 21 A, L= 0.2 mH

Table 3. Thermal resistance

Symbol	Parameter	Value	Unit
R_{thJC}	Thermal resistance junction-case max	50	°C/W
R_{thJA}	Thermal resistance junction-case max	100	°C/W
T_J	Maximum lead temperature for soldering purpose	275	°C

2 Electrical characteristics

(T_{CASE} = 25 °C unless otherwise specified)

Table 4. Static

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown Voltage	I_D = 250 µA, V_{GS}= 0	30			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = 30 V V_{DS} = 30 V, Tc = 125 °C			1 10	µA µA
I_{GSS}	Gate body leakage current (V_{DS} = 0)	V_{GS} = ± 22 V			±100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	1			V
$R_{DS(on)}$	Static drain-source on resistance	V_{GS} = 10 V, I_D= 5 A		0.019	0.021	Ω
		V_{GS} = 4.5 V, I_D= 5 A		0.023	0.028	Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min	Typ.	Max.	Unit
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 25 V, f = 1 MHz, V_{GS} = 0	-	475 97 19	-	pF pF pF
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	V_{DD} = 15 V, I_D = 10 A V_{GS} = 5 V *(Figure 14)*	-	4.6 1.7 1.9	-	nC nC nC
Q_{gs1} Q_{gs2}	Pre V_{th} gate-to-source charge Post V_{th} gate-to-source charge	V_{DD} = 15 V, I_D = 10A V_{GS} = 5 V *(Figure 19)*	-	0.67 0.84	-	nC nC
R_G	Gate input resistance	f = 1 MHz gate bias Bias = 0 test signal level = 20 mV open drain	-	2.5	-	Ω

Table 6. Switching on/off (resistive load)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r	Turn-on delay time Rise time	V_{DD} = 15 V, I_D = 5 A, R_G = 4.7 Ω, V_{GS} = 10 V *(Figure 13 and Figure 18)*	-	4 22	-	ns ns
$t_{d(off)}$ t_f	Turn-off delay time Fall time	V_{DD} = 15 V, I_D = 5 A, R_G = 4.7 Ω, V_{GS} = 10 V *(Figure 13 and Figure 18)*	-	13 2.8	-	ns ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD} I_{SDM} (1)	Source-drain current Source-drain current (pulsed)		-		10 40	A A
V_{SD}	Forward on voltage	I_{SD} = 5 A, V_{GS} = 0	-		1.1	V
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD} = 10 A, V_{DD} = 25 V di/dt = 100 A/µs, *(Figure 15)*	-	16.2 7.8 1		ns nC A

1. Pulsed: pulse duration = 300 µs, duty cycle 1.5 %

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

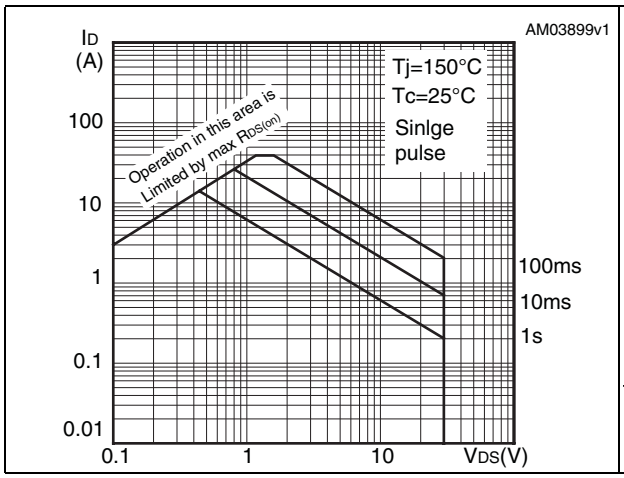


Figure 3. Thermal impedance

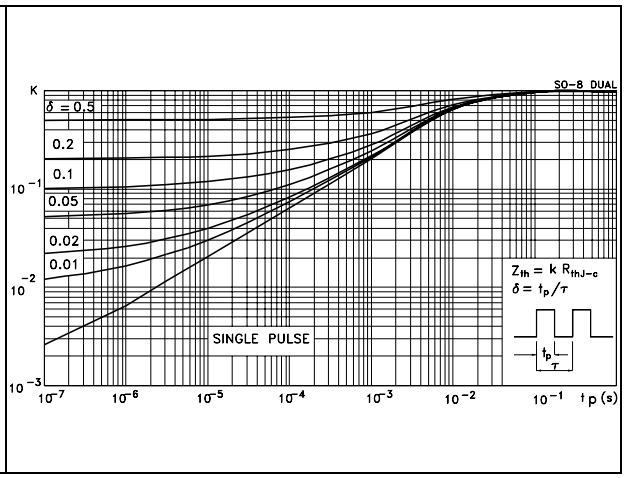


Figure 4. Output characteristics

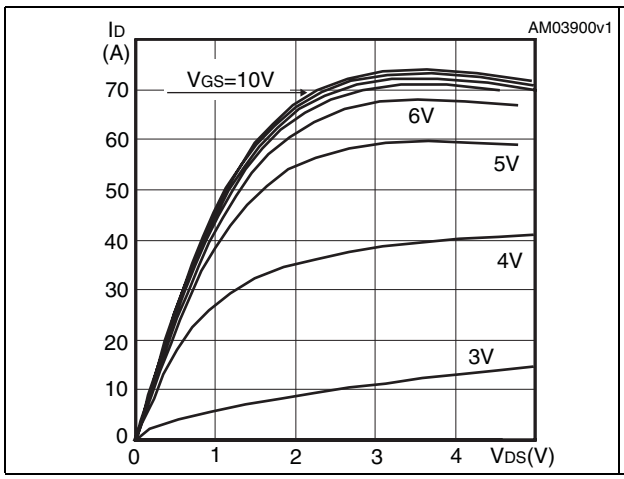


Figure 5. Transfer characteristics

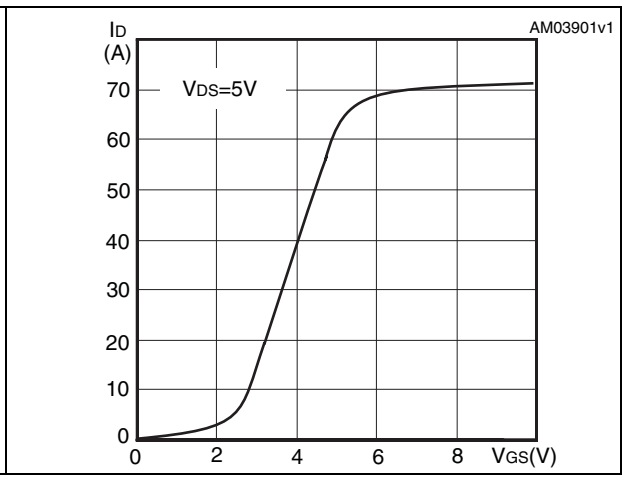


Figure 6. Normalized BV_{DSS} vs temperature

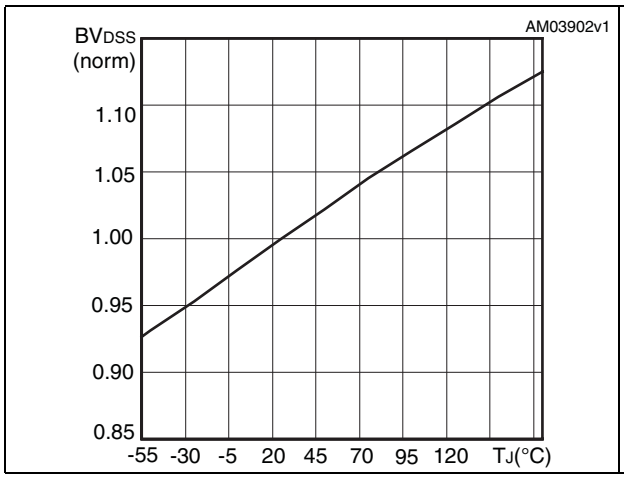


Figure 7. Static drain-source on resistance

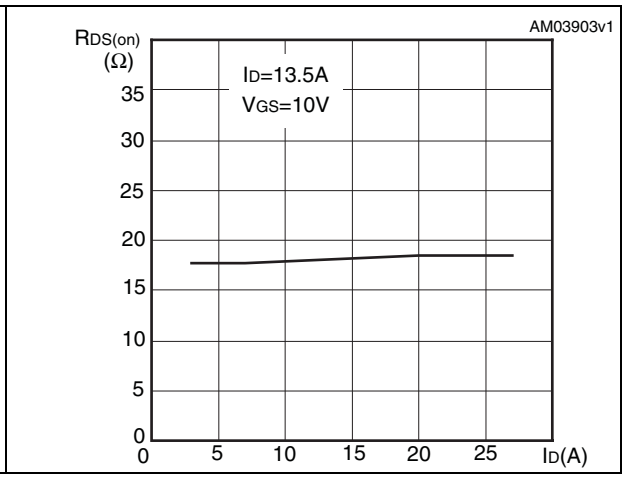


Figure 8. Gate charge vs gate-source voltage

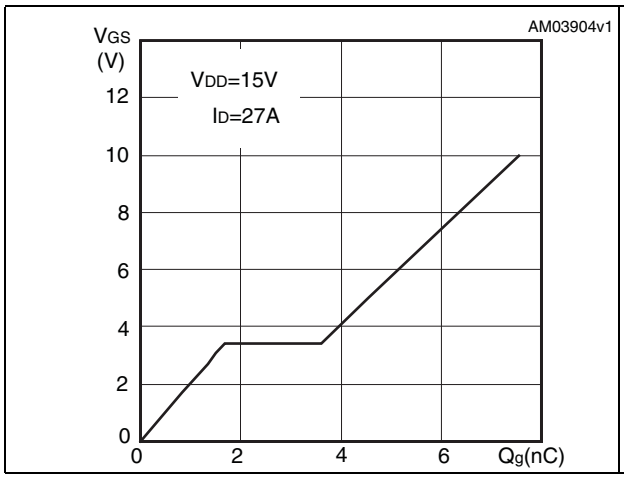


Figure 9. Capacitance variations

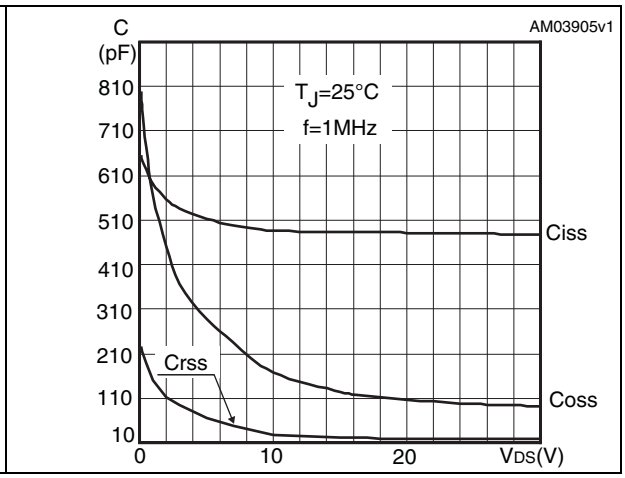


Figure 10. Normalized gate threshold voltage vs temperature

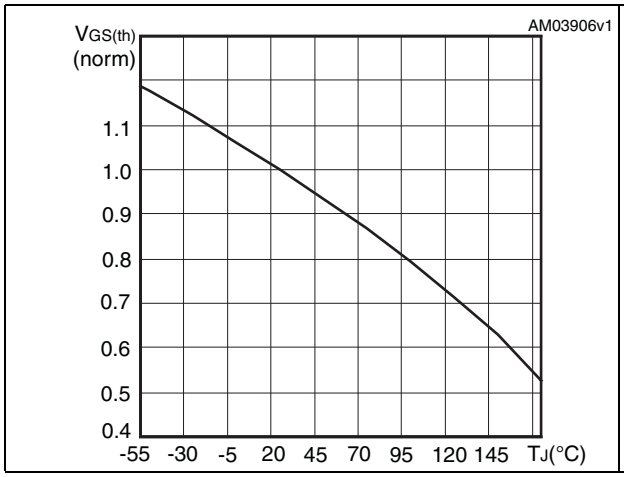


Figure 11. Normalized on resistance vs temperature

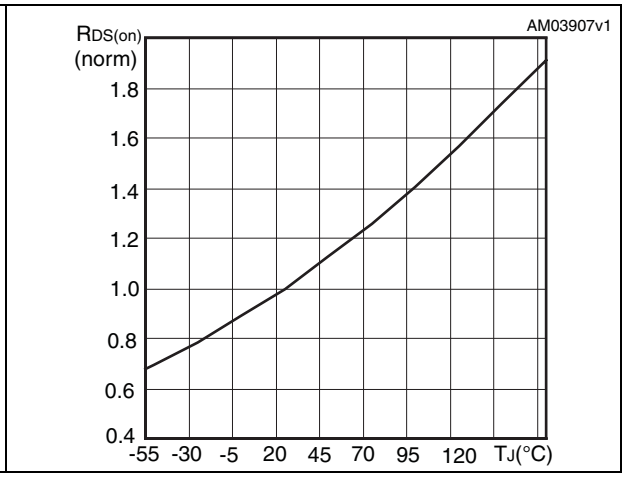
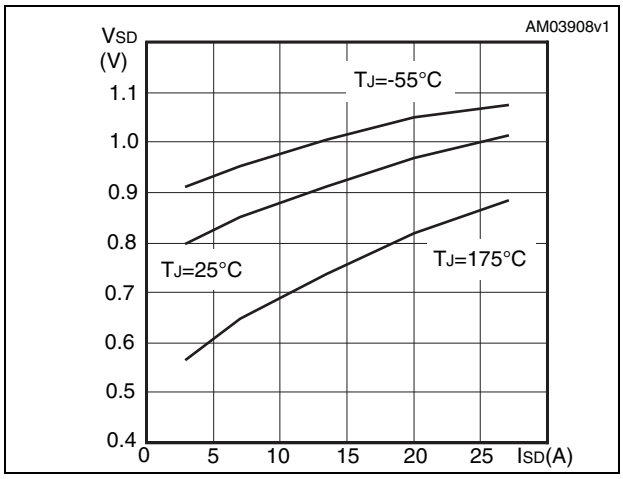


Figure 12. Source-drain diode forward characteristics



3 Test circuits

Figure 13. Switching times test circuit for resistive load

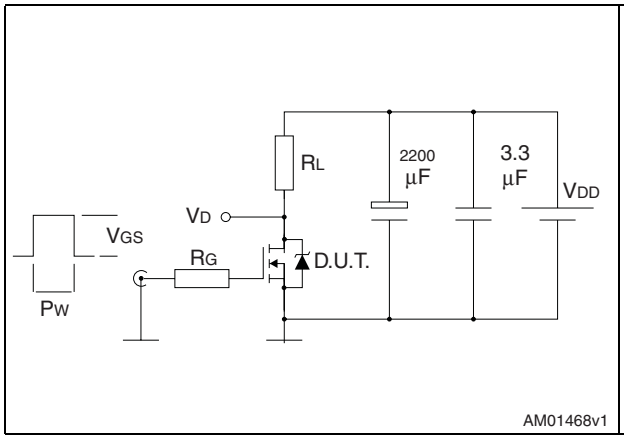


Figure 14. Gate charge test circuit

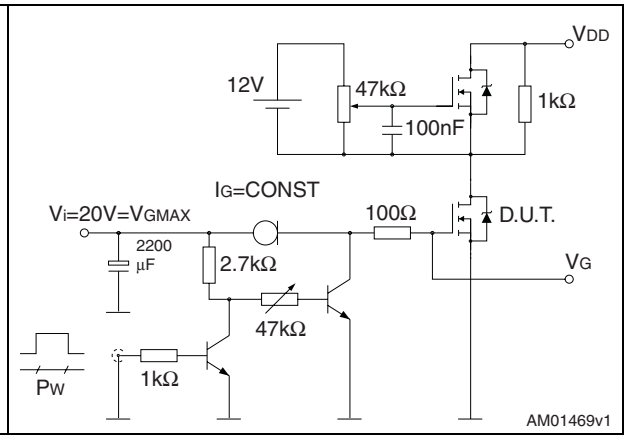


Figure 15. Test circuit for inductive load switching and diode recovery times

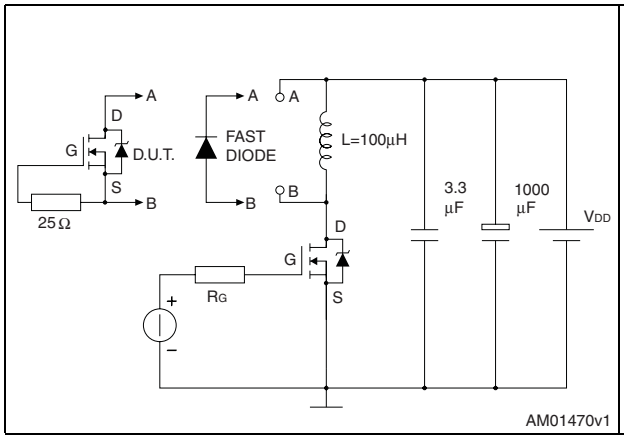


Figure 16. Unclamped inductive load test circuit

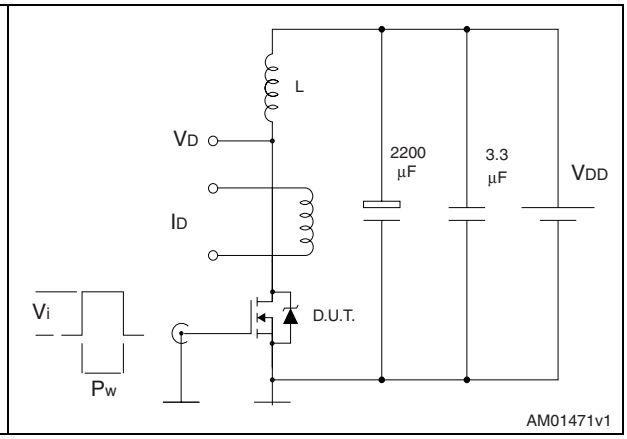


Figure 17. Unclamped inductive waveform

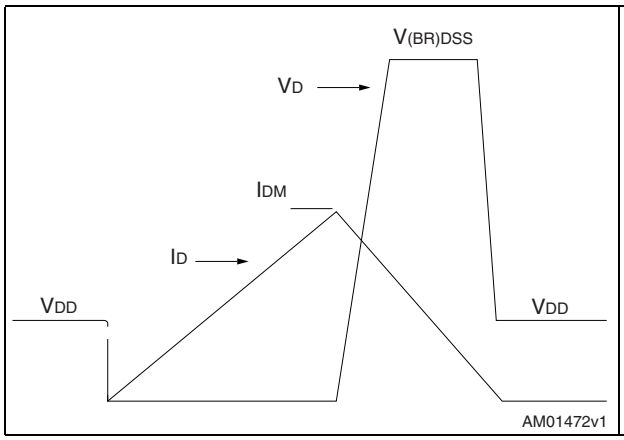


Figure 18. Switching time waveform

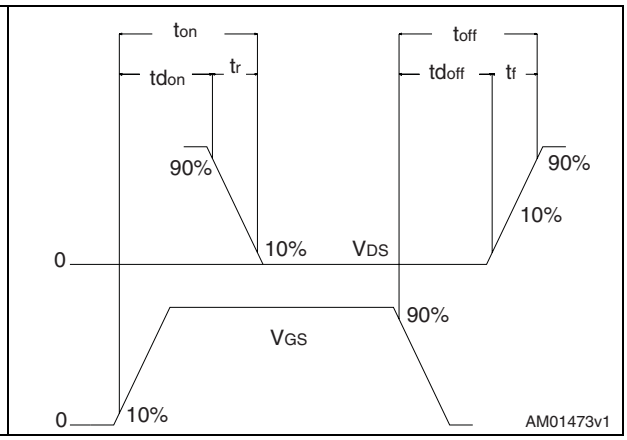
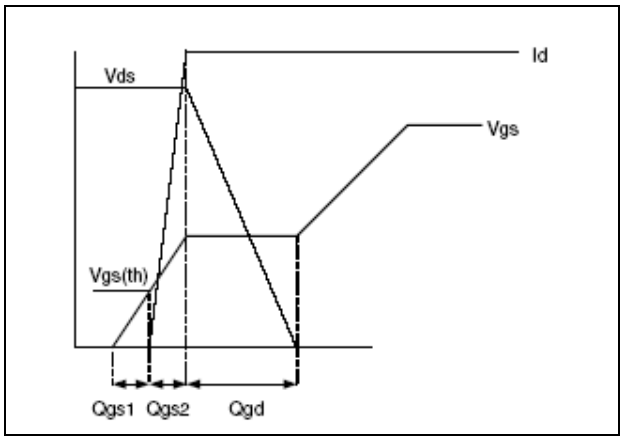


Figure 19. Gate charge waveform

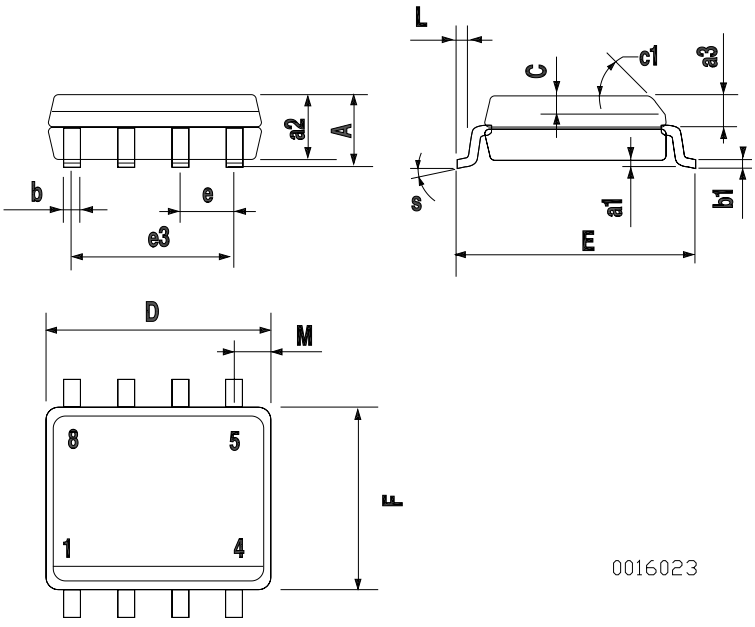


4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

SO-8 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			1.75			0.068
a1	0.1		0.25	0.003		0.009
a2			1.65			0.064
a3	0.65		0.85	0.025		0.033
b	0.35		0.48	0.013		0.018
b1	0.19		0.25	0.007		0.010
C	0.25		0.5	0.010		0.019
c1	45 (typ.)					
D	4.8		5.0	0.188		0.196
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		3.81			0.150	
F	3.8		4.0	0.14		0.157
L	0.4		1.27	0.015		0.050
M			0.6			0.023
S	8 (max.)					



5 Revision history

Table 8. Document revision history

Date	Revision	Changes
12-May-2009	1	First release

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