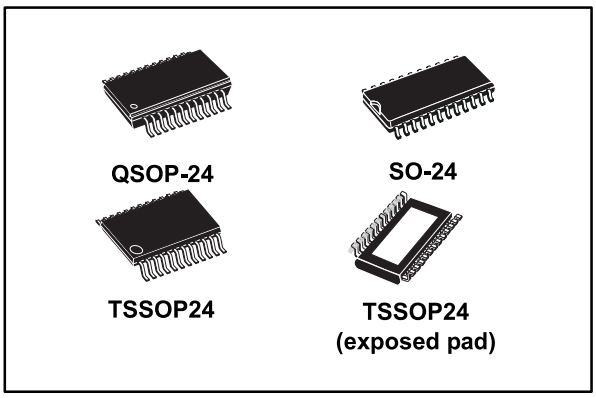
STP16DPP05

Low voltage 16-bit constant current LED sink driver with output error detection

Datasheet - production data



Features

- Low voltage power supply down to 3 V
- 16 constant current output channels
- Adjustable output current through external resistor
- Short and open output error detection
- Serial data IN/parallel data OUT
- 3.3 V MCU-driving capability
- Output current: 3 to 40 mA
- 30 MHz clock frequency
- Available in high thermal efficiency TSSOP exposed pad
- ESD protection: 2 kV HBM, 200 V MM

Description

The STP16DPP05 is a monolithic, low voltage, low current power 16-bit shift register designed for LED panel displays. The device features a 16-bit serial-in, parallel-out shift register that feeds a 16- bit D-type storage register. In the output stage, sixteen regulated current sources are designed to provide 3 to 40 mA of constant current to drive the LEDs. The STP16DPP05 features open and short LED detection on the outputs. The detection circuit checks for 3 different conditions that can occur on the output line: short to GND, short to V_O or open line. The data detection results are loaded in the shift registers and shifted out via the serial line output. The detection functionality is implemented without increasing the pin count, through a secondary function of the output enable and latch pin (DM1 and DM2 respectively). A dedicated logic sequence allows the device to enter or exit from detection mode. The STP16DPP05 output current can be adjusted through an external resistor to control the light intensity of the LEDs. LED brightness is adjustable from 0% to 100% via the $\overline{\text{OE/DM2}}$ pin. The STP16DPP05 guarantees a 20 V output driving capability, allowing users to connect more LEDs in series. The high 30 MHz clock frequency makes the device suitable for high data rate transmission. The 3.3 V supply is well suited for applications which interface a 3.3 V MCU. Compared to a standard TSSOP package, the TSSOP with exposed pad increases heat dissipation capability by a factor of 2.5.

Table 1: Device summary

Order code	Package	Packing
STP16DPP05MTR	SO-24 (tape and reel)	1000 parts per reel
STP16DPP05TTR	TSSOP24 (tape and reel)	2500 parts per reel
STP16DPP05XTTR	TSSOP24 exposed pad (tape and reel)	2500 parts per reel
STP16DPP05PTR	QSOP-24	2500 parts per reel

This is information on a product in full production.

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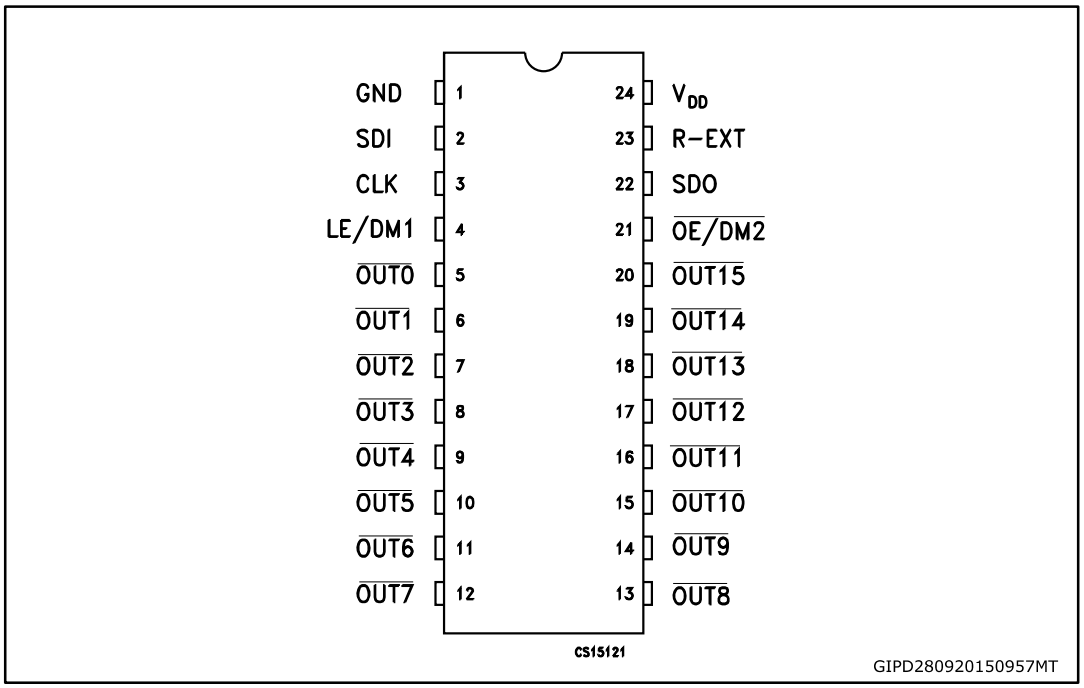
1 Summary description

Table 2: Typical current accuracy

Output voltage	Current accuracy		Output current	V_{DD}	Temperature
	Between bits	Between ICs			
≥ 1.3 V	± 1%	± 2%	5 to 40 mA	3.3 V to 5 V	25 °C

1.1 Pin connection and description

Figure 1: Pin connection



The exposed pad should be electrically connected to a metal land electrically isolated or connected to ground.

Table 3: Pin description

Pin n°	Symbol	Name and function
1	GND	Ground terminal
2	SDI	Serial data input terminal
3	CLK	Clock input terminal
4	LE/DM1	Latch input terminal - detect mode 1 (see operation principle)
5-20	OUT 0-15	Output terminal
21	OE/DM2	Input terminal of output enable (active low) - detect mode 1 (see operation principle)
22	SDO	Serial data out terminal
23	R-EXT	Input terminal for an external resistor for constant current programming
24	V_{DD}	Supply voltage terminal

2 Electrical ratings

2.1 Absolute maximum ratings

Stressing the device above the ratings listed in the “absolute maximum ratings” table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other condition above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 4: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DD}	Supply voltage	0 to 7	V
V_O	Output voltage	-0.5 to 20	V
I_O	Output current	50	mA
V_I	Input voltage	-0.4 to V_{DD}	V
I_{GND}	GND terminal current	800	mA
f_{CLK}	Clock frequency	50	MHz
T_J	Junction temperature range (1)	-40 to +170	°C

Notes:

(1) Such absolute value is based on the thermal shutdown protection.

2.2 Thermal data

Table 5: Thermal data

Symbol	Parameter		Value	Unit
T_A	Operating free-air temperature range		-40 to +125	°C
$T_{J\text{-}OPR}$	Operating thermal junction temperature range		-40 to +150	°C
T_{STG}	Storage temperature range		-55 to +150	°C
R_{thJA}	Thermal resistance junction-ambient (1)	SO-24	42.7	°C/W
		TSSOP24	55	°C/W
		TSSOP24 (2) exposed pad	37.5	°C/W
		QSOP-24	55	°C/W

Notes:

(1) According with JEDEC standard 51-7.

(2) The exposed pad should be soldered directly to the PCB to obtain the thermal benefits.

2.3 Recommended operating conditions

Table 6: Recommended operating conditions

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{DD}	Supply voltage		3		5.5	V
V_O	Output voltage				20	V
I_O	Output current	OUTn	3		40	mA
I_{OH}	Output current	SERIAL-OUT			1	mA
I_{OL}	Output current	SERIAL-OUT			-1	mA
V_{IH}	Input voltage		0.7 V_{DD}		V_{DD}	V
V_{IL}	Input voltage		-0.3		0.3 V_{DD}	V
t_{wLAT}	LE/DM1 pulse width	V_{DD} = 3.0 V to 5.0 V	20			ns
t_{wCLK}	CLK pulse width		10			ns
t_{wEN}	$\overline{OE/DM2}$ pulse width		100			ns
$t_{SETUP(D)}$	Setup time for DATA					ns
$t_{HOLD(D)}$	Hold time for DATA		5			ns
$t_{SETUP(L)}$	Setup time for LATCH		8			ns
f_{CLK}	Clock frequency	Cascade operation (1)			30	MHz

Notes:

(1) If the device is connected in cascade, it may not be possible achieve the maximum data transfer. Please consider the timings carefully.

3 Electrical characteristics

V_{DD} = 3.3 V to 5 V, T_A = 25 °C, unless otherwise specified.

Table 7: Electrical characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{IH}	Input voltage high level		0.7 V_{DD}		VDD	V
V_{IL}	Input voltage low level		GND		0.3 VDD	V
I_{OH}	Output leakage current	V_{OH} = 20 V			1	µA
V_{OL}	Output voltage (serial-OUT)	I_{OL} = 1 mA			0.4	V
V_{OH}	Output voltage (serial-OUT)	I_{OH} = -1 mA	V_{DD}-0.4V			V
I_{OL1}	Output current	V_O = 0.3 V, R_{ext} = 4 kΩ	4.75	5	5.25	
I_{OL2}		V_O = 0.3 V, R_{ext} = 1 kΩ	19	20	21	
I_{OL3}		V_O = 1.3 V, R_{ext} = 497 Ω	38	40	42	mA
ΔI_{OL1}	Output current error between bit (all output ON)	V_O = 0.3 V, I_O = 5 mA R_{ext} = 4 kΩ		± 1	± 5	
ΔI_{OL2}		V_O = 0.3 V, I_O = 20 mA R_{ext} = 980 Ω		± 0.5	± 3	%
ΔI_{OL3}		V_O = 1.3 V, I_O = 40 mA R_{ext} = 490 Ω		± 0.5	± 3	
$R_{SIN(up)}$	Pull-up resistor		150	300	600	kΩ
$R_{SIN(down)}$	Pull-down resistor		100	200	400	kΩ
$I_{DD(OFF1)}$	Supply current (OFF)	R_{ext} = 1 kΩ, I_{OUT} = 20 mA, OUT 0 to 15 = OFF		5.4	7.5	mA
$I_{DD(OFF2)}$		R_{ext} = 497 Ω, I_{OUT} = 40 mA OUT 0 to 15 = OFF		8	9.5	
$I_{DD(ON1)}$	Supply current (ON)	R_{ext} = 1 kΩ, I_{OUT} = 20 mA, OUT 0 to 15 = ON		5.5	7.5	
$I_{DD(ON2)}$		R_{ext} = 497 Ω, I_{OUT} = 40 mA OUT 0 to 15 = ON		8.1	9.5	
Thermal	Thermal protection			170		°C

V_{DD} = 3.3 V to 5 V, T_A = 25 °C, unless otherwise specified.

Table 8: Switching characteristics

Symbol	Parameter	Test conditions		Min.	Typ.	Max.	Unit
t_{PLH1}	Propagation delay time, CLK- $\overline{OUTn}$, LE/DM1 = H, $\overline{OE/DM2}$ = L	$V_{IH} = V_{DD}$ V_{IL} = GND C_L = 10 pF I_O = 20 mA V_L = 3.0 V R_{ext} = 1 KΩ R_L = 60 Ω	V_{DD} = 3.3 V		35.5	44.5	
			V_{DD} = 5 V		18.5	24	ns
t_{PLH2}	Propagation delay time, LE/DM1- $\overline{OUTn}$, $\overline{OE/DM2}$ = L		V_{DD} = 3.3 V		41.5	50	
			V_{DD} = 5 V		23	29	ns
t_{PLH3}	Propagation delay time, $\overline{OE/DM2}$ - $\overline{OUTn}$, LE = H		V_{DD} = 3.3 V		45	54	
			V_{DD} = 5 V		25	31	ns
t_{PLH}	Propagation delay time, CLK-SDO		V_{DD} = 3.3 V	15	21	31	
			V_{DD} = 5 V	11	15	21	ns
t_{PHL1}	Propagation delay time, CLK- $\overline{OUTn}$, LE/DM1 = H, $\overline{OE/DM2}$ = L		V_{DD} = 3.3 V		13.7	18	
			V_{DD} = 5 V		8.8	12.5	ns
t_{PHL2}	Propagation delay time, LE/DM1 -$\overline{OUTn}$, $\overline{OE/DM2}$ = L		V_{DD} = 3.3 V		17	22	
			V_{DD} = 5 V		13	17	ns
t_{PHL3}	Propagation delay time, $\overline{OE/DM2}$ - $\overline{OUTn}$, LE/DM1 = H		V_{DD} = 3.3 V		12.7	17	
			V_{DD} = 5 V		9.5	13	ns
t_{PHL}	Propagation delay time, CLK-SDO		V_{DD} = 3.3 V	17.5	24	36	
			V_{DD} = 5 V	12.5	17	25	ns
t_{ON}	Output rise time 10~90% of voltage waveform		V_{DD} = 3.3 V		28	39	
			V_{DD} = 5 V		17	23	ns
t_{OFF}	Output fall time 90~10% of voltage waveform		V_{DD} = 3.3 V		4.5	6	
			V_{DD} = 5 V		3.5	5	ns
t_r	CLK rise time (1)					5000	ns
t_f	CLK fall time (1)					5000	ns

Notes:

(1) In order to achieve high cascade data transfer, please consider tr/tf timings carefully.

4 Equivalent circuit and outputs

Figure 2: OE/DM2 terminal

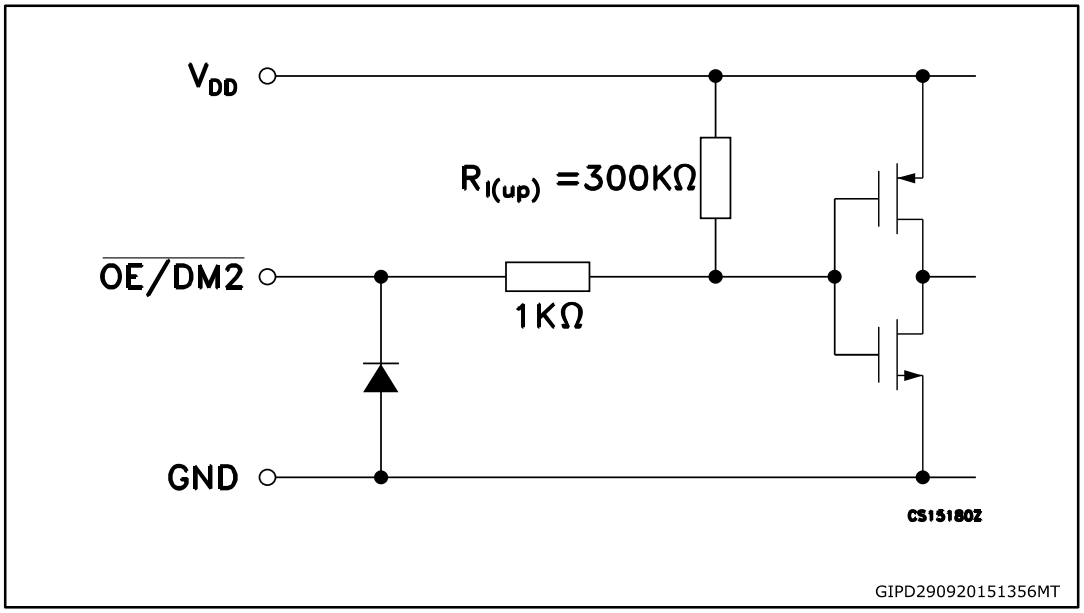


Figure 3: LE/DM1 terminal

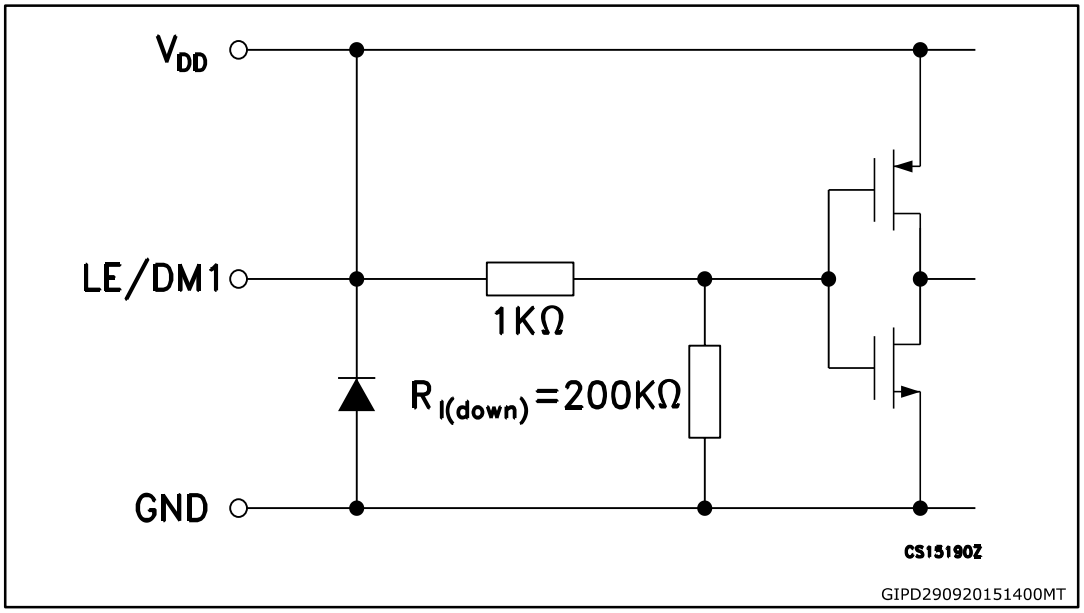


Figure 4: CLK, SDI terminal

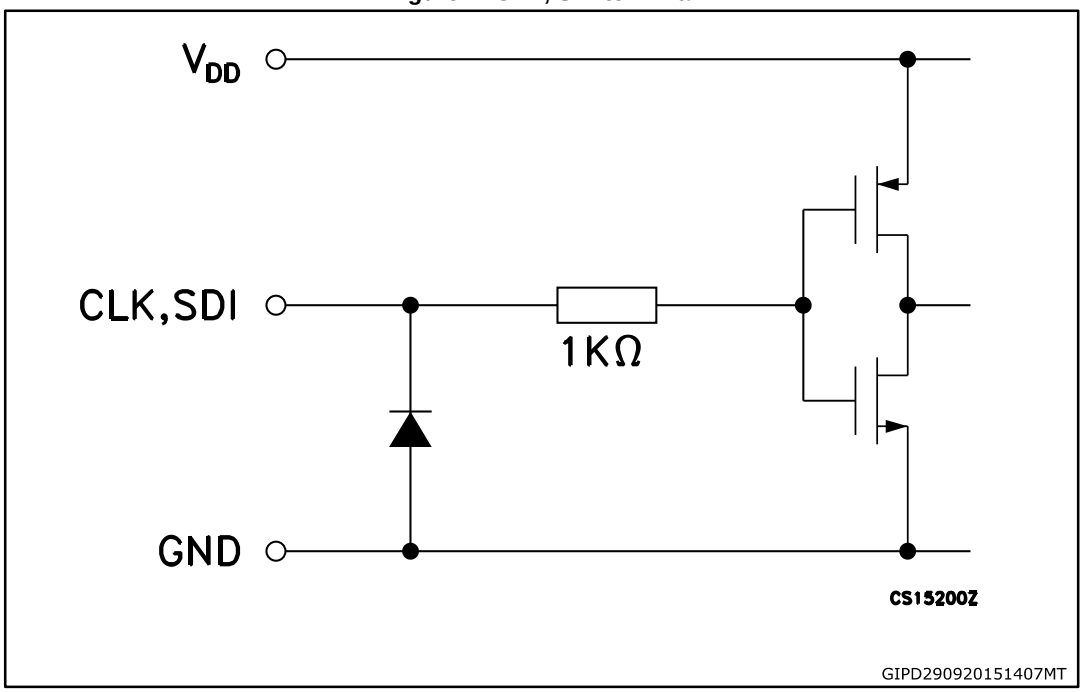


Figure 5: SDO terminal

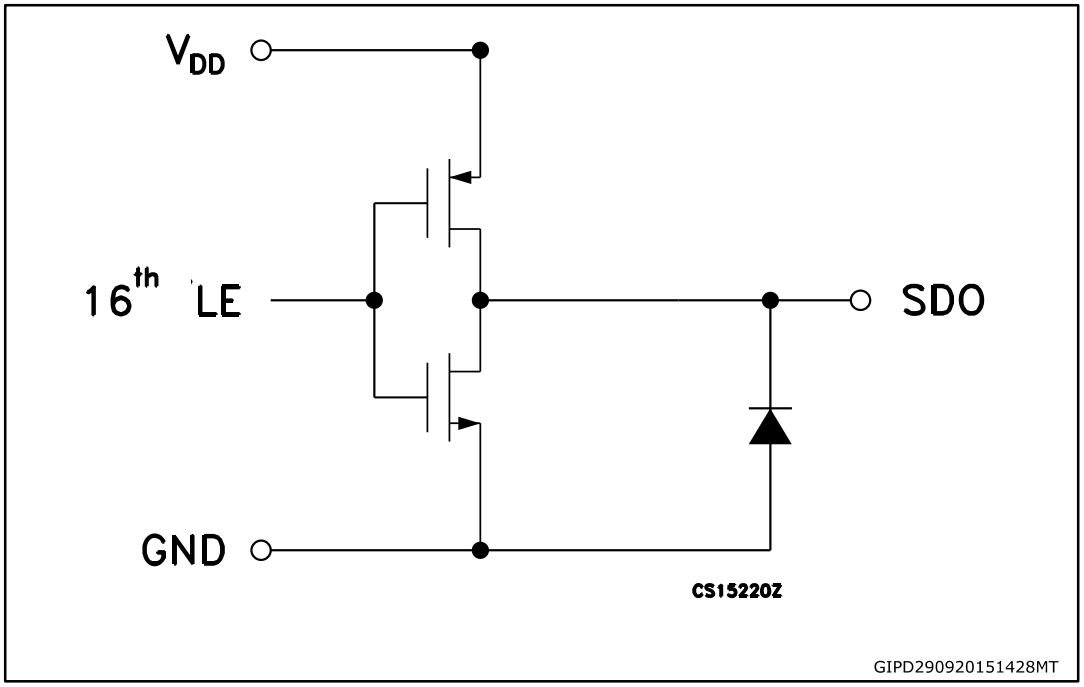
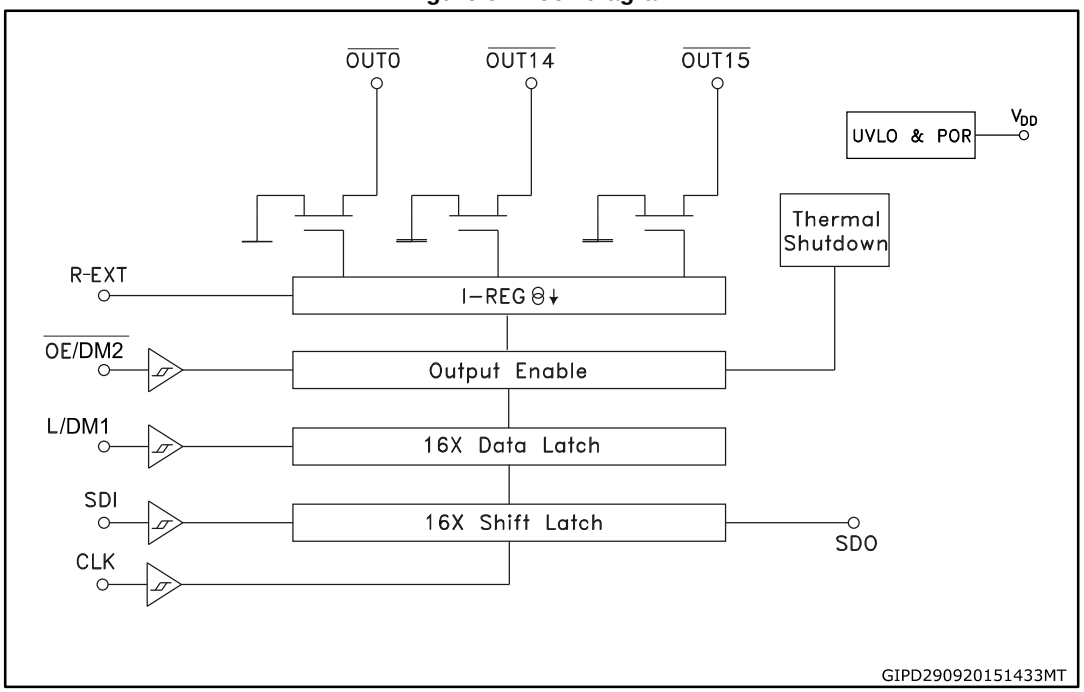


Figure 6: Block diagram



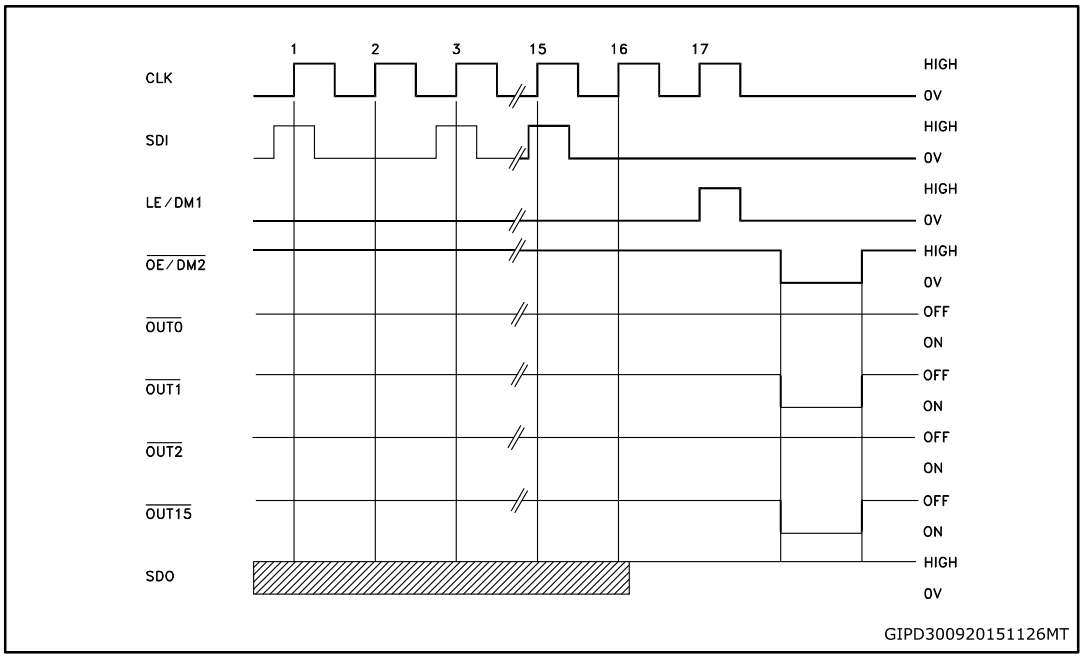
5 Timing diagrams

Table 9: Truth table

CLOCK	LE/DM1	$\overline{OE/DM2}$	SERIAL-IN	$\overline{OUT0}$ ..... $\overline{OUT7}$ ..... $\overline{OUT15}$	SDO
_|‾	H	L	Dn	Dn ..... Dn - 7 ..... Dn -15	Dn - 15
_|‾	L	L	Dn + 1	No change	Dn - 14
_|‾	H	L	Dn + 2	Dn + 2 ..... Dn - 5 ..... Dn -13	Dn - 13
‾|_	X	L	Dn + 3	Dn + 2 ..... Dn - 5 ..... Dn -13	Dn - 13
‾|_	X	H	Dn + 3	OFF	Dn - 13

OUTn = ON when Dn = H OUTn = OFF when Dn = L.

Figure 7: Timing diagram



1 Latch and output enable terminals are level-sensitive and are not synchronized with rising or falling edge of CLK signal.

2 When LE/DM1 terminal is low level, the latch circuit holds previous set of data.

3 When LE/DM1 terminal is high level, the latch circuit refreshes new set of data from SDI chain.

4 When $\overline{OE/DM2}$ terminal is at low level, the output terminals Out 0 to Out 15 respond to data in the latch circuits, either '1' for ON or '0' for OFF.

5 When $\overline{OE/DM2}$ terminal is at high level, all output terminals are switched OFF.

Table 10: Enable IO: shutdown truth table

CLOCK	LE/DM1	SDI0 .....SDI7..... SDI15	SH	Auto power-up	OUTn
_|‾	H	All = L	Active	Not active (1)	OFF
_|‾	L	No change	No change	No change	No change
_|‾	H	One or more = H	Not active	Active	X (2)

Notes:

(1) At power-up, the device starts in shutdown mode.

(2) Undefined.

Figure 8: Clock, serial-in, serial-out

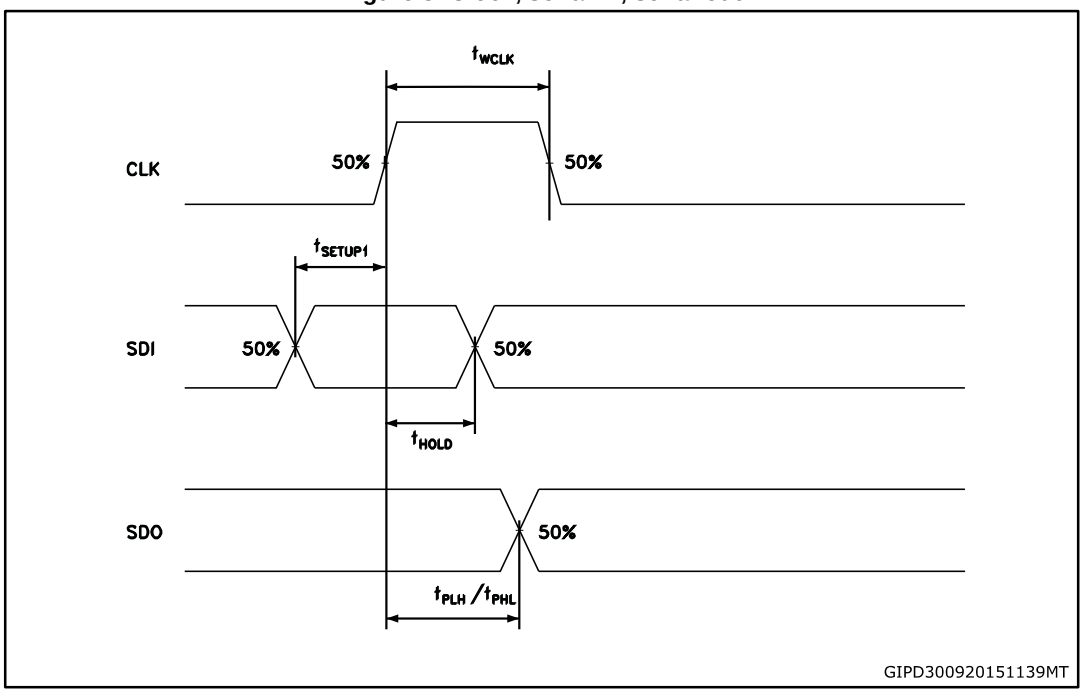


Figure 9: Clock, serial-in, latch, enable, outputs

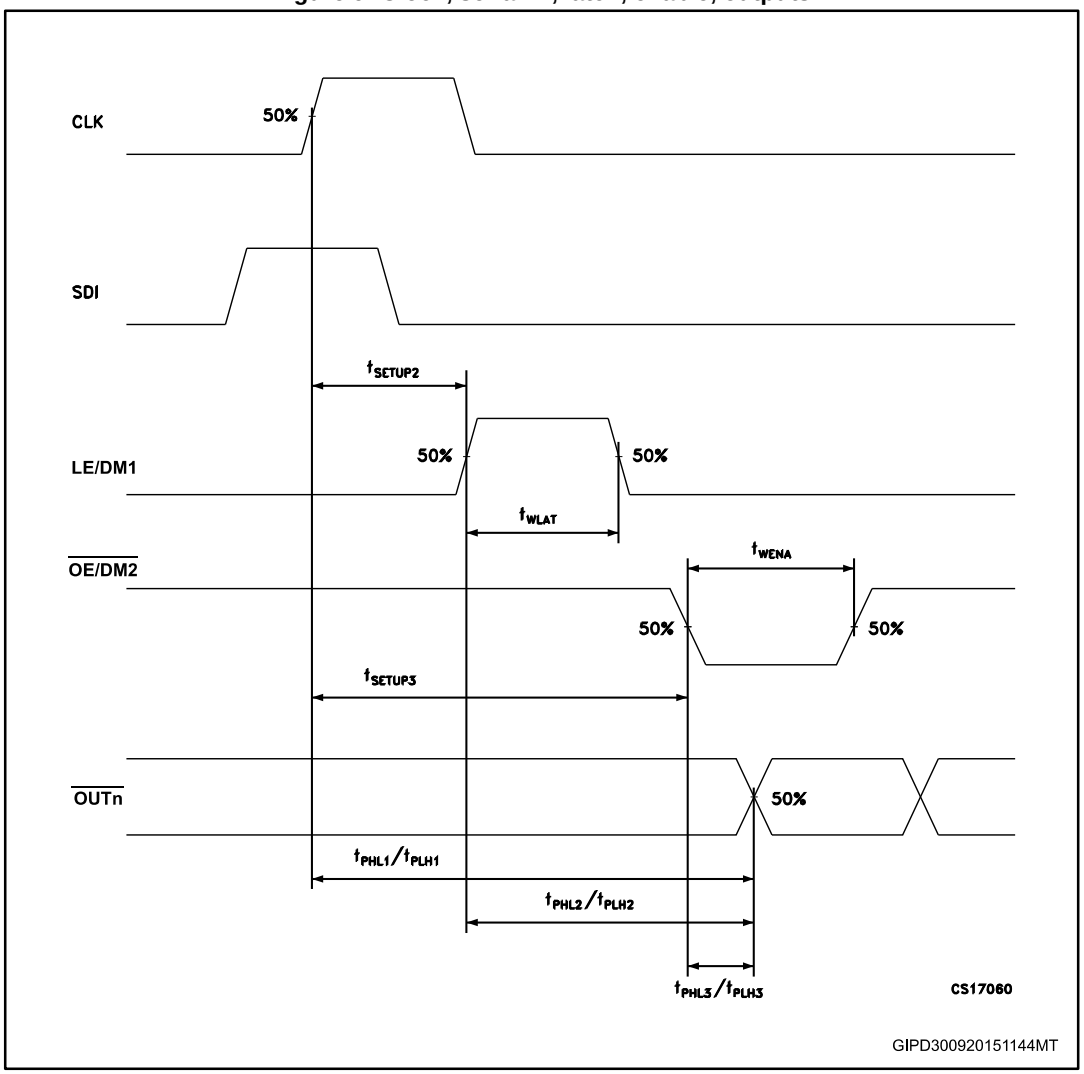
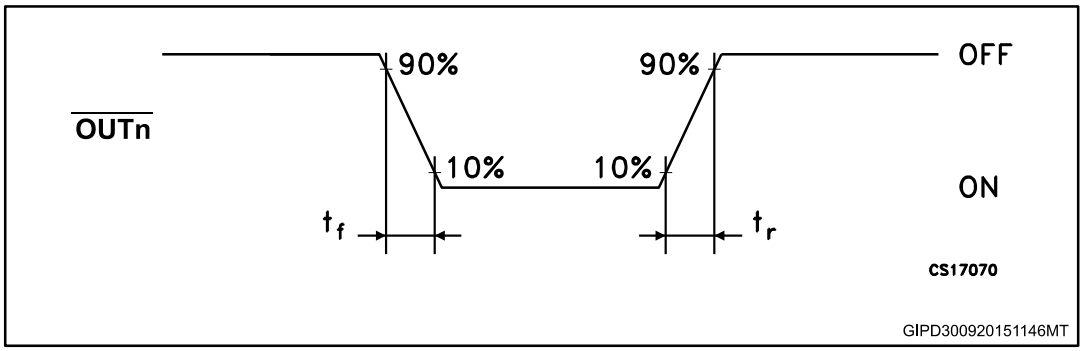


Figure 10: Outputs



6 Typical characteristics

Figure 11: Output current vs. R-EXT resistor

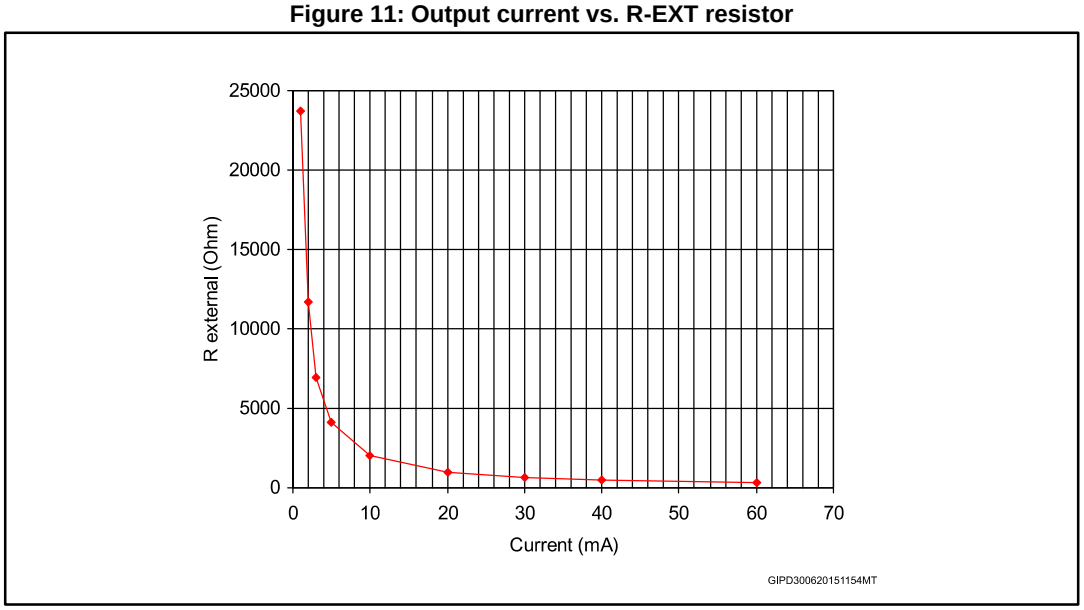


Table 11: Output current vs. R-EXT resistor

R-EXT (Ω)	Output current (mA)
23700	1
11730	2
6930	3
4090	5
2025	10
1000	20
667	30
497	40
331	60

Conditions: temperature = 25 °C, V_{DD} = 3.3 V; 5.0 V, I_{SET} = 3 mA; 5 mA; 10 mA; 20 mA; 50 mA; 60 mA.

Figure 12: I_{SET} vs. dropout voltage (V_{drop})

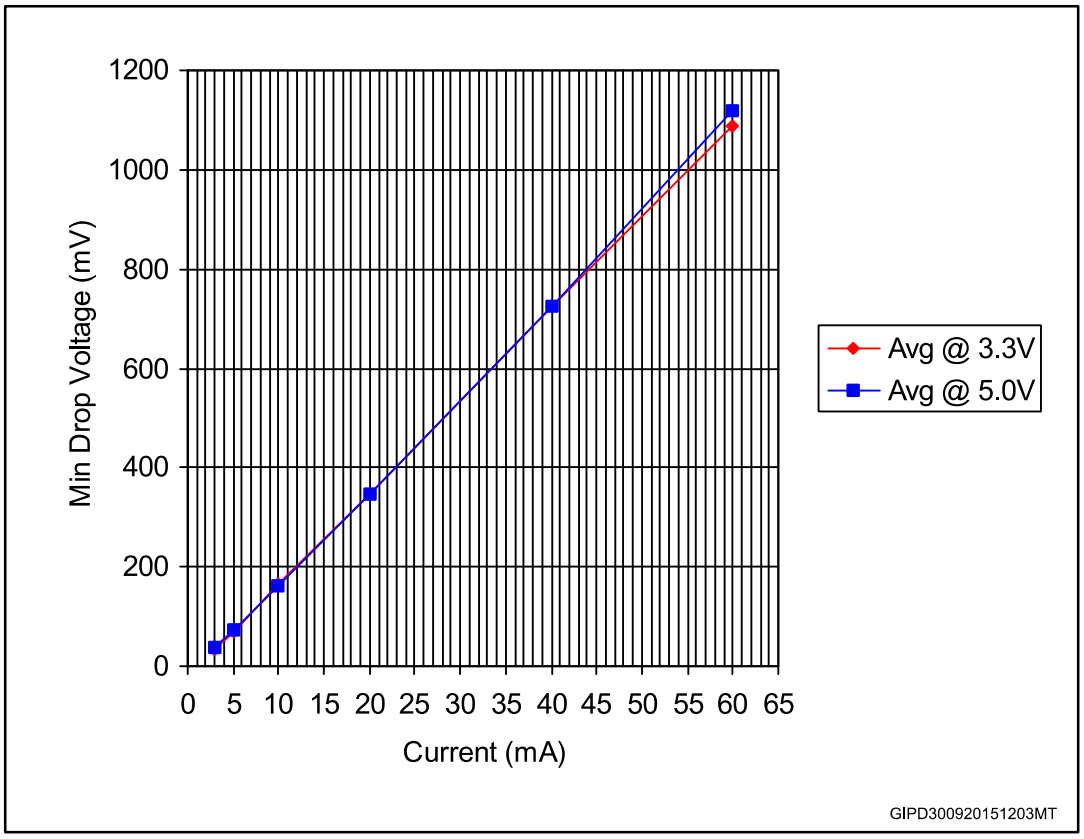


Table 12: I_{SET} vs. dropout voltage (V_{drop})

Iout (mA)	Avg (mV) @ 3.3 V	Avg (mV) @ 5.0 V
3	36	37
5	71	72
10	163	163
20	346	347
40	724	726
60	1080	1110

T_A = 25 °C, V_{dd} = 3.3 V; 5 V

Figure 13: Output current vs. ± ΔI_{OL}(%)

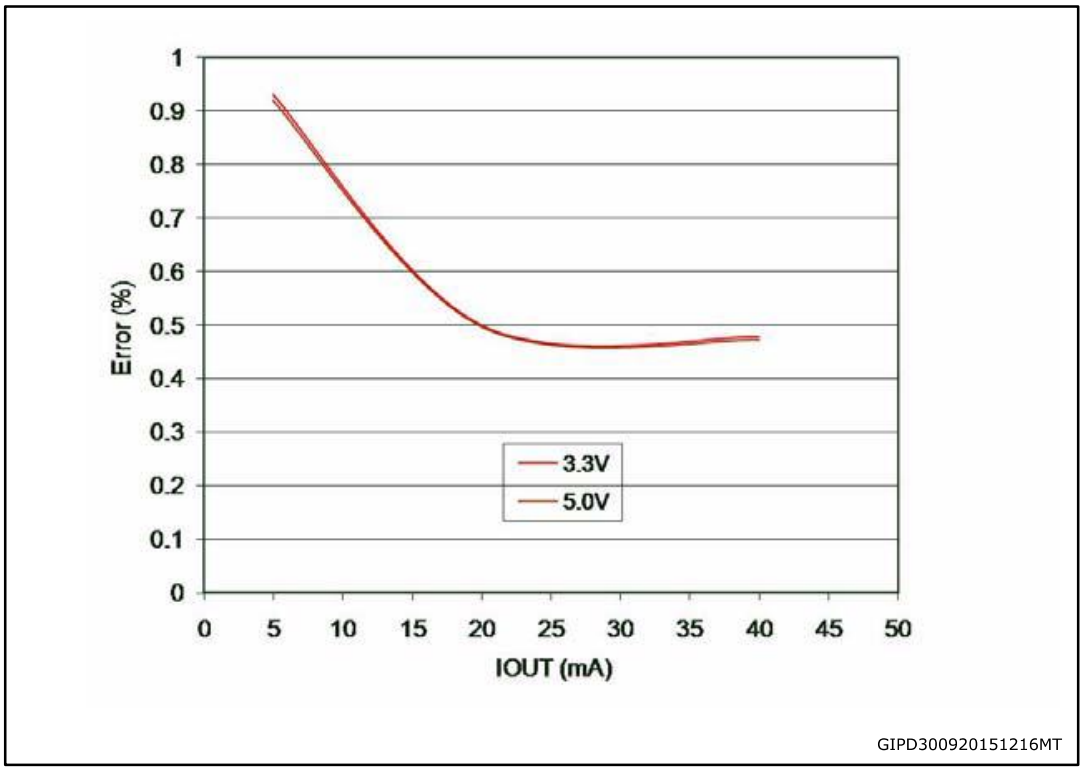


Figure 14: Idd ON/OFF

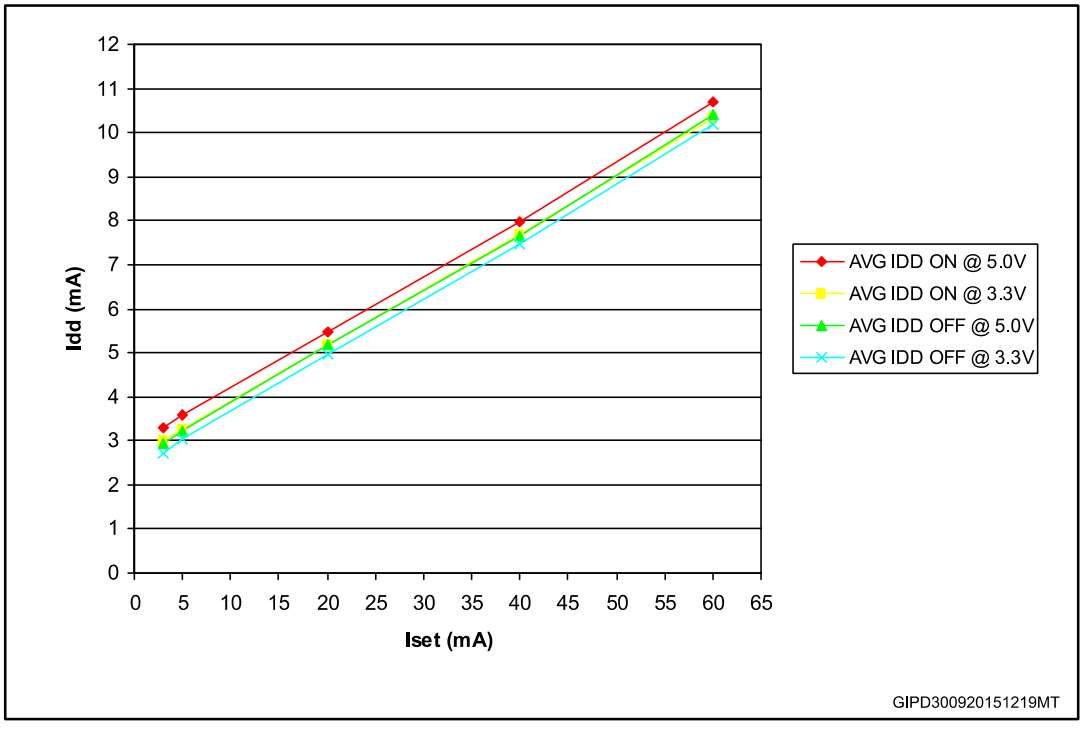
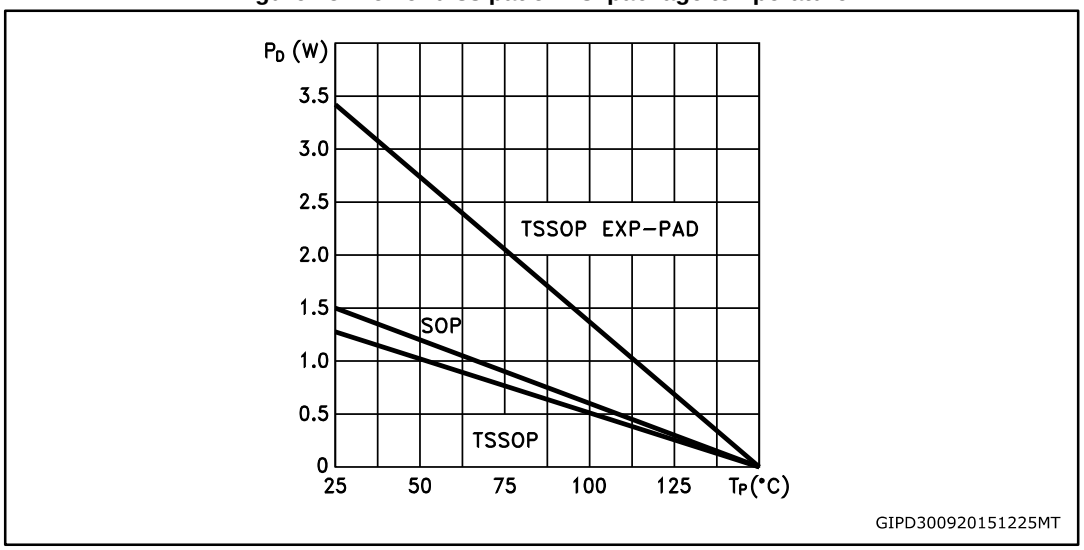


Figure 15: Power dissipation vs. package temperature



The exposed pad should be soldered to the PCB to obtain the thermal benefits.

Figure 16: Turn ON output current characteristics *(1)*

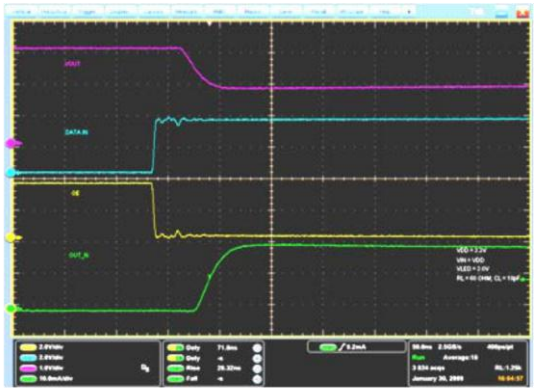
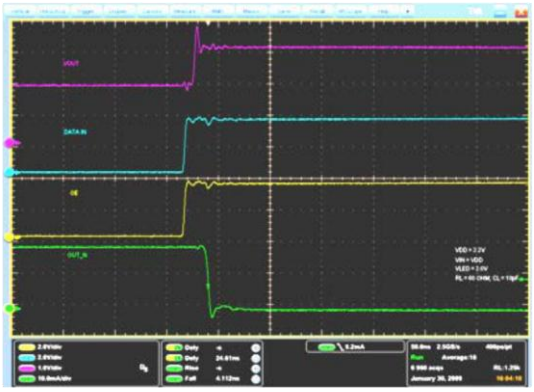


Figure 17: Turn OFF output current characteristics *(2)*



Notes:

(1) The reference level for the TON characteristics is 50% of $\overline{\text{OE/DM2}}$ signal and 90% of output current.

(2) The reference level for the TOFF characteristics is 50% of $\overline{\text{OE/DM2}}$ signal and 10% of output current.

Electrical conditions: Vdd = 3.3 V, Vin = Vdd, Vled = 3.0 V, RL = 60 Ω, CL = 10 pF Ch1 (Yellow) = $\overline{\text{OE/DM2}}$, Ch2 (Blue) = SDI, Ch3 (Purple) = VOUT, Ch4 (Green) = OUT

7 Error detection mode functionality

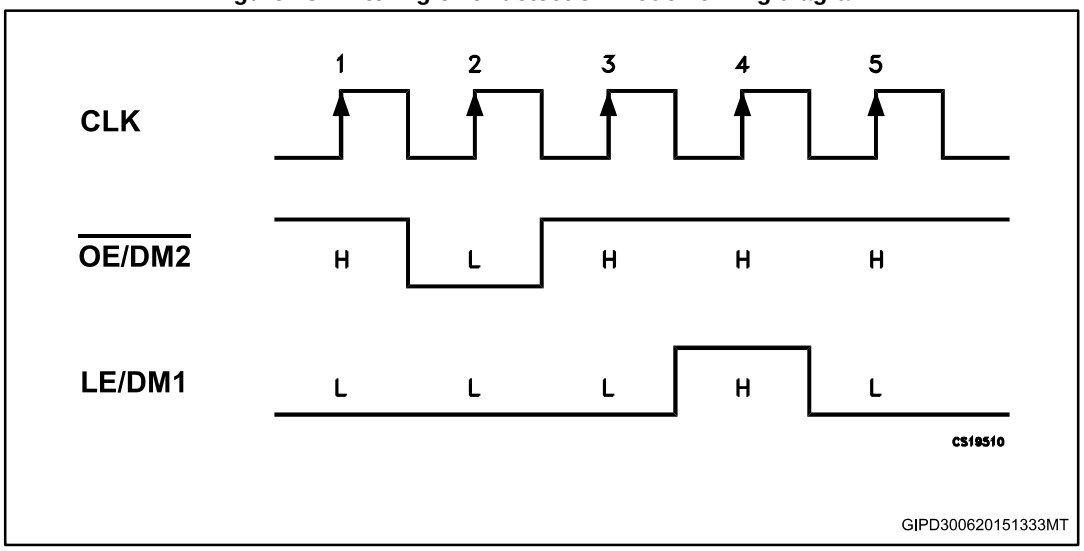
7.1 Phase one: entering error detection mode

From the “normal mode” condition the device can switch to “error mode” by a logic sequence on the $\overline{\text{OE/DM2}}$ and LE/DM1 pins, as shown in the following table and diagram:

Table 13: Entering error detection mode - truth table

CLK	1°	2°	3°	4°	5°
$\overline{\text{OE/DM2}}$	H	L	H	H	H
LE/DM1	L	L	L	H	L

Figure 18: Entering error detection mode - timing diagram

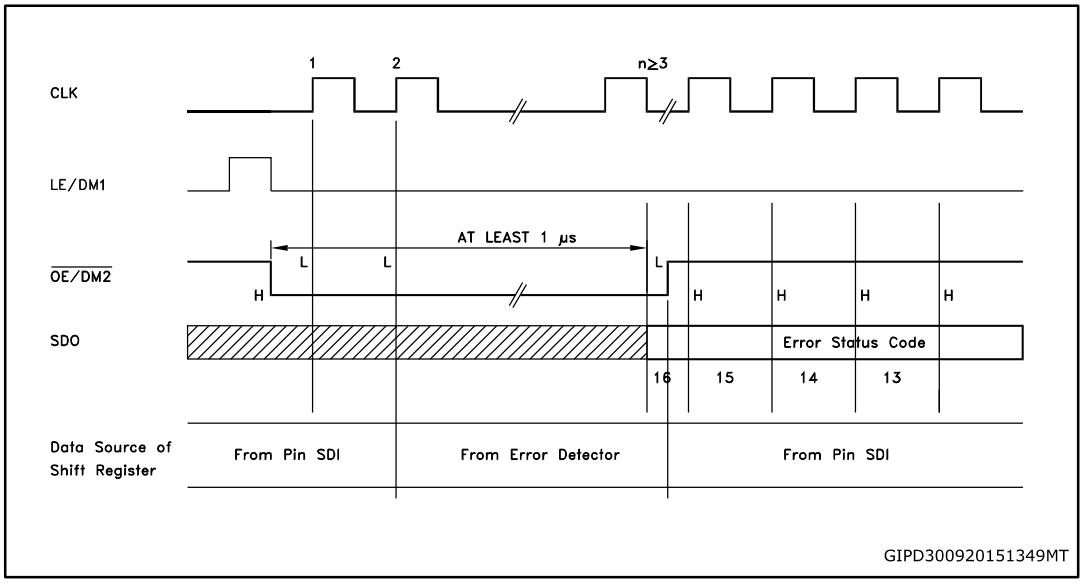


After these five CLK cycles, the device goes into “error detection mode” and at the rising edge of the 6th CLK cycle, the SDI data are ready for sampling.

7.2 Phase two: error detection

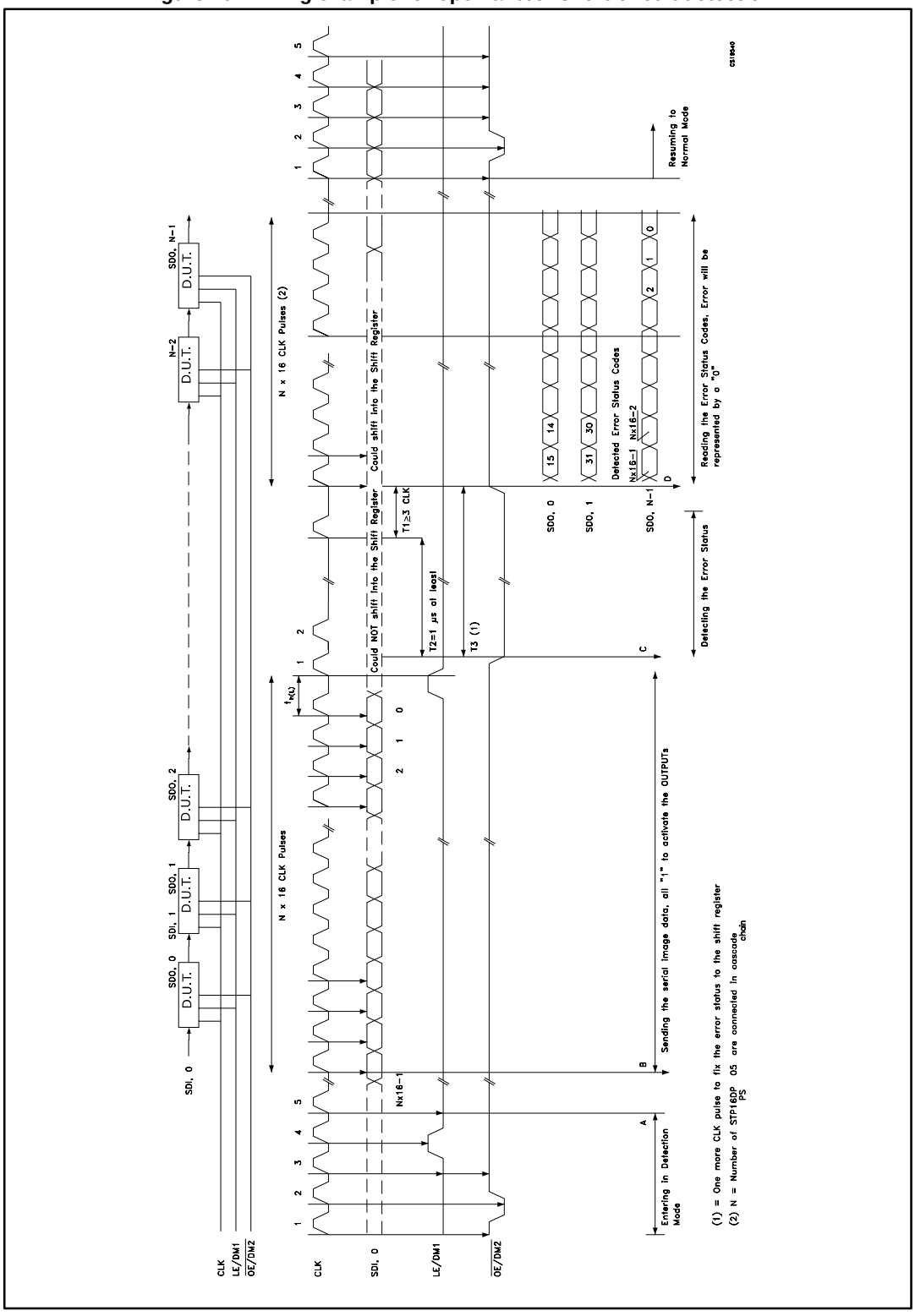
The 16 data bits must be set to “1” in order for all the outputs to be ON during error detection. The data are latched by LE/DM1, after which the outputs are ready for the detection process. When the microcontroller switches the $\overline{\text{OE/DM2}}$ to LOW, the device drives the LEDs to analyze if an OPEN or SHORT condition has occurred.

Figure 19: Detection diagram



The status of the LEDs is detected in at least 1 microsecond, and after this period the microcontroller sets $\overline{\text{OE/DM2}}$ to HIGH state and the output data detection result is sent to the microcontroller via SDO. Error detection mode and normal mode both use the same data format. As soon as all the detection data bits are available on the serial line, the device may return to normal mode of operation. To re-detect the status, the device must first return to normal mode and reenter error detection mode.

Figure 20: Timing example for open and/or short-circuit detection



7.3 Phase three: resuming normal mode

The sequence for reentering normal mode is shown in the following table:

Table 14: Resuming normal mode - timing diagram

CLK	1°	2°	3°	4°	5°
$\overline{OE/DM2}$	H	L	H	H	H
LE/DM1	L	L	L	L	L

For proper device operation, the “entering error detection” sequence must be followed by a “resume mode” sequence, it is not possible to insert consecutive equal sequences.

7.4 Error detection conditions

Table 15: Detection conditions (VDD = 3.3 to 5 V, temperature range -40 to 125 °C)

Configuration	Detect mode	Detection results		
SW-1 or SW-3b	Open line or output short to GND detected	==> $I_{ODEC} \leq 0.5 \times I_O$	No error detected	==> $I_{ODEC} \geq 0.5 \times I_O$
SW-2 or SW-3a	Short on LED or short to V-LED detected	==> $V_O \geq 2.6$ V	No error detected	==> $V_O \leq 2.3$ V

Where: I_O = the output current programmed by the R-EXT, I_{ODEC} = the detected output current in detection mode

Figure 21: Detection circuit

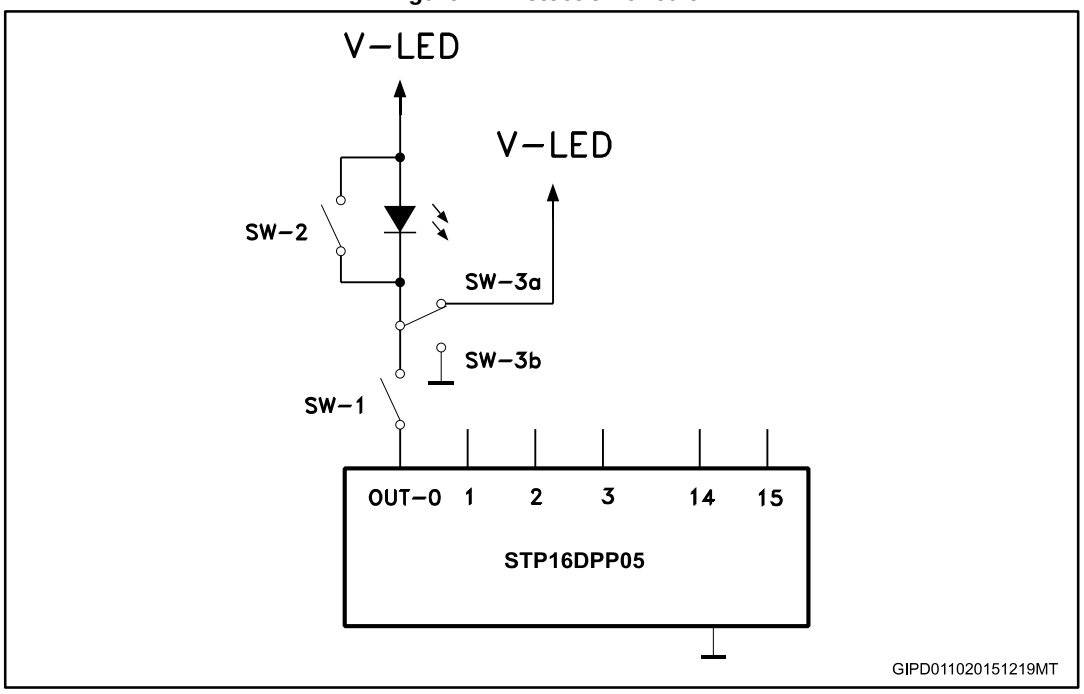
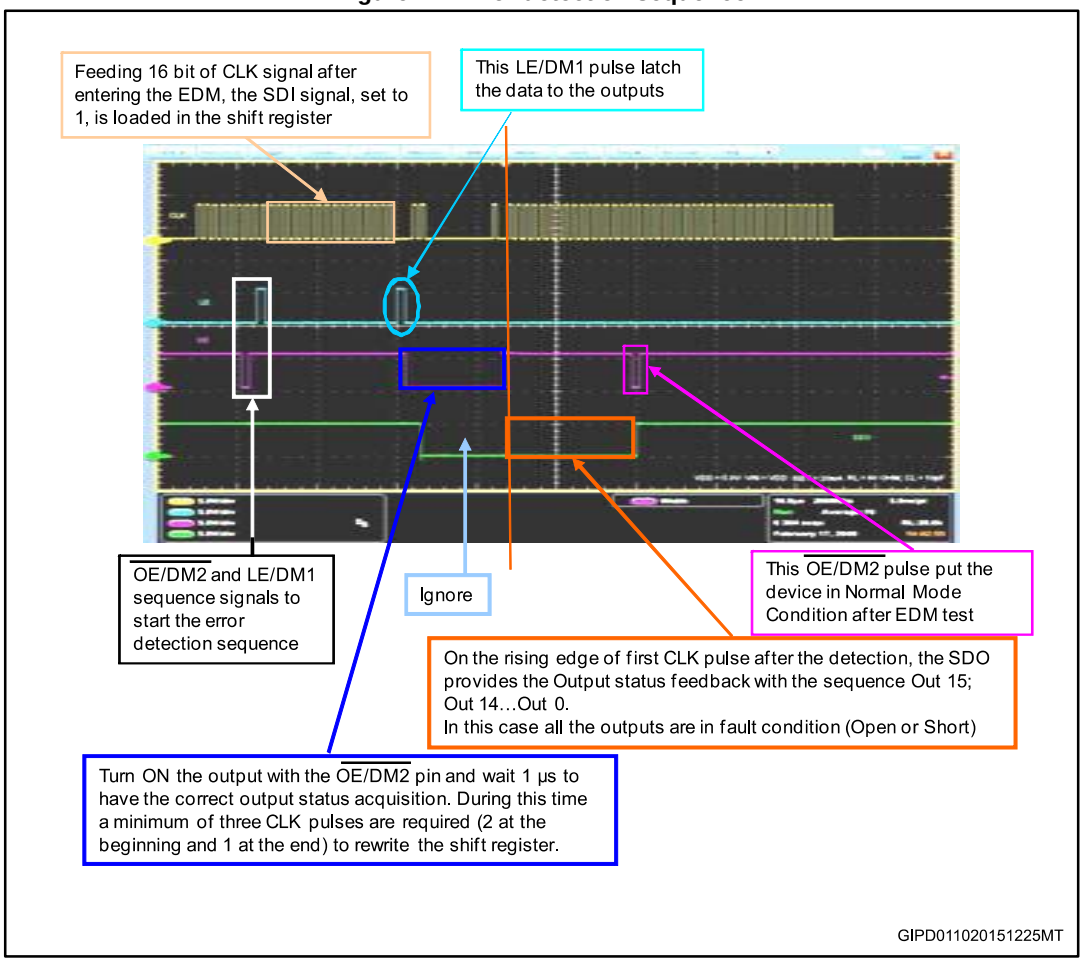


Figure 22: Error detection sequence



8 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: ***www.st.com***. ECOPACK® is an ST trademark.

8.1 QSOP-24 package information

Figure 23: QSOP-24 package outline

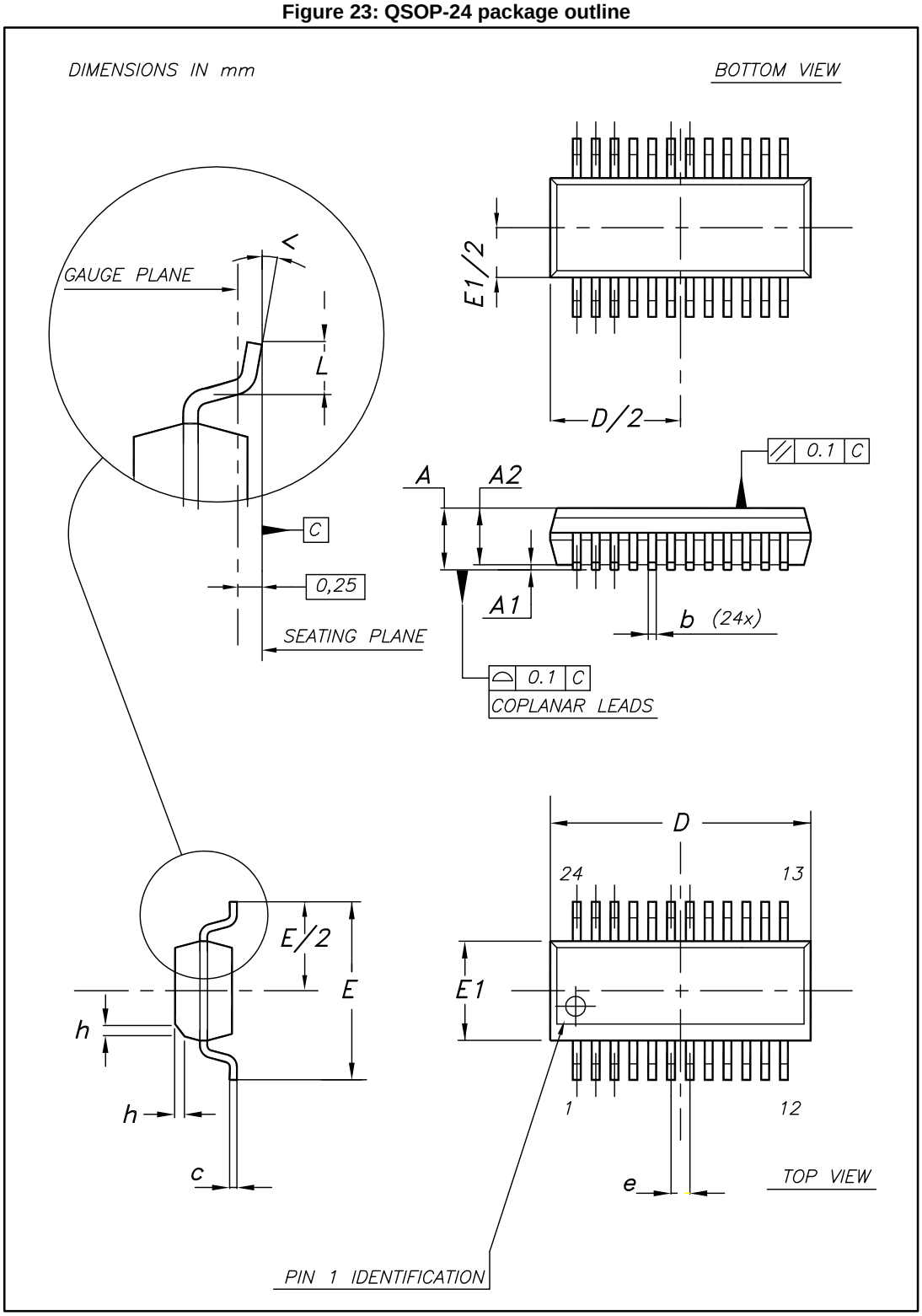


Table 16: QSOP-24 mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	1.54	1.62	1.73
A1	0.10	0.15	0.25
A2		1.47	
b	0.20		0.31
c	0.17		0.254
D	8.56	8.66	8.76
E	5.80	6.00	6.20
E1	3.80	3.91	4.01
e		0.635	
L	0.40	0.635	0.89
h	0.25	0.33	0.41
<	0°		8°

8.2 TSSOP24 package information

Figure 24: TSSOP24 package outline

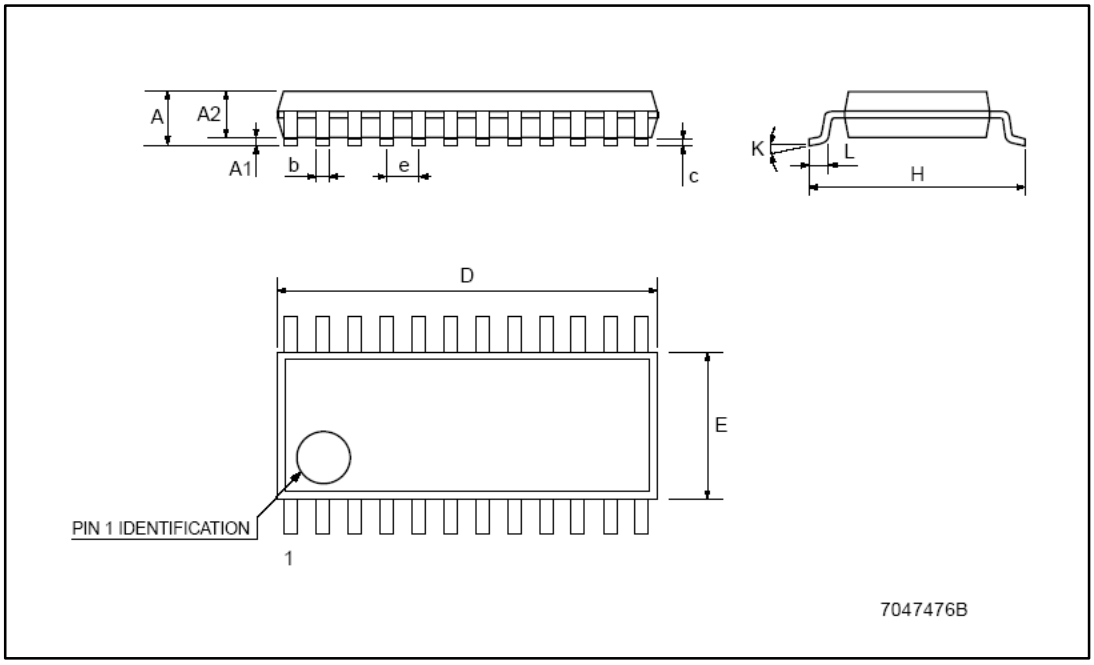


Table 17: TSSOP24 mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A			1.1
A1	0.05		0.15
A2		0.9	
b	0.19		0.30
c	0.09		0.20
D	7.7		7.9
E	4.3		4.5
e		0.65 BSC	
H	6.25		6.5
K	0°		8°
L	0.50		0.70

8.3 SO-24 package information

Figure 25: SO-24 package outline

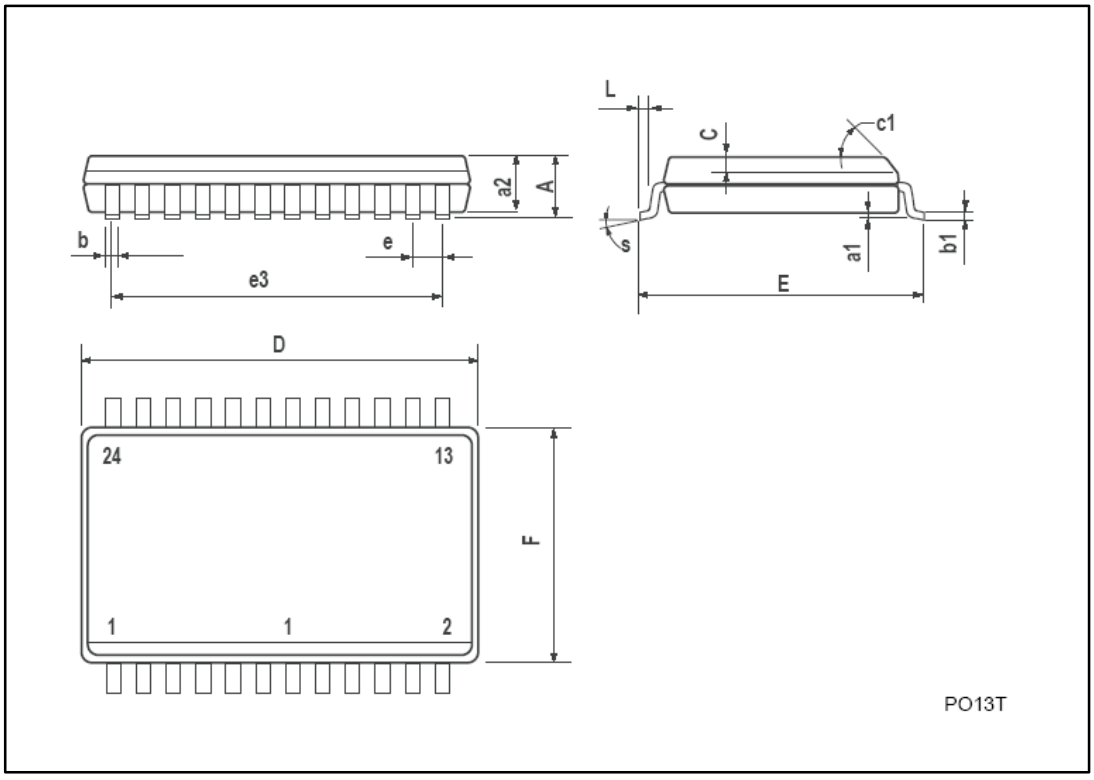


Table 18: SO-24 mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A			2.65
a1	0.1		0.2
a2			2.45
b	0.35		0.49
b1	0.23		0.32
C		0.5	
c1	45° (typ.)		
D	15.20		15.60
E	10.00		10.65
e		1.27	
e3		13.97	
F	7.40		7.60
L	0.50		1.27
S	°(max.) 8		

8.4 TSSOP24 exposed pad package information

Figure 26: TSSOP24 exposed pad package outline

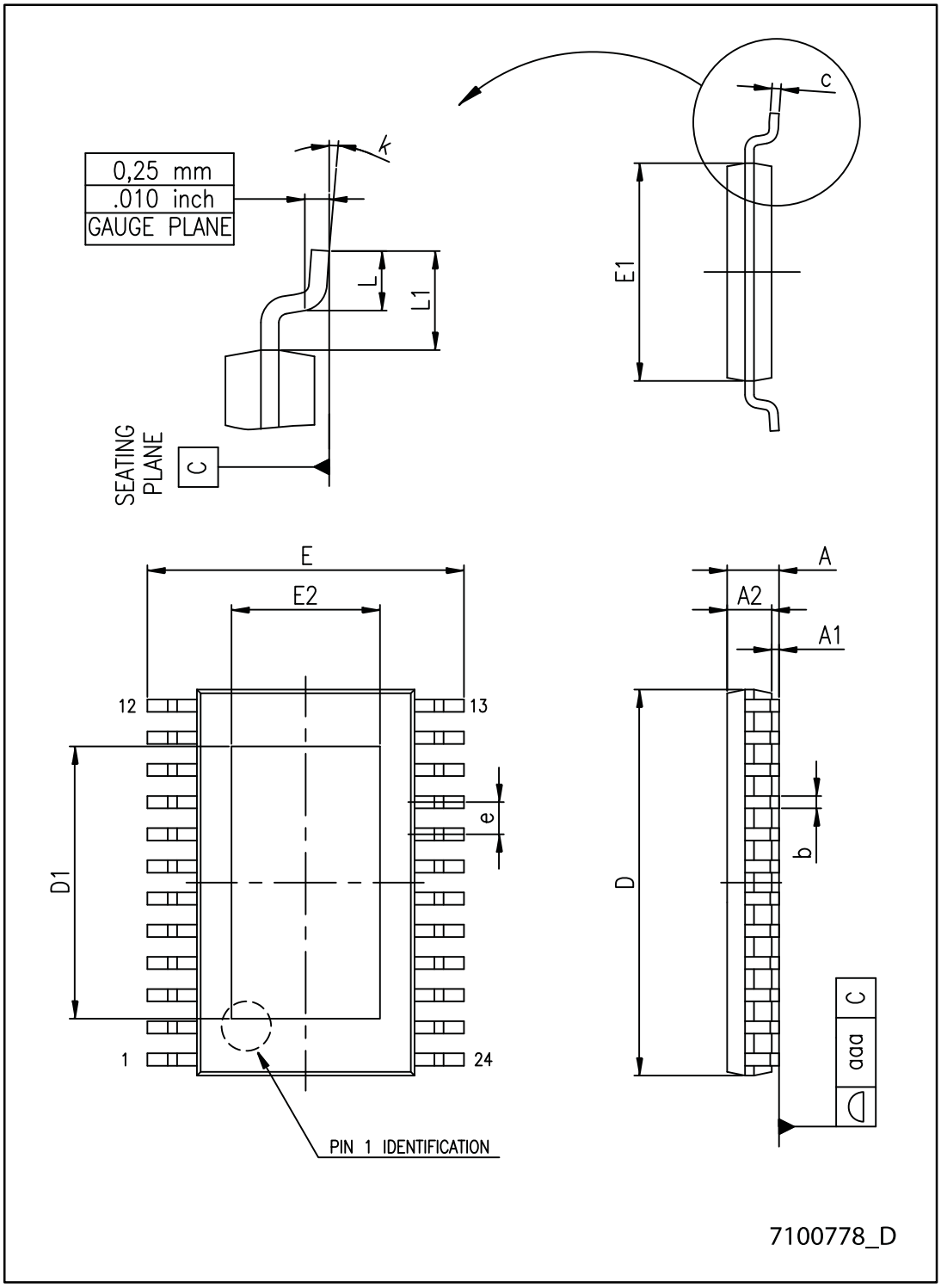


Table 19: TSSOP24 exposed pad mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A			1.20
A1			0.15
A2	0.80	1.00	1.05
b	0.19		0.30
c	0.09		0.20
D	7.70	7.80	7.90
D1	4.80	5.00	5.2
E	6.20	6.40	6.60
E1	4.30	4.40	4.50
E2	3.00	3.20	3.40
e		0.65	
L	0.45	060	075
L1		1.00	
k	0		8
aaa			0.10

8.5 TSSOP24, TSSOP24 exposed pad and SO-24 packing information

Figure 27: TSSOP24, TSSOP24 exposed pad and SO-24 reel outline

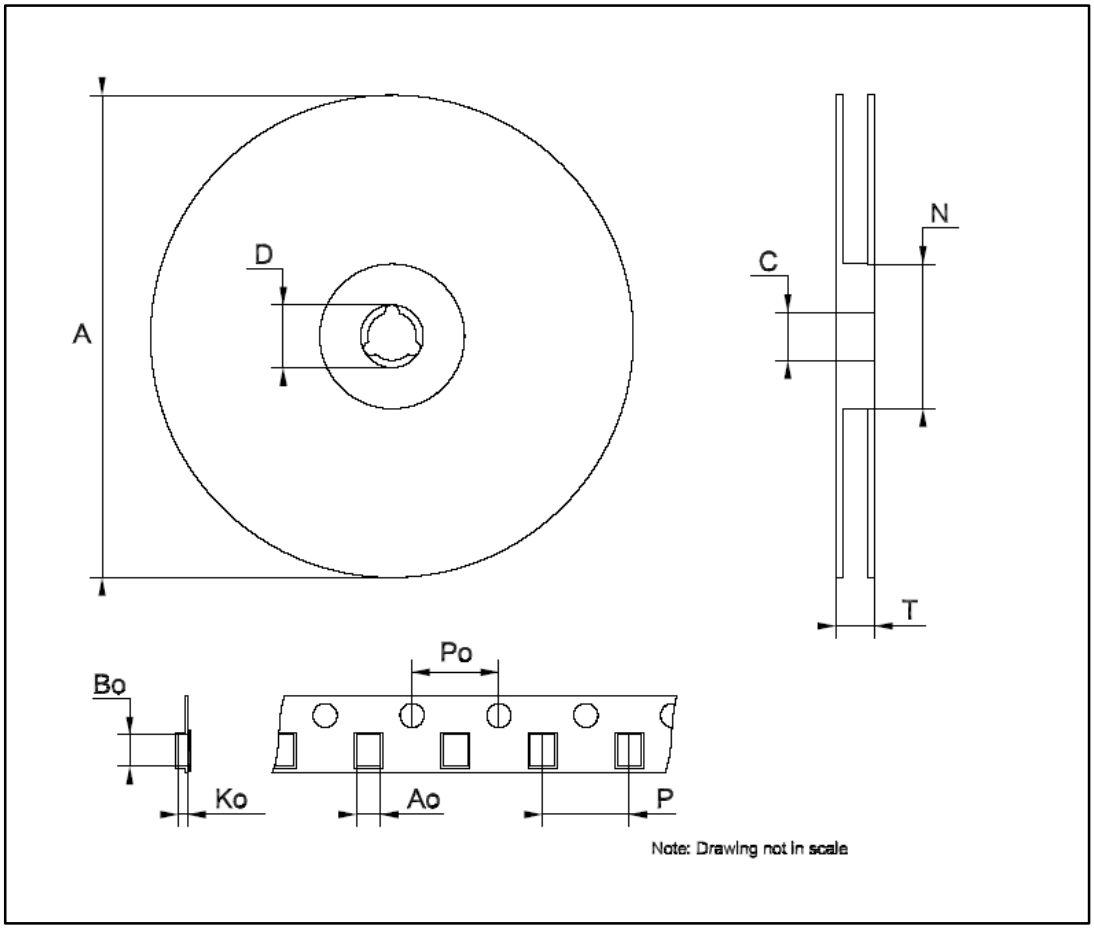


Table 20: TSSOP24 and TSSOP24 exposed pad tape and reel mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A		-	330
C	12.8	-	13.2
D	20.2	-	
N	60	-	
T		-	22.4
Ao	6.8	-	7
Bo	8.2	-	8.4
Ko	1.7	-	1.9
Po	3.9	-	4.1
P	11.9	-	12.1

Table 21: SO-24 tape and reel mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A		-	330
C	12.8	-	13.2
D	20.2	-	
N	60	-	
T		-	30.4
Ao	10.8	-	11.0
Bo	15.7	-	15.9
Ko	2.9	-	3.1
Po	3.9	-	4.1
P	11.9	-	12.1

9 Revision history

Table 22: Document revision history

Date	Revision	Changes
22-Oct-2009	1	First release.
19-Jun-2014	2	Updated Section 8: Package mechanical data. Added Section 9: Packaging mechanical data. Minor text changes.
04-Apr-2016	3	Updated *Table 16: "QSOP-24 mechanical data"*. Minor text changes.

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