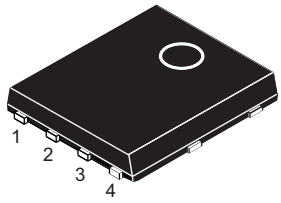
STL15DN4F5

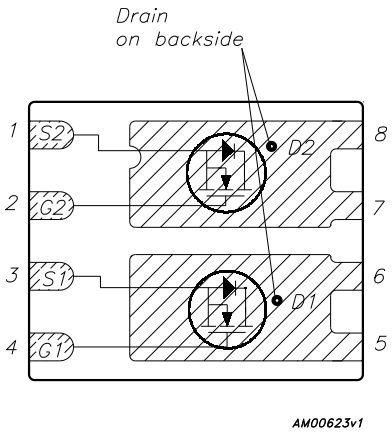
Automotive-grade dual N-channel 40 V, 8 mΩ typ., 15 A STripFET™ F5 Power MOSFET in a PowerFLAT™ 5x6 double island

Datasheet – production data



PowerFLAT™5x6 double island

Figure 1. Internal schematic diagram



Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D
STL15DN4F5	40 V	9 mΩ	15 A

- Designed for automotive applications and AEC-Q101 qualified
- Extremely low on-resistance $R_{DS(on)}$
- Very low gate charge
- Low gate drive power loss
- Wettable flank package option

Applications

- Switching applications

Description

This device is a dual N-channel Power MOSFET developed using STMicroelectronics' STripFET™ F5 technology. The device has been optimized to achieve very low on-state resistance, contributing to a FOM that is among the best in class.

Table 1. Device summary

Order code	Marking	Packages(1)	Packaging
STL15DN4F5	15DN4F5	PowerFLAT™ 5x6 double island	Tape and reel

1. For wettable flank option, please contact ST sale offices.

This is information on a product in full production. www.st.com

Contents

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	40	V
V_{GS}	Gate-source voltage	± 20	V
I_D (1)	Drain current (continuous) at T_C = 25 °C (silicon limited)	60	A
I_D (2)	Drain current (continuous) at T_{pcb} = 25 °C	15	A
I_D (2)	Drain current (continuous) at T_{pcb} = 100°C	10	A
I_{DM} (2),(3)	Drain current (pulsed)	60	A
P_{TOT} (1)	Total dissipation at T_C = 25°C	60	W
P_{TOT} (2)	Total dissipation at T_{pcb} = 25°C, t < 10 sec	4.3	W
T_J T_{stg}	Operating junction temperature Storage temperature	-55 to 175	°C

1. The value is rated according $R_{thj\text{-}c}$
2. The value is rated according $R_{thj\text{-}pcb}$
3. Pulse width limited by safe operating area

Table 3. Thermal resistance

Symbol	Parameter	Value	Unit
$R_{thj\text{-}case}$	Thermal resistance junction-case	2.5	°C/W
$R_{thj\text{-}pcb}$ (1)	Thermal resistance junction-pcb	35	°C/W

1. When mounted on FR-4 board of 1inch², 2oz Cu, t < 10 sec (see *Figure 3*)

Table 4. Avalanche data

Symbol	Parameter	Value	Unit
I_{AV}	Not-repetitive avalanche current, (pulse width limited by Tj max.)	7.5	A
E_{AS} (1)	Single pulse avalanche energy (starting T_J = 25 °C, I_D = I_{AV}, V_{DD} = 24 V)	150	mJ

1. Tested at wafer level only.

2 Electrical characteristics

(T_{CASE} = 25 °C unless otherwise specified)

Table 5. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS}= 0, I_D = 250 µA	40			V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0, V_{DS} = 40 V,			1	µA
		V_{GS} = 0, V_{DS} = 40 V, T_C= 125 °C			10	µA
I_{GSS}	Gate body leakage current	V_{DS} = 0, V_{GS} = ±20 V			±100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS}= V_{GS}, I_D = 250 µA	2		4	V
$R_{DS(on)}$	Static drain-source on- resistance	V_{GS}= 10 V, I_D= 7.5 A		8	9	mΩ

Table 6. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{GS} = 0, V_{DS} = 25 V, f = 1 MHz	-	1550	-	pF
C_{oss}	Output capacitance		-	230	-	pF
C_{rss}	Reverse transfer capacitance		-	25	-	pF
Q_g	Total gate charge	V_{DD}= 20 V, I_D = 15 A V_{GS} = 10 V *(see Figure 14)*	-	25	-	nC
Q_{gs}	Gate-source charge		-	6	-	nC
Q_{gd}	Gate-drain charge		-	5.5	-	nC

Table 7. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 20 V, I_D = 7.5 A, R_G = 4.7 Ω, V_{GS} = 10 V *(see Figure 13)*	-	18	-	ns
t_r	Rise time		-	45	-	ns
$t_{d(off)}$	Turn-off delay time		-	32	-	ns
t_f	Fall time		-	5	-	ns

Table 8. Source drain diode

Symbol	Parameter	Test conditions	Min	Typ.	Max	Unit
I_{SD}	Source-drain current		-		15	A
I_{SDM}(1)	Source-drain current (pulsed)		-		60	A
V_{SD}(2)	Forward on voltage	V_{GS} = 0, I_{SD} = 15 A	-		1.1	V
t_{rr}	Reverse recovery time	I_{SD} = 15 A, di/dt = 100 A/µs, V_{DD} = 32 V, Tj = 150 °C	-	30		ns
Q_{rr}	Reverse recovery charge		-	35		nC
I_{RRM}	Reverse recovery current		-	2.2		A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration = 300 µs, duty cycle 1.5 %

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

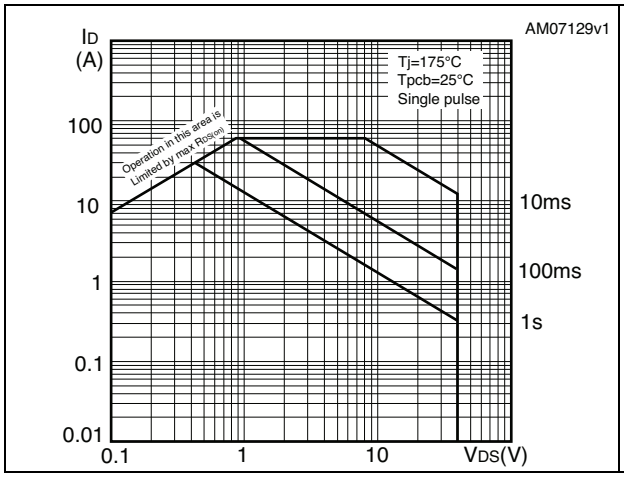


Figure 3. Thermal impedance

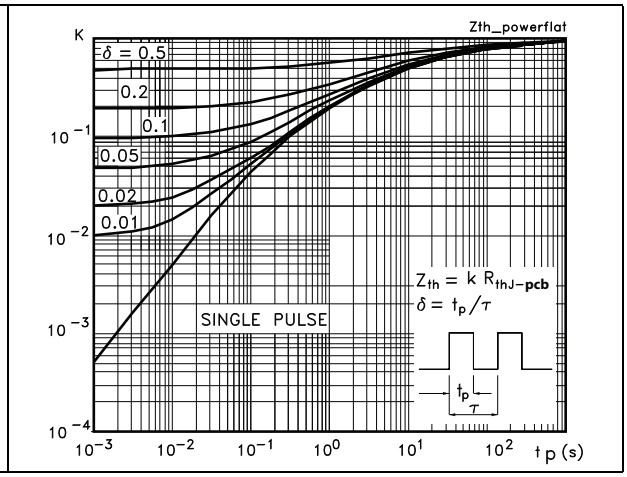


Figure 4. Output characteristics

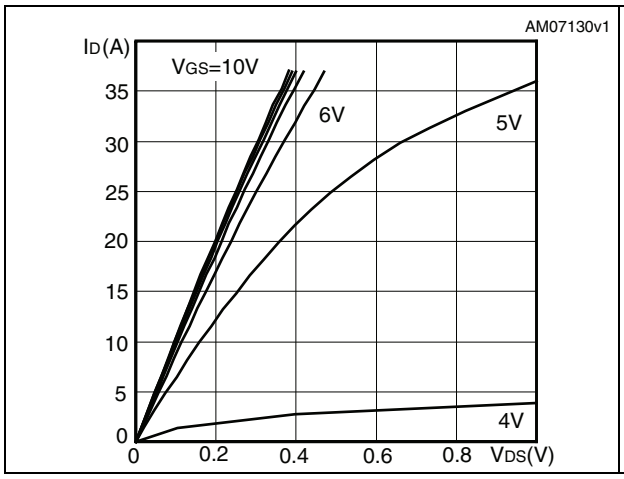


Figure 5. Transfer characteristics

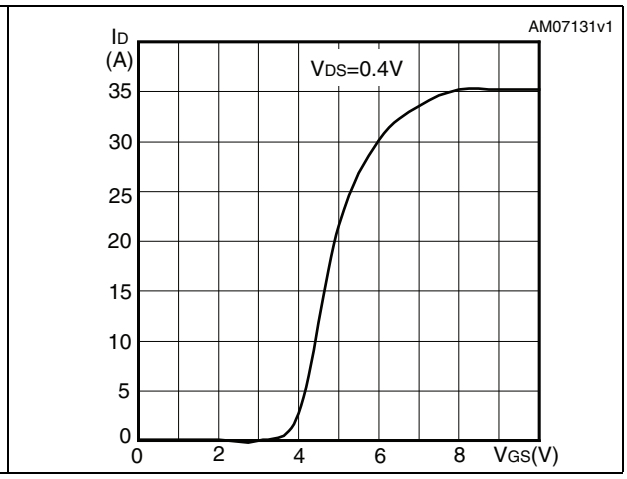


Figure 6. Normalized $V_{(BR)DSS}$ vs temperature

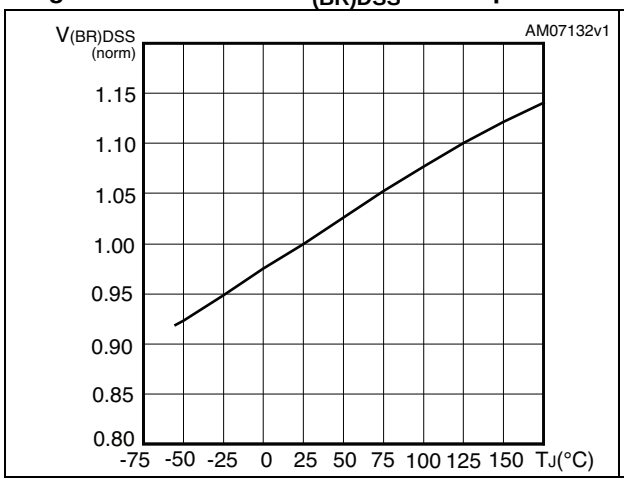


Figure 7. Static drain-source on-resistance

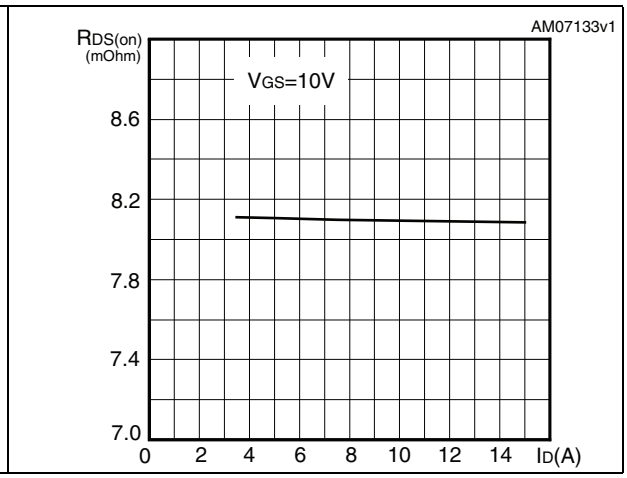


Figure 8. Gate charge vs gate-source voltage

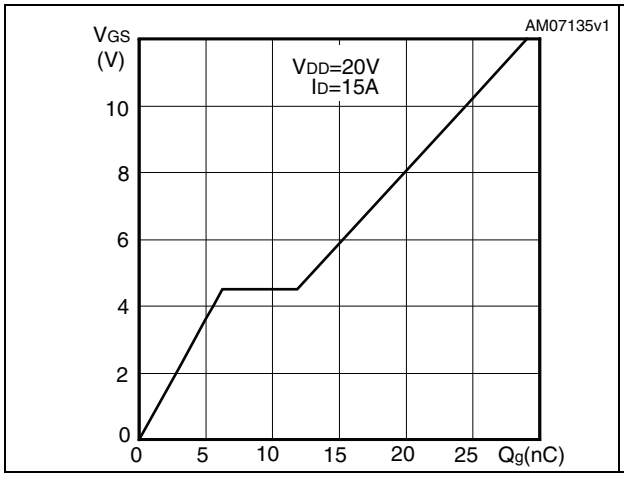


Figure 9. Capacitance variations

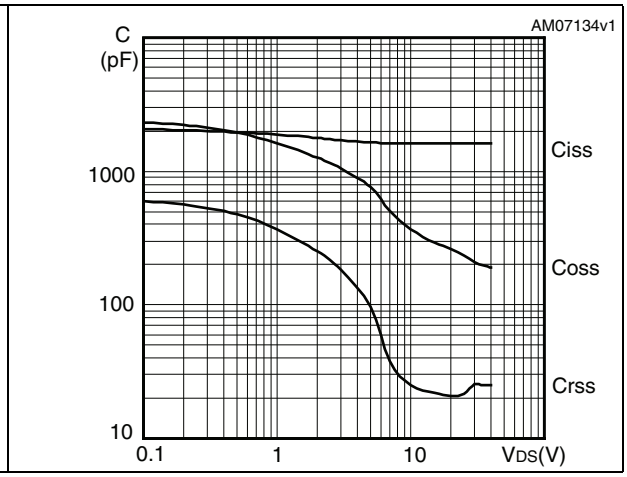


Figure 10. Normalized gate threshold voltage vs temperature

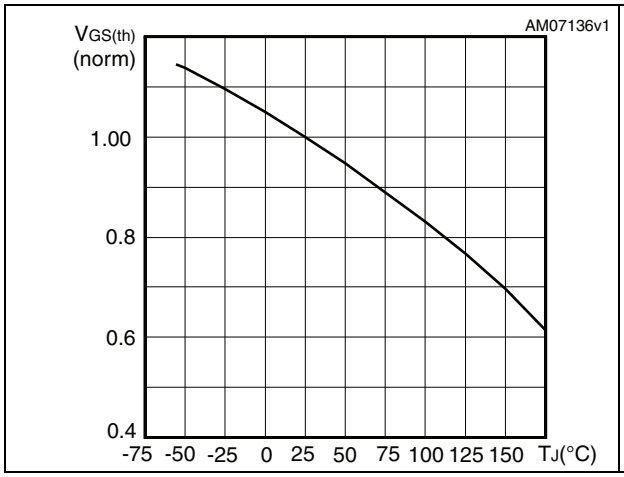


Figure 11. Normalized on-resistance vs temperature

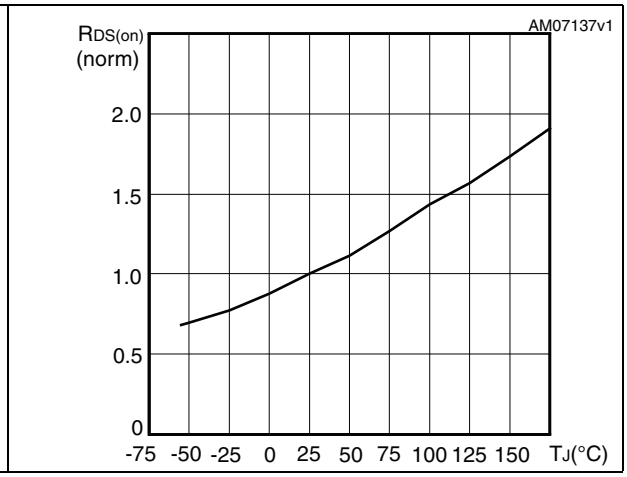
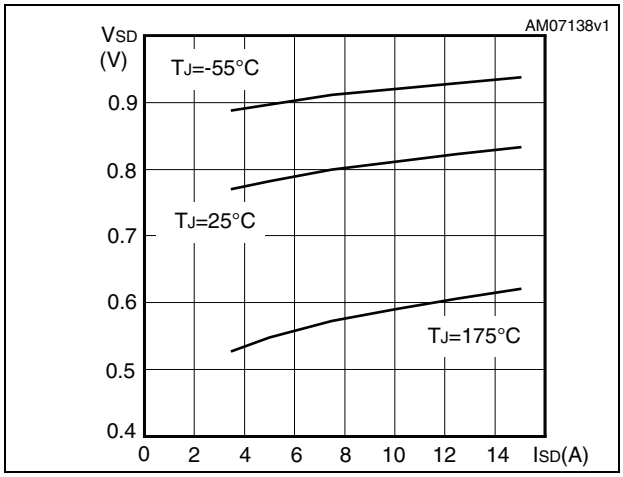


Figure 12. Source-drain diode forward characteristics



3 Test circuits

Figure 13. Switching times test circuit for resistive load

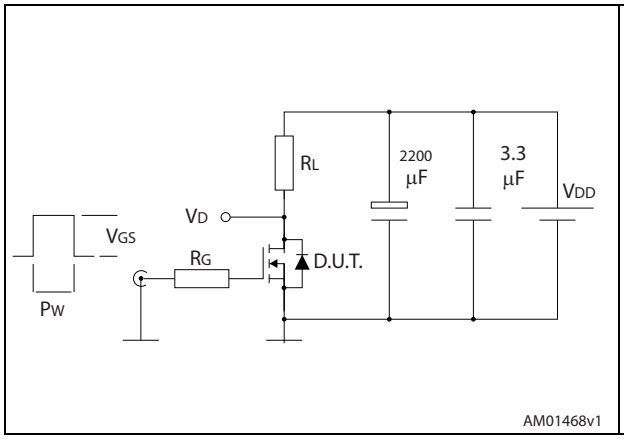


Figure 14. Gate charge test circuit

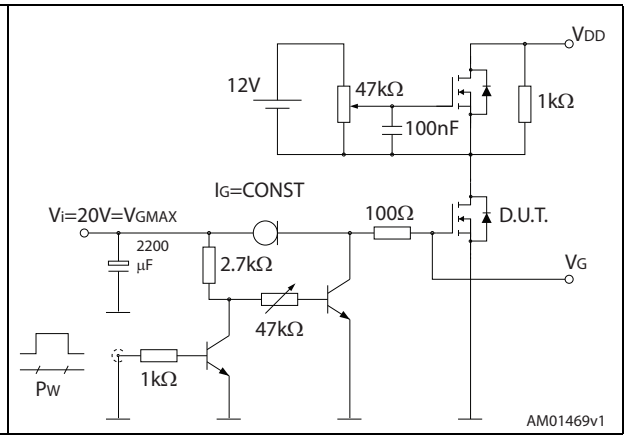


Figure 15. Test circuit for inductive load switching and diode recovery times

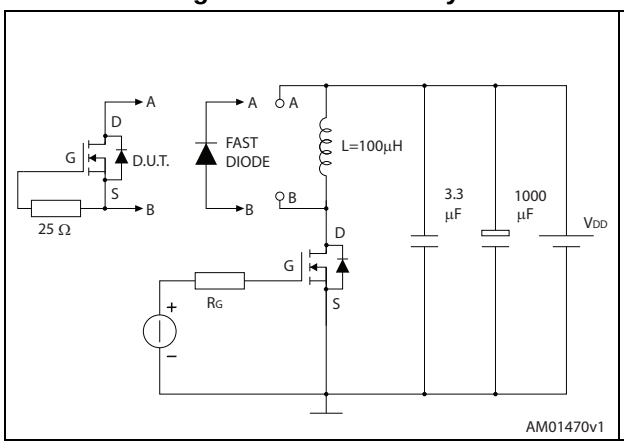


Figure 16. Unclamped inductive load test circuit

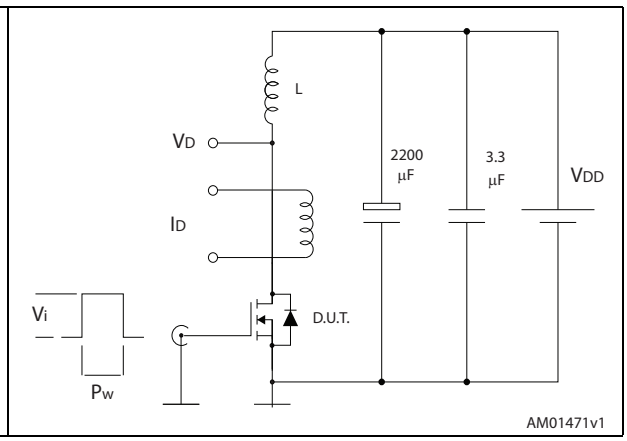


Figure 17. Unclamped inductive waveform

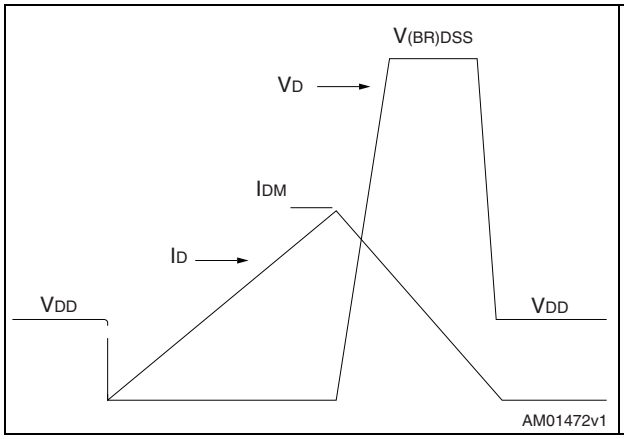
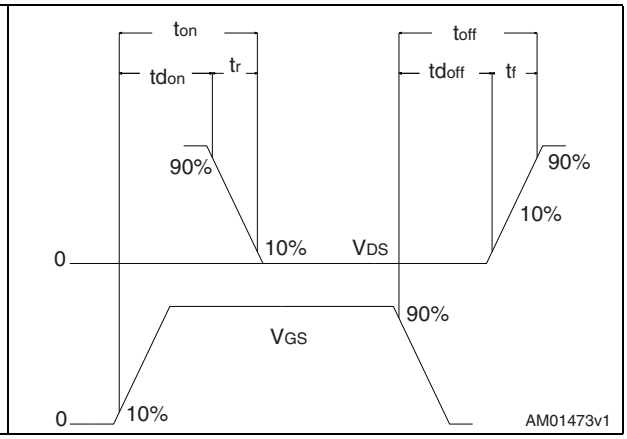


Figure 18. Switching time waveform



4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

Figure 19. PowerFLAT™ 5x6 double island type C outline

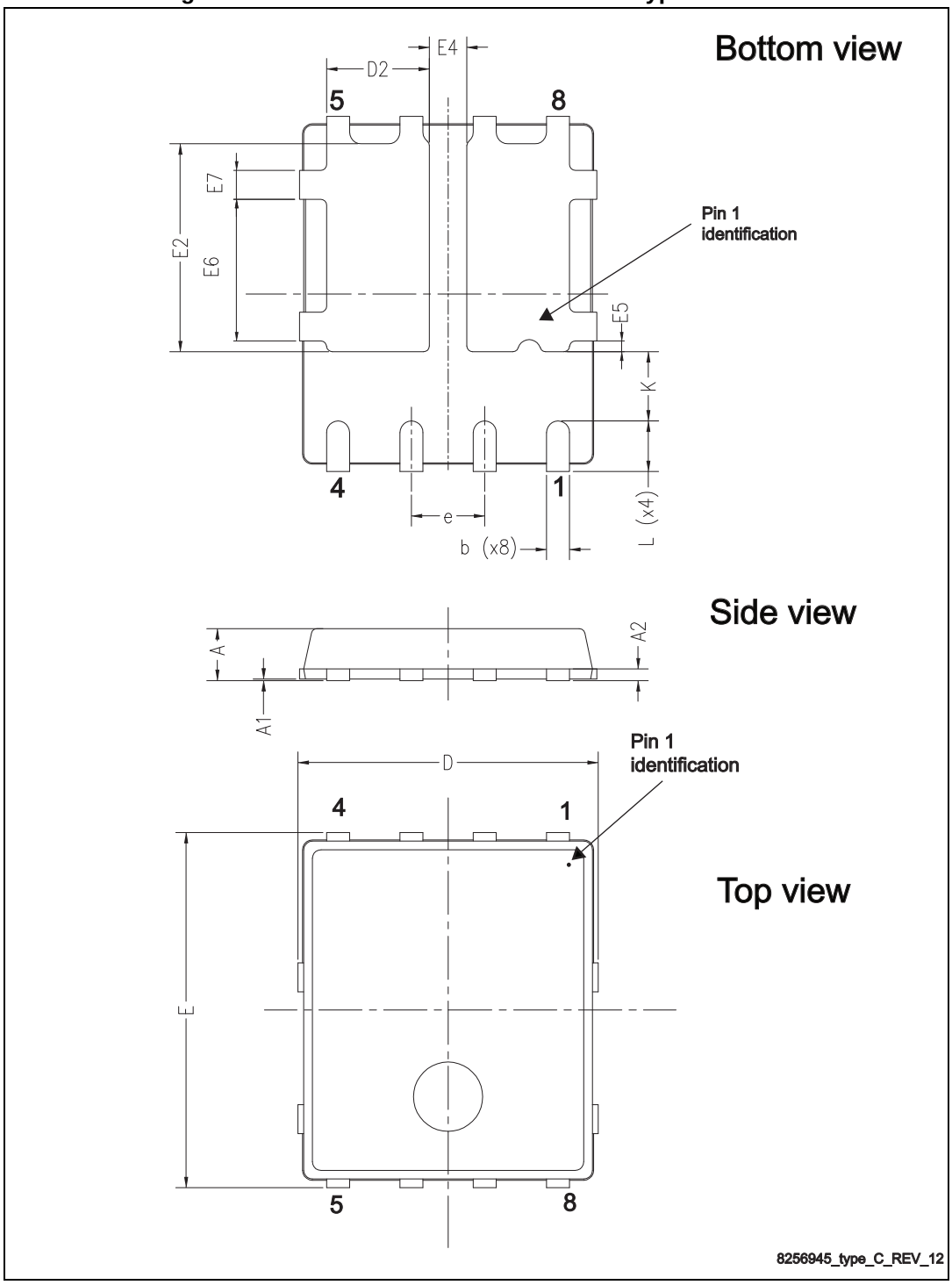


Table 9. PowerFLAT™ 5x6 double island type C mechanical data

Dim	mm		
	Min.	Typ.	Max
A	0.80		1.00
A1	0.02		0.05
A2		0.25	
b	0.30		0.50
D		5.20	
D2	1.68		1.88
E		6.15	
e		1.27	
E2	3.50		3.70
E4	0.55		0.75
E5	0.08		0.28
E6	2.35		2.55
E7	0.40		0.60
K	1.05		1.35
L	0.725		1.025

Figure 20. PowerFLAT 5x6 double island WF type C outline

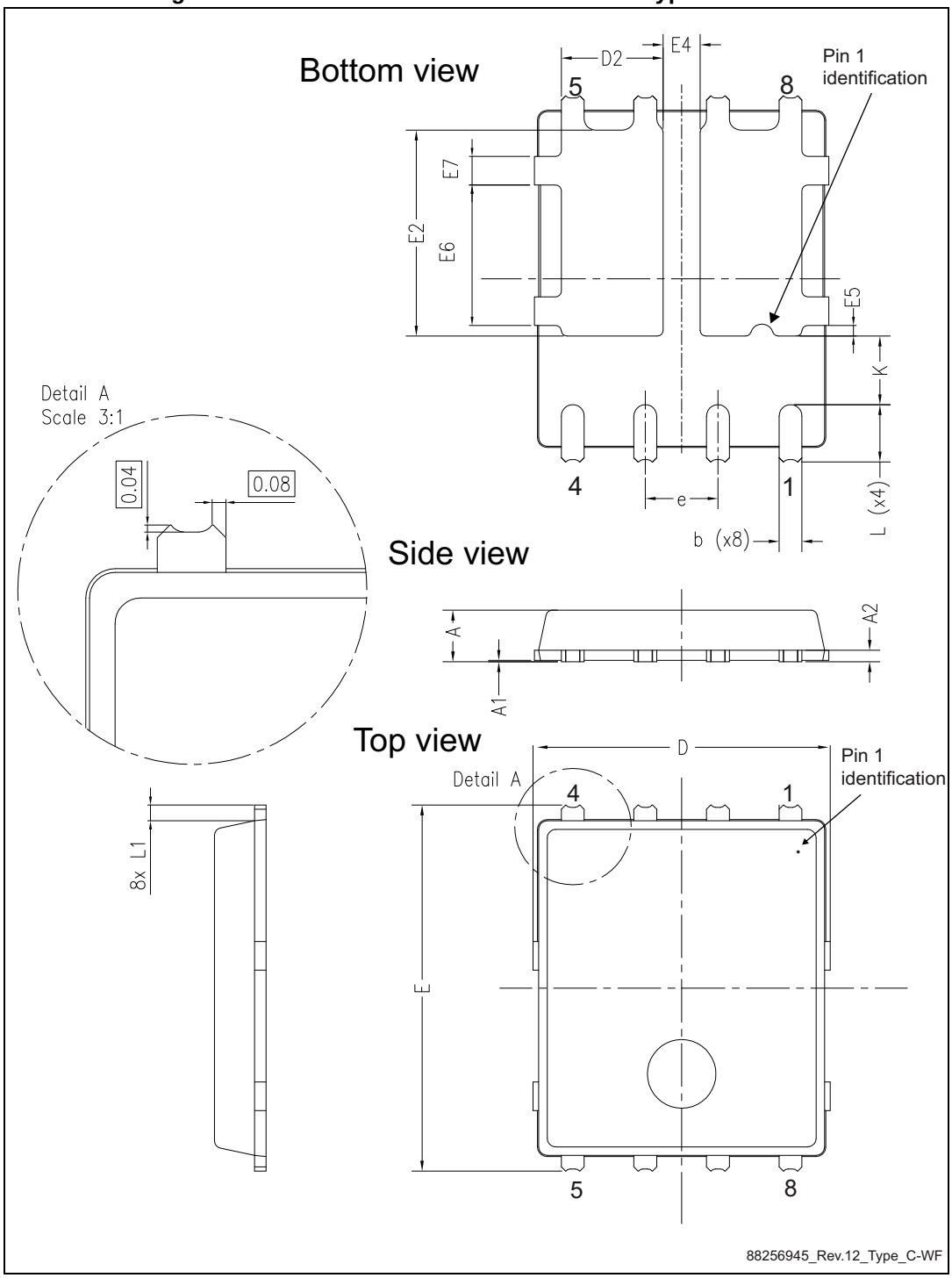
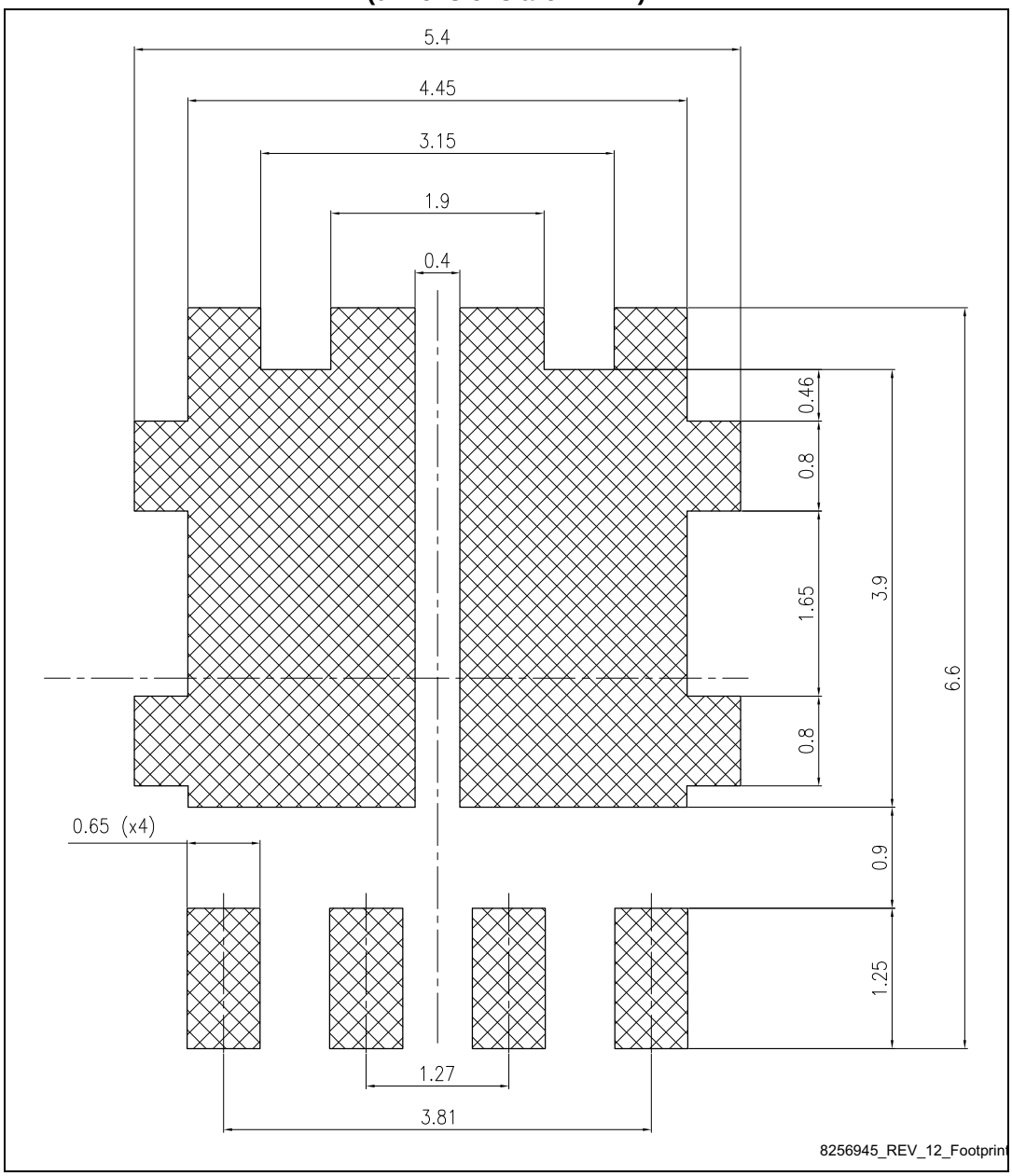


Table 10. PowerFLAT 5x6 double island WF type C mechanical data

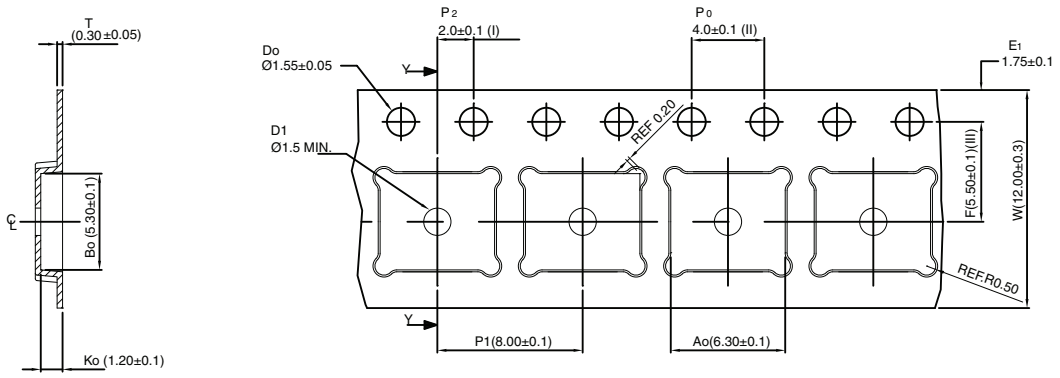
Ref.	Dimensions (mm)		
	Min.	Typ.	Max.
A	0.80		1.00
A1	0.02		0.05
A2		0.25	
b	0.30		0.50
D	5.00	5.20	5.40
D2	1.68		1.88
E	6.20	6.40	6.60
E2	3.50		3.70
E4	0.55		0.75
E5	0.08		0.28
E6	2.35		2.55
E7	0.40		0.60
e		1.27	
L	0.90		1.10
L1		0.275	
K	1.05		1.35

Figure 21. PowerFLAT™ 5x6 double island recommended footprint (dimensions are in mm)



5 Packaging information

Figure 22. PowerFLAT™ 5x6 tape[(a)]



(I) Measured from centerline of sprocket hole to centerline of pocket.

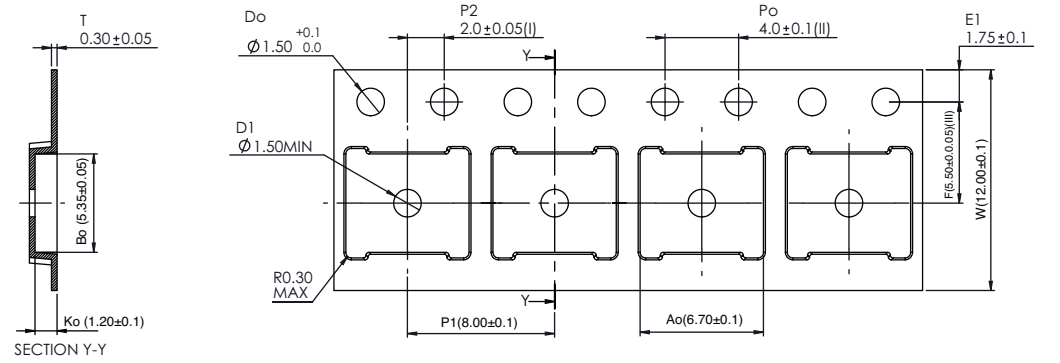
(II) Cumulative tolerance of 10 sprocket holes is ± 0.20 .

(III) Measured from centerline of sprocket hole to centerline of pocket.

Base and bulk quantity 3000 pcs

8234350_Tape_rev_C

Figure 23. PowerFLAT 5x6 WF tape[(a)]



(I) Measured from centreline of sprocket hole to centreline of pocket.

(II) Cumulative tolerance of 10 sprocket holes is ± 0.20 .

(III) Measured from centreline of sprocket hole to centreline of pocket.

Base and bulk quantity 3000 pcs

8234350_TapeWF_rev_C

a. All dimensions are in millimeters.

Figure 24. PowerFLAT™ 5x6 package orientation in carrier tape

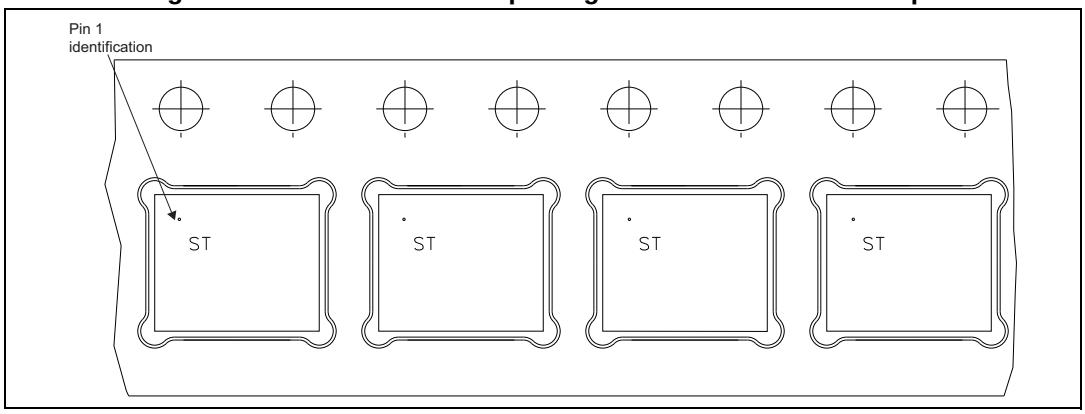
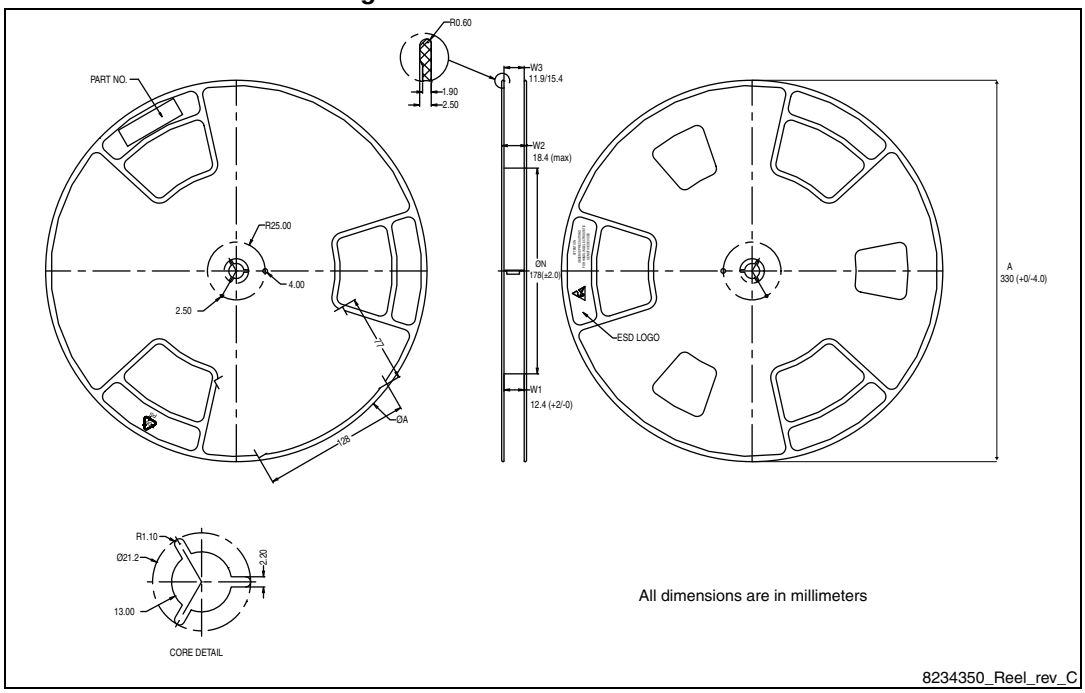


Figure 25. PowerFLAT™ 5x6 reel



6 Revision history

Table 11. Document revision history

Date	Revision	Changes
02-Sep-2010	1	First release
01-Jul-2014	2	– Updated: *Section 4: Package information* – Minor text changes
13-Feb-2015	3	– Updated *Section 4: Package information*. – Added *Section 5: Packaging information*.

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