

## N-channel 600 V, 570 mΩ typ., 8 A MDmesh™ DM2 Power MOSFET in a DPAK package

Datasheet - target specification

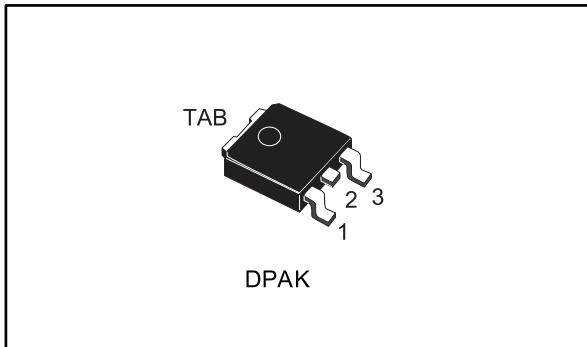
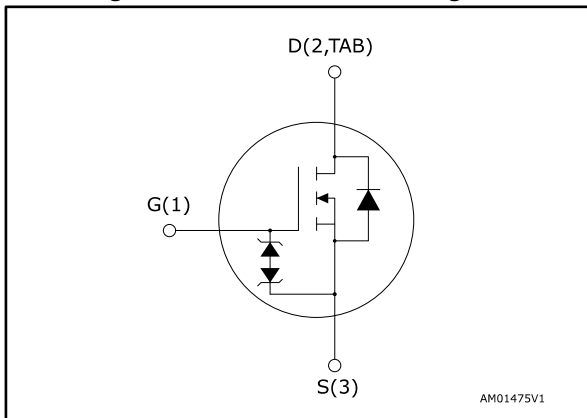


Figure 1: Internal schematic diagram



### Features

Order code	V <sub>DS</sub>	R <sub>DS(on)</sub> max.	I <sub>D</sub>	P <sub>TOT</sub>
STD8N60DM2	600 V	600 mΩ	8 A	85 W

- Fast-recovery body diode
- Extremely low gate charge and input capacitance
- Low on-resistance
- 100% avalanche tested
- Extremely high dv/dt ruggedness
- Zener-protected

### Applications

- Switching applications

### Description

This high voltage N-channel Power MOSFET is part of the MDmesh™ DM2 fast recovery diode series. It offers very low recovery charge ( $Q_{rr}$ ) and time ( $t_{rr}$ ) combined with low  $R_{DS(on)}$ , rendering it suitable for the most demanding high efficiency converters and ideal for bridge topologies and ZVS phase-shift converters.

Table 1: Device summary

Order code	Marking	Package	Packing
STD8N60DM2	8N60DM2	DPAK	Tape and reel

---

## Contents

<b>1</b>	<b>Electrical ratings .....</b>	<b>3</b>
<b>2</b>	<b>Electrical characteristics .....</b>	<b>4</b>
<b>3</b>	<b>Test circuits .....</b>	<b>6</b>
<b>4</b>	<b>Package information .....</b>	<b>7</b>
	4.1 DPAK (TO-252) type A package information.....	7
	4.2 DPAK (TO-252) packing information.....	10
<b>5</b>	<b>Revision history .....</b>	<b>12</b>

# 1 Electrical ratings

**Table 2: Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{GS}$	Gate-source voltage	$\pm 30$	V
$I_D$	Drain current (continuous) at $T_{case} = 25\text{ }^\circ\text{C}$	8	A
	Drain current (continuous) at $T_{case} = 100\text{ }^\circ\text{C}$	5	
$I_{DM}^{(1)}$	Drain current (pulsed)	32	A
$P_{TOT}$	Total dissipation at $T_{case} = 25\text{ }^\circ\text{C}$	85	W
$dv/dt^{(2)}$	Peak diode recovery voltage slope	15	V/ns
$dv/dt^{(3)}$	MOSFET $dv/dt$ ruggedness	40	
$T_{stg}$	Storage temperature	-55 to 150	$^\circ\text{C}$
$T_j$	Maximum junction temperature	150	

**Notes:**

(1) Pulse width is limited by safe operating area.

(2)  $I_{SD} \leq 8\text{ A}$ ,  $di/dt=400\text{ A}/\mu\text{s}$ ;  $V_{DS\text{ peak}} < V_{(BR)DSS}$ ,  $V_{DD} = 80\% V_{(BR)DSS}$ .

(3)  $V_{DS} \leq 480\text{ V}$ .

**Table 3: Thermal data**

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case	1.47	$^\circ\text{C}/\text{W}$
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-pcb	50	

**Notes:**

(1) When mounted on a 1-inch<sup>2</sup> FR-4, 2 Oz copper board.

**Table 4: Avalanche characteristics**

Symbol	Parameter	Value	Unit
$I_{AR}^{(1)}$	Avalanche current, repetitive or not repetitive	TBD	A
$E_{AR}^{(2)}$	Single pulse avalanche energy	TBD	mJ

**Notes:**

(1) Pulse width limited by  $T_{jmax}$ .

(2) starting  $T_j = 25\text{ }^\circ\text{C}$ ,  $I_D = I_{AR}$ ,  $V_{DD} = 50\text{ V}$ .

## 2 Electrical characteristics

( $T_{\text{case}} = 25\text{ °C}$  unless otherwise specified)

**Table 5: Static**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(\text{BR})\text{DSS}}$	Drain-source breakdown voltage	$V_{\text{GS}} = 0\text{ V}$ , $I_{\text{D}} = 1\text{ mA}$	600			V
$I_{\text{DSS}}$	Zero gate voltage drain current	$V_{\text{GS}} = 0\text{ V}$ , $V_{\text{DS}} = 600\text{ V}$			10	$\mu\text{A}$
		$V_{\text{GS}} = 0\text{ V}$ , $V_{\text{DS}} = 600\text{ V}$ , $T_{\text{case}} = 125\text{ °C}$			100	
$I_{\text{GSS}}$	Gate-body leakage current	$V_{\text{DS}} = 0\text{ V}$ , $V_{\text{GS}} = \pm 25\text{ V}$			$\pm 5$	$\mu\text{A}$
$V_{\text{GS(th)}}$	Gate threshold voltage	$V_{\text{DS}} = V_{\text{GS}}$ , $I_{\text{D}} = 100\text{ }\mu\text{A}$	3	4	5	V
$R_{\text{DS(on)}}$	Static drain-source on-resistance	$V_{\text{GS}} = 10\text{ V}$ , $I_{\text{D}} = 4\text{ A}$		570	600	$\text{m}\Omega$

**Table 6: Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$C_{\text{iss}}$	Input capacitance	$V_{\text{DS}} = 100\text{ V}$ , $f = 1\text{ MHz}$ , $V_{\text{GS}} = 0\text{ V}$	-	375	-	$\text{pF}$
$C_{\text{oss}}$	Output capacitance		-	18	-	
$C_{\text{rss}}$	Reverse transfer capacitance		-	1.2	-	
$C_{\text{oss eq.}}^{(1)}$	Equivalent output capacitance	$V_{\text{DS}} = 0\text{ to }480\text{ V}$ , $V_{\text{GS}} = 0\text{ V}$	-	TBD	-	$\text{pF}$
$R_{\text{G}}$	Intrinsic gate resistance	$f = 1\text{ MHz}$ , $I_{\text{D}} = 0\text{ A}$	-	6	-	$\Omega$
$Q_{\text{g}}$	Total gate charge	$V_{\text{DD}} = 640\text{ V}$ , $I_{\text{D}} = 8\text{ A}$ , $V_{\text{GS}} = 10\text{ V}$ (see <a href="#">Figure 3: "Gate charge test circuit"</a> )	-	4	-	$\text{nC}$
$Q_{\text{gs}}$	Gate-source charge		-	TBD	-	
$Q_{\text{gd}}$	Gate-drain charge		-	TBD	-	

**Notes:**

<sup>(1)</sup>  $C_{\text{oss eq.}}$  is defined as a constant equivalent capacitance giving the same charging time as  $C_{\text{oss}}$  when  $V_{\text{DS}}$  increases from 0 to 80%  $V_{\text{DSS}}$ .

**Table 7: Switching times**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{\text{d(on)}}$	Turn-on delay time	$V_{\text{DD}} = 300\text{ V}$ , $I_{\text{D}} = 4\text{ A}$ $R_{\text{G}} = 4.7\text{ }\Omega$ , $V_{\text{GS}} = 10\text{ V}$ (see <a href="#">Figure 2: "Switching times test circuit for resistive load"</a> and <a href="#">Figure 7: "Switching time waveform"</a> )	-	TBD	-	$\text{ns}$
$t_{\text{r}}$	Rise time		-	TBD	-	
$t_{\text{d(off)}}$	Turn-off delay time		-	TBD	-	
$t_{\text{f}}$	Fall time		-	TBD	-	

Table 8: Source-drain diode

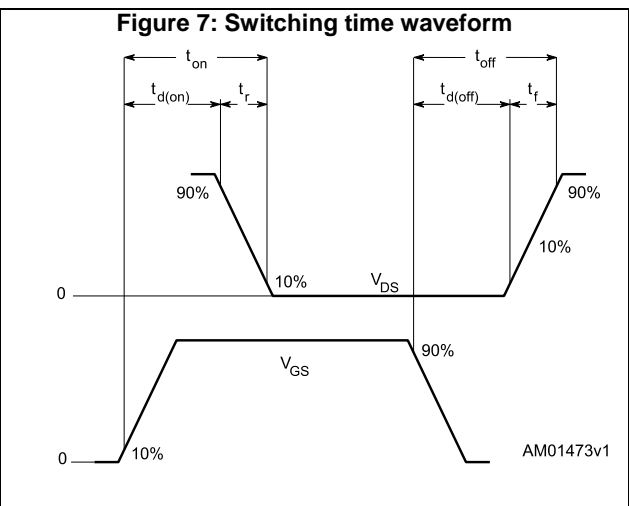
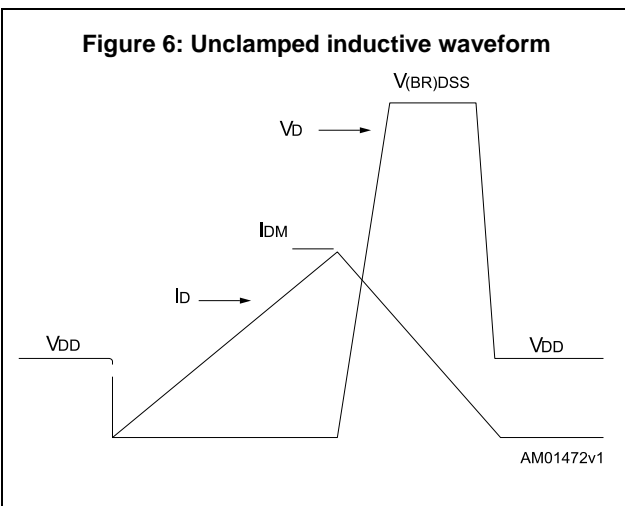
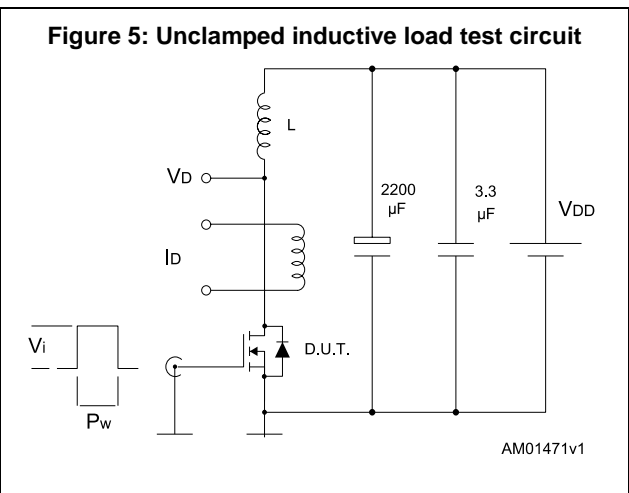
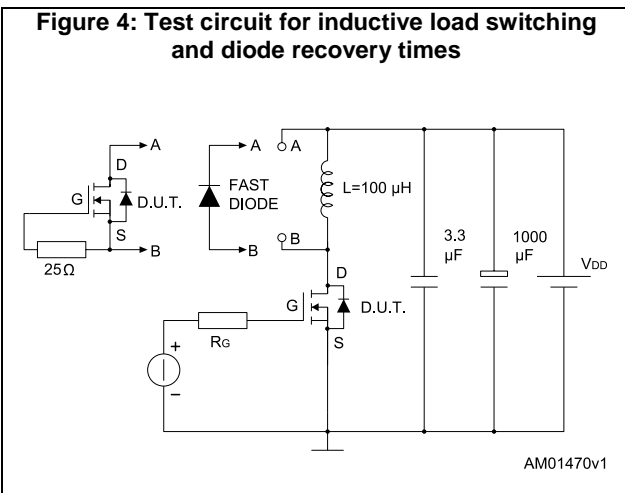
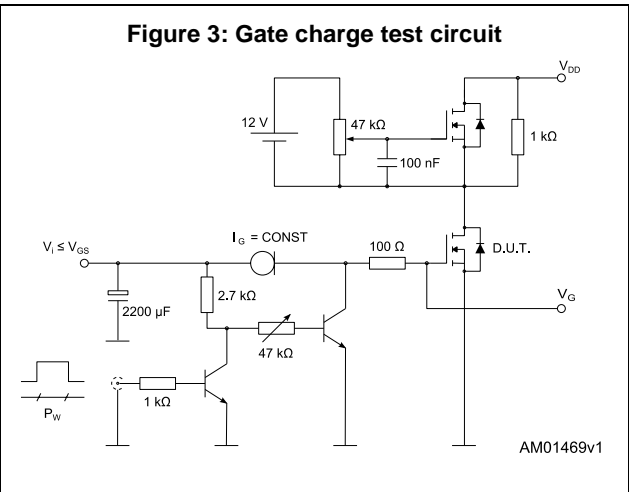
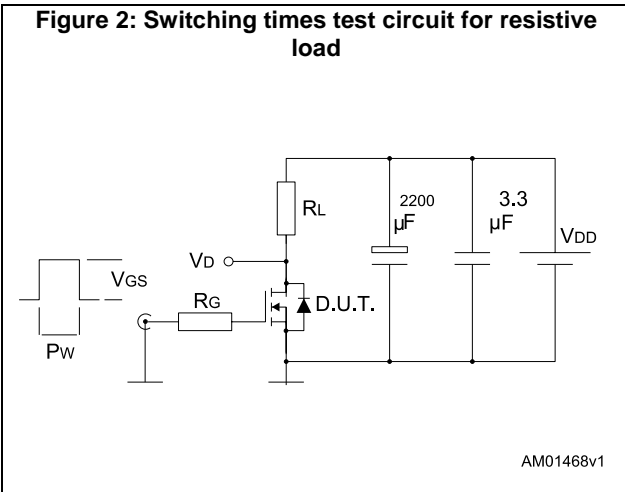
Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain current		-		8	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		32	A
$V_{SD}^{(2)}$	Forward on voltage	$V_{GS} = 0\text{ V}$ , $I_{SD} = 8\text{ A}$	-		1.6	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 8\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ , $V_{DD} = 60\text{ V}$ (see <a href="#">Figure 4: "Test circuit for inductive load switching and diode recovery times"</a> )	-	94	98	ns
$Q_{rr}$	Reverse recovery charge		-	0.20		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current		-	4.25		A
$t_{rr}$	Reverse recovery time	$I_{SD} = 8\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ , $V_{DD} = 60\text{ V}$ , $T_j = 150\text{ }^\circ\text{C}$ (see <a href="#">Figure 4: "Test circuit for inductive load switching and diode recovery times"</a> )	-	TBD		ns
$Q_{rr}$	Reverse recovery charge		-	TBD		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current		-	TBD		A

**Notes:**

(1) Pulse width is limited by safe operating area.

(2) Pulse test: pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%.

### 3 Test circuits



## 4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK<sup>®</sup> packages, depending on their level of environmental compliance. ECOPACK<sup>®</sup> specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK<sup>®</sup> is an ST trademark.

### 4.1 DPAK (TO-252) type A package information

Figure 8: DPAK (TO-252) type A package outline

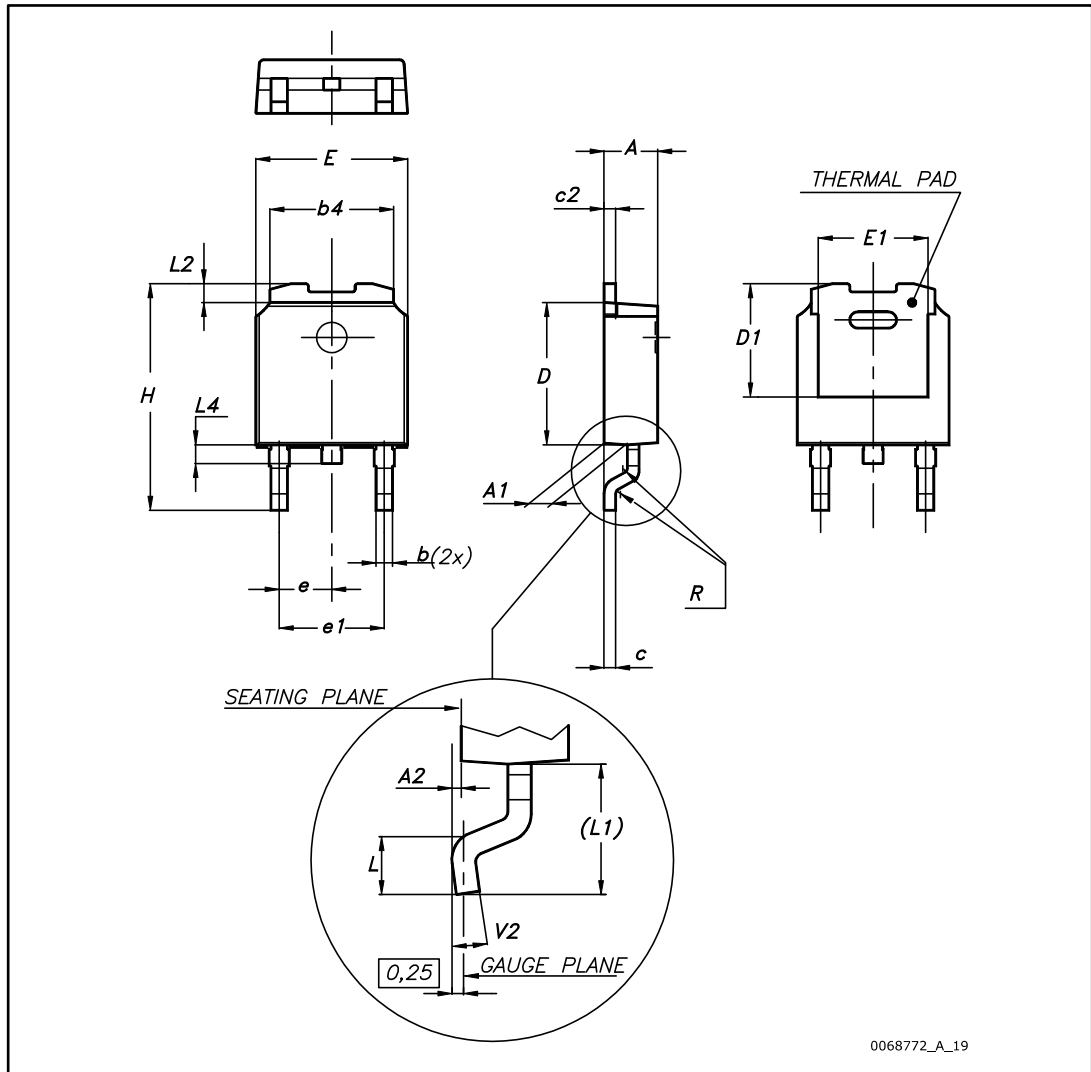


Table 10: DPAK (TO-252) type A mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
b	0.64		0.90
b4	5.20		5.40
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
D1	4.95	5.10	5.25
E	6.40		6.60
E1	4.60	4.70	4.80
e	2.16	2.28	2.40
e1	4.40		4.60
H	9.35		10.10
L	1.00		1.50
(L1)	2.60	2.80	3.00
L2	0.65	0.80	0.95
L4	0.60		1.00
R		0.20	
V2	0°		8°



### 4.2 DPAK (TO-252) packing information

Figure 10: DPAK (TO-252) tape outline

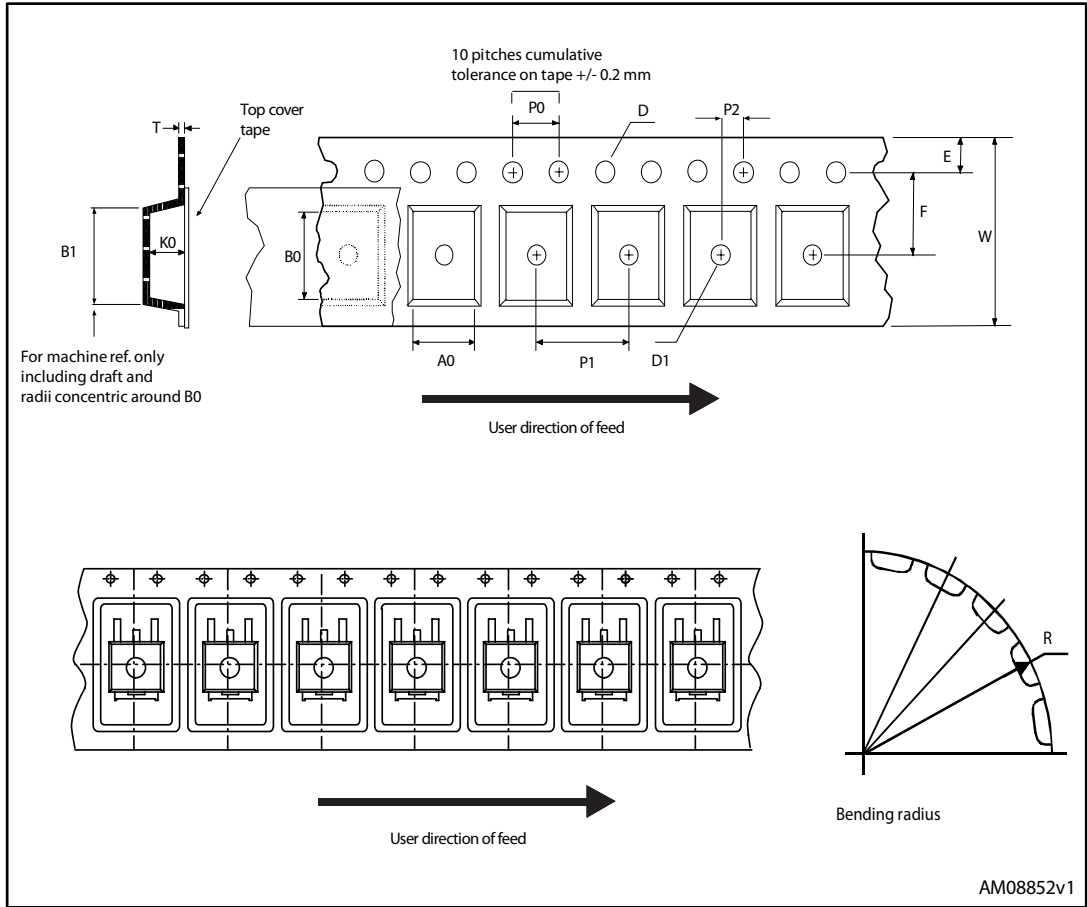
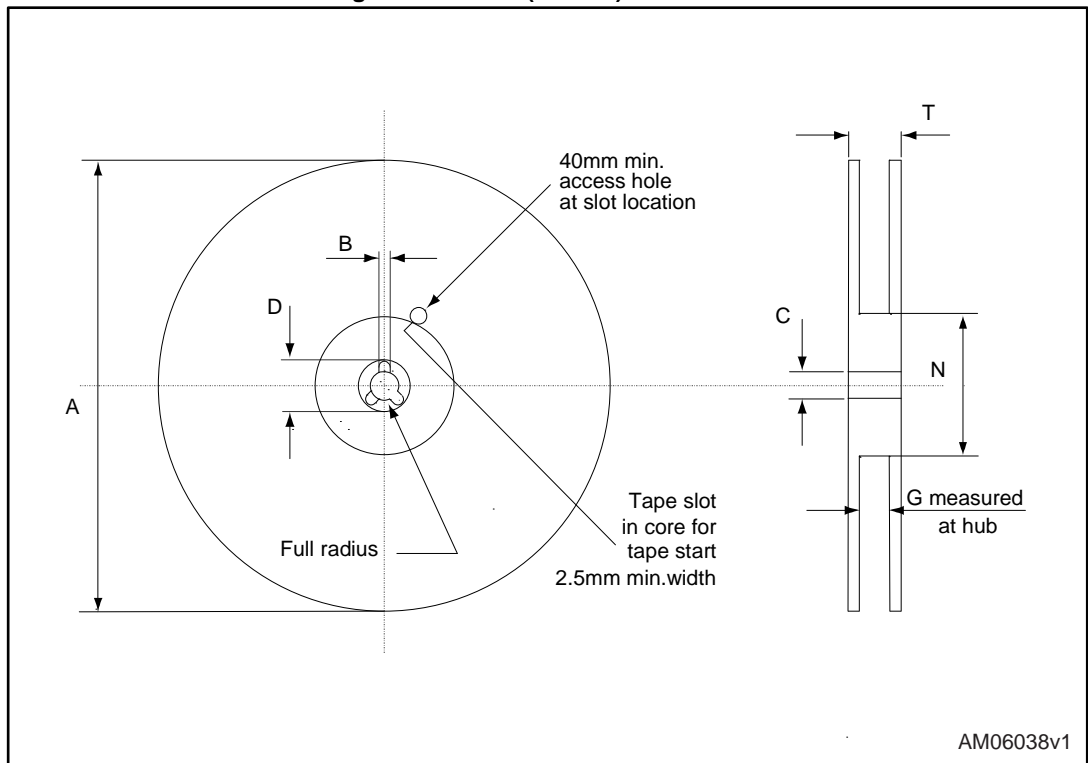


Figure 11: DPAK (TO-252) reel outline



AM06038v1

Table 11: DPAK (TO-252) tape and reel mechanical data

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	6.8	7	A		330
B0	10.4	10.6	B	1.5	
B1		12.1	C	12.8	13.2
D	1.5	1.6	D	20.2	
D1	1.5		G	16.4	18.4
E	1.65	1.85	N	50	
F	7.4	7.6	T		22.4
K0	2.55	2.75			
P0	3.9	4.1	Base qty.		2500
P1	7.9	8.1	Bulk qty.		2500
P2	1.9	2.1			
R	40				
T	0.25	0.35			
W	15.7	16.3			

## 5 Revision history

Table 12: Document revision history

Date	Revision	Changes
12-May-2015	1	First release.

**IMPORTANT NOTICE – PLEASE READ CAREFULLY**

STMicroelectronics NV and its subsidiaries ("ST") reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice. Purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST's terms and conditions of sale in place at the time of order acknowledgement.

Purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of Purchasers' products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

ST and the ST logo are trademarks of ST. All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.

© 2015 STMicroelectronics – All rights reserved