SST38LF6401RT

64-Mbit (x16) Radiation Tolerant Parallel Flash Memory

Features

- Organized as 4M x16
- Single Voltage Read and Write Operations:
  - 3V-3.6V
- Radiation Tolerance Data:
  - Total dose:
    - Unbiased: 75 krad (Si) (Read)/50 krad (Si) (Write)
    - Biased: 50 krad (Si) (Read)/50 krad (Si) (Write)
- Heavy Ion Single Event Effects:
  - Single Event Upset (SEU) Rate < 5.18 x 10^{-22} upsets/bit-day
  - Latch-up immunity > 78 MeV.cm^2/mg (+125°C)
- Superior Reliability:
  - Endurance: 10,000 cycles minimum
  - Greater than 20 years data retention
- Low-Power Consumption (typical values at 5 MHz)
  - Active current: 4 mA (typical)
  - Standby current: 3 µA (typical)
  - Auto Low-Power mode: 3 µA (typical)
- 128-Bit Unique ID
- Security ID Feature:
  - 256-word, user One-Time-Programmable (OTP)
- Hardware Reset Pin (RST#)
- Fast Read and Page Read Access Time:
  - 90 ns Read access time
  - 25 ns Page Read access time
  - 4-word Page Read buffer
- Latched Address and Data
- Fast Erase Times:
  - Sector Erase time: 18 ms (typical)
  - Block Erase time: 18 ms (typical)
  - Chip Erase time: 40 ms (typical)
- Erase Suspend/Erase Resume Capabilities
- Fast Word and Write Buffer Programming Times:
  - Word Program time: 7 µs (typical)
  - Write Buffer Programming time: 1.75 µs/word (typical)
  - 16-word Write buffer
- Automatic Write Timing:
  - Internal V_{PP} generation
- End-of-Write Detection:
  - Toggle bits
  - Data# polling
  - RY/BY# Output
- CMOS I/O Compatibility
- JEDEC® Standard:
  - Flash EEPROM pinouts and command sets
- CFI Compliant
- Temperature Range:
  - Military: -55°C to +125°C
- All Devices are RoHS Compliant

Packages

- 48-Lead TSOP
- 48-Lead Ceramic Dual Flat Package (CDFP)

Mass

- TSOP48: 0.6g
- CDFP48:
  - Formed and Cropped: 2g

Product Description

The SST38LF6401RT is a 4M x16 Radiation Tolerant device manufactured with proprietary, high-performance CMOS SuperFlash® technology. The split-gate cell design and thick-oxide tunneling injector attain better reliability and manufacturability compared with alternate approaches. The SST38LF6401RT writes (Program or Erase) with a 3V-3.6V power supply. These devices conform to JEDEC® standard pin assignments for x16 memories.

Featuring a high-performance Word Program, the SST38LF6401RT provides a typical Word Program time of 7 µsec. For faster word programming performance, the Write Buffer Programming feature has a typical word program time of 1.75 µsec. These devices use Toggle Bit or Data# Polling to indicate the completion of Program operations. In addition to single-word Read, the device also provides a Page Read feature that enables a faster word read time of 25 ns for words on the same page.

The SuperFlash technology offers fixed Erase and Program times, independent of the number of Erase/Program cycles that have occurred.

© 2020-2024 Microchip Technology Inc. and its subsidiaries

Therefore, there is no need to modify or derate the system software or hardware, as is necessary with alternative Flash technologies, where Erase and Program times increase with the accumulation of Erase/Program cycles.

To meet high-density, surface mount requirements, the SST38LF6401RT devices are offered in a 48-lead TSOP package and a 48-lead Ceramic dual flat package. See Figure 2-1 for pin assignments and Table 2-1 for pin descriptions.

Space Quality Grade

The hermetic SST38LF6401RT is manufactured in compliance with the following MIL class Q or class V requirements: screening tests, qualification tests and TCI/QCI specifications. The plastic SST38LF6401RT is compliant with AEC-Q100 automotive requirements, with specific additional tests necessary for space applications. Screening and qualification flows are described in the Aerospace and Defense AEQA0242 specification available on the Microchip website.

TO OUR VALUED CUSTOMERS

It is our intention to provide our valued customers with the best documentation possible to ensure successful use of your Microchip products. To this end, we will continue to improve our publications to better suit your needs. Our publications will be refined and enhanced as new volumes and updates are introduced.

If you have any questions or comments regarding this publication, please contact the Marketing Communications Department via E-mail at at **doc.errors@microchip.com**. We welcome your feedback.

Most Current Data Sheet

To obtain the most up-to-date version of this data sheet, please register at our website:

http://www.microchip.com

You can determine the version of a data sheet by examining its literature number found on the bottom outside corner of any page. The last character of the literature number is the version number, (e.g., DS30000000A is version A of document DS30000000).

Errata

An errata sheet, describing minor operational differences from the data sheet and recommended workarounds, may exist for current devices. As device/documentation issues become known to us, we will publish an errata sheet. The errata will specify the revision of silicon and revision of document to which it applies.

To determine if an errata sheet exists for a particular device, please check with one of the following:

- Microchip's website: **http://www.microchip.com**
- Your local Microchip sales office (see last page)

When contacting a sales office, please specify which device, revision of silicon and data sheet (include literature number) you are using.

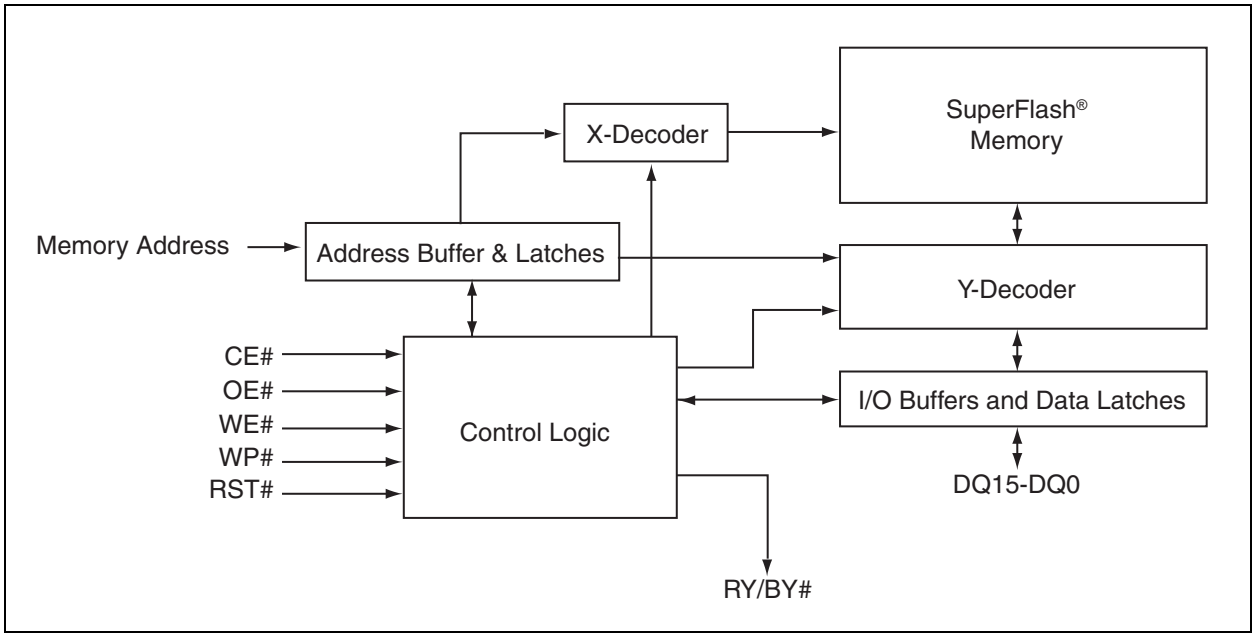
Customer Notification System

Register on our website at **www.microchip.com** to receive the most current information on all of our products.

© 2020-2024 Microchip Technology Inc. and its subsidiaries

1.0 BLOCK DIAGRAM

FIGURE 1-1: FUNCTIONAL BLOCK DIAGRAM



2.0 PIN DESCRIPTION

FIGURE 2-1: PIN DESCRIPTIONS

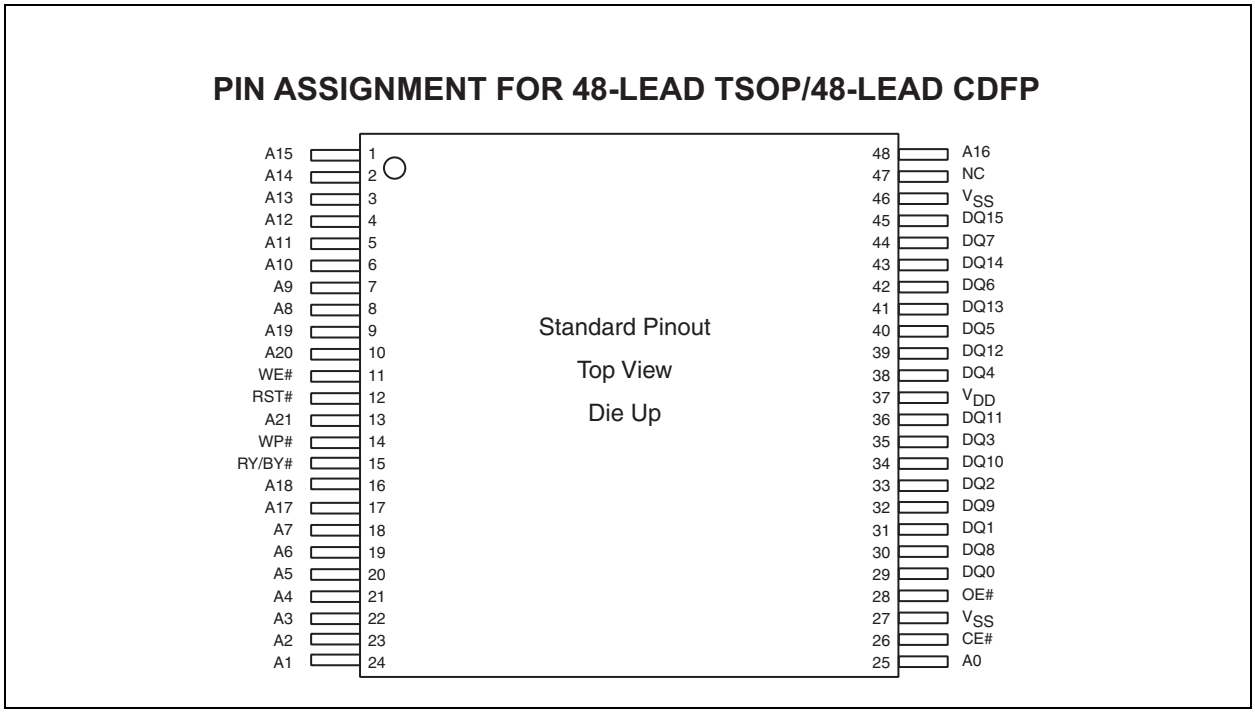


TABLE 2-1: PIN DESCRIPTION

Symbol	Pin Name	Functions
A_{MS}[1]-A0	Address Inputs	Provide memory addresses. During Sector Erase A_{MS}-A12 address lines will select the sector. During Block Erase A_{MS}-A15 address lines will select the block.
DQ15-DQ0	Data Input/Output	Output data during Read cycles and receive input data during Write cycles. Data are internally latched during a Write cycle. The outputs are in tri-state when OE# or CE# is high.
WP#	Write-Protect	Protect the top/bottom Boot Block from Erase/Program operation when grounded.
RY/BY#	Ready/Busy	Indicate when the device is actively programming or erasing.
RST#	Reset	Reset and return the device to Read mode.
CE#	Chip Enable	Activate the device when CE# is low.
OE#	Output Enable	Gate the data output buffers.
WE#	Write Enable	Control the Write operations.
V_{DD}	Power Supply	Provide power supply voltage: 3V-3.6V
V_{SS}	Ground	
NC	No Connection	Unconnected pins.

Note 1: A_{MS} = Most significant address
A_{MS} = A21 for SST38LF6401RT

© 2020-2024 Microchip Technology Inc. and its subsidiaries

3.0 MEMORY MAPS

TABLE 3-1: SST38LF6401RT MEMORY MAP

SST38LF6401RT			
Block(1,2)	**Sectors(3)**	**Address A21-12(4)**	**WP**
B0(5)	S0-S7	0000000XXX	YES
B1	S8-S15	0000001XXX	NO
B2	S16-S23	0000010XXX	NO
B3	S24-S31	0000011XXX	NO
B4	S32-S39	0000100XXX	NO
B5	S40-S47	0000101XXX	NO
B6	S48-S55	0000110XXX	NO
B7	S56-S63	0000111XXX	NO
B8-B119 follow the same pattern			
B120	S960-S967	1111000XXX	NO
B121	S968-S975	1111001XXX	NO
B122	S976-S983	1111010XXX	NO
B123	S984-S991	1111011XXX	NO
B124	S992-S999	1111100XXX	NO
B125	S1000-S1007	1111101XXX	NO
B126	S1008-S1015	1111110XXX	NO
B127	S1016-S1023	1111111XXX	NO

Note 1: Each block, B0-B127 is 32-KWord.

2: Each block consists of eight sectors.

3: Each sector, S0-S1023 is 4-KWord.

4: X = 0 or 1. Block Address (BA) = A21-A15; Sector Address (SA) = A21-A12.

5: Block B0 is the Boot Block.

© 2020-2024 Microchip Technology Inc. and its subsidiaries

4.0 DEVICE OPERATION

The memory operation functions of this device are initiated using commands written to the device using standard microprocessor Write sequences. A command is written by asserting WE# low while keeping CE# low. The address bus is latched on the falling edge of WE# or CE#, whichever occurs last. The data bus is latched on the rising edge of WE# or CE#, whichever occurs first.

The SST38LF6401RT also has Auto Low-Power mode, which puts the device in a near-standby mode after data have been accessed with a valid Read operation. This reduces the I_{DD} active read current from typically 4 mA to typically 3 µA.

Auto Low-Power mode reduces the typical I_{DD} active read current to the range of 2 mA/MHz of Read cycle time. The device requires no access time to exit Auto Low-Power mode after any address transition or control signal transition used to initiate another Read cycle. The device does not enter Auto Low-Power mode after power-up with CE# held steadily low until the first address transition, or until CE# is driven high.

4.1 Read

The Read operation of the SST38LF6401RT is controlled by CE# and OE#, both of which have to be low for the system to obtain data from the outputs. CE# is used for device selection. When CE# is high, the chip is deselected, and only standby power is consumed. OE# is the output control and is used to gate data from the output pins. The data bus is in a high-impedance state when either CE# or OE# is high. Refer to Figure 7-1 for further details.

4.2 Page Read

The Page Read operation utilizes an asynchronous method that enables the system to read data from the SST38LF6401RT at a faster rate. This operation allows users to read a four-word page of data at an average speed of 41.25 ns per word.

In Page Read, the initial word read from the page requires T_{ACC} to be valid, while the remaining three words in the page require only T_{PACC}. All four words on the page have the same address bits, A21-A2, which are used to select the page. Address bits A1 and A0 are toggled, in any order, to read the words within the page.

The Page Read operation of the SST38LF6401RT is controlled by CE# and OE#. Both CE# and OE# must be low for the system to obtain data from the output pins. CE# controls device selection. When CE# is high, the chip is deselected, and only standby power is consumed. OE# is the output control and is used to gate data from the output pins. The data bus is in a high- impedance state when either CE# or OE# is high. Refer to Figure 7-2 for further details.

4.3 Word Program Operation

The SST38LF6401RT can be programmed on a word-by-word basis. Before programming, the sector where the word exists must be fully erased. The Program operation is accomplished in three steps.

1. The first step is the three-byte load sequence.
2. The second step is to load the word address and word data. During the Word Program operation, the addresses are latched on the falling edge of either CE# or WE#, whichever occurs last. The data are latched on the rising edge of either CE# or WE#, whichever occurs first.
3. The third step is the internal Program operation, which is initiated after the rising edge of the fourth WE# or CE#, whichever occurs first. The Program operation, once initiated, will be completed within 10 µs. See Figures 7-3 and 7-4 for WE# and CE# controlled Program operation timing diagrams and Figure 7-20 for flowcharts.

During the Program operation, the only valid reads are Data# Polling, Toggle Bits and RY/BY#. During the internal Program operation, the host is free to perform additional tasks. Any commands issued during the internal Program operation are ignored. During the command sequence, WP# should be statically held high or low.

When programming more than a few words, Microchip recommends Write-Buffer Programming.

4.4 Write Buffer Programming

The SST38LF6401RT offers Write Buffer Programming, a feature that enables faster and more effective word programming. To use this feature, write up to 16 words with the Write-to-Buffer command, then use the Program Buffer-to-Flash command to program the Write Buffer to memory.

The Write-to-Buffer command consists of between 5 and 20 write cycles. The total number of write cycles in the Write-to-Buffer command sequence is equal to the number of words to be written to the buffer plus four.

The first three cycles in the command sequence tell the device that a Write-to-Buffer operation will begin.

The fourth cycle tells the device the number of words to be written into the buffer and the block address of these words. Specifically, the write cycle includes a block address and a data value called the Word Count (WC), which is the number of words to be written to the buffer minus one. If the WC exceeds 15 (the maximum buffer size minus one), the operation is aborted.

© 2020-2024 Microchip Technology Inc. and its subsidiaries

For the fifth cycle and all subsequent cycles of the Write-to-Buffer command, the command sequence consists of the addresses and data of the words to be written into the buffer. All of these cycles must have the same A21-A4 address; otherwise, the operation aborts. The number of Write cycles required is equal to the number of words to be written into the Write Buffer, which is equal to WC plus one. The correct number of Write cycles must be issued, or the operation will abort. Each Write cycle decrements the Write Buffer counter, even if two or more of the Write cycles have identical address values. Only the final data loaded for each buffer location is retained in the Write Buffer.

Once the Write-to-Buffer command sequence is completed, the Program Buffer-to-Flash command should be issued to program the Write Buffer contents to the specified block in memory.

The block address (i.e., A21-A15) in this command must match the block address in the fourth write cycle of the Write-to-Buffer command, or the operation aborts. See Table 5-2 for details on Write-to-Buffer and Program Buffer-to-Flash commands.

While issuing these command sequences, the Write Buffer Programming Abort detection bit (DQ1) indicates if the operation has aborted. There are several cases in which the device can abort:

- In the fourth write cycle of the Write-to-Buffer command, if the WC is greater than 15, the operation aborts.
- In the fifth and all subsequent cycles of the Write-to-Buffer command, if the address values, (A21-A4) are not identical, the operation aborts.
- If the number of write cycles from the fifth to the last cycle of the Write-to-Buffer command is greater than WC + 1, the operation aborts.
- After completing the Write-to-Buffer command sequence, issuing any command other than the Program Buffer-to-Flash command aborts the operation.
- Loading a block address (i.e., A21-A15) in the Program Buffer-to-Flash command that does not match the block address used in the Write-to-Buffer command aborts the operation.

If the Write-to-Buffer or Program Buffer-to-Flash operation aborts, then DQ1 = 1, and the device enters Write-Buffer-Abort mode. To execute another operation, a Write-to-Buffer Abort Reset command must be issued to clear DQ1 and return the device to standard Read mode.

After the Write-to-Buffer and Program Buffer-to-Flash commands are successfully issued, the programming operation can be monitored using Data# Polling, Toggle Bits and RY/BY#.

4.5 Sector/Block Erase Operations

The Sector Erase and Block Erase operations allow the system to erase the device on a sector-by-sector or block-by-block basis. The SST38LF6401RT offers both Sector Erase and Block Erase modes.

The Sector Erase architecture is based on a sector size of 4 KWords. The Sector Erase command can erase any 4-KWord sector (S0-S1023).

The Block Erase architecture is based on block size of 32 KWords. In SST38LF6401RT device, the Block Erase command can erase any 32-KWord block (B0-B127).

The Sector Erase operation is initiated by executing a six-byte command sequence with the Sector Erase command (50H) and the sector address (SA) in the last bus cycle. The Block Erase operation is initiated by executing a six-byte command sequence with the Block Erase command (30H) and the block address (BA) in the last bus cycle. The sector or block address is latched on the falling edge of the sixth WE# pulse, while the command (50H or 30H) is latched on the rising edge of the sixth WE# pulse. The internal Erase operation begins after the sixth WE# pulse. The End-of-Erase operation can be determined using either Data# Polling or Toggle Bit methods. The RY/BY# pin can also be used to monitor the erase operation. For more information, see Figures 7-10 and 7-11 for timing waveforms and Figure 7-25 for the flowchart.

Any commands, other than Erase Suspend, issued during the Sector or Block Erase operation are ignored. Any attempt to perform a Sector or Block Erase on memory inside a block protected by Volatile Block Protection, Nonvolatile Block Protection, or WP# (low) will be ignored. During the command sequence, WP# should be statically held high or low.

© 2020-2024 Microchip Technology Inc. and its subsidiaries

4.6 Erase Suspend/Erase Resume Commands

The Erase Suspend operation temporarily suspends a Sector or Block Erase operation, thus allowing data to be read or programmed into any sector or block that is not engaged in an Erase operation. The operation is executed with a one-byte command sequence with Erase Suspend command (B0H). The device automatically enters Read mode within 20 µs (maximum) after the Erase Suspend command is issued. Valid data can be read, using a Read or Page Read operation, from any sector or block that is not being erased. Reading at an address location within Erase Suspended sectors or blocks will output DQ2 toggling and DQ6 at '1'. While in Erase Suspend, a Word Program or Write Buffer Programming operation is allowed anywhere except in the sector or block selected for Erase Suspend.

To resume a suspended Sector Erase or Block Erase operation, the system must issue the Erase Resume command. The operation is executed by issuing one byte command sequence with Erase Resume command (30H) at any address in the last byte sequence.

When an erase operation is suspended or re-suspended after Erase Resume, the cumulative time needed for the erase operation to complete is greater than the erase time of a non-suspended erase operation. If the hold time from Erase Resume to the next Erase Suspend operation is less than 200 µs, the cumulative erase time can become very long. Therefore, after issuing an Erase Resume command, the system must wait at least 200 µs before issuing another Erase Suspend command. The Erase Resume command will be ignored until any program operations initiated during Erase Suspend are complete.

Bypass mode can be entered while in Erase Suspend, but only Bypass Word Program is available for those sectors or blocks that are not suspended. Bypass Sector Erase, Bypass Block Erase and Bypass Chip Erase, as well as Erase Suspend and Erase Resume, are not available. To resume an Erase operation, Bypass mode must be exited before issuing an Erase Resume command. For more information about Bypass mode, see **Section 4.12 "Bypass Mode"**.

4.7 Chip Erase Operation

The SST38LF6401RT devices provide a Chip Erase operation that erases the entire memory array to the '1' state. This operation is useful when the entire device must be quickly erased.

The Chip Erase operation is initiated by executing a six-byte command sequence with the Chip Erase command (10H) at address 555H in the last byte of the sequence. The Erase operation begins with the rising edge of the sixth WE# or CE#, whichever occurs first.

During the Erase operation, the only valid reads are Toggle Bit, Data# Polling or RY/BY#. See Table 5-2 for the command sequence, Figure 7-9 for timing diagram and Figure 7-26 for the flowchart. Any commands issued during the Chip Erase operation are ignored. If WP# is low or any VPBs or NVPBs are in a protected state, any attempt to execute a Chip Erase operation is ignored. During the command sequence, WP# should be statically held high or low.

4.8 Write Operation Status Detection

To optimize the system's Write cycle time, the SST38LF6401RT provides two software means to detect the completion of a Write (Program or Erase) cycle. The software detection includes two status bits: Data# Polling (DQ7) and Toggle Bit (DQ6). The End-of-Write detection mode is enabled after the rising edge of WE#, which initiates the internal Program or Erase operation.

The actual completion of the nonvolatile write is asynchronous with the system. Therefore, Data# Polling or Toggle Bit may be read concurrently with the completion of the write cycle. If this occurs, the system may get an incorrect result from the status detection process. For example, valid data may appear to conflict with either DQ7 or DQ6. To prevent false results upon the detection of failures, the software routine should loop to read the accessed location an additional two times. If both reads are valid, then the device has completed the Write cycle; otherwise the failure is valid.

For the Write Buffer Programming feature, DQ1 informs the user if either the Write-to-Buffer or Program Buffer-to-Flash operation aborts. If either operation aborts, then DQ1 = 1. DQ1 must be cleared to '0' by issuing the Write-to-Buffer Abort Reset command.

The SST38LF6401RT also provides an RY/BY# signal. This signal indicates the status of a Program or Erase operation.

If a Program or Erase operation is attempted on a protected sector or block, the operation will abort. After the device initiates an abort, the corresponding Write Operation Status Detection Bits will stay active for approximately 200 ns (program or erase) before the device returns to Read mode.

For the status of these bits during a Write operation, see Table 4-1.

4.8.1 DATA# POLLING (DQ7)

When the SST38LF6401RT is in an internal Program operation, any attempt to read DQ7 will produce the complement of the true data. For a Program Buffer-to-Flash operation, DQ7 is the complement of the last word loaded into the Write Buffer using the Write-to-Buffer command. Once the Program operation is completed, DQ7 will produce valid data.

© 2020-2024 Microchip Technology Inc. and its subsidiaries

Note that even though DQ7 may have valid data immediately following the completion of an internal Write operation, the remaining data outputs may still be invalid. Valid data on the entire data bus will appear in subsequent successive Read cycles after an interval of 1 µs.

During an internal Erase operation, any attempt to read DQ7 will produce a '0'. Once the internal Erase operation is completed, DQ7 will produce a '1'. Data# Polling is valid after the rising edge of the fourth WE# (or CE#) pulse for the Program operation. For Sector, Block or Chip Erase, Data# Polling is valid after the rising edge of the sixth WE# (or CE#) pulse. See Figure 7-7 for Data# Polling timing diagram and Figure 7-22 for a flowchart.

4.8.2 TOGGLE BITS (DQ6 AND DQ2)

During the internal Program or Erase operation, any consecutive attempts to read DQ6 will produce alternating '1's and '0's, i.e., toggling between '1' and '0'. When the internal Program or Erase operation is completed, the DQ6 bit will stop toggling, and the device is then ready for the next operation. For Sector, Block or Chip Erase, the toggle bit (DQ6) is valid after the rising edge of the sixth WE# (or CE#) pulse. DQ6 will be set to '1' if a Read operation is attempted on an Erase Suspended Sector or Block. If Program operation is initiated in a sector/block not selected in Erase Suspend mode, DQ6 will toggle.

An additional Toggle Bit is available on DQ2, which can be used in conjunction with DQ6 to check whether a particular sector or block is being actively erased or erase-suspended. Table 4-1 shows detailed bit status information. The Toggle Bit (DQ2) is valid after the rising edge of the last WE# (or CE#) pulse of the Write operation. See Figure 7-8 for the Toggle Bit timing diagram and Figure 7-22 for a flowchart.

4.8.3 DQ1

If an operation is aborted during a Write-to-Buffer or Program Buffer-to-Flash operation, DQ1 is set to '1'. To reset DQ1 to '0', issue the Write-to-Buffer Abort Reset command to exit the abort state. Alternatively, a power-off/power-on cycle or a Hardware Reset (RST# = 0) will also clear DQ1.

4.8.4 RY/BY#

The RY/BY# pin can be used to determine the status of a Program or Erase operation. The RY/BY# pin is valid after the rising edge of the final WE# pulse in the command sequence. If RY/BY# = 0, then the device is actively programming or erasing. If RY/BY# = 1, the device is in Read mode. The RY/BY# pin is an open-drain output pin. This means several RY/BY# pins can be tied together with a pull-up resistor to V_{DD}.

TABLE 4-1: WRITE OPERATION STATUS

Status		DQ7(1)	DQ6	DQ2(1)	DQ1	RY/BY#(2)
Normal Operation	Standard Program	DQ7#	Toggle	No Toggle	0	0
	Standard Erase	0	Toggle	Toggle	N/A	0
Erase Suspend Mode	Read from Erase Suspended Sector/Block	1	No Toggle	Toggle	N/A	1
	Read from Non-Erase Suspended Sector/Block	Data	Data	Data	Data	1
	Program	DQ7#	Toggle	N/A	N/A	0
Program Buffer-to-Flash	Busy	DQ7#(3)	Toggle	N/A	0	0
	Abort	DQ7#(3)	Toggle	N/A	1	0

Note 1: DQ7 and DQ2 require a valid address to read status information.

2: RY/BY# is an open-drain pin.

3: During a Program Buffer-to-Flash operation, the datum on the DQ7 pin is the complement of DQ7 of the last word loaded into the Write Buffer using the Write-to-Buffer command.

© 2020-2024 Microchip Technology Inc. and its subsidiaries

4.9 Data Protection

4.9.1 HARDWARE BLOCK PROTECTION

The SST38LF6401RT device supports bottom hardware block protection, which protects the bottom Boot Block of the device. For SST38LF6401RT, the Boot Block consists of the bottom 32-KWord block. The Boot Block addresses are described in Table 4-2.

TABLE 4-2: BOOT BLOCK ADDRESS RANGES

Product	Size	Address Range
SST38LF6401RT	32 kW	000000H-007FFFH

Program and Erase operations are prevented on the Boot Block when WP# is low. If WP# is left floating, it is internally held high via a pull-up resistor. When WP# is high, the Boot Block is unprotected, allowing Program and Erase operations on that area.

4.9.2 HARDWARE RESET (RST#)

The RST# pin provides a hardware method of resetting the device to read array data. When the RST# pin is held low for at least T_{RP}, any in-progress operation will terminate and return to Read mode. When no internal Program/Erase operation is in progress, a minimum period of T_{RHR} is required after RST# is driven high before a valid Read can take place. See Figure 7-16 for more information.

The interrupted Erase or Program operation must be re-initiated after the device resumes normal operation mode to ensure data integrity.

4.9.3 COMMON FLASH MEMORY INTERFACE (CFI)

The SST38LF6401RT contains Common Flash Memory Interface (CFI) information that describes the characteristics of the device. To enter CFI Query mode, the system can either write a one-byte sequence using a standard CFI Query Entry command or a three-byte sequence using the SST CFI Query Entry command. A comparison of these two commands is shown in Table 5-2. Once the device enters CFI Query mode, the system can read CFI data at the addresses given in Table 5-3 through Table 5-5.

The system must write the CFI Exit command to return to Read mode. Note that the CFI Exit command is ignored during an internal Program or Erase operation. See Table 5-2 for software command codes, Figures 7-13 and 7-14 for timing waveform and Figures 7-23 and 7-24 for flowcharts.

4.10 Product Identification

Product Identification mode identifies the device as the SST38LF6401RT and the manufacturer as SST. See Table 4-3 for specific address and data information. Product Identification mode is accessed through software operations. The software Product Identification operations identify the part and can be useful when using multiple manufacturers in the same socket. For details, see Table 5-2 for software operation, Figure 7-12 for the software ID Entry and Read timing diagram and Figure 7-23 for the software ID Entry command sequence flowchart.

TABLE 4-3: PRODUCT IDENTIFICATION

	Address	Data
Manufacturer's ID	0000H	BFH
Device ID	0001H	536BH

To return to the standard Read mode, the software Product Identification mode must be exited. The exit is accomplished by issuing the software ID Exit command sequence, which returns the device to Read mode.

See Table 5-2 for software command codes, Figure 7-14 for timing waveform and Figures 7-23 and 7-24 for flowcharts.

© 2020-2024 Microchip Technology Inc. and its subsidiaries

4.11 Security ID

The SST38LF6401RT devices offer a Security ID feature. The Secure ID space is divided into two segments:

- One factory-programmed 128-bit segment
- One user-programmable 256-word segment

See Table 4-4 for address information. The first segment is programmed and locked and contains a 128-bit Unique ID that uniquely identifies the device. The user segment is left unprogrammed for the customer to program as desired.

TABLE 4-4: ADDRESS RANGE FOR SEC ID

	Size	Address
Unique ID	128 bits	000H-007H
User	256W	100H-1FFH

The user segment of the Security ID can be programmed in several ways. For smaller datasets, use the Security ID Word Program command for word-by-word programming. To program larger sets of data more quickly, use the SEC ID Entry command to enter the Secure ID space. Once in the Secure ID space, use the Write Buffer Programming or Bypass mode feature. Note that the Word Programming command can also be used while in this mode.

To detect the end-of-write for the SEC ID, read the toggle bits. Do not use Data# Polling to detect the end of the Write.

The Secure ID space can be queried by executing a three-byte command sequence with the Enter Sec ID command (88H) at address 555H in the last byte of the sequence. To exit this mode, the Exit Sec ID command should be executed. Refer to Table 5-2 for software commands and to Figures 7-23 and 7-24 for flowcharts.

4.12 Bypass Mode

Bypass mode shortens the time needed to issue program and erase commands by reducing these commands to two write cycles each. After using the Bypass Entry command to enter Bypass mode, only the Bypass Word Program, Bypass Sector Erase, Bypass Block Erase, Bypass Chip Erase, Erase Suspend and Erase Resume commands are available. The Bypass Exit command exits Bypass mode. See Table 5-2 for further details.

Entering Bypass Mode while already in Erase Suspend limits the available commands. See **Section 4.6 "Erase Suspend/Erase Resume Commands"** for more information.

5.0 OPERATIONS

TABLE 5-1: OPERATION MODES SELECTION

Mode	CE#	OE#	WE#	RST#	WP#	DQ	Address
Read	V_{IL}	V_{IL}	V_{IH}	H	X	D_{OUT}	A_{IN}
Program	V_{IL}	V_{IH}	V_{IL}	H	V_{IL}/V_{IH}(1)	D_{IN}	A_{IN}
Erase	V_{IL}	V_{IH}	V_{IL}	H	V_{IL}/V_{IH}(1)	X(2)	Sector or block address, XXH for Chip Erase
Standby	V_{IH}	X	X	V_{IH}	X	High-Z	X
Write Inhibit	X	V_{IL}	X	X	X	High-Z/D_{OUT}	X
Product Identification	X	X	V_{IH}	H	X	High-Z/D_{OUT}	X
Reset	X	X	X	L	X	High-Z	X
Software Mode	V_{IL}	V_{IH}	V_{IL}	H	X	see Table 5-2	see Table 5-2

Note 1: WP# can be V_{IL} when programming or erasing outside of the Boot Block.
WP# must be V_{IH} when programming or erasing inside the Boot Block area.

2: X can be V_{IL} or V_{IH}, but no other value.

TABLE 5-2: SOFTWARE COMMAND SEQUENCE

Command Sequence	1st Bus Cycle		2nd Bus Cycle		3rd Bus Cycle		4th Bus Cycle		5th Bus Cycle		6th Bus Cycle		7th Bus Cycle	
	Addr[1]	Data[2]	Addr[1]	Data[2]	Addr[1]	Data[2]	Addr[1]	Data[2]	Addr[1]	Data[2]	Addr[1]	Data[2]	Addr[1]	Data[2]
Read[3]	WA	Data												
Page Read[3]	WA0	Data0	WA1	Data1	WA2	Data2	WA3	Data3						
Word Program	555H	AAH	2AAH	55H	555H	A0H	WA	Data						
Write Buffer Programming														
Write to Buffer[4]	555H	AAH	2AAH	55H	BA	25H	BA	WC	WA_X	Data	WA_X	Data	WA_X	Data
Program Buffer to Flash	BA_X	29H												
Write to Buffer Abort Reset	555H	AAH	2AAH	55H	555H	F0H								

Note 1: Address format A10-A0 (Hex). Addresses A11- A21 can be V_{IL} or V_{IH}, but no other value, for the SST38LF6401RT command sequence.

2: DQ15-DQ8 can be V_{IL} or V_{IH}, but no other value, for command sequence.

3: All read commands are in ***bold italics***.

4: The total number of cycles in this command sequence depends on the number of words to be written to the buffer. Additional words are written by repeating Write Cycle 5. Address (WA_X) values for Write Cycle 6 and later must have the same A21-A4 values as WA_X in Write Cycle 5. WC = Word Count. The value of WC is the number of words to be written into the buffer, minus one. Maximum WC value is 15 (i.e., F Hex)

5: Erase Suspend and Erase Resume commands are also available in Bypass mode.

6: Once in Sec ID mode, the Word Program, Write Buffer Programming and Bypass Word Program features can be used to program the Sec ID area.

7: The Unique ID is read with A3 = 0 (Address range = 000000H to 000007H), the User portion of Sec ID is read with A8 = 1 (Address range = 000100H to 0001FFH), and the lockout status is read with A7-A0 = FFH. Unlocked: DQ3 = 1; Locked: DQ3 = 0.

8: Both Software ID Exit operations are equivalent.

9: If bits are not locked, then the user-programmable portion of the Sec ID can be programmed over the previously unprogrammed bits (Data = 1) using the Sec ID mode again (bits programmed as '0' cannot be reversed to '1'). Valid Word Addresses for the user-programmable portion of the Sec ID are from 000100H to 0001FFH.

10: The device does not remain in Software Product ID Mode if powered down.

11: With A_{MS}-A1 = 0; Manufacturer ID = 00BFH, is read with A0 = 0, SST38LF6401RT Device ID = 536BH, is read with A0 = 1.

12: CFI Query Entry and SST CFI Query Entry are equivalent. Both allow access to the same CFI tables.

© 2020-2024 Microchip Technology Inc. and its subsidiaries

TABLE 5-2: SOFTWARE COMMAND SEQUENCE (CONTINUED)

Command Sequence	1st Bus Cycle		2nd Bus Cycle		3rd Bus Cycle		4th Bus Cycle		5th Bus Cycle		6th Bus Cycle		7th Bus Cycle	
	Addr[1]	Data[2]	Addr[1]	Data[2]	Addr[1]	Data[2]	Addr[1]	Data[2]	Addr[1]	Data[2]	Addr[1]	Data[2]	Addr[1]	Data[2]
Bypass Mode[5]														
Bypass Mode Entry	555H	AAH	2AAH	55H	555H	20H								
Bypass Word Program	XXXH	A0H	WA_X	Data										
Bypass Sector Erase	XXXH	80H	SA_X	50H										
Bypass Block Erase	XXXH	80H	BA_X	30H										
Bypass Chip Erase	XXXH	80H	555H	10H										
Bypass Mode Exit	XXXH	90H	XXH	00H										
Erase Related														
Sector Erase	555H	AAH	2AAH	55H	555H	80H	555H	AAH	2AAH	55H	SA_X	50H		
Block Erase	555H	AAH	2AAH	55H	555H	80H	555H	AAH	2AAH	55H	BA_X	30H		
Chip Erase	555H	AAH	2AAH	55H	555H	80H	555H	AAH	2AAH	55H	555H	10H		
Erase Suspend	XXXH	B0H												
Erase Resume	XXXH	30H												
Security ID														
Sec ID Entry[6]	555H	AAH	2AAH	55H	555H	88H								
Sec ID Read[3,7]	WA_X	Data												
Sec ID Exit	555H	AAH	2AAH	55H	555H	90H	XXH	00H						
Software ID Exit/CFI Exit/Sec ID Exit[8]	555H	AAH	2AAH	55H	555H	F0H								
Software ID Exit/CFI Exit/Sec ID Exit[9]	XXH	F0H												

Note 1: Address format A10-A0 (Hex). Addresses A11- A21 can be VIL or VIH, but no other value, for the SST38LF6401RT command sequence.

2: DQ15-DQ8 can be VIL or VIH, but no other value, for command sequence.

3: All read commands are in ***bold italics***.

4: The total number of cycles in this command sequence depends on the number of words to be written to the buffer. Additional words are written by repeating Write Cycle 5. Address (WA_X) values for Write Cycle 6 and later must have the same A21-A4 values as WA_X in Write Cycle 5. WC = Word Count. The value of WC is the number of words to be written into the buffer, minus one. Maximum WC value is 15 (i.e., F Hex)

5: Erase Suspend and Erase Resume commands are also available in Bypass mode.

6: Once in Sec ID mode, the Word Program, Write Buffer Programming and Bypass Word Program features can be used to program the Sec ID area.

7: The Unique ID is read with A3 = 0 (Address range = 000000H to 000007H), the User portion of Sec ID is read with A8 = 1 (Address range = 000100H to 0001FFH), and the lockout status is read with A7-A0 = FFH. Unlocked: DQ3 = 1; Locked: DQ3 = 0.

8: Both Software ID Exit operations are equivalent.

9: If bits are not locked, then the user-programmable portion of the Sec ID can be programmed over the previously unprogrammed bits (Data = 1) using the Sec ID mode again (bits programmed as '0' cannot be reversed to '1'). Valid Word Addresses for the user-programmable portion of the Sec ID are from 000100H to 0001FFH.

10: The device does not remain in Software Product ID Mode if powered down.

11: With AMS-A1 = 0; Manufacturer ID = 00BFH, is read with A0 = 0, SST38LF6401RT Device ID = 536BH, is read with A0 = 1.

12: CFI Query Entry and SST CFI Query Entry are equivalent. Both allow access to the same CFI tables.

© 2020-2024 Microchip Technology Inc. and its subsidiaries

TABLE 5-2: SOFTWARE COMMAND SEQUENCE (CONTINUED)

Command Sequence	1st Bus Cycle		2nd Bus Cycle		3rd Bus Cycle		4th Bus Cycle		5th Bus Cycle		6th Bus Cycle		7th Bus Cycle	
	Addr[1]	Data[2]	Addr[1]	Data[2]	Addr[1]	Data[2]	Addr[1]	Data[2]	Addr[1]	Data[2]	Addr[1]	Data[2]	Addr[1]	Data[2]
User Security ID Word Program	555H	AAH	2AAH	55H	555H	A5H	WA_X	Data						
User Security ID Program Lock-Out	555H	AAH	2AAH	55H	555H	85H	XXH	0000H						
Product Identification														
Software ID Entry[10]	555H	AAH	2AAH	55H	555H	90H								
Manufacturer ID[3,11]	X00	BFH												
Device ID[3,11]	X01	Data												
Software ID Exit/CFI Exit/Sec ID Exit[8]	555H	AAH	2AAH	55H	555H	F0H								
Software ID Exit/CFI Exit/Sec ID Exit[8]	XXH	F0H												
CFI														
CFI Query Entry[12]	55H	98H												
SST CFI Query Entry[12]	555H	AAH	2AAH	55H	555H	98H								
Software ID Exit/CFI Exit/Sec ID Exit[8]	555H	AAH	2AAH	55H	555H	F0H								
Software ID Exit/CFI Exit/Sec ID Exit[8]	XXH	F0H												

Note 1: Address format A10-A0 (Hex). Addresses A11- A21 can be V_{IL} or V_{IH}, but no other value, for the SST38LF6401RT command sequence.

2: DQ15-DQ8 can be V_{IL} or V_{IH}, but no other value, for command sequence.

3: All read commands are in ***bold italics***.

4: The total number of cycles in this command sequence depends on the number of words to be written to the buffer. Additional words are written by repeating Write Cycle 5. Address (WA_X) values for Write Cycle 6 and later must have the same A21-A4 values as WA_X in Write Cycle 5. WC = Word Count. The value of WC is the number of words to be written into the buffer, minus one. Maximum WC value is 15 (i.e., F Hex)

5: Erase Suspend and Erase Resume commands are also available in Bypass mode.

6: Once in Sec ID mode, the Word Program, Write Buffer Programming and Bypass Word Program features can be used to program the Sec ID area.

7: The Unique ID is read with A3 = 0 (Address range = 000000H to 000007H), the User portion of Sec ID is read with A8 = 1 (Address range = 000100H to 0001FFH), and the lockout status is read with A7-A0 = FFH. Unlocked: DQ3 = 1; Locked: DQ3 = 0.

8: Both Software ID Exit operations are equivalent.

9: If bits are not locked, then the user-programmable portion of the Sec ID can be programmed over the previously unprogrammed bits (Data = 1) using the Sec ID mode again (bits programmed as '0' cannot be reversed to '1'). Valid Word Addresses for the user-programmable portion of the Sec ID are from 000100H to 0001FFH.

10: The device does not remain in Software Product ID Mode if powered down.

11: With A_{MS}-A1 = 0; Manufacturer ID = 00BFH, is read with A0 = 0, SST38LF6401RT Device ID = 536BH, is read with A0 = 1.

12: CFI Query Entry and SST CFI Query Entry are equivalent. Both allow access to the same CFI tables.

© 2020-2024 Microchip Technology Inc. and its subsidiaries

Note: Table 5-2 uses the following abbreviations:

- X = Don't care (V_{IL} or V_{IH}, but no other value)
- SA_X = Sector Address; uses A_{MS}-A_{12} address lines
- BA_X= Block Address; uses A_{MS}-A_{15} address lines
- WA = Word Address
- WC = Word Count
- PWA_X = Password Address; PWA_X = PWA_0, PWA_1, PWA_2 or PWA_3; A1 and A0 are used to select each 16-bit portion of the password
- PWD_X = Password Data; PWD_X = $PSWD_0$, PWD_1, PWD_2 or PWD_3
- A_{MS} = Most significant address

TABLE 5-3: CFI QUERY IDENTIFICATION STRING(1)

Address	Data	Description
10H	0051H	Query Unique ASCII string "QRY"
11H	0052H	
12H	0059H	
13H	0002H	Primary OEM command set
14H	0000H	
15H	0040H	Address for Primary Extended Table
16H	0000H	
17H	0000H	Alternate OEM command set (00H = none exists)
18H	0000H	
19H	0000H	Address for Alternate OEM Extended Table (00H = none exits)
1AH	0000H	

Note 1: Refer to CFI publication 100 for more details.

TABLE 5-4: SYSTEM INTERFACE INFORMATION

Address	Data	Description
1BH	0030H	V_{DD} Minimum (Program/Erase) DQ7-DQ4: Volts, DQ3-DQ0: 100 millivolts
1CH	0036H	V_{DD} Maximum (Program/Erase) DQ7-DQ4: Volts, DQ3-DQ0: 100 millivolts
1DH	0000H	V_{PP} Minimum (00H = no V_{PP} pin)
1EH	0000H	V_{PP} Maximum (00H = no V_{PP} pin)
1FH	0003H	Typical time out for Word Program 2^N µs (2^3 = 8 µs)
20H	0003H	Typical time out for minimum size buffer program 2^N µs (00H = not supported)
21H	0004H	Typical time out for individual Sector/Block-Erase 2^N ms (2^4 = 16 ms)
22H	0005H	Typical time out for Chip Erase 2^N ms (2^5 = 32 ms)
23H	0001H	Maximum time out for Word Program 2^N times typical (2^1 x 2^3 = 16 µs)
24H	0003H	Maximum time out for buffer program 2^N times typical
25H	0001H	Maximum time out for individual Sector/Block-Erase 2^N times typical (2^1 x 2^4 = 32 ms)
26H	0001H	Maximum time out for Chip Erase 2^N times typical (2^1 x 2^5 = 64 ms)

© 2020-2024 Microchip Technology Inc. and its subsidiaries

TABLE 5-5: DEVICE GEOMETRY INFORMATION

Address	Data	Description
27H	0017H	Device size = 2^N Bytes (17H = 23; 2^{23} = 8 Mbyte)
28H	0001H	Flash Device Interface description; 0001H = x16-only asynchronous interface
29H	0000H	
2AH	0005H	Maximum number of bytes in multi-byte write = 2^N (00H = not supported)
2BH	0000H	
2CH	0002H	Number of Erase Sector/Block sizes supported by device
2DH	00FFH	Sector Information (y + 1 = Number of sectors; z x 256B = sector size) y = 2047 + 1 = 2048 sectors (03FFH = 1023) z = 32 x 256 Bytes = 8 Kbytes/sector (0100H = 32)
2EH	0003H	
2FH	0000H	
30H	0001H	
31H	007FH	Block Information (y + 1 = Number of blocks; z x 256B = block size) y =127 + 1 = 128 blocks (007FH = 127) z = 256 x 256 Bytes = 64 Kbytes/block (0100H = 256)
32H	0000H	
33H	0000H	
34H	0001H	

© 2020-2024 Microchip Technology Inc. and its subsidiaries

6.0 ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings (†)

Temperature under bias ..... -55°C to +125°C

Storage temperature ..... -65°C to +150°C

DC voltage on any pin to ground potential ..... -0.5V to V_{DD}+0.5V

Transient voltage (<20 ns) on any pin to ground potential ..... -2.0V to V_{DD}+2.0V

Surface mount solder reflow temperature ..... +260°C for 10 seconds

Output short circuit current[1] ..... 50 mA

† NOTICE: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Note 1: Output shorted for no more than one second. No more than one output shorted at a time.

TABLE 6-1: OPERATING RANGE

Range	Ambient Temperature	V_{DD}
Military	-55°C to +125°C	3V-3.6V

TABLE 6-2: AC CONDITIONS OF TEST[1]

Input Rise/Fall Time	Output Load
5 ns	C_L = 30 pF

Note 1: See Figures 7-18 and 7-19.

TABLE 6-3: RECOMMENDED THERMAL OPERATING CONDITION

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
T_A	Operating Temperature	-55	—	125	°C	—
T_J	Junction Temperature	—	—	145	°C	—
R_{JC}[1]	Junction-to-Case Thermal Resistance	—	—	8.0	°C/W	TSOP
R_{JC}[1]	Junction-to-Case Thermal Resistance	—	—	3.7	°C/W	CDFP
P_D	Power Dissipation	—	—	0.18	W	V_{CC} = 3.6V, I_{CC} = 50 mA during Program Write Buffer to Flash

Note 1: Simulated in vacuum environment.

© 2020-2024 Microchip Technology Inc. and its subsidiaries

6.1 Power-Up Specifications

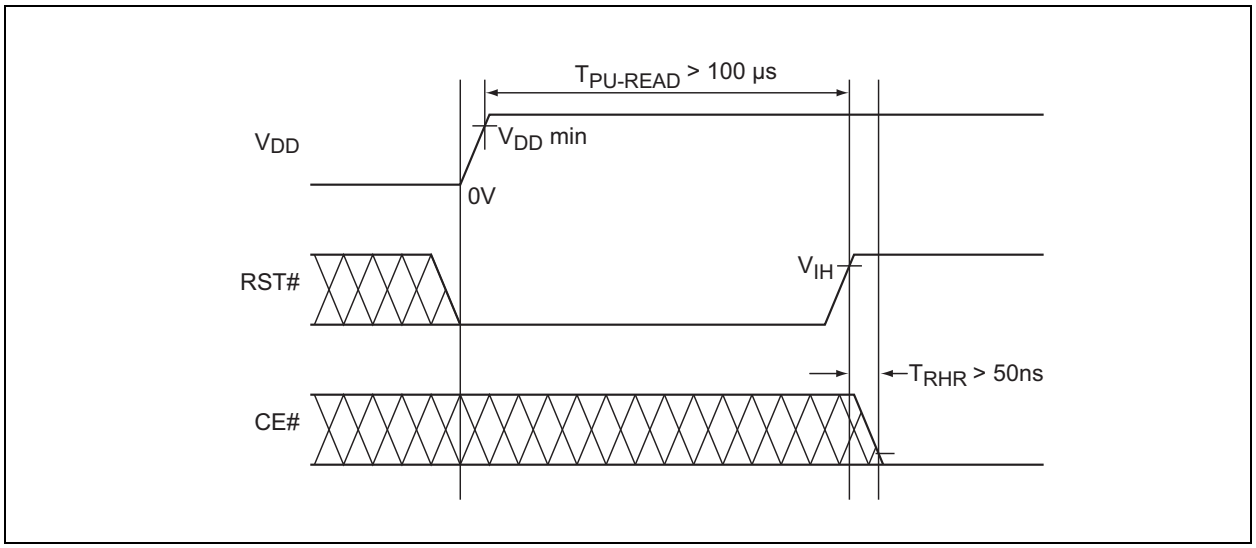
All functionalities and DC specifications are specified for a V_{DD} ramp rate greater than 1V per 100 ms (0V to 3.0V in less than 300 ms). If the V_{DD} ramp rate is slower than 1V per 100 ms, a hardware Reset is required. The recommended V_{DD} power-up to RST# high time should be greater than 100 µs to ensure a proper Reset. See Table 6-4 and Figure 6-1 for more information.

TABLE 6-4: RECOMMENDED SYSTEM POWER-UP TIMINGS

Symbol	Parameter	Minimum	Units
$T_{PU-READ}$(1)	Power-Up to Read Operation	100	µs
$T_{PU-WRITE}$(1)	Power-Up to Erase/Program Operation	100	µs

Note 1: This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

FIGURE 6-1: POWER-UP DIAGRAM



© 2020-2024 Microchip Technology Inc. and its subsidiaries

7.0 DC CHARACTERISTICS

TABLE 7-1: DC OPERATING CHARACTERISTICS (V_{DD} = 3.0V-3.6V)[1]

Symbol	Parameter	Limits			Test Conditions
		Min.	Max.	Unit	
I_{DD}	Power Supply Current	—	—		Address Input = V_{ILT}/V_{ILT}[2], V_{DD} = V_{DD} maximum
	Read[3]	—	18	mA	CE# = V_{IL}, OE# = WE# = V_{IH} at f = 5 MHz
	Intra-Page Read @5 MHz	—	2.5	mA	CE# = V_{IL}, OE# = WE# = V_{IH}
	Intra-Page Read @40 MHz	—	20	mA	CE# = V_{IL}, OE# = WE# = V_{IH}
	Program and Erase	—	35	mA	CE# = WE# = V_{IL}, OE# = V_{IH}
	Program Write Buffer-to-Flash	—	50	mA	CE# = WE# = V_{IL}, OE# = V_{IH}
I_{SB}	Standby Current V_{DD}	—	60	µA	CE# = V_{IH}, V_{DD} = V_{DD} maximum
I_{ALP}	Auto Low Power	—	60	µA	CE# = V_{ILC}, V_{DD} = V_{DD} maximum All inputs = V_{SS} or V_{DD}, WE# = V_{IHC}
I_{LI}	Input Leakage Current	—	1	µA	V_{IN} = GND to V_{DD}, V_{DD} = V_{DD} maximum
I_{LIW}	Input Leakage Current on WP# Pin and RST#	—	10	µA	WP# = GND to V_{DD} or RST# = GND to V_{DD}
I_{LO}	Output Leakage Current	—	10	µA	V_{OUT} = GND to V_{DD}, V_{DD} = V_{DD} maximum
V_{IL}	Input Low Voltage	—	0.8	V	V_{DD} = V_{DD} minimum
V_{ILC}	Input Low Voltage (CMOS)	—	0.3	V	V_{DD} = V_{DD} maximum
V_{IH}	Input High Voltage	0.7V_{DD}	—	V	V_{DD} = V_{DD} maximum
V_{IHC}	Input High Voltage (CMOS)	V_{DD}-0.3	—	V	V_{DD} = V_{DD} maximum
V_{OL}	Output Low Voltage	—	0.2	V	I_{OL} = 100 µA, V_{DD} = V_{DD} minimum
V_{OH}	Output High Voltage	V_{DD}-0.2	—	V	I_{OH} = 100 µA, V_{DD} = V_{DD} minimum

Note 1: Typical conditions for the Active Current shown on the front page of the data sheet are average values at +25°C (room temperature) and V_{DD} = 3V. Not 100% tested.

2: See Figure 7-23.

3: The I_{DD} current listed is typically less than 2 mA/MHz, with OE# at V_{IH}. Typical V_{DD} is 3V.

TABLE 7-2: CAPACITANCE (T_A = 25°C, F = 1 MHZ, OTHER PINS OPEN)

Parameter	Description	Test Condition	Maximum
$C_{I/O}$[1]	I/O Pin Capacitance	$V_{I/O}$ = 0V	12 pF
C_{IN}[1]	Input Capacitance	V_{IN} = 0V	6 pF

Note 1: This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

TABLE 7-3: RELIABILITY CHARACTERISTICS

Symbol	Parameter	Minimum Specification	Unit	Test Method
N_{END}[1,2]	Endurance	10,000	Cycles	JEDEC® Standard A117
T_{DR}[1,3]	Data Retention	20	Years	JEDEC® Standard A103
I_{LTH}[1]	Latch Up	100 + I_{DD}	mA	JEDEC® Standard A78

Note 1: This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

2: N_{END} endurance rating is qualified as 10,000 cycles minimum per block.

3: Data retention performed after 1K cycles endurance.

© 2020-2024 Microchip Technology Inc. and its subsidiaries

TABLE 7-4: READ CYCLE TIMING PARAMETERS (V_{DD} = 3V-3.6V)

Symbol	Parameter	Minimum	Maximum	Unit
T_{RC}	Read Cycle Time	90	—	ns
T_{CE}	Chip Enable Access Time	—	90	ns
T_{AA}	Address Access Time	—	90	ns
T_{PACC}(1)	Page Access Time	—	25	ns
T_{OE}	Output Enable Access Time	—	25	ns
T_{CLZ}(1)	CE# Low to Active Output	0	—	ns
T_{OLZ}(1)	OE# Low to Active Output	0	—	ns
T_{CHZ}(1)	CE# High to High-Z Output	—	20	ns
T_{OHZ}(1)	OE# High to High-Z Output	—	20	ns
T_{OH}(1)	Output Hold from Address Change	0	—	ns
T_{RP}(1)	RST# Pulse Width	500	—	ns
T_{RHR}(1)	RST# High before Read	50	—	ns
T_{RYE}(1,2)	RST# Pin Low to Read Mode	—	20	µs
T_{RY}(1)	RST# Pin Low to Read Mode – not during Program or Erase Algorithms	—	500	ns
T_{RPD}(1)	RST# Input Low to Standby Mode	20	—	µs
T_{RB}(1)	RY/BY# Output High to CE#/OE# Pin Low	0	—	ns

Note 1: This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

2: This parameter applies to Sector Erase, Block Erase and Program operations. This parameter does not apply to Chip Erase operations.

TABLE 7-5: PROGRAM/ERASE CYCLE TIMING PARAMETERS

Symbol	Parameter	Minimum	Maximum	Unit
T_{BP}	Word Program Time	—	10	µs
T_{WBP}(1)	Program Buffer-to-Flash Time	—	40	µs
T_{AS}	Address Setup Time	0	—	ns
T_{AH}	Address Hold Time	30	—	ns
T_{CS}	WE# and CE# Setup Time	0	—	ns
T_{CH}	WE# and CE# Hold Time	0	—	ns
T_{OES}	OE# High Setup Time	0	—	ns
T_{OEH}	OE# High Hold Time	10	—	ns
T_{CP}	CE# Pulse Width	40	—	ns
T_{WP}	WE# Pulse Width	40	—	ns
T_{WPH}(2)	WE# Pulse Width High	30	—	ns
T_{CPH}(2)	CE# Pulse Width High	30	—	ns
T_{DS}	Data Setup Time	30	—	ns
T_{DH}(2)	Data Hold Time	0	—	ns
T_{IDA}(2)	Software ID, Bypass Entry and Exit Times	—	150	ns
T_{SE}	Sector Erase	—	25	ms
T_{BE}	Block Erase	—	25	ms
T_{SCE}	Chip Erase	—	50	ms

Note 1: Effective programming time is 2.5 µs per word if 16 words are programmed during this operation.

2: This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

© 2020-2024 Microchip Technology Inc. and its subsidiaries

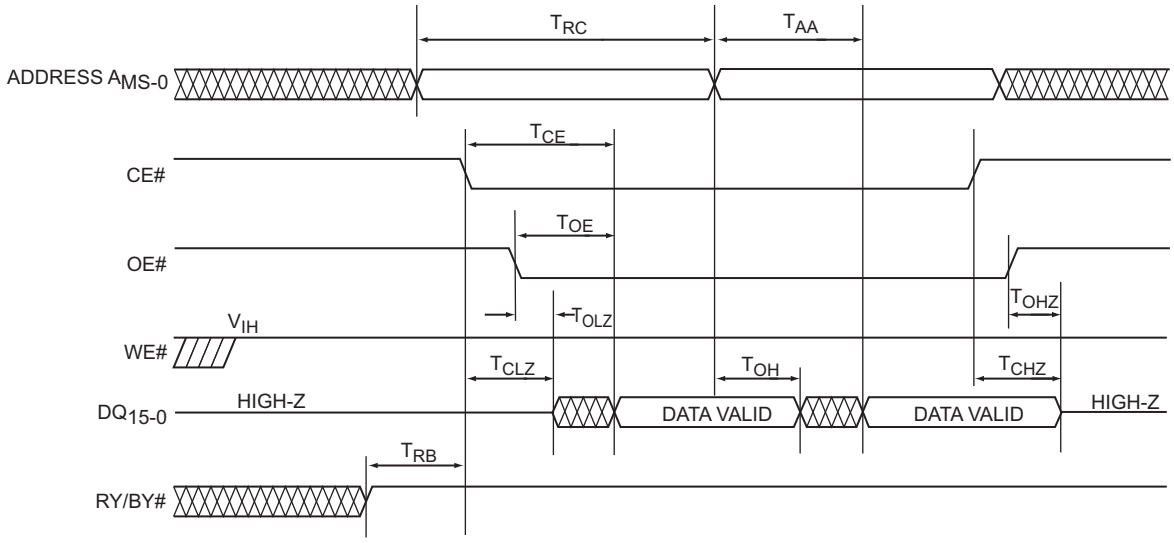
TABLE 7-5: PROGRAM/ERASE CYCLE TIMING PARAMETERS (CONTINUED)

Symbol	Parameter	Minimum	Maximum	Unit
T_{BUSY}	CE# High or WE# High to RY/BY# Low	90	—	ns

Note 1: Effective programming time is 2.5 µs per word if 16 words are programmed during this operation.

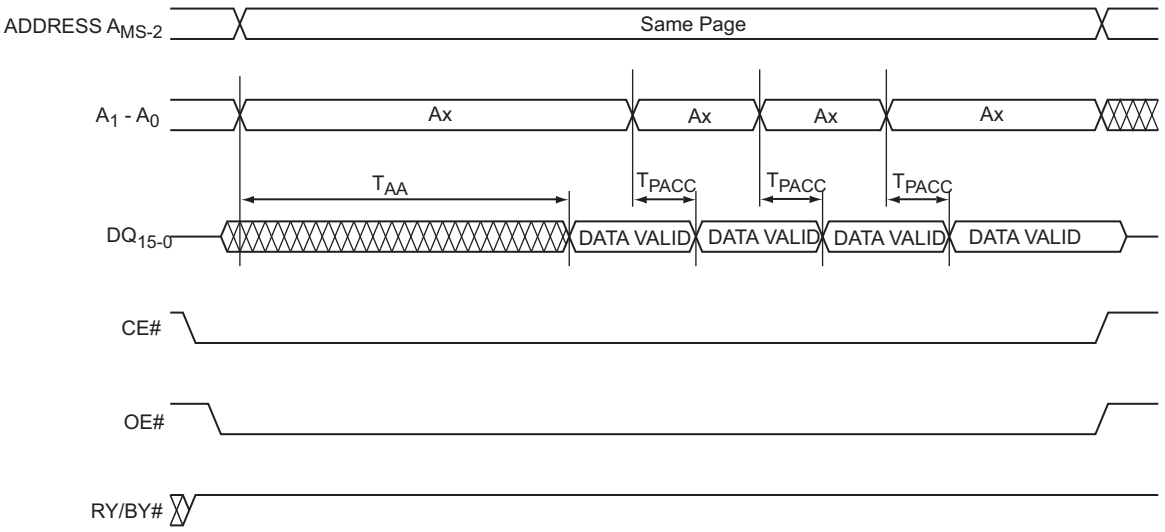
2: This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

FIGURE 7-1: READ CYCLE TIMING DIAGRAM



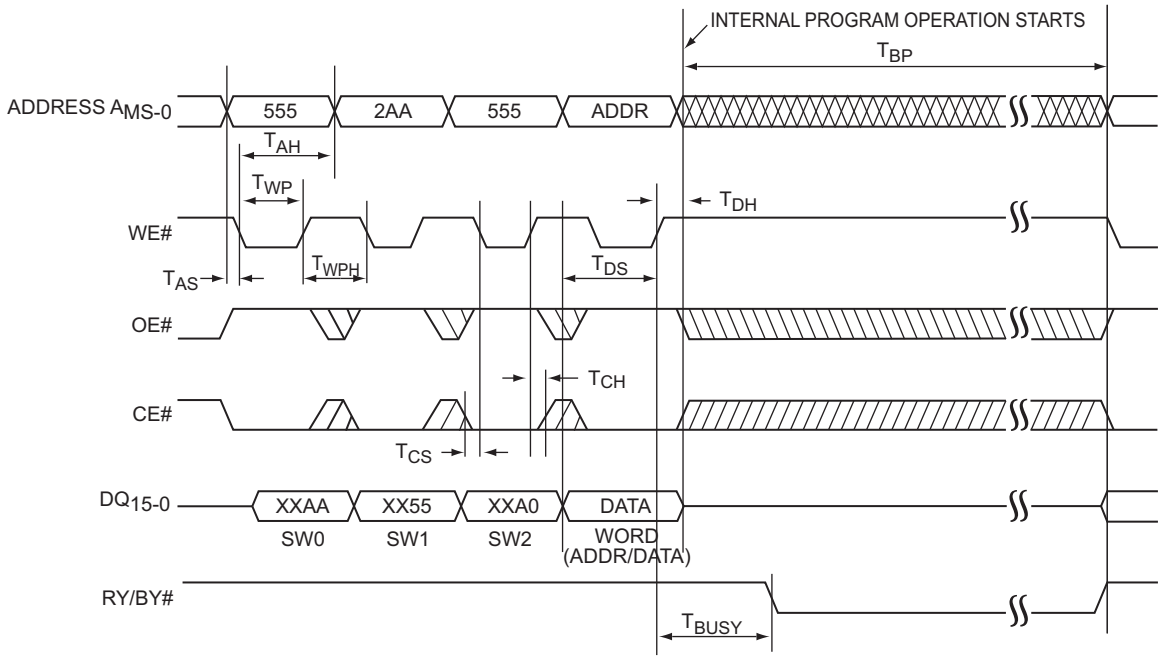
Note 1: AMS = Most significant address

FIGURE 7-2: PAGE READ TIMING DIAGRAM



Note 1: AMS = Most significant address
AMS = A21 for SST38LF6401RT

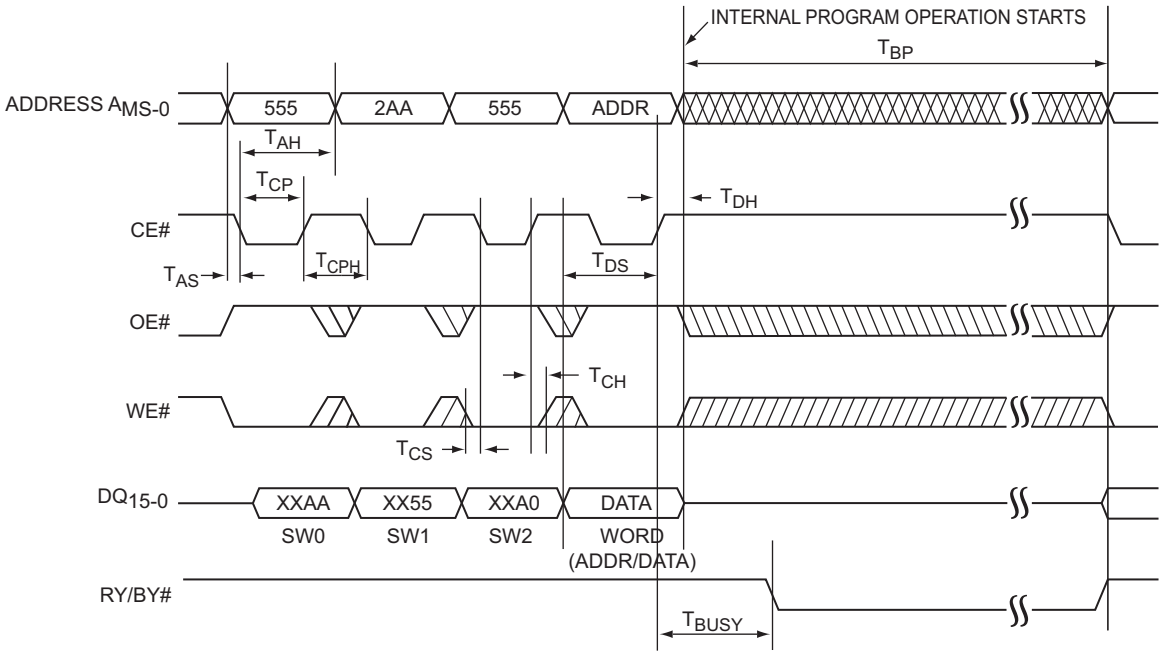
FIGURE 7-3: WE# CONTROLLED PROGRAM CYCLE TIMING DIAGRAM



Note 1: AMS = Most significant address
AMS = A21 for SST38LF6401RT
WP# must be held in proper logic state (VIL or VIH) 1 µs prior to and 1 µs after the command sequence.
X can be VIL or VIH, but no other value.

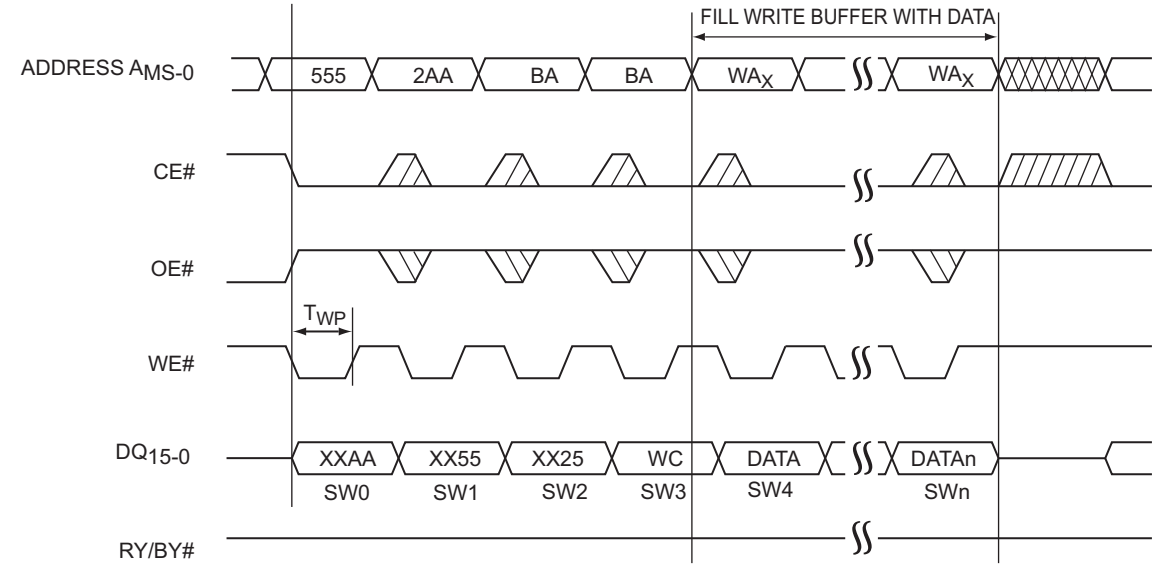
© 2020-2024 Microchip Technology Inc. and its subsidiaries

FIGURE 7-4: CE# CONTROLLED PROGRAM CYCLE TIMING DIAGRAM



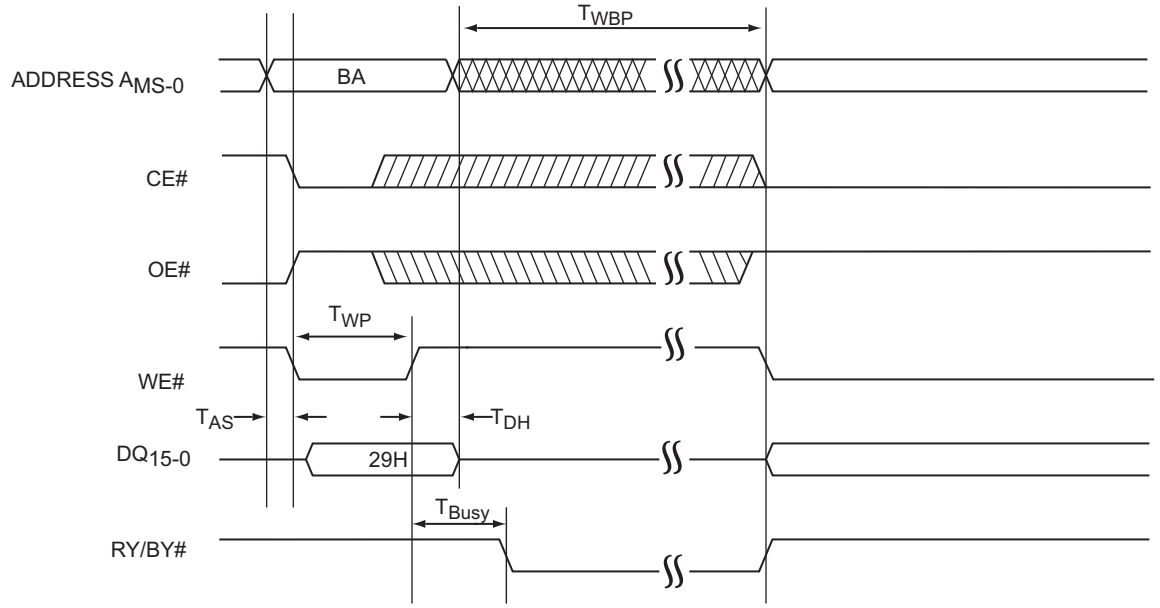
Note 1: AMS = Most significant address
AMS = A21 for SST38LF6401RT
WP# must be held in proper logic state (VIL or VIH) 1 µs prior to and 1 µs after the command sequence.

FIGURE 7-5: WE# CONTROLLED WRITE BUFFER CYCLE TIMING DIAGRAM



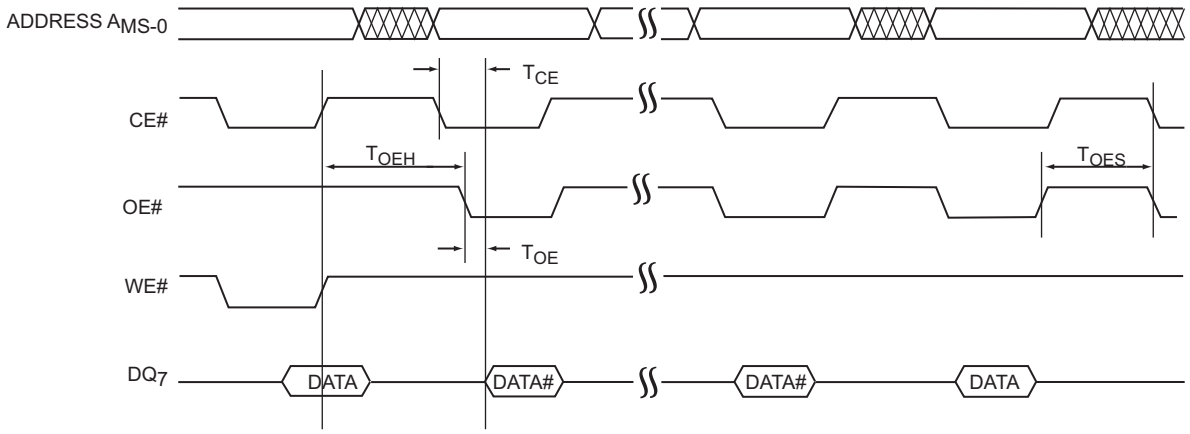
Note 1: BA = Block address
VAX = Word address
WC = Word count
DATAn = nth data

FIGURE 7-6: WE# CONTROLLED PROGRAM WRITE BUFFER-TO-FLASH CYCLE TIMING DIAGRAM



Note 1: BA = Block address

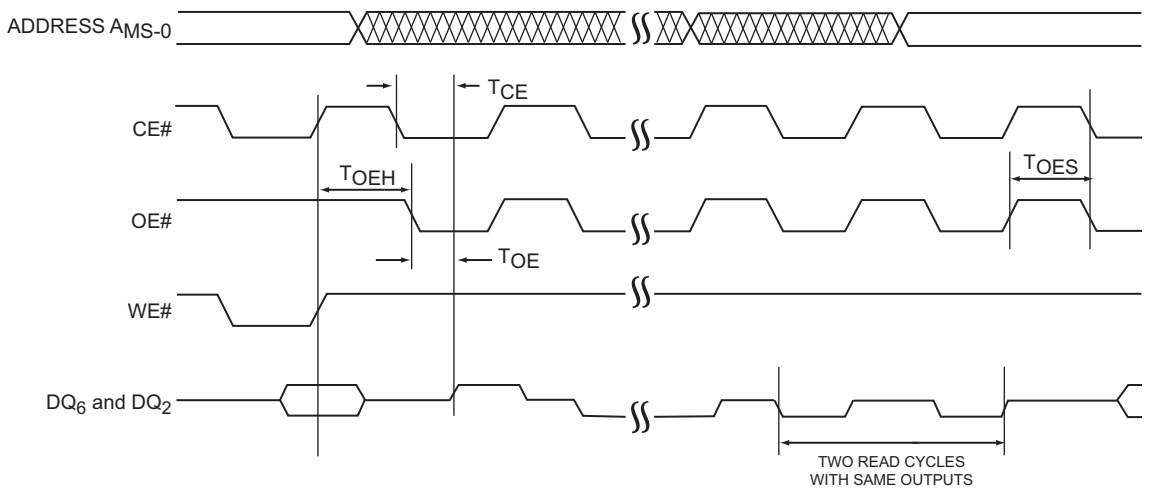
FIGURE 7-7: DATA POLLING TIMING DIAGRAM



Note 1: AMS = Most significant address
AMS = A21 for SST38LF6401RT

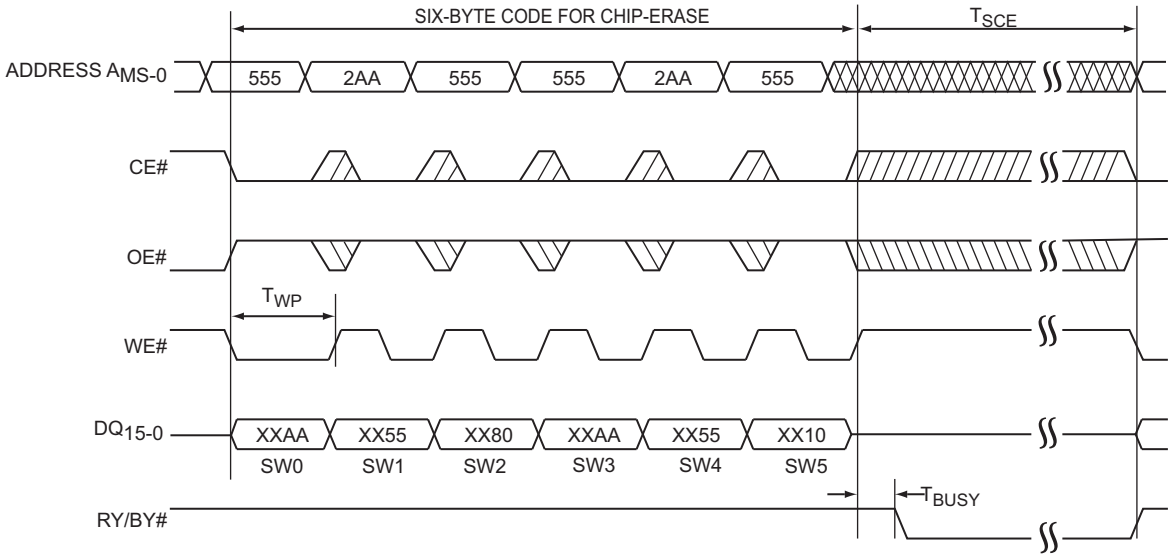
© 2020-2024 Microchip Technology Inc. and its subsidiaries

FIGURE 7-8: TOGGLE BITS TIMING DIAGRAM



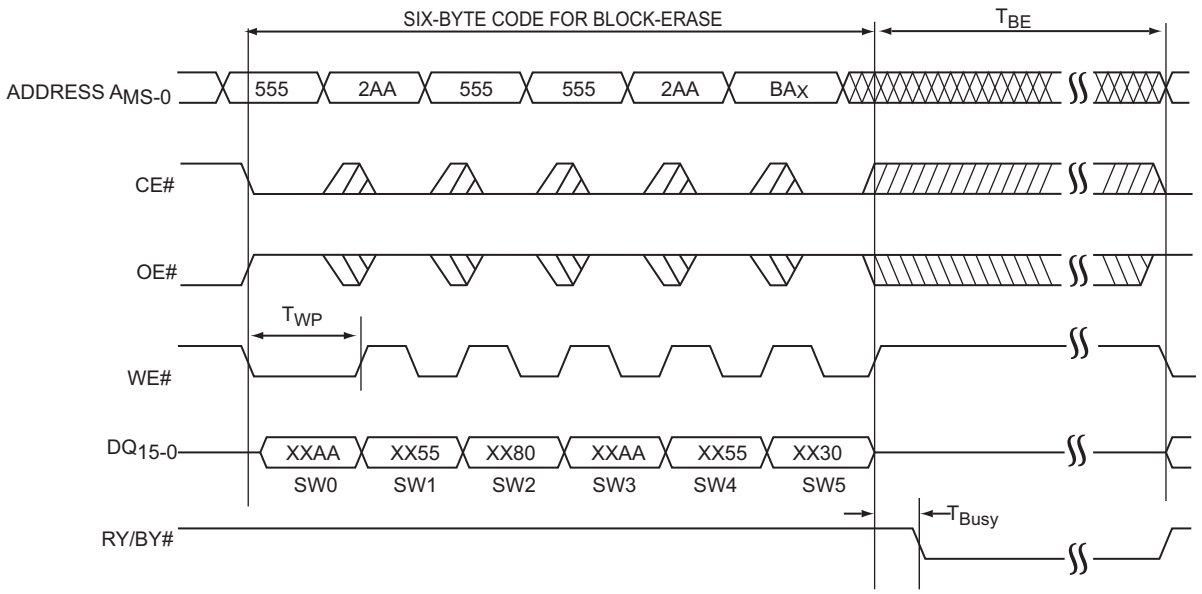
Note 1: AMS = Most significant address
AMS = A21 for SST38LF6401RT

FIGURE 7-9: WE# CONTROLLED CHIP ERASE TIMING DIAGRAM



Note 1: This device also supports CE# controlled Chip Erase operation. The WE# and CE# signals are interchangeable as long as minimum timings are met (see Table 7-5).
AMS = Most significant address
AMS = A21 for SST38LF6401RT
WP# must be held in proper logic state (VIL or VIH) 1 µs prior to and 1 µs after the command sequence.

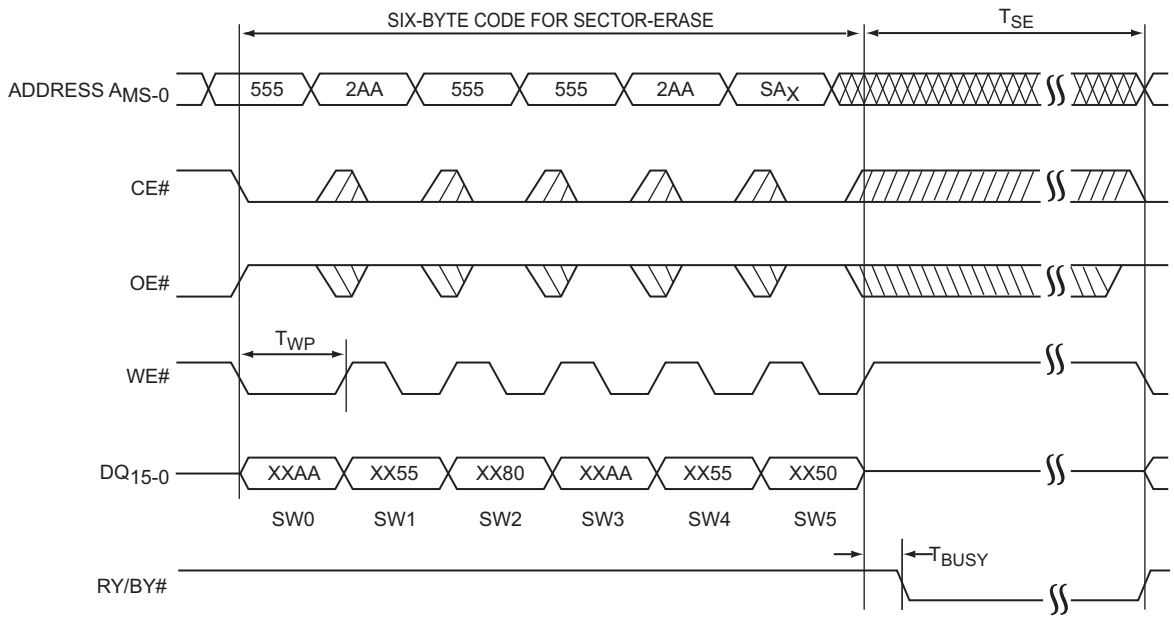
FIGURE 7-10: WE# CONTROLLED BLOCK ERASE TIMING DIAGRAM



Note 1: This device also supports CE# controlled Block Erase operation. The WE# and CE# signals are interchangeable as long as minimum timings are met (see Table 7-5).
BAX = Block address
AMS = Most significant address
AMS = A21 for SST38LF6401RT
WP# must be held in proper logic state (VIL or VIH) 1 µs prior to and 1 µs after the command sequence.

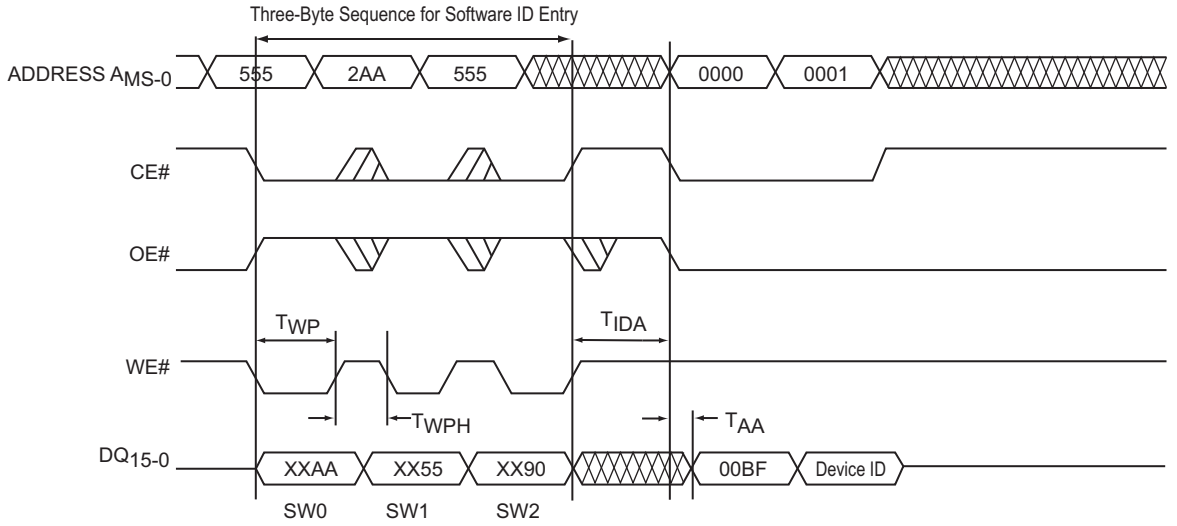
© 2020-2024 Microchip Technology Inc. and its subsidiaries

FIGURE 7-11: WE# CONTROLLED SECTOR ERASE TIMING DIAGRAM



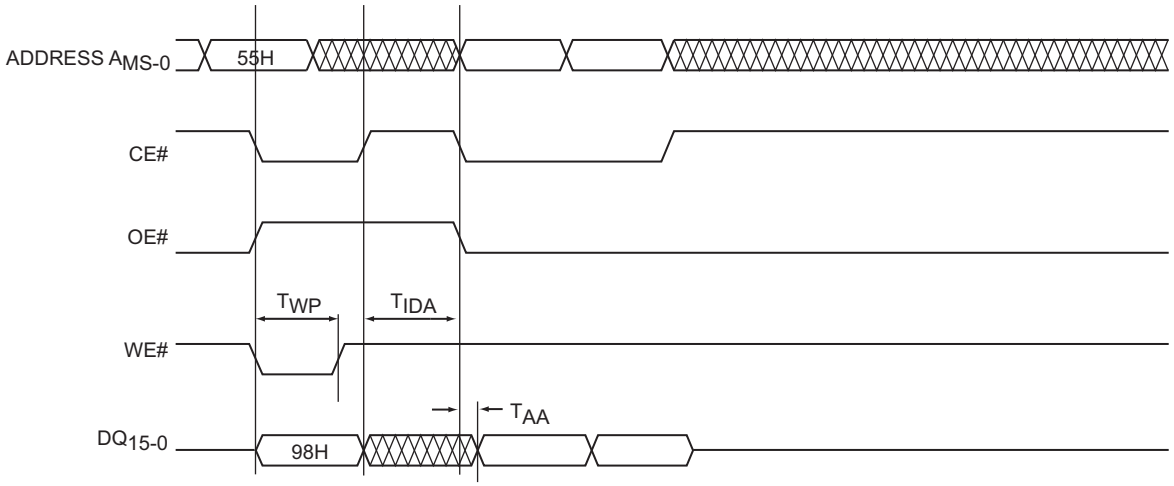
Note 1: This device also supports CE# controlled Sector Erase operation. The WE# and CE# signals are interchangeable as long as minimum timings are met (see Table 7-5).
SA_X = Sector address
A_{MS} = Most significant address
A_{MS} = A21 for SST38LF6401RT
WP# must be held in proper logic state (V_{IL} or V_{IH}) 1 µs prior to and 1 µs after the command sequence.
X can be V_{IL} or V_{IH}, but no other value.

FIGURE 7-12: SOFTWARE ID ENTRY AND READ



Note 1: Device ID = 536BH for SST38LF6401RT
AMS = Most significant address
AMS = A21 for SST38LF6401RT
WP# must be held in proper logic state (VIL or VIH) 1 µs prior to and 1 µs after the command sequence.

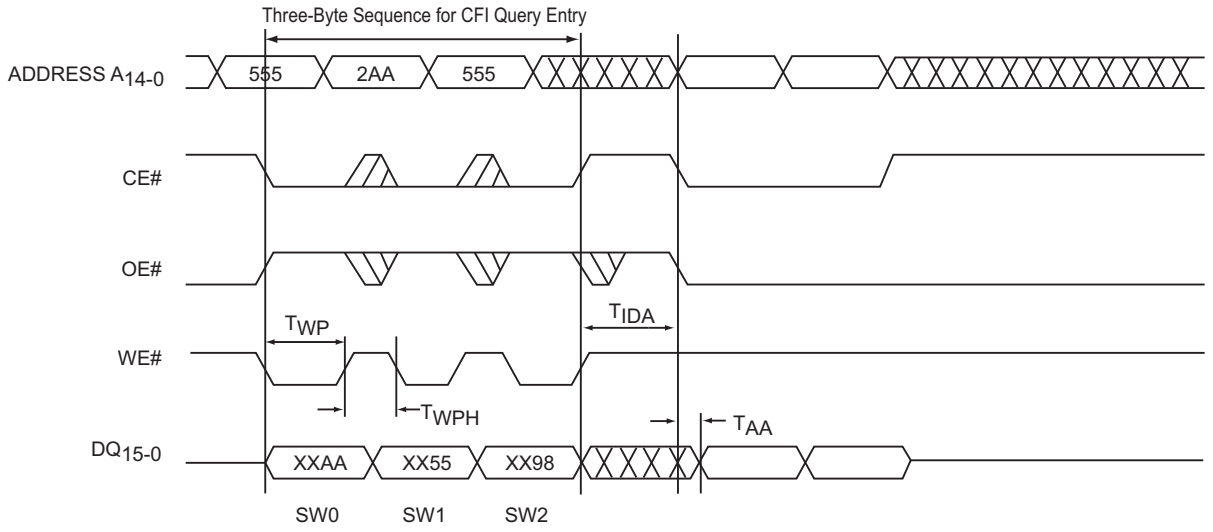
FIGURE 7-13: CFI QUERY ENTRY AND READ



Note 1: WP# must be held in proper logic state (VIL or VIH) 1 µs prior to and 1 µs after the command sequence.
AMS = Most significant address
AMS = A21 for SST38LF6401RT

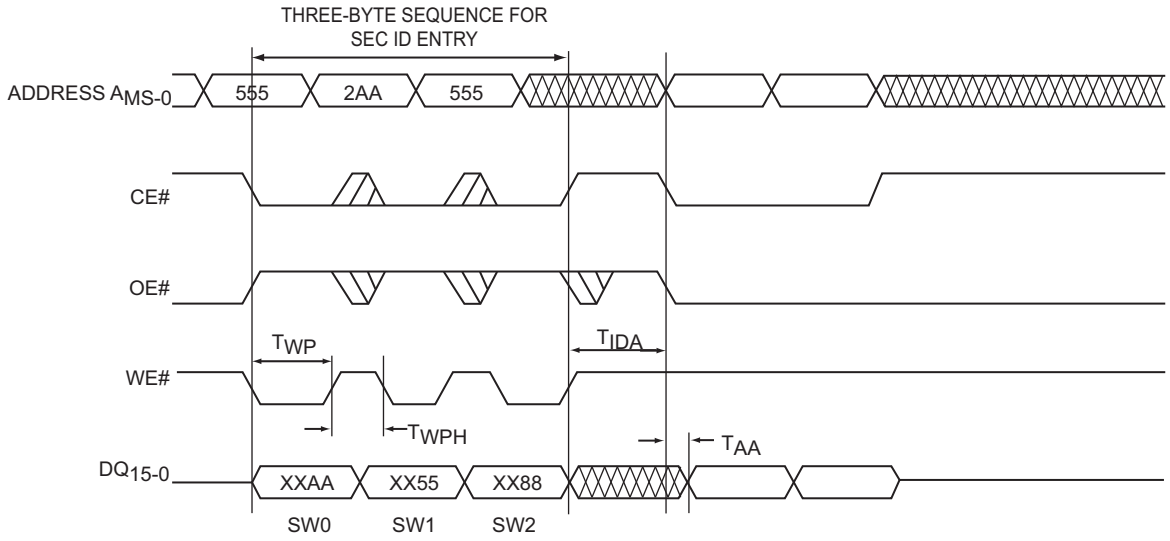
© 2020-2024 Microchip Technology Inc. and its subsidiaries

FIGURE 7-14: SOFTWARE ID EXIT/CFI EXIT



Note 1: WP# must be held in proper logic state (V_{IL} or V_{IH}) 1 µs prior to and 1 µs after the command sequence.
A_{MS} = Most significant address
A_{MS} = A21 for SST38LF6401RT

FIGURE 7-15: SEC ID ENTRY



Note 1: A_{MS} = Most significant address
A_{MS} = A21 for SST38LF6401RT
WP# must be held in proper logic state (V_{IL} or V_{IH}) 1 µs prior to and 1 µs after the command sequence.
X can be V_{IL} or V_{IH}, but no other value.

FIGURE 7-16: RST# TIMING DIAGRAM (WHEN NO INTERNAL OPERATION IS IN PROGRESS)

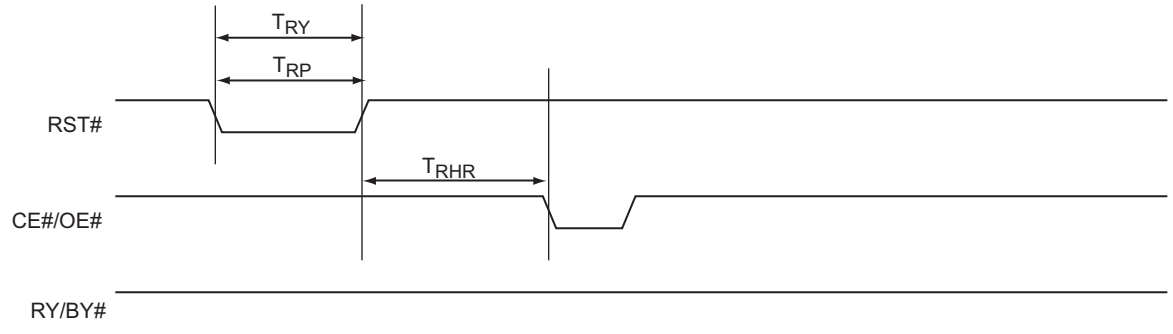


FIGURE 7-17: RST# TIMING DIAGRAM (DURING PROGRAM OR ERASE OPERATION)

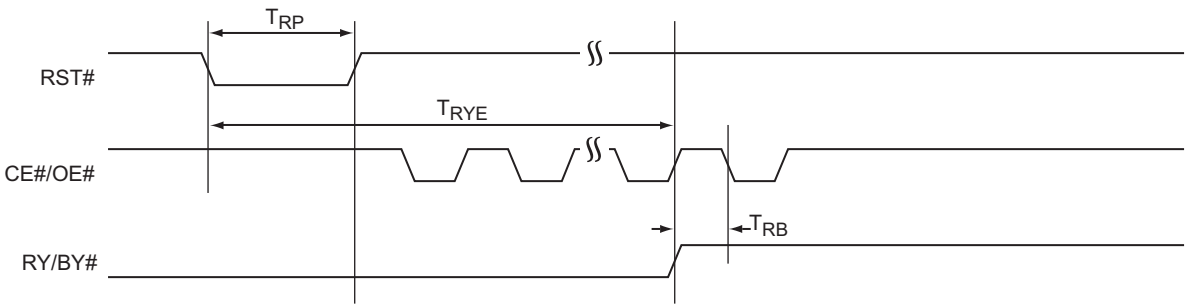
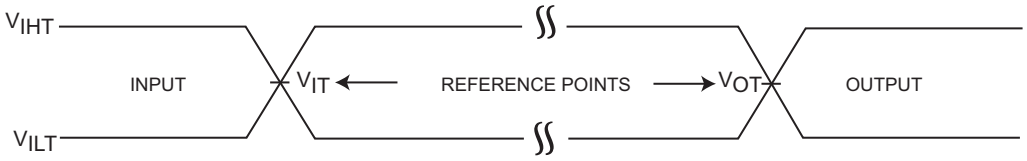


FIGURE 7-18: AC INPUT/OUTPUT REFERENCE WAVEFORMS



Note 1: AC test inputs are driven at V_{IHT} (0.9 V_{DD}) for a logic '1' and V_{ILT} (0.1 V_{DD}) for a logic '0'. Measurement reference points for inputs and outputs are V_{IT} (0.5 V_{DD}) and V_{OT} (0.5 V_{DD}). Input rise and fall times (10% ↔ 90%) are <5 ns.

2: V_{IT} = V_{INPUT} Test
V_{OT} = V_{OUTPUT} Test
V_{IHT} = V_{INPUT} HIGH Test
V_{ILT} = V_{INPUT} LOW Test

© 2020-2024 Microchip Technology Inc. and its subsidiaries

FIGURE 7-19: A TEST LOAD EXAMPLE

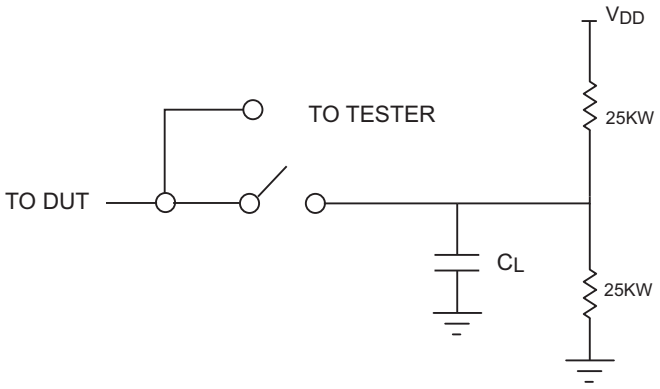
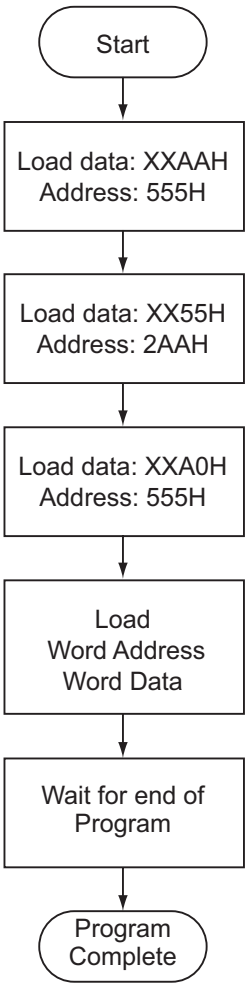
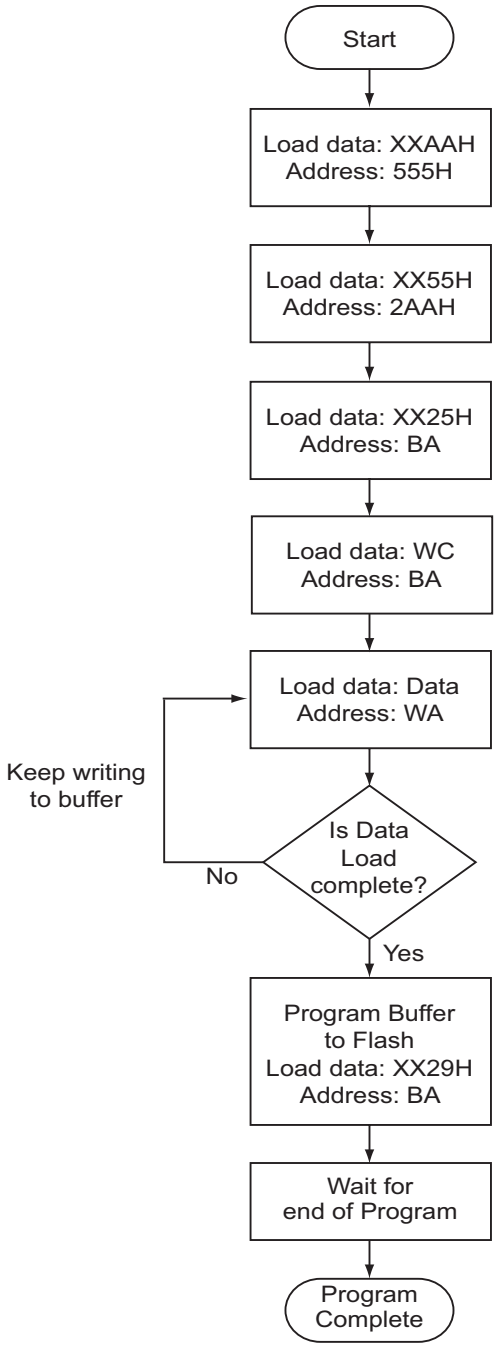


FIGURE 7-20: WORD PROGRAM ALGORITHM



Note 1: X can be VIL or VIH, but no other value.

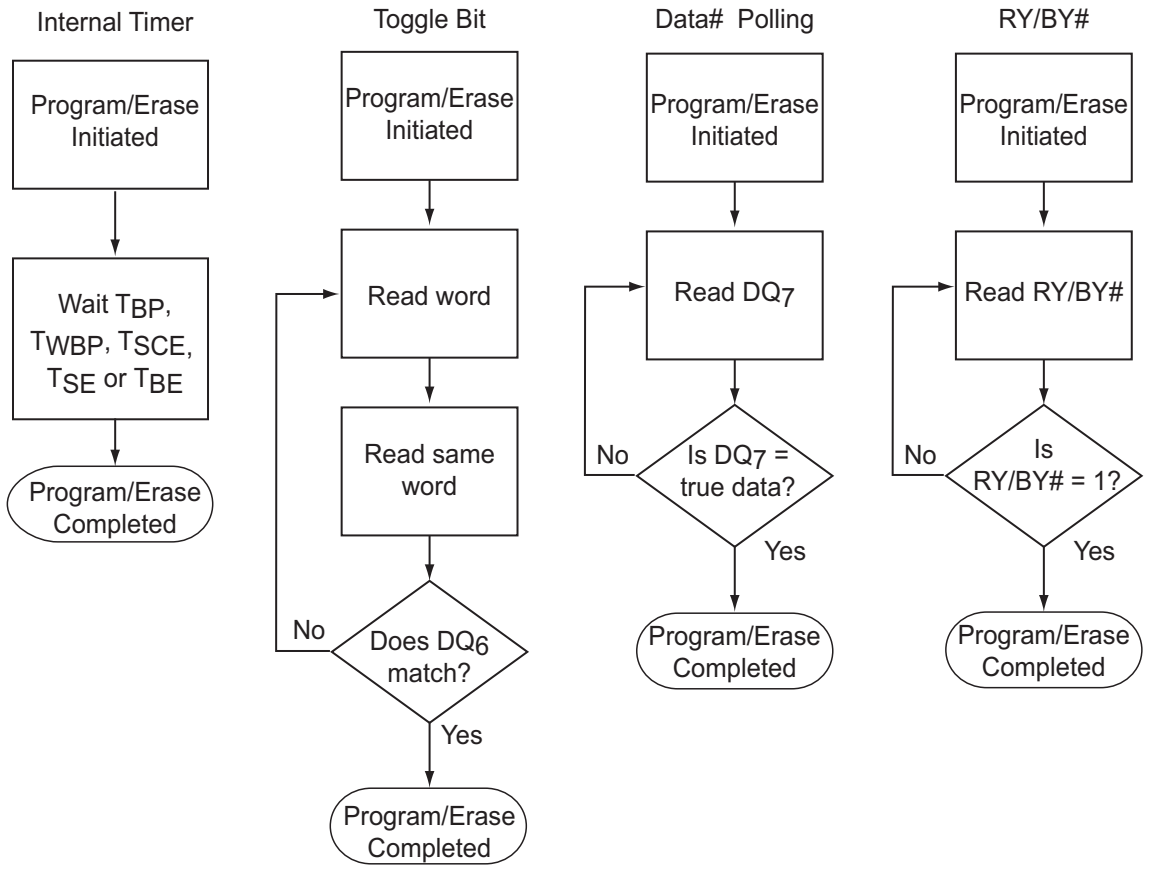
FIGURE 7-21: WRITE BUFFER PROGRAMMING



Note 1: BA = Block address
WC = Word count
WA = Address of word to program
All subsequent Address values (WAX) in Write Cycle 6 and later must have the same A21-A4 as WAX in Write Cycle 5.
X can be VIL or VIH, but no other value

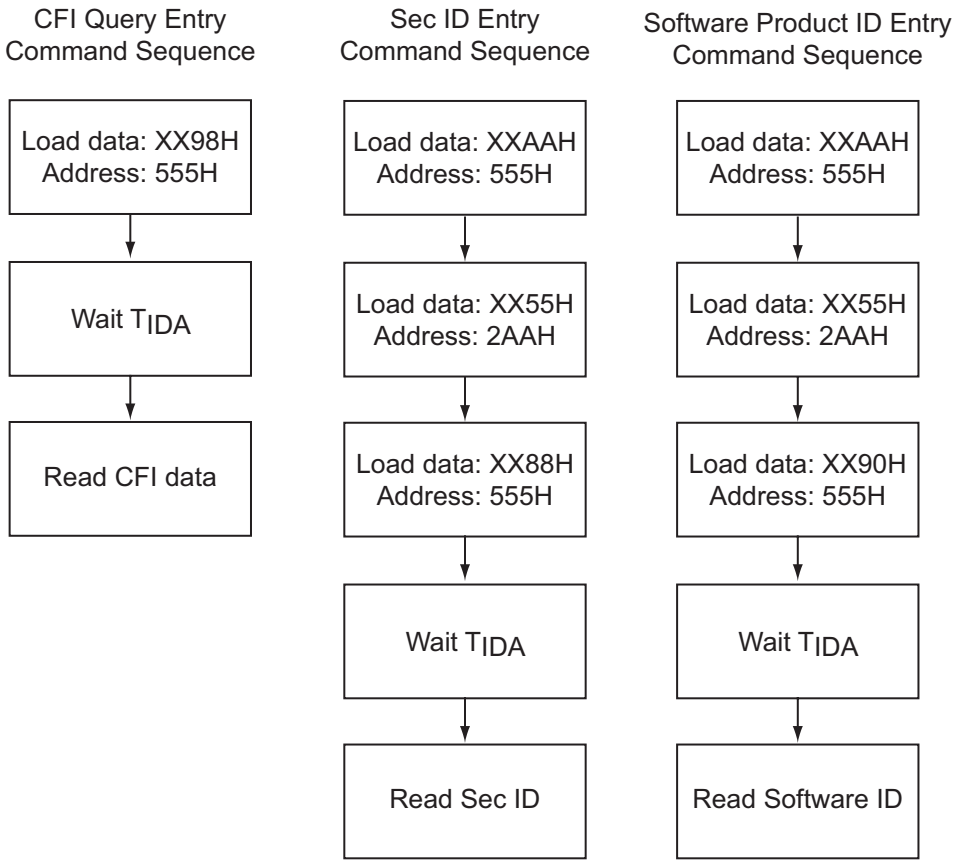
© 2020-2024 Microchip Technology Inc. and its subsidiaries

FIGURE 7-22: WAIT OPTIONS



Note 1: For a Program Buffer-to-Flash Operation, the valid DQ7 is from the last word loaded in the buffer using the Write-to-Program Buffer command.

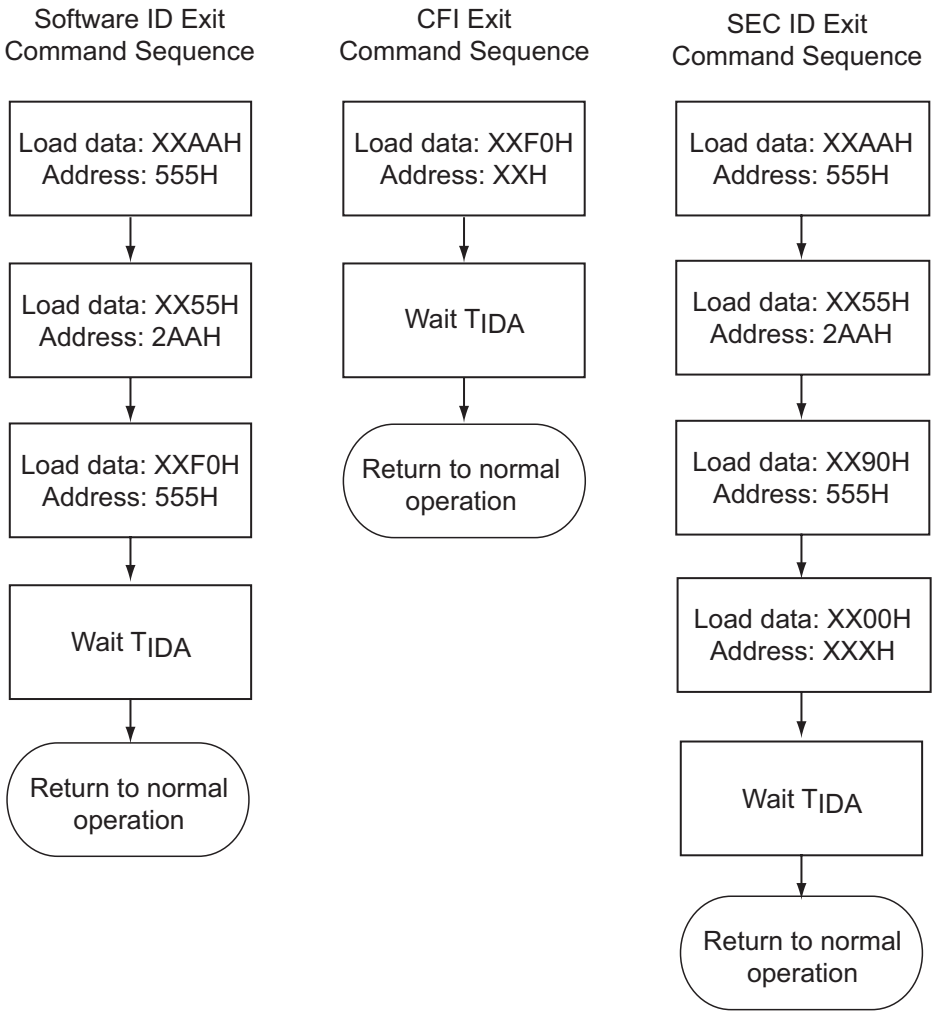
FIGURE 7-23: CFI/SEC ID/SOFTWARE ID ENTRY COMMAND FLOWCHARTS



Note 1: X can be V_{IL} or V_{IH}, but no other value.

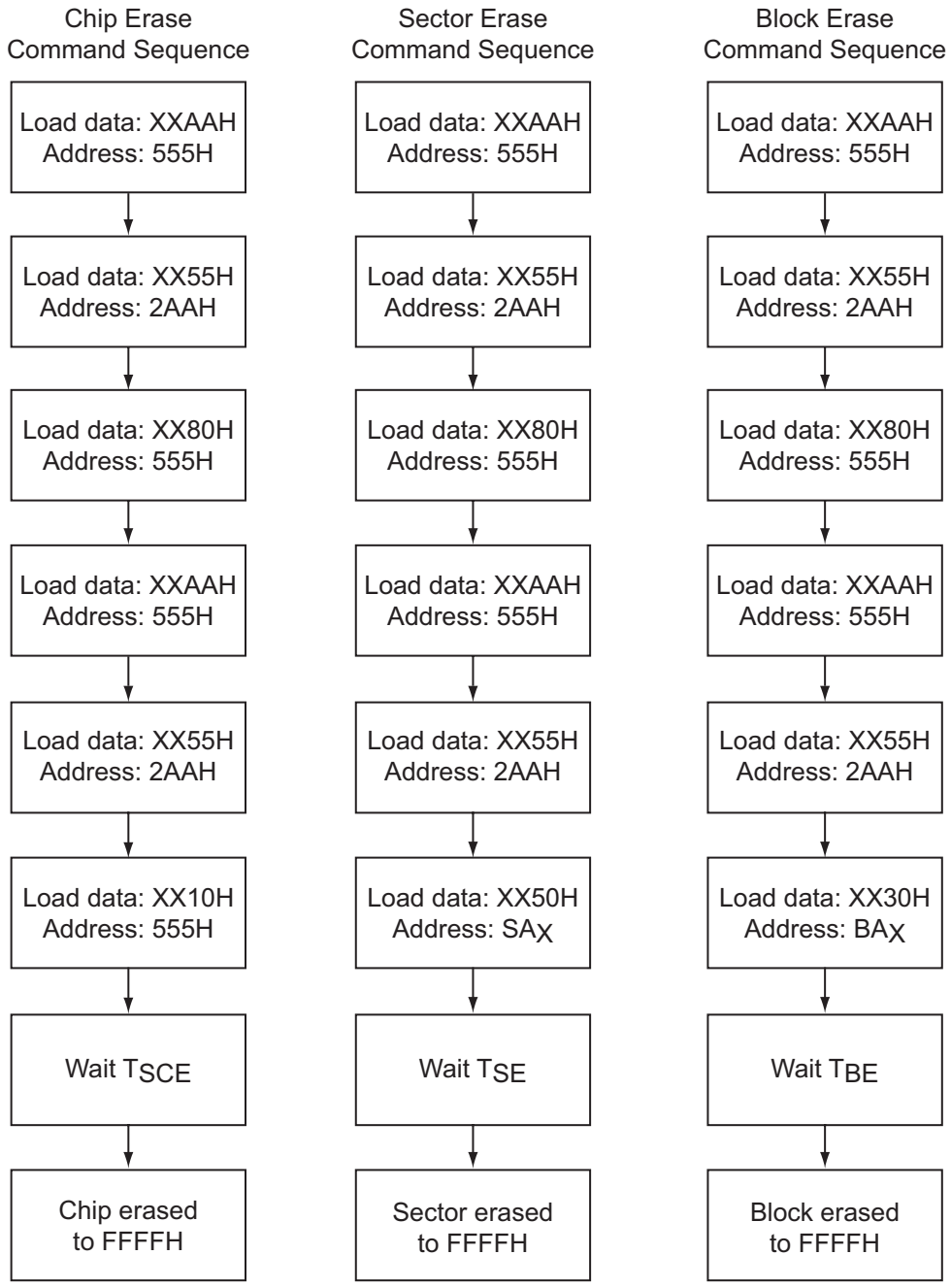
© 2020-2024 Microchip Technology Inc. and its subsidiaries

FIGURE 7-24: SOFTWARE ID/CFI/SEC ID EXIT COMMAND FLOWCHARTS



Note 1: X can be V_{IL} or V_{IH}, but no other value.

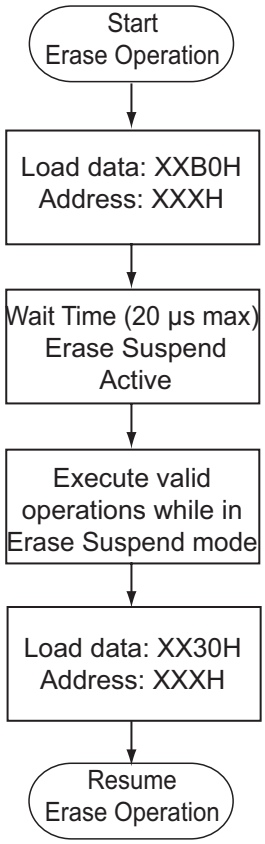
FIGURE 7-25: ERASE COMMAND SEQUENCE



Note 1: X can be V_{IL} or V_{IH}, but no other value.
BA = Block address
SA = Sector address

© 2020-2024 Microchip Technology Inc. and its subsidiaries

FIGURE 7-26: ERASE SUSPEND/RESUME

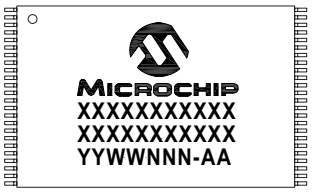


Note 1: X can be VIL or VIH, but no other value.

8.0 PACKAGING INFORMATION

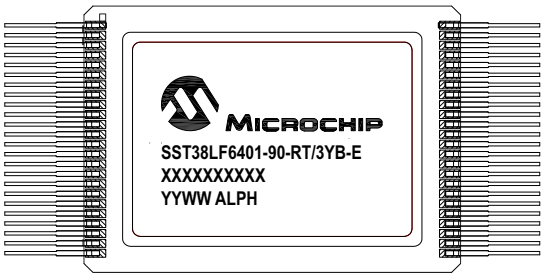
8.1 Package Marking

48-Lead TSOP (12x20 mm)

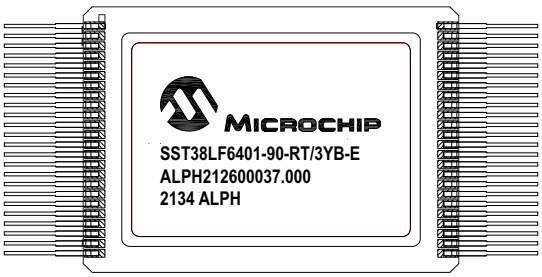


Examples

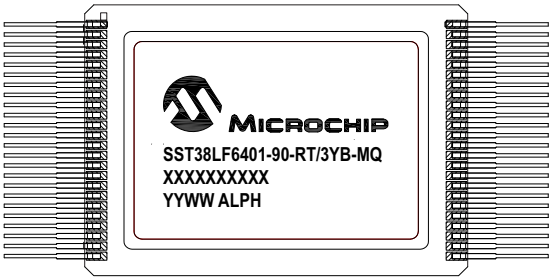
48-Lead CDFP (19x13.44 mm)



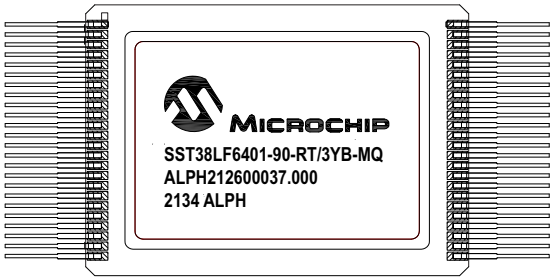
Examples



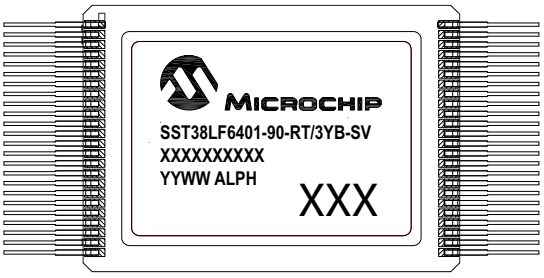
48-Lead CDFP (19x13.44 mm)



Examples



48-Lead CDFP (19x13.44 mm)



Examples

Legend:	XX...X	Part number for TSOP package
	XX...X	Lot reference number for CDFP package type
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	AA	Location code
	NNN	Alphanumeric traceability code
	ALPH	Location Code
	XXX	Serialization on last line of CDFP package

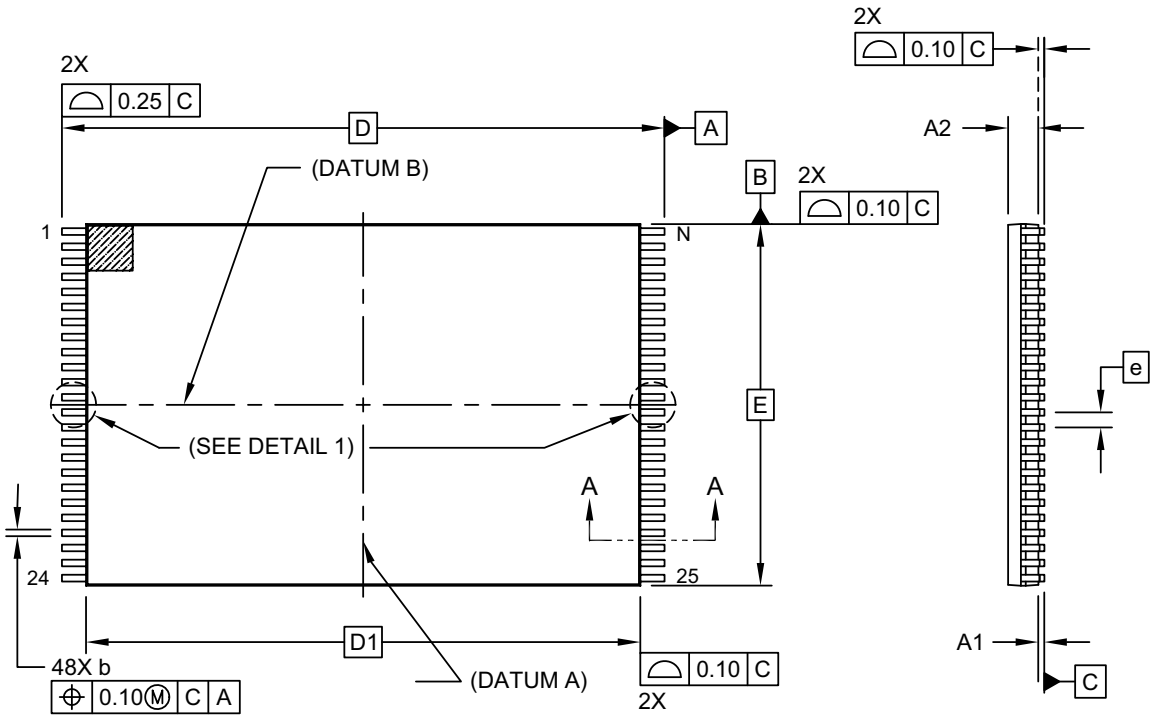
Note: The JEDEC® designator (e3) for plastic and (e4) for ceramic marking will only appear on the outer carton label.

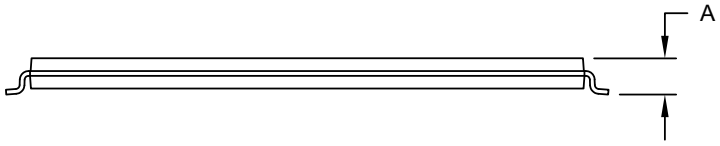
© 2020-2024 Microchip Technology Inc. and its subsidiaries

8.2 Packaging Diagrams

48-Lead Thin Small Outline Package (TV) - 12x20 mm Body [TSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

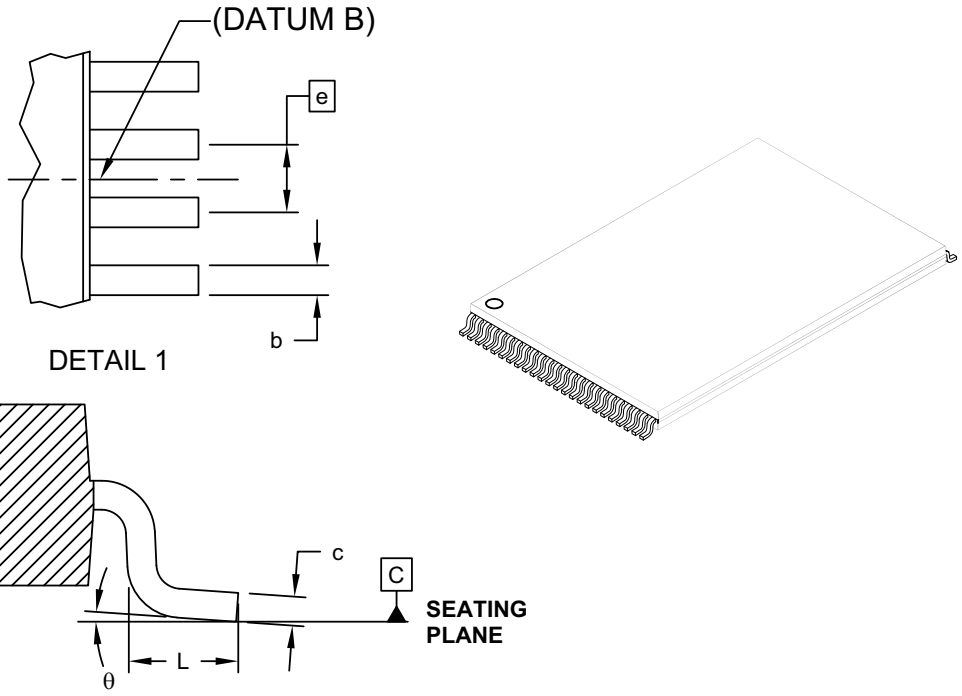




Microchip Technology Drawing C04-177-TV Rev. C Sheet 1 of 2

48-Lead Thin Small Outline Package (TV) - 12x20 mm Body [TSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		48	
Pitch	e		0.50 BSC	
Overall Height	A	-	-	1.20
Standoff	A1	0.05	-	0.15
Molded Package Height	A2	0.95	1.00	1.05
Overall Width	E		12.00 BSC	
Overall Length	D		20.00 BSC	
Molded Package Length	D1		18.40 BSC	
Lead Width	b	0.17	0.22	0.27
Lead Thickness	c	0.10	-	0.21
Lead Length	L	0.50	0.60	0.70
Lead Foot Angle	θ	0°	5°	8°

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

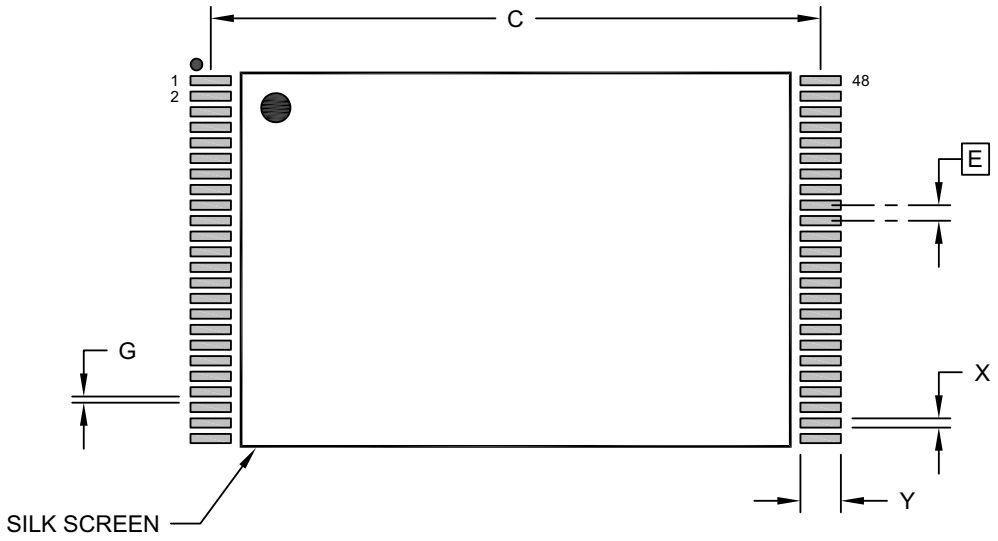
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-177-TV Rev. C Sheet 2 of 2

© 2020-2024 Microchip Technology Inc. and its subsidiaries

48-Lead Thin Small Outline Package (TV)-12x20mm Body [TSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.50 BSC	
Contact Pad Spacing	C		19.60	
Contact Pad Width (X48)	X			0.30
Contact Pad Length (X48)	Y			1.30
Contact Pad to Contact Pad (X46)	G	0.20		

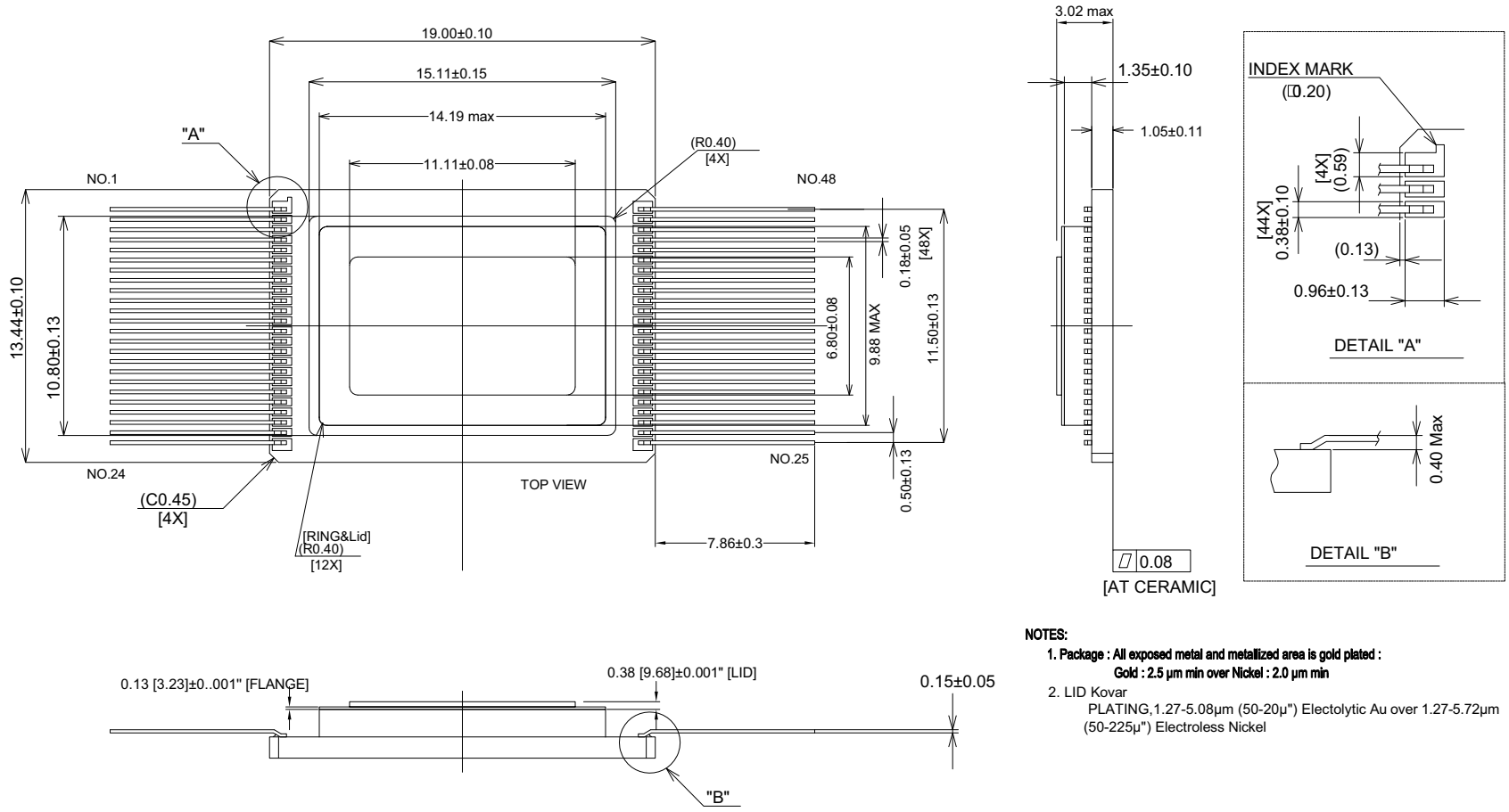
Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-2177-TV Rev C

© 2020-2024 Microchip Technology Inc. and its subsidiaries

48-Lead Ceramic Dual Flat Package (CDFP)



NOTES:

1. **Package : All exposed metal and metallized area is gold plated : Gold : 2.5 µm min over Nickel : 2.0 µm min**
2. LID Kovar
   PLATING,1.27-5.08µm (50-20µ") Electolytic Au over 1.27-5.72µm (50-225µ") Electroless Nickel

Unit : mm	Tolerance : unless otherwise specified : +/- 0.13

© 2020-2024 Microchip Technology Inc.

APPENDIX A: REVISION HISTORY

Revision D (April 2024)

Corrected Bypass mode software command sequence; minor editorial updates throughout the document.

Revision C (December 2023)

Added the Mass section; Replaced the 48-Lead Ceramic Multi Layer Flat Pack (3YB) - 19x13.44x2.78 mm Body [MFPF] image with a new one in the Packaging Diagrams section.

Revision B (October 2021)

Removed “Preliminary” status; Added temperature range to “Features” section. Other minor edits.

Revision A (November 2020)

Initial release of the document.

© 2020-2024 Microchip Technology Inc. and its subsidiaries

THE MICROCHIP WEBSITE

Microchip provides online support via our website at https://www.microchip.com. This website is used to make files and information easily available to customers. Some of the available content includes:

- **Product Support** – Data sheets and errata, application notes and sample programs, design resources, user's guides and hardware support documents, the latest software releases and archived software
- **General Technical Support** – Frequently Asked Questions (FAQs), technical support requests, online discussion groups and a Microchip design partner program member listing
- **Business of Microchip** – Product selector and ordering guides, the latest Microchip press releases, a listing of seminars and events, listings of Microchip sales offices, distributors and factory representatives

PRODUCT CHANGE NOTIFICATION SERVICE

Microchip's product change notification service helps keep customers current on Microchip products. Subscribers will receive email notifications whenever there are changes, updates, revisions or errata related to a specified product family or development tool of interest.

To register, go to https://www.microchip.com/pcn and follow the registration instructions.

CUSTOMER SUPPORT

Users of Microchip products can receive assistance through several channels:

- Distributor or Representative
- Local Sales Office
- Embedded Solutions Engineer (ESE)
- Technical Support

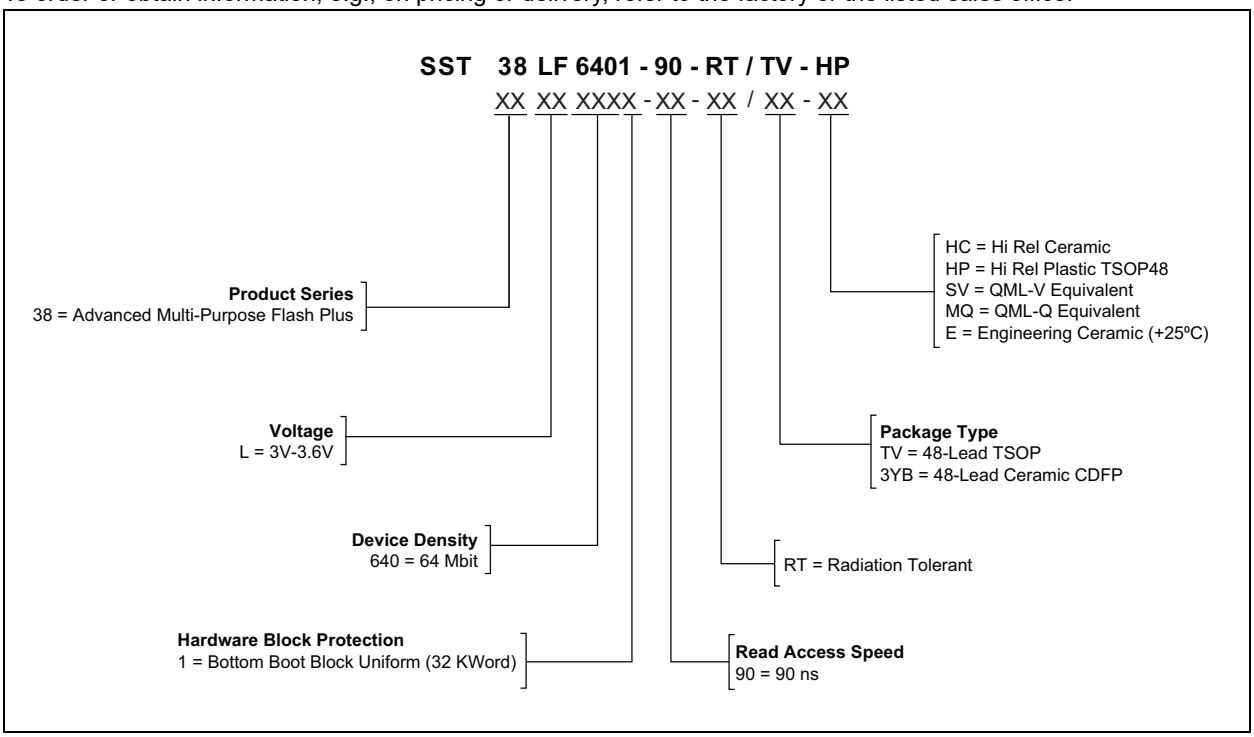
Customers should contact their distributor, representative or ESE for support. Local sales offices are also available to help customers. A listing of sales offices and locations is included in this document.

Technical support is available through the website at: https://www.microchip.com/support

© 2020-2024 Microchip Technology Inc. and its subsidiaries

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.



Valid Combinations
SST38LF6401-90-RT/TV-HP
SST38LF6401-90-RT/3YB-E
SST38LF6401-90-RT/3YB-MQ
SST38LF6401-90-RT/3YB-SV
SST38LF6401-90-RT/3YB-HC (On demand special order - please contact Microchip)

Note the following details of the code protection feature on Microchip products:

- Microchip products meet the specifications contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is secure when used in the intended manner, within operating specifications, and under normal conditions.
- Microchip values and aggressively protects its intellectual property rights. Attempts to breach the code protection features of Microchip product is strictly prohibited and may violate the Digital Millennium Copyright Act.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of its code. Code protection does not mean that we are guaranteeing the product is "unbreakable" Code protection is constantly evolving. Microchip is committed to continuously improving the code protection features of our products.

This publication and the information herein may be used only with Microchip products, including to design, test, and integrate Microchip products with your application. Use of this information in any other manner violates these terms. Information regarding device applications is provided only for your convenience and may be superseded by updates. It is your responsibility to ensure that your application meets with your specifications. Contact your local Microchip sales office for additional support or, obtain additional support at https://www.microchip.com/en-us/support/design-help/client-support-services.

THIS INFORMATION IS PROVIDED BY MICROCHIP "AS IS". MICROCHIP MAKES NO REPRESENTATIONS OR WARRANTIES OF ANY KIND WHETHER EXPRESS OR IMPLIED, WRITTEN OR ORAL, STATUTORY OR OTHERWISE, RELATED TO THE INFORMATION INCLUDING BUT NOT LIMITED TO ANY IMPLIED WARRANTIES OF NON-INFRINGEMENT, MERCHANTABILITY, AND FITNESS FOR A PARTICULAR PURPOSE, OR WARRANTIES RELATED TO ITS CONDITION, QUALITY, OR PERFORMANCE.

IN NO EVENT WILL MICROCHIP BE LIABLE FOR ANY INDIRECT, SPECIAL, PUNITIVE, INCIDENTAL, OR CONSEQUENTIAL LOSS, DAMAGE, COST, OR EXPENSE OF ANY KIND WHATSOEVER RELATED TO THE INFORMATION OR ITS USE, HOWEVER CAUSED, EVEN IF MICROCHIP HAS BEEN ADVISED OF THE POSSIBILITY OR THE DAMAGES ARE FORESEEABLE. TO THE FULLEST EXTENT ALLOWED BY LAW, MICROCHIP'S TOTAL LIABILITY ON ALL CLAIMS IN ANY WAY RELATED TO THE INFORMATION OR ITS USE WILL NOT EXCEED THE AMOUNT OF FEES, IF ANY, THAT YOU HAVE PAID DIRECTLY TO MICROCHIP FOR THE INFORMATION.

Use of Microchip devices in life support and/or safety applications is entirely at the buyer's risk, and the buyer agrees to defend, indemnify and hold harmless Microchip from any and all damages, claims, suits, or expenses resulting from such use. No licenses are conveyed, implicitly or otherwise, under any Microchip intellectual property rights unless otherwise stated.

Trademarks

The Microchip name and logo, the Microchip logo, Adaptec, AVR, AVR logo, AVR Freaks, BesTime, BitCloud, CryptoMemory, CryptoRF, dsPIC, flexPWR, HELDO, IGLOO, JukeBlox, KeeLoq, Kleer, LANCheck, LinkMD, maXStylus, maXTouch, MediaLB, megaAVR, Microsemi, Microsemi logo, MOST, MOST logo, MPLAB, OptoLyzer, PIC, picoPower, PICSTART, PIC32 logo, PolarFire, Prochip Designer, QTouch, SAM-BA, SenGenuity, SpyNIC, SST, SST Logo, SuperFlash, Symmetricom, SyncServer, Tachyon, TimeSource, tinyAVR, UNI/O, Vectron, and XMEGA are registered trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

AgileSwitch, ClockWorks, The Embedded Control Solutions Company, EtherSynch, Flashtec, Hyper Speed Control, HyperLight Load, Libero, motorBench, mTouch, Powermite 3, Precision Edge, ProASIC, ProASIC Plus, ProASIC Plus logo, Quiet-Wire, SmartFusion, SyncWorld, TimeCesium, TimeHub, TimePictra, TimeProvider, and ZL are registered trademarks of Microchip Technology Incorporated in the U.S.A.

Adjacent Key Suppression, AKS, Analog-for-the-Digital Age, Any Capacitor, AnyIn, AnyOut, Augmented Switching, BlueSky, BodyCom, Clockstudio, CodeGuard, CryptoAuthentication, CryptoAutomotive, CryptoCompanion, CryptoController, dsPICDEM, dsPICDEM.net, Dynamic Average Matching, DAM, ECAN, Espresso T1S, EtherGREEN, EyeOpen, GridTime, IdealBridge, IGaT, In-Circuit Serial Programming, ICSP, INICnet, Intelligent Paralleling, IntelliMOS, Inter-Chip Connectivity, JitterBlocker, Knob-on-Display, MarginLink, maxCrypto, maxView, memBrain, Mindi, MiWi, MPASM, MPF, MPLAB Certified logo, MPLIB, MPLINK, mSiC, MultiTRAK, NetDetach, Omniscient Code Generation, PICDEM, PICDEM.net, PICkit, PICtail, Power MOS IV, Power MOS 7, PowerSmart, PureSilicon, QMatrix, REAL ICE, Ripple Blocker, RTAX, RTG4, SAM-ICE, Serial Quad I/O, simpleMAP, SimpliPHY, SmartBuffer, SmartHLS, SMART-I.S., storClad, SQI, SuperSwitcher, SuperSwitcher II, Switchtec, SynchroPHY, Total Endurance, Trusted Time, TSHARC, Turing, USBCheck, VariSense, VectorBlox, VeriPHY, ViewSpan, WiperLock, XpressConnect, and ZENA are trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

SQTP is a service mark of Microchip Technology Incorporated in the U.S.A.

The Adaptec logo, Frequency on Demand, Silicon Storage Technology, and Symmcom are registered trademarks of Microchip Technology Inc. in other countries.

GestIC is a registered trademark of Microchip Technology Germany II GmbH & Co. KG, a subsidiary of Microchip Technology Inc., in other countries.

All other trademarks mentioned herein are property of their respective companies.
© 2020-2024, Microchip Technology Incorporated and its subsidiaries.

All Rights Reserved.

ISBN: 978-1-6683-4236-7

For information regarding Microchip's Quality Management Systems, please visit www.microchip.com/quality.

© 2020-2024 Microchip Technology Inc. and its subsidiaries

Worldwide Sales and Service

AMERICAS

Corporate Office
2355 West Chandler Blvd.
Chandler, AZ 85224-6199
Tel: 480-792-7200
Fax: 480-792-7277
Technical Support:
http://www.microchip.com/support
Web Address:
www.microchip.com

Atlanta
Duluth, GA
Tel: 678-957-9614
Fax: 678-957-1455

Austin, TX
Tel: 512-257-3370

Boston
Westborough, MA
Tel: 774-760-0087
Fax: 774-760-0088

Chicago
Itasca, IL
Tel: 630-285-0071
Fax: 630-285-0075

Dallas
Addison, TX
Tel: 972-818-7423
Fax: 972-818-2924

Detroit
Novi, MI
Tel: 248-848-4000

Houston, TX
Tel: 281-894-5983

Indianapolis
Noblesville, IN
Tel: 317-773-8323
Fax: 317-773-5453
Tel: 317-536-2380

Los Angeles
Mission Viejo, CA
Tel: 949-462-9523
Fax: 949-462-9608
Tel: 951-273-7800

Raleigh, NC
Tel: 919-844-7510

New York, NY
Tel: 631-435-6000

San Jose, CA
Tel: 408-735-9110
Tel: 408-436-4270

Canada - Toronto
Tel: 905-695-1980
Fax: 905-695-2078

ASIA/PACIFIC

Australia - Sydney
Tel: 61-2-9868-6733

China - Beijing
Tel: 86-10-8569-7000

China - Chengdu
Tel: 86-28-8665-5511

China - Chongqing
Tel: 86-23-8980-9588

China - Dongguan
Tel: 86-769-8702-9880

China - Guangzhou
Tel: 86-20-8755-8029

China - Hangzhou
Tel: 86-571-8792-8115

China - Hong Kong SAR
Tel: 852-2943-5100

China - Nanjing
Tel: 86-25-8473-2460

China - Qingdao
Tel: 86-532-8502-7355

China - Shanghai
Tel: 86-21-3326-8000

China - Shenyang
Tel: 86-24-2334-2829

China - Shenzhen
Tel: 86-755-8864-2200

China - Suzhou
Tel: 86-186-6233-1526

China - Wuhan
Tel: 86-27-5980-5300

China - Xian
Tel: 86-29-8833-7252

China - Xiamen
Tel: 86-592-2388138

China - Zhuhai
Tel: 86-756-3210040

ASIA/PACIFIC

India - Bangalore
Tel: 91-80-3090-4444

India - New Delhi
Tel: 91-11-4160-8631

India - Pune
Tel: 91-20-4121-0141

Japan - Osaka
Tel: 81-6-6152-7160

Japan - Tokyo
Tel: 81-3-6880- 3770

Korea - Daegu
Tel: 82-53-744-4301

Korea - Seoul
Tel: 82-2-554-7200

Malaysia - Kuala Lumpur
Tel: 60-3-7651-7906

Malaysia - Penang
Tel: 60-4-227-8870

Philippines - Manila
Tel: 63-2-634-9065

Singapore
Tel: 65-6334-8870

Taiwan - Hsin Chu
Tel: 886-3-577-8366

Taiwan - Kaohsiung
Tel: 886-7-213-7830

Taiwan - Taipei
Tel: 886-2-2508-8600

Thailand - Bangkok
Tel: 66-2-694-1351

Vietnam - Ho Chi Minh
Tel: 84-28-5448-2100

EUROPE

Austria - Wels
Tel: 43-7242-2244-39
Fax: 43-7242-2244-393

Denmark - Copenhagen
Tel: 45-4485-5910
Fax: 45-4485-2829

Finland - Espoo
Tel: 358-9-4520-820

France - Paris
Tel: 33-1-69-53-63-20
Fax: 33-1-69-30-90-79

Germany - Garching
Tel: 49-8931-9700

Germany - Haan
Tel: 49-2129-3766400

Germany - Heilbronn
Tel: 49-7131-72400

Germany - Karlsruhe
Tel: 49-721-625370

Germany - Munich
Tel: 49-89-627-144-0
Fax: 49-89-627-144-44

Germany - Rosenheim
Tel: 49-8031-354-560

Israel - Ra'anana
Tel: 972-9-744-7705

Italy - Milan
Tel: 39-0331-742611
Fax: 39-0331-466781

Italy - Padova
Tel: 39-049-7625286

Netherlands - Drunen
Tel: 31-416-690399
Fax: 31-416-690340

Norway - Trondheim
Tel: 47-7288-4388

Poland - Warsaw
Tel: 48-22-3325737

Romania - Bucharest
Tel: 40-21-407-87-50

Spain - Madrid
Tel: 34-91-708-08-90
Fax: 34-91-708-08-91

Sweden - Gothenberg
Tel: 46-31-704-60-40

Sweden - Stockholm
Tel: 46-8-5090-4654

UK - Wokingham
Tel: 44-118-921-5800
Fax: 44-118-921-5820

© 2020-2024 Microchip Technology Inc. and its subsidiaries