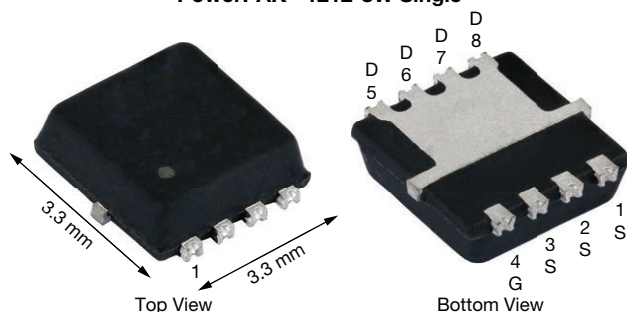


Automotive N-Channel 100 V (D-S) 175 °C MOSFET

PowerPAK® 1212-8W Single


Marking code: Q043

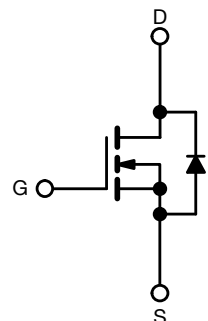
PRODUCT SUMMARY

V_{DS} (V)	100
$R_{DS(on)}$ (Ω) at $V_{GS} = 10$ V	0.022
$R_{DS(on)}$ (Ω) at $V_{GS} = 4.5$ V	0.025
I_D (A)	18
Configuration	Single
Package	PowerPAK 1212-8W

FEATURES

- TrenchFET® power MOSFET
- AEC-Q101 qualified
- 100 % R_g and UIS tested
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

AUTOMOTIVE
GRADE

RoHS
COMPLIANT
HALOGEN
FREE


N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS ($T_C = 25$ °C, unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-source voltage	V_{DS}	100	V
Gate-source voltage	V_{GS}	± 20	
Continuous drain current ^a	I_D	$T_C = 25$ °C	18
		$T_C = 125$ °C	18
Continuous source current (diode conduction) ^a	I_S	18	A
Pulsed drain current ^b	I_{DM}	72	
Single pulse avalanche current	I_{AS}	20.5	
Single pulse avalanche energy	E_{AS}	21	mJ
Maximum power dissipation ^b	P_D	$T_C = 25$ °C	62.5
		$T_C = 125$ °C	20
Operating junction and storage temperature range	T_J, T_{stg}	-55 to +175	°C
Soldering recommendations (peak temperature) ^{d, e}		260	

THERMAL RESISTANCE RATINGS

PARAMETER	SYMBOL	LIMIT	UNIT
Junction-to-ambient	R_{thJA}	81	°C/W
Junction-to-case (drain)	R_{thJC}	2.4	

Notes

- Package limited
- Pulse test; pulse width ≤ 300 μ s, duty cycle ≤ 2 %
- When mounted on 1" square PCB (FR4 material)
- See solder profile (www.vishay.com/doc?73257). The PowerPAK 1212-8W is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection
- Rework conditions: manual soldering with a soldering iron is not recommended for leadless components

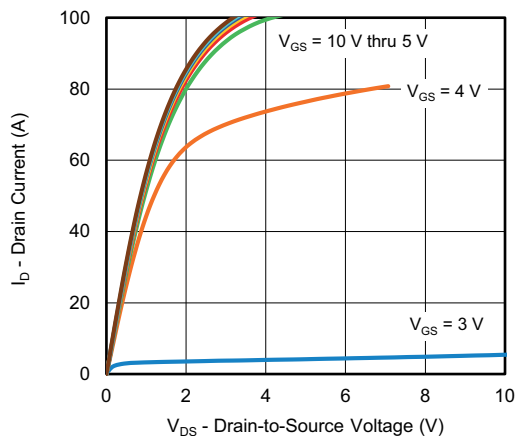
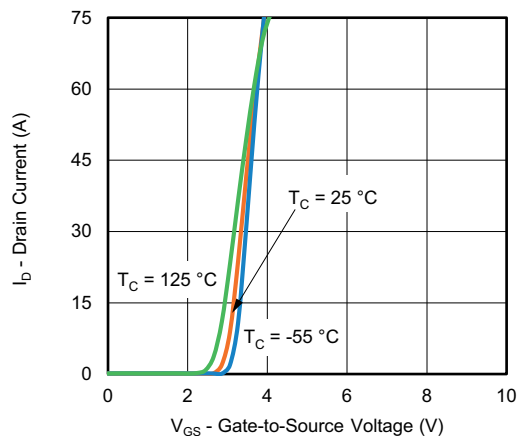
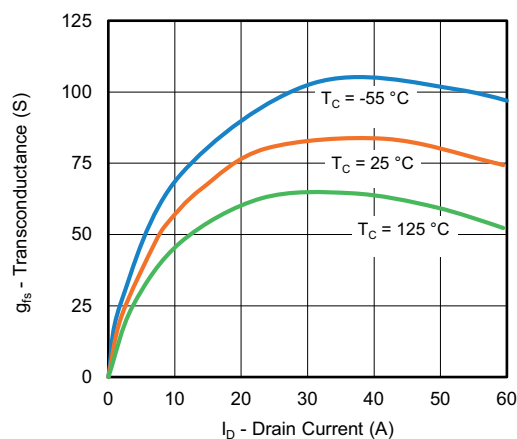
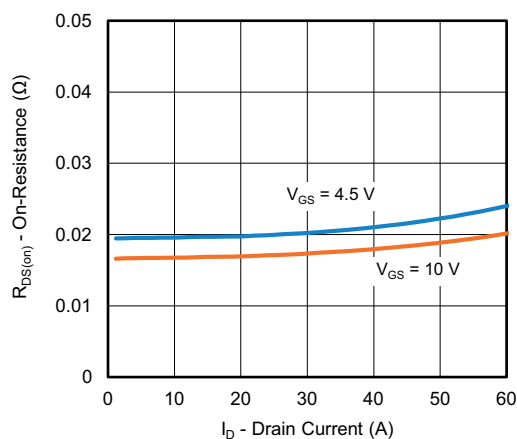
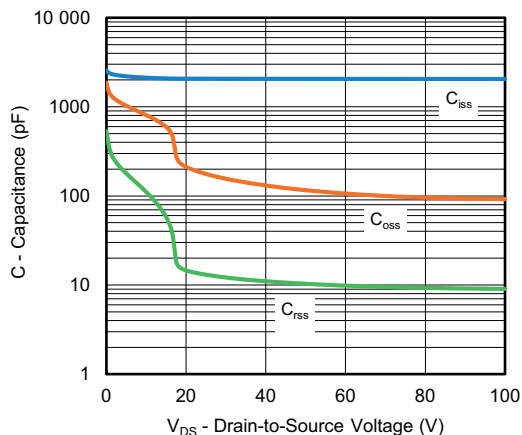
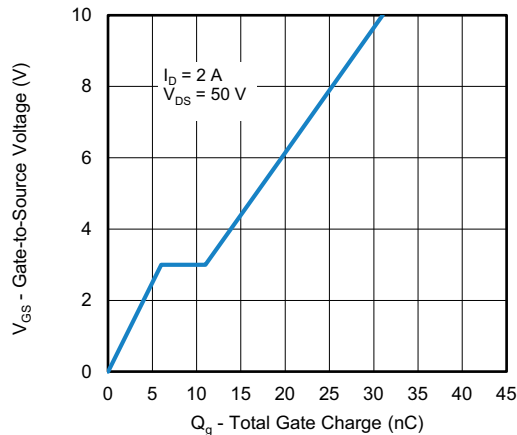


SPECIFICATIONS (T _C = 25 °C, unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-source breakdown voltage	V _{DS}	V _{GS} = 0, I _D = 250 μA		100	-	-	V
Gate-source threshold voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA		1.5	2.0	2.5	
Gate-source leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ± 20 V		-	-	± 100	
Zero gate voltage drain current	I _{DSS}	V _{GS} = 0 V	V _{DS} = 100 V	-	-	1	μA
		V _{GS} = 0 V	V _{DS} = 100 V, T _J = 125 °C	-	-	50	
		V _{GS} = 0 V	V _{DS} = 100 V, T _J = 175 °C	-	-	150	
On-state drain current ^a	I _{D(on)}	V _{GS} = 10 V	V _{DS} ≥ 5 V	15	-	-	A
Drain-source on-state resistance ^a	R _{DS(on)}	V _{GS} = 10 V	I _D = 7 A	-	0.017	0.022	Ω
		V _{GS} = 10 V	I _D = 7 A, T _J = 125 °C	-	-	0.041	
		V _{GS} = 10 V	I _D = 7 A, T _J = 175 °C	-	-	0.050	
		V _{GS} = 4.5 V	I _D = 5 A	-	0.020	0.025	
Forward transconductance ^b	g _{fs}	V _{DS} = 15 V, I _D = 7 A		-	47	-	S
Dynamic ^b							
Input capacitance	C _{iss}	V _{GS} = 0 V	V _{DS} = 25 V, f = 1 MHz	-	2068	2900	pF
Output capacitance	C _{OSS}			-	177	250	
Reverse transfer capacitance	C _{rss}			-	13	20	
Total gate charge ^c	Q _g	V _{GS} = 10 V	V _{DS} = 50 V, I _D = 2 A	-	31	47	nC
Gate-source charge ^c	Q _{gs}			-	6	-	
Gate-drain charge ^c	Q _{gd}			-	5	-	
Gate resistance	R _g	f = 1 MHz		0.2	0.5	0.8	Ω
Turn-on delay time ^c	t _{d(on)}	V _{DD} = 50 V, R _L = 25 Ω I _D ≡ 2 A, V _{GEN} = 10 V, R _g = 1 Ω		-	11	20	ns
Rise time ^c	t _r			-	4	10	
Turn-off delay time ^c	t _{d(off)}			-	25	40	
Fall time ^c	t _f			-	9	15	
Source-Drain Diode Ratings and Characteristic ^b							
Pulsed current ^a	I _{SM}			-	-	72	A
Forward voltage	V _{SD}	I _F = 7 A, V _{GS} = 0 V		-	0.8	1.1	V
Body diode reverse recovery time	t _{rr}	I _F = 2 A, di/dt = 100 A/μs		-	32	64	ns
Body diode reverse recovery charge	Q _{rr}			-	46	92	nC
Reverse recovery fall time	t _a			-	26	-	ns
Reverse recovery rise time	t _b			-	6	-	
Body diode peak reverse recovery current	I _{RM(REC)}			-	-3.4	-	A

Notes

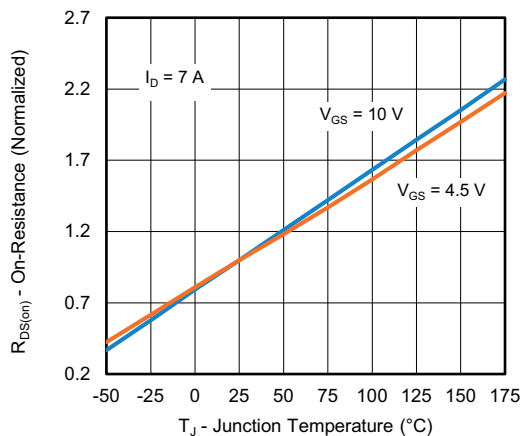
- a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$
b. Guaranteed by design, not subject to production testing
c. Independent of operating temperature

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

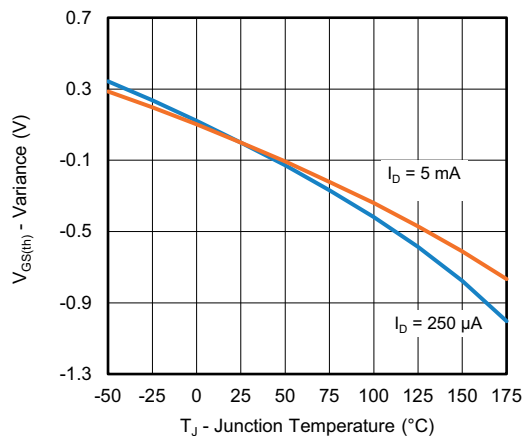
TYPICAL CHARACTERISTICS ($T_A = 25\text{ }^{\circ}\text{C}$, unless otherwise noted)

Output Characteristics

Transfer Characteristics

Transconductance

On-Resistance vs. Drain Current

Capacitance

Gate Charge



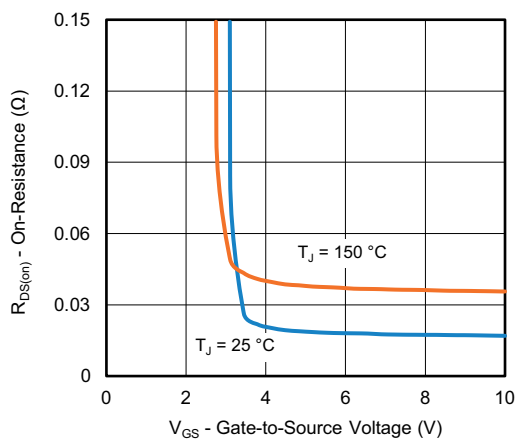
TYPICAL CHARACTERISTICS ($T_A = 25\text{ }^{\circ}\text{C}$, unless otherwise noted)



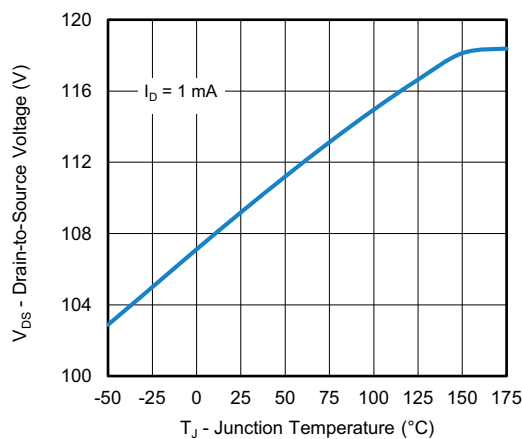
On-Resistance vs. Junction Temperature



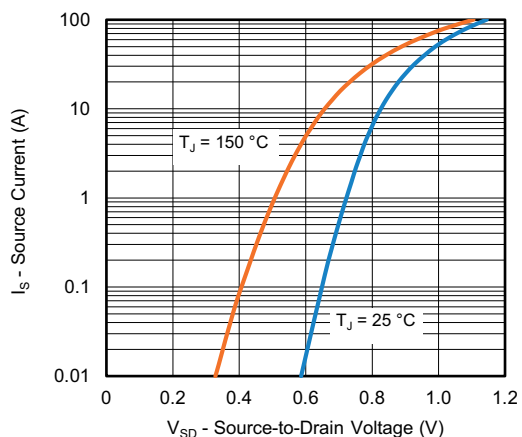
Threshold Voltage



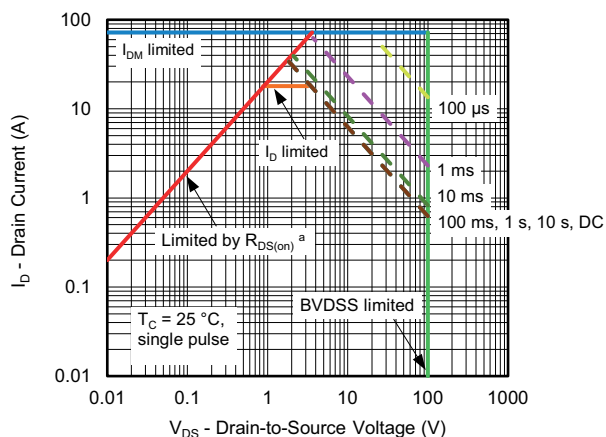
On-Resistance vs. Gate-to-Source Voltage



Drain Source Breakdown vs. Junction Temperature



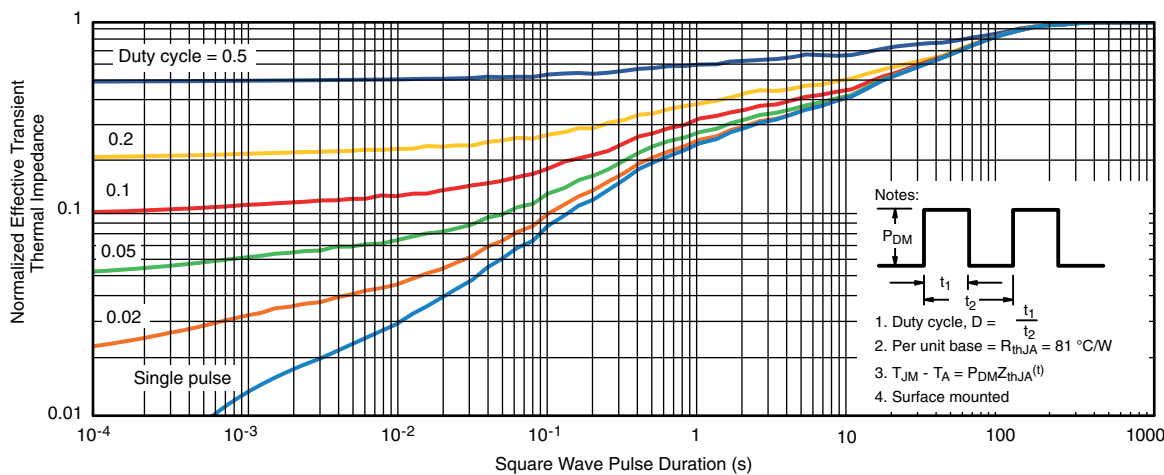
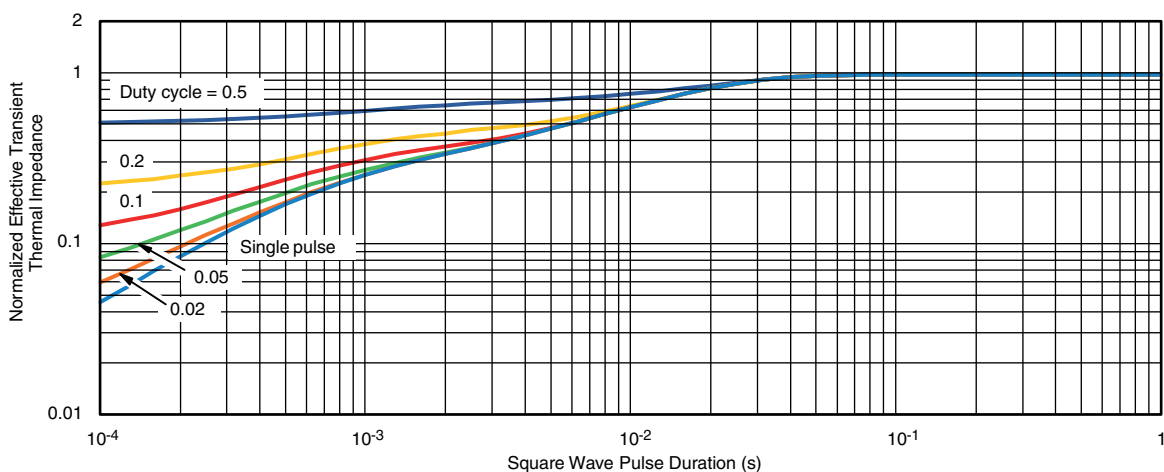
Source Drain Diode Forward Voltage



Safe Operating Area

Note

- a. $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified

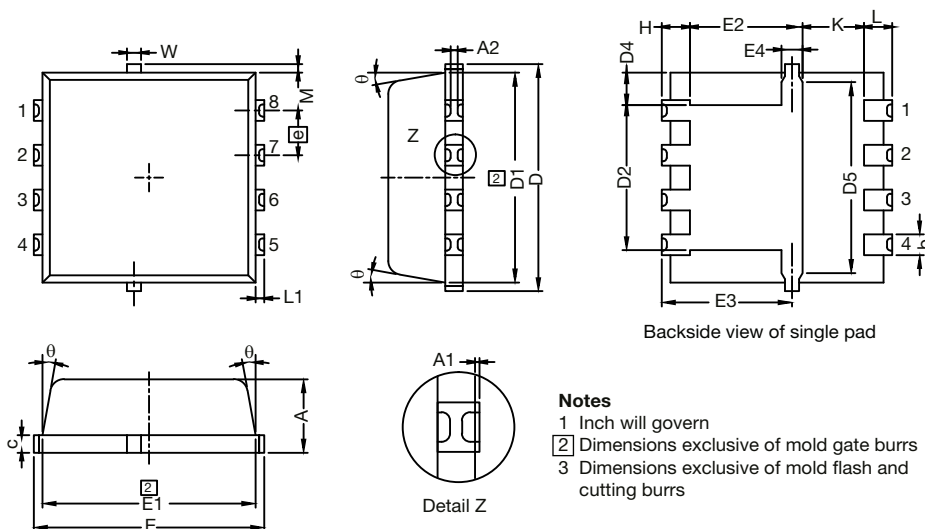
**THERMAL RATINGS** ($T_A = 25\text{ }^{\circ}\text{C}$, unless otherwise noted)**Normalized Thermal Transient Impedance, Junction-to-Ambient****Normalized Thermal Transient Impedance, Junction-to-Case****Note**

- The characteristics shown in the two graphs
 - Normalized Transient Thermal Impedance Junction-to-Ambient ($25\text{ }^{\circ}\text{C}$)
 - Normalized Transient Thermal Impedance Junction-to-Case ($25\text{ }^{\circ}\text{C}$)
 are given for general guidelines only to enable the user to get a “ball park” indication of part capabilities. The data are extracted from single pulse transient thermal impedance characteristics which are developed from empirical measurements. The latter is valid for the part mounted on printed circuit board - FR4, size 1" x 1" x 0.062", double sided with 2 oz. copper, 100 % on both sides. The part capabilities can widely vary depending on actual application parameters and operating conditions

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package / tape drawings, part marking, and reliability data, see www.vishay.com/ppg?78974.

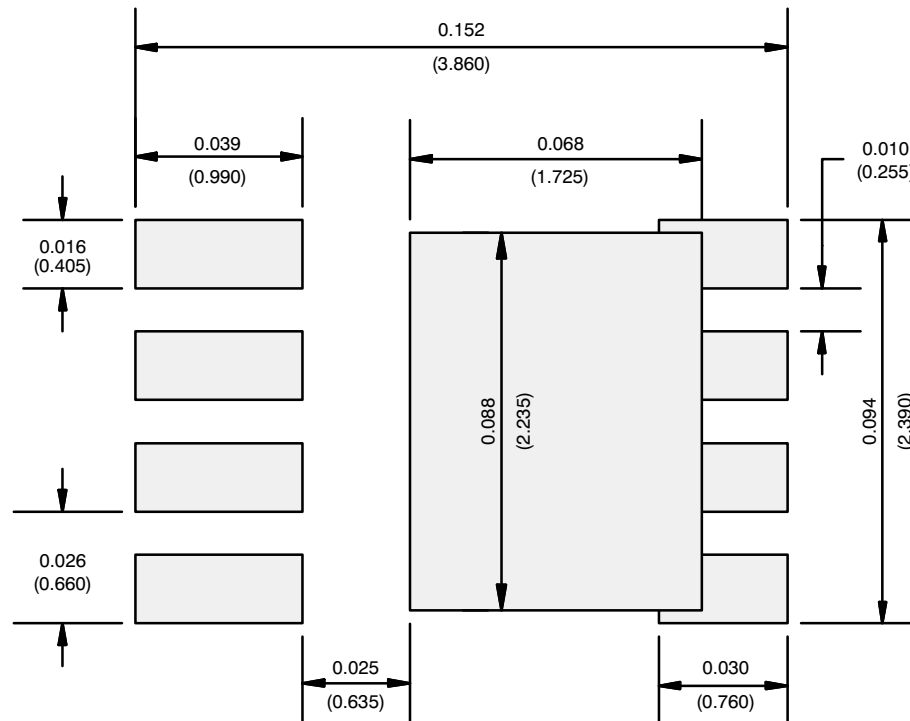


PowerPAK® 1212-8W Case Outline



DIM.	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.97	1.04	1.12	0.038	0.041	0.044
A1	0	-	0.05	0	-	0.002
A2	0	-	0.13	0	-	0.005
b	0.23	0.30	0.41	0.009	0.012	0.016
c	0.23	0.28	0.33	0.009	0.011	0.013
D	3.20	3.30	3.40	0.126	0.130	0.134
D1	2.95	3.05	3.15	0.116	0.120	0.124
D2	1.98	2.11	2.24	0.078	0.083	0.088
D4	0.47 typ.			0.0185 typ.		
D5	2.3 typ.			0.090 typ.		
E	3.20	3.30	3.40	0.126	0.130	0.134
E1	2.95	3.05	3.15	0.116	0.120	0.124
E2	1.47	1.60	1.73	0.058	0.063	0.068
E3	1.75	1.85	1.98	0.069	0.073	0.078
E4	0.34 typ.			0.013 typ.		
e	0.65 BSC.			0.026 BSC		
K	0.86 typ.			0.034 typ.		
H	0.30	0.41	0.51	0.012	0.016	0.020
L	0.30	0.43	0.56	0.012	0.017	0.022
L1	0.06	0.13	0.20	0.002	0.005	0.008
θ	0°	-	12°	0°	-	12°
W	0.15	0.25	0.36	0.006	0.010	0.014
M	0.125 typ.			0.005 typ.		
ECN: C15-1530-Rev. B, 16-Nov-15						
DWG: 6032						

RECOMMENDED MINIMUM PADS FOR PowerPAK® 1212-8 Single



Recommended Minimum Pads
Dimensions in Inches/(mm)

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