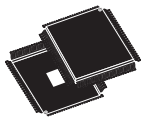
SPC574K70E5, SPC574K72E5

32-bit Power Architecture® based MCU for automotive applications

Datasheet - production data



eTQFP144
(20 mm × 20 mm × 1.0 mm)

Features

- Two main 32-bit Power Architecture® VLE compliant CPU core (e200z4), dual issue, running in lockstep
  - Single-precision floating point operations
  - 16 KB local instruction SRAM and 64 KB local data SRAM
  - 4 KB I-Cache and 2 KB D-Cache
- One 32-bit Power Architecture® VLE compliant I/O processor core (e200z2)
  - Single-precision floating point operations
  - Lightweight Signal Processing Auxiliary Processing Unit (LSP APU) instruction support for digital signal processing (DSP)
  - 16 KB local instruction SRAM and 48 KB local data SRAM
- 2624 KB on-chip flash memory
  - Supporting EEPROM emulation (64 KB)
- 64 KB on-chip general-purpose SRAM (+112 KB data RAM included in the CPUs)
- Multi-channel direct memory access controller (eDMA) with 32 channels
- Dual interrupt controller (INTC)
- Dual phase-locked loops, including one Frequency-modulated
- System integration unit lite (SIUL)
- Boot Assist Flash (BAF) supports factory programming using serial bootload through 'Serial Boot Mode Protocol'.
  Physical Interface (PHY) can be:
  - UART
  - CAN
- Generic timer module (GTM122)
  - Intelligent complex timer module
  - 88 channels (24 input and 64 output)
  - 3 programmable fine grain multi-threaded cores
  - 26 KB of dedicated SRAM
  - Hardware support for engine control, motor control and safety related applications
- Enhanced analog-to-digital converter system with:
  - 5 separate 12-bit SAR analog converters
  - 2 separate 16-bit Sigma-Delta analog converters
- 5 Deserial Serial Peripheral Interface (DSPI) modules
- 5 LIN and UART communication interface (LINFlexD) modules
- 2 modular controller area network (M_CAN) modules, and one time-triggered controller area network (M_TTCAN).
- Dual-channel FlexRay controller
- Nexus development interface (NDI) per IEEE-ISTO 5001-2003 standard, with partial support for 2010 standard
- Device and board test support per Joint Test Action Group (JTAG) (IEEE 1149.1)
- On-chip voltage regulator controller manages the supply voltage down to 1.2 V for core logic
- Designed for eTQFP144 and eLQFP176

Table 1. Device summary

Memory Flash size	Root Part Numbers
	Package eTQFP144
2624 KByte	SPC574K72E5
2112 KByte	SPC574K70E5

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1 Introduction

1.1 Document overview

This document provides electrical specifications, pin assignments, and package diagrams for the SPC574Kxx series of microcontroller units (MCUs). For functional characteristics, see the SPC574Kxx microcontroller reference manual.

1.2 Description

This family of MCUs targets automotive powertrain controller applications for four-cylinder gasoline and diesel engines, chassis control applications, transmission control applications, steering and braking applications, as well as low-end hybrid applications.

Many of the applications are considered to be functionally safe and the family is designed to achieve ISO26262 ASIL-D compliance.

1.3 Device feature summary

Table 2. SPC574Kxx device feature summary

Feature		Description
Process		55 nm
Main processor	Core	e200z4
	Number of main cores	1
	Number of checker cores	1
	Local RAM (per main core)	16 KB Instruction 64 KB Data
	Single precision floating point	Yes
	VLE	Yes
	Cache	4 KB Instruction 2 KB Data
I/O processor	Core	e200z2
	Local RAM	16 KB Instruction 48 KB Data
	Single precision floating point	Yes
	LSP	Yes
	VLE	Yes
	Cache	No
Main processor frequency		160 MHz
I/O processor frequency		80 MHz
MPU		Yes

Table 2. SPC574Kxx device feature summary(Continued)

Feature	Description
Semaphores	Yes
CRC channels	2
Software watchdog timer (task SWT/safety SWT)	3 (2/1)
Core Nexus class	3+
Sequence processing unit (SPU)	Yes
Debug and calibration interface (DCI) / run control module	Yes
System SRAM	64 KB
Flash memory	2560 KB
Flash memory fetch accelerator	2 × 2 × 256-bit
Data flash memory (EEPROM)	4 × 16 KB
Flash memory overlay RAM	16 KB
UTEST flash memory	16 KB
Boot assist flash (BAF)	16 KB
Calibration interface	64-bit IPS slave
DMA channels	32
DMA Nexus Class	3
LINFlexD (UART/MSC)	5 (3/2)
CAN (M_CAN/M_TTCAN)	3 (2/1)
DSPI (SPI/MSC/sync SCI)	5 (3/2/1)(1)
Microsecond bus downlink	Yes
SENT bus	6
I^2C	1
PSI5 bus	2
FlexRay	1 × dual channel
Ethernet (RMII)	Yes
Zipwire (SIPI/LFAST) interprocessor bus	High speed
System timers	6 PIT channels 2 AUTOSAR® (STM) 64-bit PIT
GTM timer	24 input channels, 64 output channels
GTM RAM	26 KB
Interrupt controller	360 sources
ADC (SAR)	5
ADC (SD)	2
Temperature sensor	Yes

Table 2. SPC574Kxx device feature summary(Continued)

Feature	Description
Self-test control unit (STCU2)	Yes
PLL	Dual PLL with FM
Internal linear voltage regulator	1.2 V
External power supplies	5 V 3.3 V(2)
Low-power modes	Stop mode Slow mode
Packages	eTQFP144 eLQFP176 172-pin FusionQuad®(3) 216-pin FusionQuad®(3)

1. One of the two MSC DSPIs is remapped to be used as sync SCI.
2. Optional: can be used for special I/O segments.
3. Also available in a 172-pin FusionQuad® package, which allows an eTQFP144 pin-compatible package for development, and in a 216-pin FusionQuad® package, which allows an eLQFP176 pin-compatible package for development.

1.4 Block diagram

Figure 1 and *Figure 2* show the top-level block diagrams.

Figure 1. Block diagram

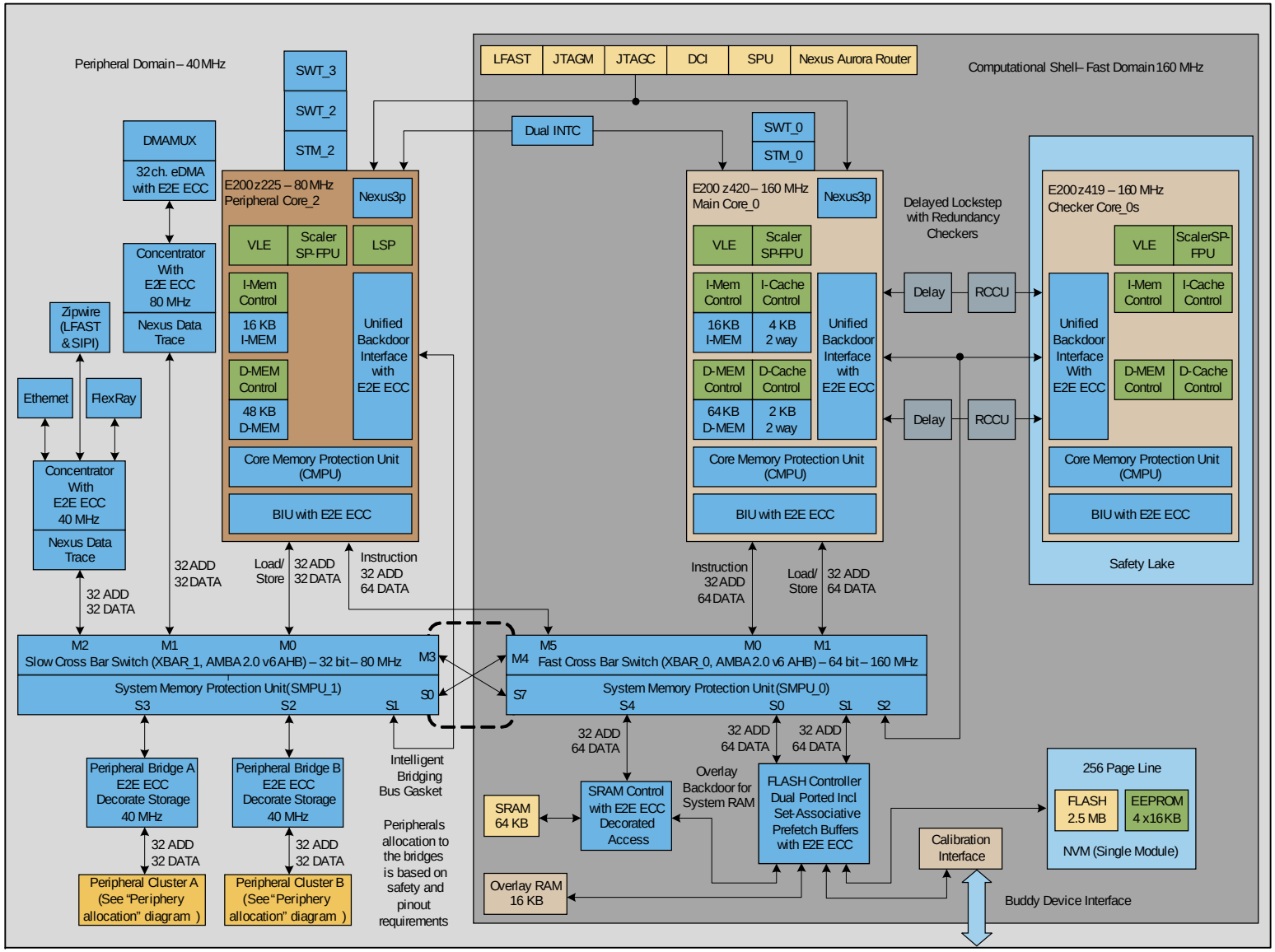
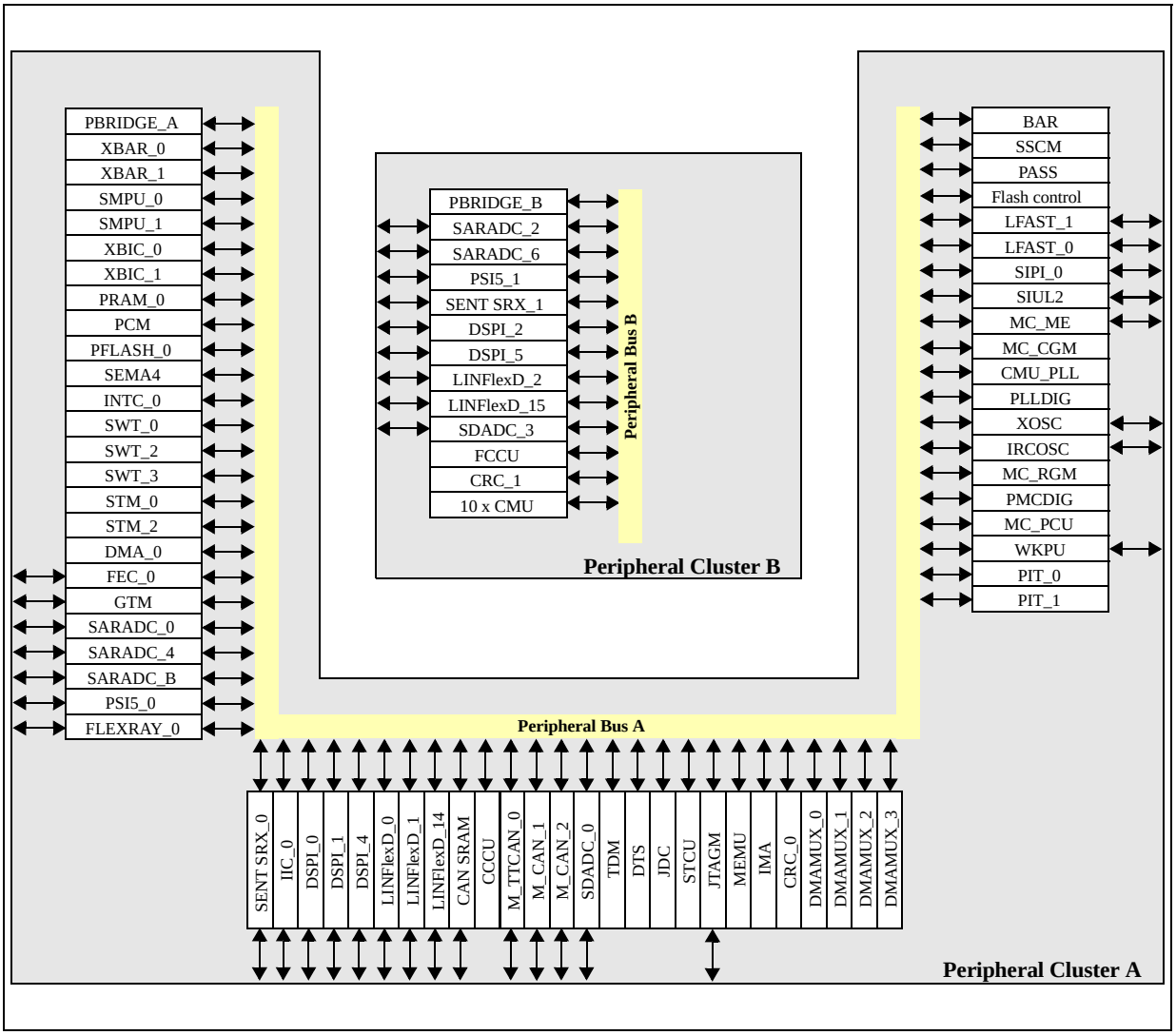


Figure 2. Periphery allocation



1.5 Feature overview

On-chip modules within SPC574Kxx include the following features:

- One main processor core and one checker core, single-issue, 32-bit CPU core complexes (e200z4), running in lockstep
  - Power Architecture embedded specification compliance
  - Instruction set enhancement allowing variable length encoding (VLE), encoding a mix of 16-bit and 32-bit instructions, for code size footprint reduction
  - Single-precision floating point operations
  - 16 KB local instruction SRAM and 64 KB local data SRAM
  - 4 KB I-Cache and 2 KB D-Cache
- I/O processor, single issue, 32-bit CPU core complexes (e200z2), with
  - Power Architecture embedded specification compliance
  - Instruction set enhancement allowing variable length encoding (VLE), encoding a mix of 16-bit and 32-bit instructions, for code size footprint reduction
  - Single-precision floating point operations
  - Lightweight Signal Processing Auxiliary Processing Unit (LSP APU) instruction support for digital signal processing (DSP)
  - 16 KB local instruction SRAM and 48 KB local data SRAM
- 2624 KB (2560 KB code + 64 KB EEPROM) on-chip flash memory: supports read during program and erase operations, and multiple blocks allowing EEPROM emulation
- 64 KB on-chip general-purpose SRAM (+ 112 KB data RAM included in the CPUs)
- Multi-channel direct memory access controller (eDMA) with 32 channels
- Dual interrupt controller (INTC)
- Dual phase-locked loops with stable clock domain for peripherals and FM modulation domain for computational shell
- Dual crossbar switch architecture for concurrent access to peripherals, flash memory, or SRAM from multiple bus masters with end-to-end ECC
- System integration unit lite (SIUL2)
- Boot Assist Flash (BAF) supports factory programming using serial bootload through ‘Serial Boot Mode Protocol’. Physical Interface (PHY) can be
  - UART
  - CAN
- Generic timer module (GTM122)
  - Intelligent complex timer module
  - 88 channels (24 input and 64 output)
  - 3 programmable fine grain multi-threaded cores
  - 26 KB of dedicated SRAM
  - 24-bit wide channels
  - Hardware support for engine control, motor control and safety related applications
- Enhanced analog-to-digital converter system with:
  - 5 separate 12-bit SAR analog converters
  - 2 separate 16-bit Sigma-Delta analog converters

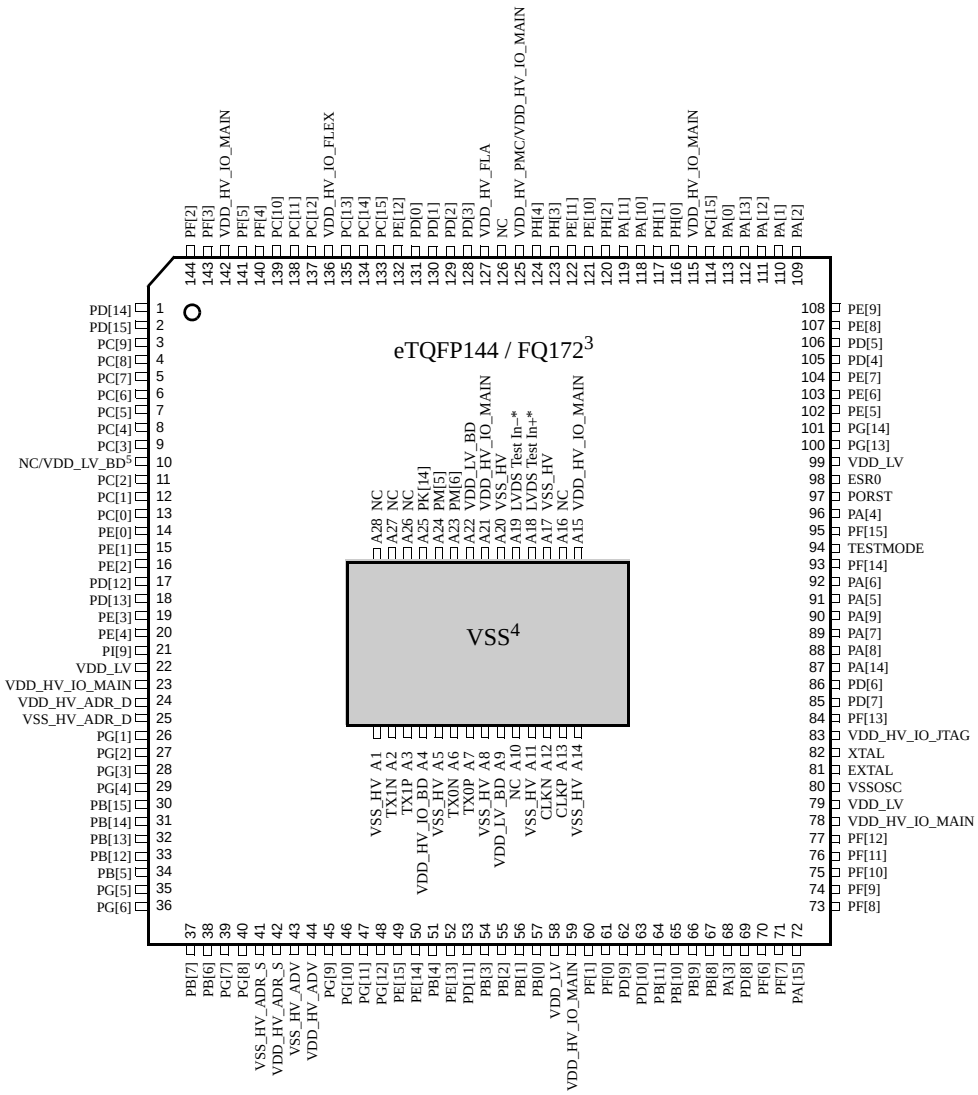
- 5 Deserial Serial Peripheral Interface (DSPI) modules
- 5 LIN and UART communication interface (LINFlexD) modules
  - LINFlexD_0 is a Master/Slave
  - LINFlexD_1, LINFlexD_2, LINFlexD_14, and LINFlexD_15 are Masters
- 2 modular Controller Area Network (M_CAN) modules, and one time-triggered Controller Area Network (M_TTCAN)
- Dual-channel FlexRay controller
- Nexus development interface (NDI) per IEEE-ISTO 5001-2003 standard, with partial support for 2010 standard
- Device and board test support per Joint Test Action Group (JTAG) (IEEE 1149.1)
- On-chip voltage regulator controller manages the supply voltage down to 1.2 V for core logic

2 Package pinouts and signal descriptions

2.1 Package pinouts

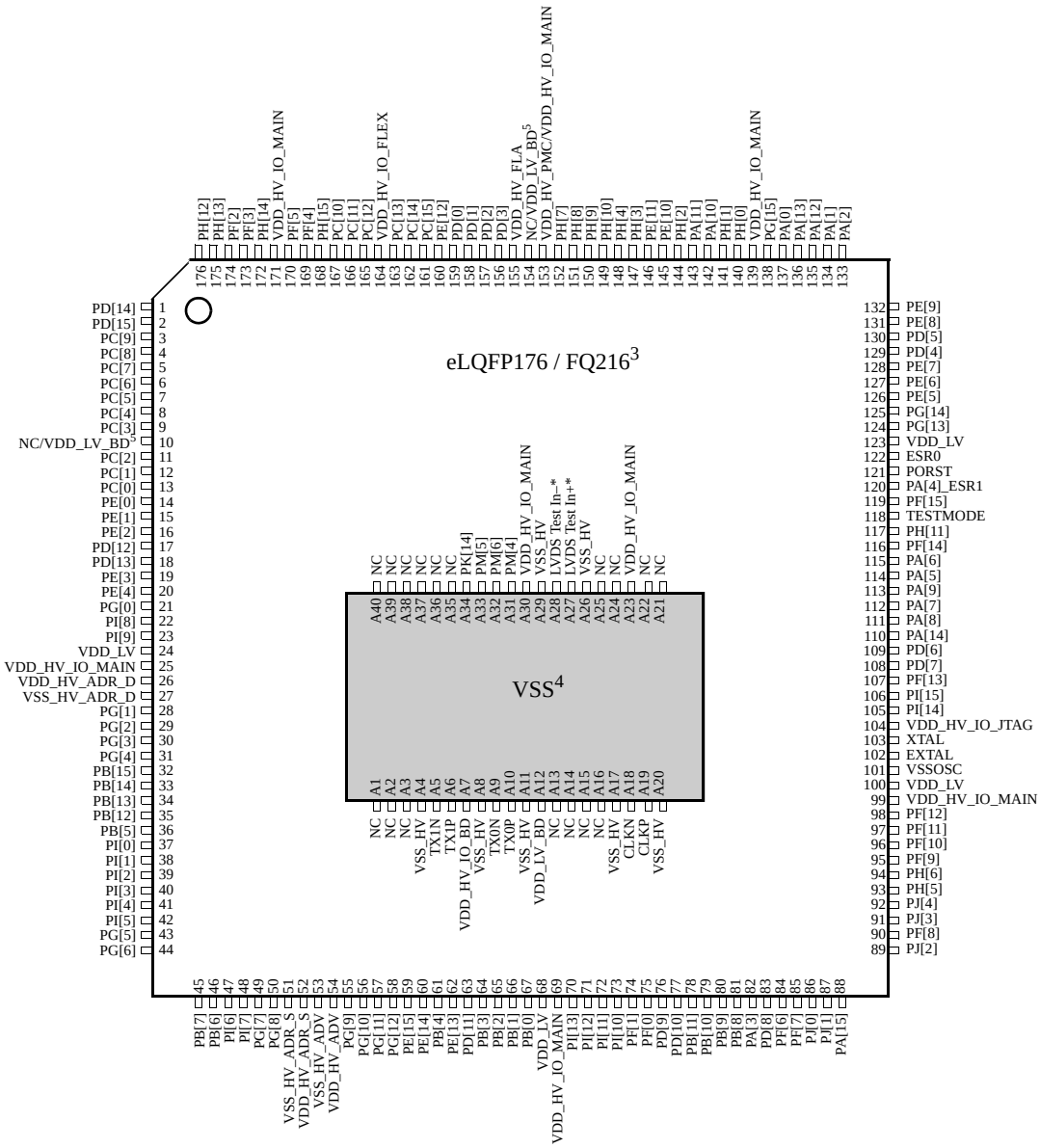
The QFP and FusionQuad® package pinouts are shown in *Figure 3* and *Figure 4*.

Figure 3. 144-pin QFP and 172-pin FQ configuration (top view)



Note:
1 Pins marked “NC” have no connection.
2 LVDS Test pins marked with an asterix (*) can be soldered to GND or left unconnected.
3 The eLQFP144 and FQ172 package pinouts are nearly identical, with the following exception: A1–A28 are additional pins that appear only on the FQ172 package.
4 The shaded area in the middle of the pinout is an exposed pad that on both the eLQFP144 and FQ172 packages is the primary V_{SS} connection.
5 Pin 10 is NC in the 144-pin package and VDD_LV_BD in the 172-pin package.

Figure 4. 176-pin QFP and 216-pin FQ configuration (top view)



Note:
1. Pins marked “NC” have no connection.
2. FQ LVDS Test pins marked with an asterix (*) can be soldered to GND or left unconnected.
3. The eLQFP176 and FQ216 package pinouts are nearly identical, with the following exception: A1–A40 are additional pins that appear only on the FQ216 package.
4. The shaded area in the middle of the pinout is an exposed pad that on both the eLQFP176 and FQ216 packages is the primary V_{SS} connection.
5. Pins 10 and 154 are NC in the 176-pin package and VDD_LV_BD in the 216-pin package.

Note: The FusionQuad® package is for development purposes only and is not available as a production device. The FusionQuad package is not intended to be qualified and is available only in small quantities.

2.2 Pin descriptions

The following sections provide signal descriptions and related information about device functionality and configuration.

2.2.1 Power supply and reference voltage pins

The Supply Pins Table contains information on power supply and reference pins. See the Signal Table (Excel file) attached to this document. Locate the paperclip symbol on the left side of the PDF window, and click it. Double-click on the excel file to open it and select the Supply Pins Table tab.

Note: All ground supplies must be toed to ground. They must not float.

2.2.2 System pins

Table 3 contains information on system pin functions for the devices.

Table 3. System pins

Symbol	Description	Direction	QFP pin			
			144	FQ172	176	FQ216
PORST	Power on reset with Schmitt trigger characteristics and noise filter. PORST is active low	Bidirectional	97		121	
ESR0	External functional reset with Schmitt trigger characteristics and noise filter. ESR0 is active low	Bidirectional	98		122	
TESTMODE	Pin for testing purpose only. An internal pull-down is implemented on the TESTMODE pin to prevent the device from entering TESTMODE. It is recommended to connect the TESTMODE pin to $V_{SS\_HV\_IO}$ on the board. The value of the TESTMODE pin is latched at the negation of reset and has no affect afterward. The device will not exit reset with the TESTMODE pin asserted during power-up.	Input only	94		118	
XTAL	Analog output of the oscillator amplifier circuit needs to be grounded if oscillator is used in bypass mode.	Output	82		103	
EXTAL	Analog input of the oscillator amplifier circuit when oscillator is not in bypass mode Analog input for the clock generator when oscillator is in bypass mode	Input	81		102	

2.2.3 LVDS pins

Table 4 contains information on LVDS pin functions for the devices.

Table 4. LVDSM pin descriptions

Functional block	Port pin	Signal	Signal description	Direction	Package pin number	
					eTQFP144, FQ172	eLQFP176, FQ216
SIPI LFAST(1)	PF[13]	SIPI_RXN	Interprocessor Bus LFAST, LVDS Receive Negative Terminal	I	84	107
	PD[7]	SIPI_RXP	Interprocessor Bus LFAST, LVDS Receive Positive Terminal	I	85	108
	PD[6]	SIPI_TXN	Interprocessor Bus LFAST, LVDS Transmit Negative Terminal	O	86	109
	PA[14]	SIPI_TXP	Interprocessor Bus LFAST, LVDS Transmit Positive Terminal	O	87	110
Debug LFAST(1)(2)	PA[8]	DEBUG_TXN	Debug LFAST, LVDS Transmit Positive Terminal	O	88	111
	PA[7]	DEBUG_TXP	Debug LFAST, LVDS Transmit Negative Terminal	O	89	112
	PA[9]	DEBUG_RXP	Debug LFAST, LVDS Receive Negative Terminal	I	90	113
	PA[5]	DEBUG_RXN	Debug LFAST, LVDS Receive Positive Terminal	I	91	114
DSPI 4 Microsecond Bus	PD[3]	SCK_N	DSPI 4 Microsecond Bus Serial Clock, LVDS Negative Terminal	O	128	156
	PD[2]	SCK_P	DSPI 4 Microsecond Bus Serial Clock, LVDS Positive Terminal	O	129	157
	PD[1]	SOUT_N	DSPI 4 Microsecond Bus Serial Data, LVDS Negative Terminal	O	130	158
	PD[0]	SOUT_P	DSPI 4 Microsecond Bus Serial Data, LVDS Positive Terminal	O	131	159
DSPI 5 Microsecond Bus	PF[9]	SCK_N	DSPI 5 Microsecond Bus Serial Clock, LVDS Negative Terminal	O	74	95
	PF[10]	SCK_P	DSPI 5 Microsecond Bus Serial Clock, LVDS Positive Terminal	O	75	96
	PF[11]	SOUT_N	DSPI 5 Microsecond Bus Serial Data, LVDS Negative Terminal	O	76	97
	PF[12]	SOUT_P	DSPI 5 Microsecond Bus Serial Data, LVDS Positive Terminal	O	77	98

Table 4. LVDSM pin descriptions(Continued)

Functional block	Port pin	Signal	Signal description	Direction	Package pin number	
					eTQFP144, FQ172	eLQFP176, FQ216
Differential DSPI 2	PD[3]	SCK_N	Differential DSPI 2 Clock, LVDS Negative Terminal	O	128	156
	PD[2]	SCK_P	Differential DSPI 2 Clock, LVDS Positive Terminal	O	129	157
	PD[1]	SOUT_N	Differential DSPI 2 Serial Output, LVDS Negative Terminal	O	130	158
	PD[0]	SOUT_P	Differential DSPI 2 Serial Output, LVDS Positive Terminal	O	131	159
	PF[13]	SIN_N	Differential DSPI 2 Serial Input, LVDS Negative Terminal	I	84	107
	PD[7]	SIN_P	Differential DSPI 2 Serial Input, LVDS Positive Terminal	I	85	108
Differential DSPI 5	PF[9]	SCK_N	Differential DSPI 5 Clock, LVDS Negative Terminal	O	74	95
	PF[10]	SCK_P	Differential DSPI 5 Clock, LVDS Positive Terminal	O	75	96
	PF[11]	SOUT_N	Differential DSPI 5 Serial Output, LVDS Negative Terminal	O	76	97
	PF[12]	SOUT_P	Differential DSPI 5 Serial Output, LVDS Positive Terminal	O	77	98
	PF[13]	SIN_N	Differential DSPI 5 Serial Input, LVDS Negative Terminal	I	84	107
	PD[7]	SIN_P	Differential DSPI 5 Serial Input, LVDS Positive Terminal	I	85	108

1. DRCLK and TCK/DRCLK usage for SIPI LFAST and Debug LFAST are described in the SPC574Kxx reference manual, refer to SIPI LFAST and Debug LFAST chapters.
2. Pads use special enable signal from DCI block: DCI driven enable for Debug LFAST pads is transparent to user.

Table 5. LVDSF pin descriptions

Functional block	Pad	Signal	Signal description	Direction	Package pin number			
					eTQFP144	FQ172	eLQFP176	FQ216
Nexus Aurora High Speed Trace	—	TXAP	Not available	O	—	—	—	—
	—	TXAN	Not available	O	—	—	—	—
	—	TXBP (TX0P)	Nexus Aurora High Speed Trace Lane 0, LVDS Positive Terminal	O	—	A7	—	A10
	—	TXBN (TX0N)	Nexus Aurora High Speed Trace Lane 0, LVDS Negative Terminal	O	—	A6	—	A9
	—	TXCP (TX1P)	Nexus Aurora High Speed Trace Lane 1, LVDS Positive Terminal	O	—	A3	—	A6
	—	TXCN (TX1N)	Nexus Aurora High Speed Trace Lane 1, LVDS Negative Terminal	O	—	A2	—	A5
	—	TXDP	Not available	O	—	—	—	—
	—	TXDN	Not available	O	—	—	—	—
	—	CLKP (BD-AGBTCLKP)	Nexus Aurora High Speed Trace Clock, LVDS Positive Terminal	O	—	A13	—	A19
	—	CLKN (BD-AGBTCLKN)	Nexus Aurora High Speed Trace Clock, LVDS Negative Terminal	O	—	A12	—	A18
	—	LPBK_P	Aurora High Speed Trace Loopback, LVDS Positive Terminal (LVDS Test In +)	I	—	A18	—	A27
	—	LPBK_N	Aurora High Speed Trace Loopback, LVDS Negative Terminal (LVDS Test In –)	I	—	A19	—	A28

2.2.4 Generic pins

The I/O Signal Description Table contains information on generic pins. See the I/O Signal Description and Input Multiplexing Tables (Excel file) attached to this document. Locate the paperclip symbol on the left side of the PDF window, and click it. Double-click on the excel file to open it and select the I/O Signal Description Table tab.

3 Electrical characteristics

3.1 Introduction

This section contains detailed information on power considerations, DC/AC electrical characteristics, and AC timing specifications.

In the tables where the device logic provides signals with their respective timing characteristics, the symbol “CC” (Controller Characteristics) is included in the “Symbol” column.

In the tables where the external system must provide signals with their respective timing characteristics to the device, the symbol “SR” (System Requirement) is included in the “Symbol” column.

Note: Parameters given to junction temperature T_J = 150 °C are for packaged parts .

Note: Within this document, $V_{DD\_HV\_IO}$ refers to supply pins $V_{DD\_HV\_IO\_MAIN}$, $V_{DD\_HV\_IO\_JTAG}$, $V_{DD\_HV\_IO\_FLEX}$, and $V_{DD\_HV\_FLA}$.

3.2 Parameter classification

The electrical parameters shown in this supplement are guaranteed by various methods. To give the customer a better understanding, the classifications listed in *Table 6* are used and the parameters are tagged accordingly in the tables where appropriate.

Table 6. Parameter classifications

Classification tag	Tag description
P	Parameters are guaranteed by production testing on each individual device.
C	Parameters are guaranteed by the design characterization by measuring a statistically relevant sample size across process variations.
T	Parameters are guaranteed by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted. All values shown in the typical column are within this category.
D	Parameters are derived mainly from simulations.

3.3 Absolute maximum ratings

Table 7 describes the maximum ratings of the device.

Table 7. Absolute maximum ratings(1)

Symbol		Parameter	Conditions	Value		Unit
				Min	Max	
Cycle	T	Lifetime power cycles	—	—	1000 k	—
V_{SS_HV}	D	Ground voltage	—	—	—	—
V_{DD_LV}	D	1.2 V core supply voltage(2),(3),(4)	—	–0.3	1.5	V

Table 7. Absolute maximum ratings(1)(Continued)

Symbol		Parameter	Conditions	Value		Unit
				Min	Max	
$V_{DD\_LV\_BD}$	D	1.2 V Emulation module supply (3),(3),(4)	—	–0.3	1.5	V
$V_{DD\_HV\_IO}$(5)	D	I/O supply voltage(6)	—	–0.3	6.0	V
$V_{DD\_HV\_IO\_BD}$	D	I/O Emulation module supply	—	–0.3	6.0	V
$V_{DD\_HV\_PMC}$	D	Power Management Controller supply voltage(6)	—	–0.3	6.0	V
$V_{SS\_HV\_ADV}$	D	SAR and S/D ADC ground voltage	Reference to V_{SS_HV}	–0.3	0.3	V
$V_{DD\_HV\_ADV}$(7)	D	SAR and S/D ADC supply voltage	Reference to $V_{SS\_HV\_ADV}$	–0.3	6.0	V
$V_{SS\_HV\_ADR\_D}$	D	S/D ADC ground reference	—	–0.3	0.3	V
$V_{DD\_HV\_ADR\_D}$	D	S/D ADC voltage reference	Reference to $V_{SS\_HV\_ADR\_D}$	–0.3	6.0	V
$V_{SS\_HV\_ADR\_S}$	D	SAR ADC ground reference	—	–0.3	0.3	V
$V_{DD\_HV\_ADR\_S}$	D	SAR ADC voltage reference	Reference to $V_{SS\_HV\_ADR\_S}$	–0.3	6.0	V
$V_{DD\_LV\_BD} – V_{DD\_LV}$	—	Emulation module supply differential to 1.2 V core supply	—	–0.3	1.5	V
$V_{SS} – V_{SS\_HV\_ADR\_D}$	D	$V_{SS\_HV\_ADR\_D}$ differential voltage	—	–0.3	0.3	V
$V_{SS} – V_{SS\_HV\_ADR\_S}$	D	$V_{SS\_HV\_ADR\_S}$ differential voltage	—	–0.3	0.3	V
$V_{SS\_HV} – V_{SS\_HV\_ADV}$	D	$V_{SS\_HV\_ADV}$ differential voltage	—	–0.3	0.3	V
V_{IN}	D	I/O input voltage range(8)	—	–0.3	6.0	V
			Relative to $V_{SS\_HV\_IO}$(9),(10)	–0.3	—	
			Relative to $V_{DD\_HV\_IO}$(9),(10)	—	0.3	
			Relative to $V_{DD\_HV\_ADV}$	—	0.3	
I_{INJD}	T	Maximum DC injection current for digital pad	Per pin, applies to all digital pins	–5	5	mA
I_{INJA}	T	Maximum DC injection current for analog pad	Per pin, applies to all analog pins	–5	5	mA
I_{MAXD}	SR	Maximum output DC current when driven	Medium	–7	8	mA
			Strong	–10	10	
			Very strong	–11	11	
I_{MAXSEG}	SR	Maximum current per power segment(11)	—	–90	90	mA
T_{STG}	T	Storage temperature range and non-operating times	—	–55	175	°C

Table 7. Absolute maximum ratings(1)(Continued)

Symbol		Parameter	Conditions	Value		Unit
				Min	Max	
STORAGE	—	Maximum storage time, assembled part programmed in ECU	No supply; storage temperature in range –40 °C to 85 °C	—	20	years
T_{SDR}	T	Maximum solder temperature(12) Pb-free package	—	—	260	°C
MSL	T	Moisture sensitivity level(13)	—	—	3	—
t_{XRAY}	T	X-ray screen time	At 80÷130 KV; 20÷50 µA; max 1 Gy dose	—	200	ms

1. Functional operating conditions are given in the DC electrical specifications. Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond the listed maxima may affect device reliability or cause permanent damage to the device.
2. Allowed 1.45 – 1.5 V for 60 seconds cumulative time at maximum T_J = 125 °C, remaining time as defined in note 3 and note 4
3. Allowed 1.375 – 1.45 V for 10 hours cumulative time at maximum T_J = 125 °C, remaining time as defined in note 4
4. 1.32 – 1.375 V range allowed periodically for supply with sinusoidal shape and average supply value below 1.288 V at maximum T_J = 125 °C
5. $V_{DD\_HV\_IO}$ refers to supply pins $V_{DD\_HV\_IO\_MAIN}$, $V_{DD\_HV\_IO\_JTAG}$, $V_{DD\_HV\_IO\_FLEX}$, $V_{DD\_HV\_OSC}$, $V_{DD\_HV\_FLA}$.
6. Allowed 5.5–6.0 V for 60 seconds cumulative time with no restrictions, for 10 hours cumulative time device in reset, T_J = 125 °C, remaining time at or below 5.5 V.
7. Includes ADC supplies $V_{DD\_HV\_ADV\_S}$ and $V_{DD\_HV\_ADV\_D}$. $V_{DD\_HV\_ADV}$ is also the supply for the device temperature sensor and bandgap reference.
8. The maximum input voltage on an I/O pin tracks with the associated I/O supply maximum. For the injection current condition on a pin, the voltage equals the supply plus the voltage drop across the internal ESD diode from I/O pin to supply. The diode voltage varies significantly across process and temperature, but a value of 0.3V can be used for nominal calculations.
9. $V_{DD\_HV\_IO}/V_{SS\_HV\_IO}$ refers to supply pins and corresponding grounds: $V_{DD\_HV\_IO\_MAIN}$, $V_{DD\_HV\_IO\_FLEX}$, $V_{DD\_HV\_IO\_JTAG}$, $V_{DD\_HV\_OSC}$, $V_{DD\_HV\_FLA}$.
10. Relative value can be exceeded if design measures are taken to ensure injection current limitation (parameters I_{INJD} and I_{INJA}).
11. Sum of all controller pins (including both digital and analog) must not exceed 200 mA. A $V_{DD\_HV\_IO}$ power segment is defined as one or more GPIO pins located between two $V_{DD\_HV\_IO}$ supply pins.
12. Solder profile per IPC/JEDEC J-STD-020D.
13. Moisture sensitivity per JEDEC test method A112.

3.4 Electrostatic discharge (ESD)

The following table describes the ESD ratings of the device.

Table 8. ESD ratings(1)(2)

Parameter	C	Conditions	Value	Unit
ESD for Human Body Model (HBM)(3)	T	All pins	2000	V
ESD for field induced Charged Device Model (CDM)(4)	T	All pins	500	V

1. All ESD testing is in conformity with CDF-AEC-Q100 Stress Test Qualification for Automotive Grade Integrated Circuits.
2. Device failure is defined as: “If after exposure to ESD pulses, the device does not meet the device specification requirements, which includes the complete DC parametric and functional testing at room temperature and hot temperature. Maximum DC parametrics variation within 10% of maximum specification”

3. This parameter tested in conformity with ANSI/ESD STM5.1-2007 Electrostatic Discharge Sensitivity Testing
4. This parameter tested in conformity with ANSI/ESD STM5.3-1990 Charged Device Model - Component Level

3.5 Operating conditions

The following table describes the operating conditions for the device for which all specifications in the datasheet are valid, except where explicitly noted.

The device operating conditions must not be exceeded or the functionality of the device is not guaranteed.

Table 9. Device operating conditions(1)

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
Frequency								
f_{SYS}	SR	C	Device operating frequency(2)	T_J = –40 °C to 150 °C	—	—	160	MHz
f_{LBIST}	SR	C	Self-test operating frequency	T_J = –40 °C to 150 °C	—	—	20	MHz
Temperature								
T_J	SR	P	Junction Temperature		–40.0	—	150.0	°C
T_A (T_L to T_H)	SR	P	Ambient temperature		–40.0	—	125.0	°C
Voltage								
V_{DD_LV}	CC	P	Core supply voltage measured at external pin(3),(4)	Refer to *Section 3.15: Power management: PMC, POR/LVD, sequencing*				V
$V_{DD\_HV\_IO\_MAIN}$	SR	P	I/O supply voltage	LVD400/HVD600 enabled	4.5	—	5.5	V
		C		LVD400/HVD600 disabled (5),(6),(7)	4.0	—	5.9	
		C			3.0	—	5.9	
$V_{DD\_HV\_IO\_JTAG}$	SR	P	JTAG I/O supply voltage(8)	5 V range	4.5	—	5.5	V
		C		3.3 V range	3.0	—	3.6	
		C		5 V range	4.0	—	5.9	
$V_{DD\_HV\_IO\_FLEX}$	SR	P	FlexRay I/O supply voltage	5 V range	4.5	—	5.5	V
		C		3.3 V range	3.0	—	3.6	
$V_{DD\_HV\_PMC}$(9)	SR	P	Power Management Controller (PMC) supply voltage	Full functionality	4.5	—	5.5	V
		C			3.0	—	5.5	
$V_{DD\_HV\_FLA}$(10),(11)	CC	P	Flash core voltage	—	3.0	—	5.5	V

Table 9. Device operating conditions[1](Continued)

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
$V_{DD\_HV\_ADV}$	SR	P	SARADC and SDADC supply voltage	LVD295/ enabled	4.5	—	5.5	V
		C		LVD295/ disabled[5],[6]	4.0	—	5.9	
		C		LVD295/ disabled[5],[6]	3.7	—	5.9	
$V_{DD\_HV\_ADR\_D}$	SR	P	SD ADC supply reference voltage	—	4.5	$V_{DD\_HV\_ADV}$	5.5	V
		C			4.0		5.9	
		C			3.0		4.0	
$V_{DD\_HV\_ADR\_D} - V_{DD\_HV\_ADV}$	SR	D	SD ADC reference differential voltage	—	—	—	25	mV
$V_{SS\_HV\_ADR}$	SR	P	SD ADC ground reference voltage	—	$V_{SS\_HV\_ADV}$			V
$V_{SS\_HV\_ADR\_D} - V_{SS\_HV\_ADV}$	SR	D	$V_{SS\_HV\_ADR\_D}$ differential voltage	—	–25	—	25	mV
$V_{DD\_HV\_ADR\_S}$[12]	SR	P	SARADC reference	—	4.5	—	5.5	V
		C			4.0		5.9	
		C			2.0		4.0	
$V_{DD\_HV\_ADR\_S} - V_{DD\_HV\_ADV}$	SR	D	SARADC reference differential voltage	—	—	—	25	mV
$V_{SS\_HV\_ADR\_S} - V_{SS\_HV\_ADV}$	SR	D	$V_{SS\_HV\_ADR\_S}$ differential voltage	—	–25	—	25	mV
$V_{SS\_HV\_ADV} - V_{SS}$	SR	D	$V_{SS\_HV\_ADV}$ differential voltage	—	–25	—	25	mV
V_{RAMP_HV}	SR	D	Slew rate on HV power supply pins	—	—	—	100	V/ms
V_{IN}	SR	C	I/O input voltage range	—	0	—	5.5	V
Injection current								
I_{IC}	SR	T	DC injection current (per pin)[13],[14],[15]	Digital pins and analog pins	–3.0	—	3.0	mA
I_{MAXSEG}	SR	D	Maximum current per power segment[16]	—	–80	—	80	mA

1. The ranges in this table are design targets and actual data may vary in the given range.
2. Maximum operating frequency is applicable to the computational cores and platform for the device. See the Clocking chapter in the SPC574Kxx *Microcontroller Reference Manual* for more information on the clock limitations for the various IP blocks on the device.
3. Core voltage as measured on device pin to guarantee published silicon performance.
4. During power ramp, voltage measured on silicon might be lower. Maximum performance is not guaranteed, but correct silicon operation is guaranteed. Refer to the Power Management and Reset Generation Module chapters in the SPC574Kxx *Microcontroller Reference Manual* for further information.
5. Maximum voltage is not permitted for entire product life. See *Table 7: Absolute maximum ratings*.

6. When internal LVD/HVDs are disabled, external monitoring is required to guarantee correct device operation.
7. Reduced output/input capabilities below 4.2 V. See performance derating values in *I/O pad electrical characteristics*
8. $V_{DD\_HV\_IO\_JTAG}$ supply is shorted with $V_{DD\_HV\_OSC}$ supply within package.
9. $V_{DD\_HV\_PMC}$ is shorted with $V_{DD\_HV\_IO\_MAIN}$ in the package.
10. Flash read operation is supported for a minimum $V_{DD\_HV\_FLA}$ value of 3.0 V. Flash read, program, and erase operations are supported for a minimum $V_{DD\_HV\_FLA}$ value of 3.0 V.
11. This voltage can be measured on the pin but is not supplied by an external regulator. The Power Management Controller generates PORs based on this voltage.
12. $V_{DD\_HV\_ADR\_S}$ must be between 4.5 V and 5.5 V for accurate reading of the device Temperature Sensor.
13. Full device lifetime without performance degradation
14. I/O and analog input specifications are only valid if the injection current on adjacent pins is within these limits. See *Table 7: Absolute maximum ratings* for maximum input current for reliability requirements.
15. The I/O pins on the device are clamped to the I/O supply rails for ESD protection. When the voltage of the input pin is above the supply rail, current is injected through the clamp diode to the supply rail. For external RC network calculation, assume typical 0.3 V drop across the active diode. The diode voltage drop varies with temperature.
16. Sum of all controller pins (including both digital and analog) must not exceed 200 mA. A $V_{DD\_HV\_IO}$ power segment is defined as one or more GPIO pins located between two $V_{DD\_HV\_IO}$ supply pins.

Table 10. Emulation (buddy) device operating conditions(1)

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
Frequency								
—	SR	C	Standard JTAG 1149.1/1149.7 frequency	—	—	—	50	MHz
—	SR	C	High-speed debug frequency	—	—	—	320	MHz
—	SR	T	Data trace frequency	—	—	—	1250	MHz
Temperature								
T_{J_BD}	SR	P	Device junction operating temperature range	—	–40.0	—	150.0	°C
T_{A_BD}	SR	P	Ambient operating temperature range	—	–40.0	—	125.0	°C
Voltage								
$V_{DD\_LV\_BD}$	SR	P	Buddy core supply voltage	—	1.2	—	1.32	V
$V_{DD\_HV\_IO\_BD}$	SR	P	Buddy I/O supply voltage	—	3.0	—	5.5	V
$V_{RAMP\_LV\_BD}$	SR	D	Buddy slew rate on core power supply pins	—	—	—	100	V/ms
$V_{RAMP\_HV\_BD}$	SR	D	Buddy slew rate on HV power supply pins	—	—	—	100	V/ms

1. The ranges in this table are design targets and actual data may vary in the given range.

Table 11. Temperature profile – Packaged parts

Vehicle category	Operation	Temperature	Cumulated duration (hours)
Passenger cars	Active operation	T_J = 150 °C	3000
		T_J = 135 °C	—
		T_J = 125 °C	9000
		T_J = 110 °C	6000
		T_J = 85 °C	1000
		T_J = 40 °C	500
		T_J = –40 °C	500
		Total operation time	20000
Passenger cars – low end	Active operation	T_A = 120 to 125 °C	100
		T_A = 115 to 120 °C	100
		T_A = 110 to 115 °C	100
		T_A = 105 to 110 °C	100
		T_A = 100 to 105 °C	100
		T_A = 95 to 100 °C	100
		T_A = 90 to 95 °C	100
		T_A = 85 to 90 °C	150
		T_A = 80 to 85 °C	300
		T_A = 50 to 80 °C	800
		T_A = 40 to 50 °C	1600
		T_A = 25 to 40 °C	2200
		T_A = –10 to 25 °C	1500
		T_A = –40 to –10 °C	500
		Total operation time	7750
Commercial vehicles	Active operation	T_J = 150 °C	360
		T_J = 140 °C	1200
		T_J = 130 °C	2100
		T_J = 120 °C	29000
		T_J = 110 °C	3600
		T_J = 85 °C	2740
		T_J = 40 °C	500
		T_J = –40 °C	500
		Total operation time	40000

3.6 DC electrical specifications

The following table describes the DC electrical specifications.

Table 12. DC electrical specifications(1)

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
I_{DDAPP}(2)	CC	C	Operating current all supplies with typical application	f_{SYS} = 160 MHz T_J < 150 °C	—	—	400(3)	mA
$I_{DD\_MAIN\_CORE\_AC}$	CC	C	Main Core 0 dynamic operating current	f_{SYS} = 160 MHz	—	—	56	mA
$I_{DD\_CHKR\_CORE\_AC}$	CC	C	Checker Core 0 dynamic operating current	f_{SYS} = 160 MHz	—	—	40	mA
I_{DDAR}	CC	T	$V_{DD\_HV\_IO}$ After Run operating current at 1.32 V(4)	T_{amb} = 55°C Total device consumption on $V_{DD\_HV\_IO}$, including consumption for V_{DD_LV} generation. No I/O activity	—	—	35	mA
		P		T_{amb} = 40°C	—	—	33	
$I_{DD\_LV\_BD}$	CC	P	Debug/Emulation low voltage supply operating current(5),(6)	T_J = 150 °C $V_{DD\_LV\_BD}$ = 1.32 V	—	—	250	mA
$I_{DD\_HV\_IO\_BD}$	CC	D	Debug/Emulation high voltage supply operating current (Aurora + JTAGM/LFAST)	T_J = 150 °C	—	—	130	mA
I_{SPIKE}	CC	T	Maximum short term current spike(7)	< 20 µs observation window	—	—	90	mA
dI	CC	T	Current difference ratio to average current (dI/avg(I))(8)	20 µs observation window	—	—	20	%
I_{SR}	CC	D	Current variation during boot/shut-down	—(9)	—	—	90(10)	mA
I_{DDOFF}	CC	T	Power-off current on $V_{DD\_HV\_IO}$ supply rails(11)	$V_{DD\_HV\_IO}$ = 2.5 V	100	—	—	µA
$V_{REF\_BG\_T}$	CC	P	Bandgap trimmed reference voltage	T_J = –40 °C to 150 °C $V_{DD\_HV\_ADV}$ = 5 V ± 10%	1.200	—	1.237	V
$V_{REF\_BG\_TC}$	CC	C	Bandgap temperature coefficient(12)	T_J = –40 °C to 150 °C $V_{DD\_HV\_ADV}$ = 5 V ± 10%	—	—	50	ppm/°C
$V_{REF\_BG\_LR}$	CC	C	Bandgap line regulation	T_J = –40 °C $V_{DD\_HV\_ADV}$ = 5 V ± 10%	—	—	8000	ppm/V
		C		T_J = 150 °C $V_{DD\_HV\_ADV}$ = 5 V ± 10%	—	—	4000	

1. The ranges in this table are design targets and actual data may vary in the given range.

2. Typical application consumption, unloaded I/O with LVDS pins active and terminated.
3. Maximum V_{DD_LV} consumption as for *Section 3.15.2, Main voltage regulator electrical characteristics*. Maximum junction temperature including temperature due to power dissipation as for *Section 4.5, Thermal characteristics*.
4. Device in STOP mode running from the internal RCOSC, with the external oscillator and ADCs disabled. Includes regulator consumption for V_{DD_LV} generation. Includes static I/O current with no pins toggling. V_{DD_HV} refers to all 5 V supplies ($V_{DD\_HV\_ADV}$, $V_{DD\_HV\_IO\_MAIN}$, $V_{DD\_HV\_IO\_JTAG}$, $V_{DD\_HV\_IO\_FLEX}$, and $V_{DD\_HV\_PMC}$). The I_{DDAR} current can be further reduced by disabling the I/O pad compensation cells via the PDO bits in the ME_<mode>_MC registers in the mode entry module (MC_ME).
5. Leakage of $V_{DD\_LV\_BD}$ at junction temperature of 150 °C with production device powered estimated at 120 mA
6. Aurora and LFAST enabled, further consumption of 70 mA on $V_{DD\_HV\_IO\_BD}$ supply for Aurora transmission line
7. I_{SPIKE} value is only valid for the use cases defined for the I_{DDAPP} and I_{DDAPP_LV} specifications and its conditions given in *Table 12 (DC electrical specifications)*.
8. Moving window, valid for I_{DDAPP} and its conditions given in *Table 12 (DC electrical specifications)*, with a maximum of 90 mA for the worst case application.
9. Condition 1: For power on period from 0 V up to normal operation with reset asserted.
   Condition 2: From reset asserted until IRCOSC frequency.
   Condition 3: Increasing frequency from IRCOSC to PLL full frequency.
   Condition 4: reverse order for power down to 0 V.
10. Current variation is considered during boot or during shut-down sequence. Progressive clock switching should be use to guarantee low current variation.This does not include current requested for the loading of the capacitances on the VDD_LV domain. Please refer to *Section 3.15.1, Power management integration*, Iclamp specification
11. I_{DDOFF} is the minimum guaranteed consumption of the device during power-up. It can be used to correctly size power-off ballast in case of current injection during power-off state.Power up/down current transients can be limited by controlling the clock ramp rates with the Progressive Clock Frequency Switching block on the device.
12. The temperature coefficient and line regulation specifications are used to calculate the reference voltage drift at an operating point within the specified voltage and temperature operating conditions.

3.7 I/O pad specification

The following table describes the different pad type configurations.

Table 13. I/O pad specification descriptions

Pad type	Description
Weak configuration	Provides a good compromise between transition time and low electromagnetic emission. Pad impedance is centered around 800 Ω.
Medium configuration	Provides transition fast enough for the serial communication channels with controlled current to reduce electromagnetic emission. Pad impedance is centered around 200 Ω.
Strong configuration	Provides fast transition speed; used for fast interface. Pad impedance is centered around 50 Ω.
Very strong configuration	Provides maximum speed and controlled symmetric behavior for rise and fall transition. Used for fast interface including Ethernet and FlexRay interfaces requiring fine control of rising/falling edge jitter. Pad impedance is centered around 40 Ω.
Differential configuration	A few pads provide differential capability providing very fast interface together with good EMC performances.
Input only pads	These low input leakage pads are associated with the ADC channels.

Note: Each I/O pin on the device supports specific drive configurations. See the signal description table in the device reference manual for the available drive configurations for each I/O pin.

3.7.1 I/O input DC characteristics

Table 14 provides input DC electrical characteristics as described in *Figure 5*.

Figure 5. I/O input DC electrical characteristics definition

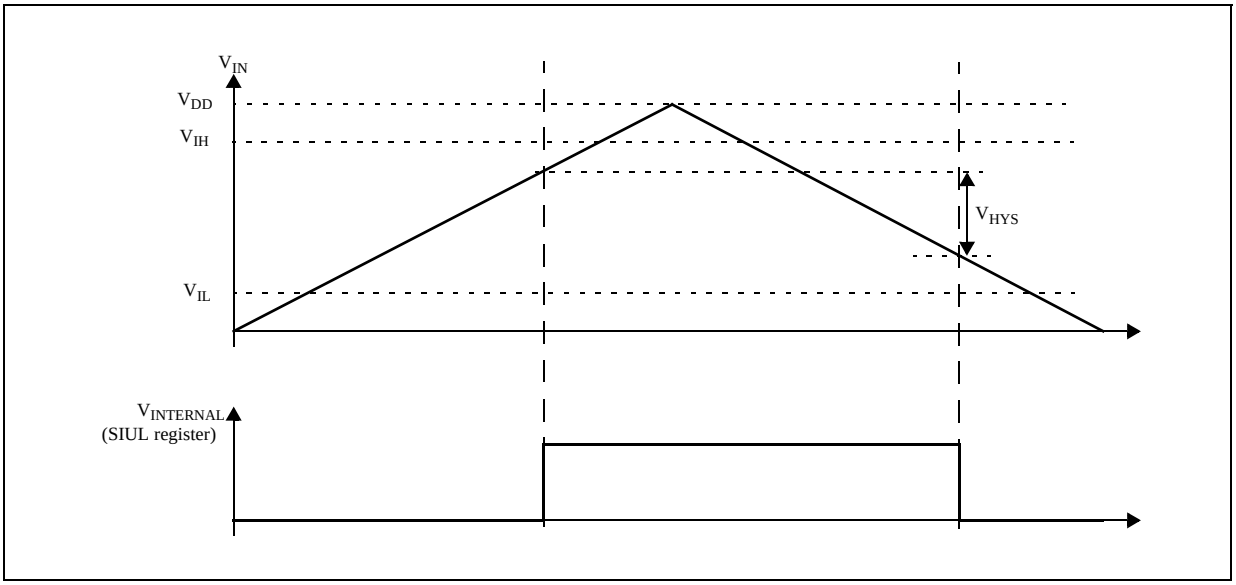


Table 14. I/O input DC electrical characteristics

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
TTL								
V_{IHTTL}	SR	P	Input high level TTL	4.75 V < $V_{DD\_HV\_IO}$ < 5.25 V(5)	2	—	$V_{DD\_HV\_IO}$ + 0.3	V
V_{ILTTL}	SR	P	Input low level TTL	4.75 V < $V_{DD\_HV\_IO}$ < 5.25 V(5)	–0.3	—	0.8	
V_{HYSTTL}	—	C	Input hysteresis TTL	4.75 V < $V_{DD\_HV\_IO}$ < 5.25 V(5)	0.275	—	—	
$V_{DRFTTTL}$	—	C	Input V_{IL}/V_{IH} temperature drift TTL	—	—	—	100	mV
AUTOMOTIVE								
V_{IHAUT}(1)	SR	P	Input high level AUTOMOTIVE	4.75 V < $V_{DD\_HV\_IO}$ < 5.25 V	3.8	—	$V_{DD\_HV\_IO}$ + 0.3	V
V_{ILAUT}(2)	SR	P	Input low level AUTOMOTIVE	4.75 V < $V_{DD\_HV\_IO}$ < 5.25 V	–0.3	—	2.1	V
V_{HYSAUT}(3)	—	C	Input hysteresis AUTOMOTIVE	4.75 V < $V_{DD\_HV\_IO}$ < 5.25 V	0.4(5)	—	—	V
$V_{DRFTAUT}$	—	C	Input V_{IL}/V_{IH} temperature drift	4.75 V < $V_{DD\_HV\_IO}$ < 5.25 V	—	—	100(4)	mV
CMOS								
V_{IHCMOS_H}(5)	SR	C	Input high level CMOS (with hysteresis)	3.0 V < $V_{DD\_HV\_IO}$ < 3.6 V	0.65 * $V_{DD\_HV\_IO}$	—	$V_{DD\_HV\_IO}$ + 0.3	V
		P		4.75 V < $V_{DD\_HV\_IO}$ < 5.25 V				

Table 14. I/O input DC electrical characteristics(Continued)

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
V_{IHCMOS}(5)	SR	C	Input high level CMOS (without hysteresis)	3.0 V < $V_{DD\_HV\_IO}$ < 3.6 V	0.6 * $V_{DD\_HV\_IO}$	—	$V_{DD\_HV\_IO}$ + 0.3	V
		P		4.75 V < $V_{DD\_HV\_IO}$ < 5.25 V				
V_{ILCMOS_H}(5)	SR	C	Input low level CMOS (with hysteresis)	3.0 V < $V_{DD\_HV\_IO}$ < 3.6 V	–0.3	—	0.35 * $V_{DD\_HV\_IO}$	V
		P		4.75 V < $V_{DD\_HV\_IO}$ < 5.25 V				
V_{ILCMOS}(5)	SR	C	Input low level CMOS (without hysteresis)	3.0 V < $V_{DD\_HV\_IO}$ < 3.6 V	–0.3	—	0.4 * $V_{DD\_HV\_IO}$	V
		P		4.75 V < $V_{DD\_HV\_IO}$ < 5.25 V				
$V_{HYSCMOS}$	—	C	Input hysteresis CMOS	3.0 V < $V_{DD\_HV\_IO}$ < 3.6 V	0.1 * $V_{DD\_HV\_IO}$	—	—	V
				4.75 V < $V_{DD\_HV\_IO}$ < 5.25 V(6)				
$V_{DRFTCMOS}$	—	C	Input V_{IL}/V_{IH} temperature drift CMOS	3.0 V < $V_{DD\_HV\_IO}$ < 3.6 V	—	—	100(4)	mV
				4.75 V < $V_{DD\_HV\_IO}$ < 5.25 V				
INPUT CHARACTERISTICS(7)								
I_{LKG}	CC	P	Digital input leakage	4.5 V < V_{DD_HV} < 5.5 V 0.1*V_{DD_HV} < V_{IN} < 0.9*V_{DD_HV} TJ < 150 °C	—	—	1	µA
I_{LKG_MED}	CC	C	Digital input leakage for MEDIUM pad	4.5 V < V_{DD_H}V < 5.5 V V_{SS_HV} < V_{IN} < V_{DD_HV}	—	—	500	nA
C_{IN}	CC	D	Digital input capacitance	GPIO input pins	—	—	10	pF
				Ethernet input pins	—	—	8	

1. A good approximation for the variation of the minimum value with supply is given by formula V_{IHAUT} = 0.69 × $V_{DD\_HV\_IO}$.
2. A good approximation for the variation of the maximum value with supply is given by formula V_{ILAUT} = 0.49 × $V_{DD\_HV\_IO}$.
3. A good approximation of the variation of the minimum value with supply is given by formula V_{HYSAUT} = 0.11 × $V_{DD\_HV\_IO}$.
4. In a 1 ms period, assuming stable voltage and a temperature variation of ±30 °C, V_{IL}/V_{IH} shift is within ±50 mV. For SENT requirement refer to *Note: on page 41*.
5. Only for $V_{DD\_HV\_IO\_JTAG}$ and $V_{DD\_HV\_IO\_FLEX}$ power segment. The TTL threshold are controlled by the VSIO bit. VSIO[VSIO_xx] = 0 in the range 3.0 V < $V_{DD\_HV\_IO}$ < 3.6 V, VSIO[VSIO_xx] = 1 in the range 4.5 V < $V_{DD\_HV\_IO}$ < 5.5 V.
6. Only for $V_{DD\_HV\_IO\_JTAG}$ and $V_{DD\_HV\_IO\_FLEX}$ power segment.
7. For LFAST, microsecond bus and LVDS input characteristics, refer to dedicated communication module chapters.

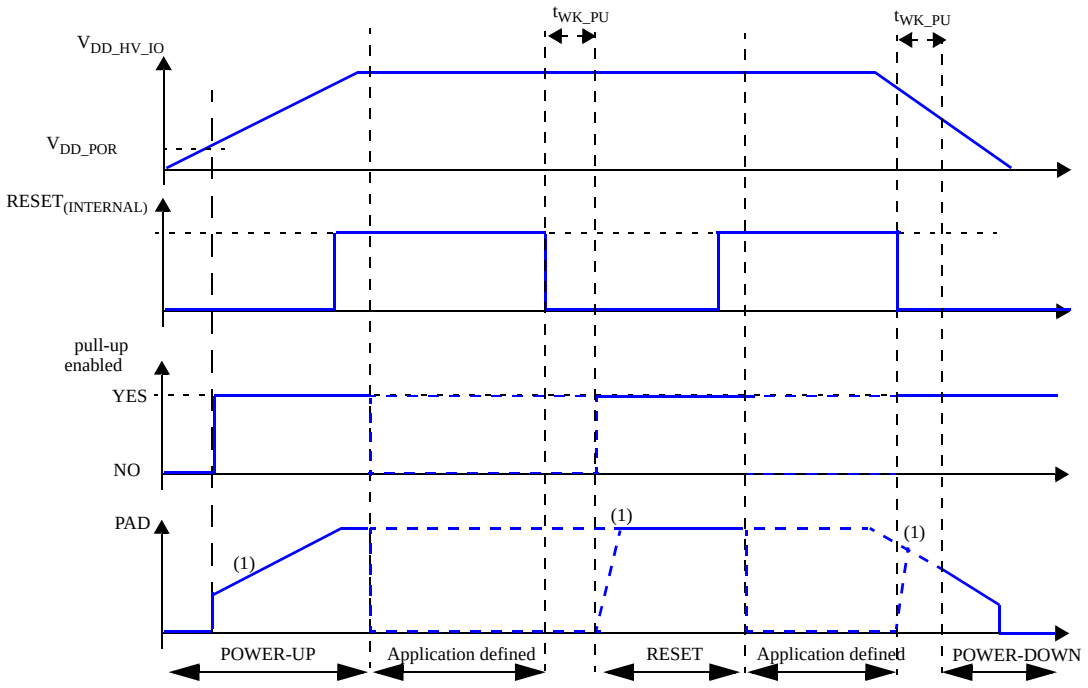
Table 15 provides weak pull figures. Both pull-up and pull-down current specifications are provided.

Table 15. I/O pull-up/pull-down DC electrical characteristics

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
$\|I_{WPU}\|$	CC	T	Weak pull-up current absolute value(1)	V_{IN} = 0 V V_{DD_POR}(2) < $V_{DD\_HV\_IO}$ < 3.0 V(3)(4)	10.6 * V_{DD_HV} – 10.6	—	—	µA
	CC	T		V_{IN} > V_{IL} = 1.1 V (TTL) 4.5 V < $V_{DD\_HV\_IO}$ < 5.5 V	—	—	130	
	CC	P		V_{IN} = 0.69* $V_{DD\_HV\_IO}$ 4.5 V < $V_{DD\_HV\_IO}$ < 5.5 V	23	—	65	
	CC	T		V_{IN} = 0.49* $V_{DD\_HV\_IO}$ 4.5 V < $V_{DD\_HV\_IO}$ < 5.5 V	—	—	82	
R_{WPU}	CC	D	Weak pull-up resistance	0.49* $V_{DD\_HV\_IO}$ < V_{IN} < 0.69* $V_{DD\_HV\_IO}$ 4.5 V < $V_{DD\_HV\_IO}$ < 5.5 V	34	—	62	kΩ
$\|I_{WPD}\|$	CC	T	Weak pull-down current absolute value	V_{IN} < V_{IL} = 0.9 V (TTL) 4.5 V < $V_{DD\_HV\_IO}$ < 5.5 V	16	—	—	µA
		P		V_{IN} = 0.69* $V_{DD\_HV\_IO}$ 4.5 V < $V_{DD\_HV\_IO}$ < 5.5 V	50	—	130	
		T		V_{IN} = 0.49* $V_{DD\_HV\_IO}$ 4.5 V < $V_{DD\_HV\_IO}$ < 5.5 V	40	—	—	
R_{WPD}	CC	D	Weak pull-down resistance	0.49* $V_{DD\_HV\_IO}$ < V_{IN} < 0.69* $V_{DD\_HV\_IO}$ 4.5 V < $V_{DD\_HV\_IO}$ < 5.5 V	30	—	55	kΩ

1. Weak pull-up/down is enabled within t_{WK_PU} = 1 µs after internal/external reset has been asserted. Output voltage will depend on the amount of capacitance connected to the pin.
2. V_{DD_POR} is the minimum $V_{DD\_HV\_IO}$ supply voltage for the activation of the device pull-up/down, and is given in the *Table 21: Reset electrical characteristics* of *Section 3.9: Reset pad (PORST, ESR0) electrical characteristics*.
3. V_{DD_POR} is defined in the *Table 21: Reset electrical characteristics* of *Section 3.9: Reset pad (PORST, ESR0) electrical characteristics*.
4. Weak pull-up behavior during power-up. Operational with $V_{DD\_HV\_IO}$ > V_{DD_POR}.

Figure 6. Weak pull-up electrical characteristics definition

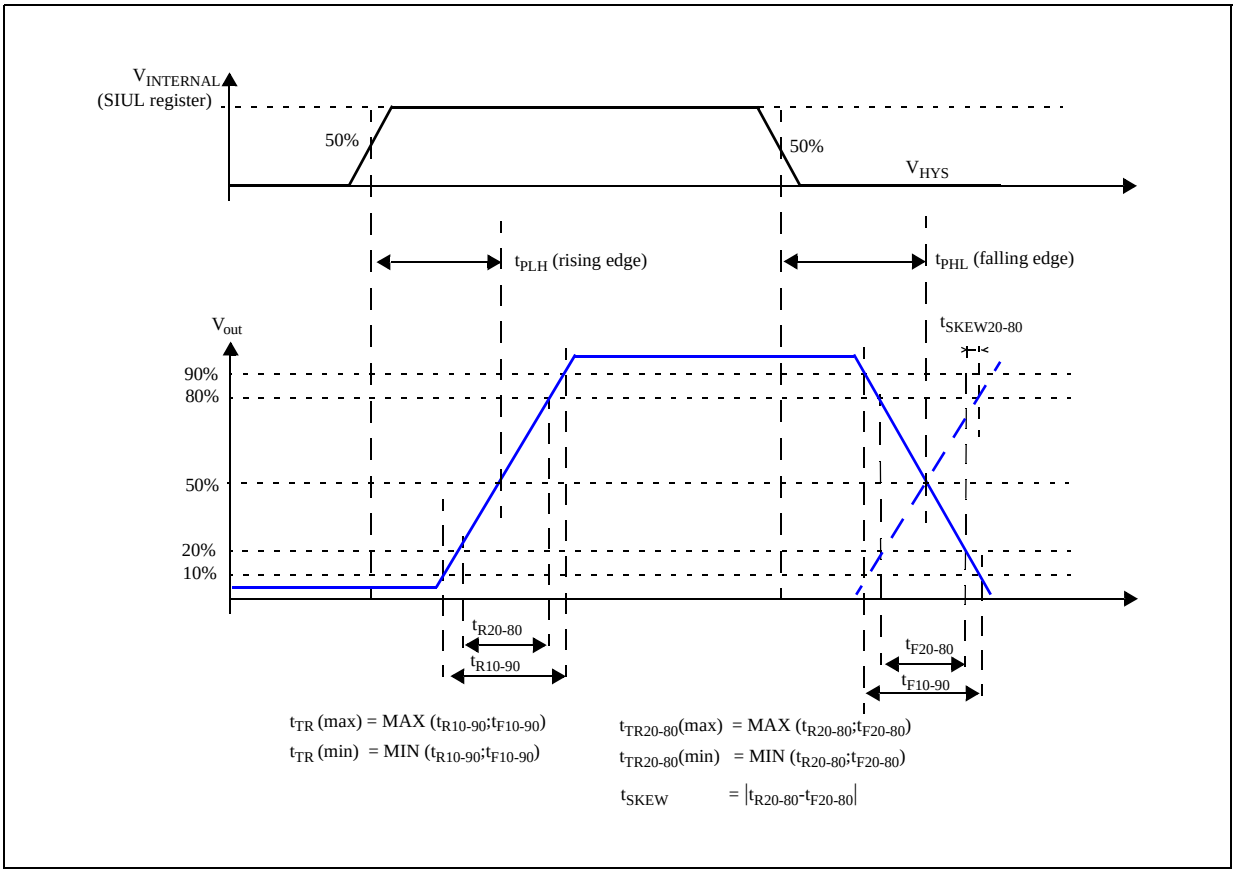


1. Actual PAD slopes will depend on external capacitances and VDD_HV_IO supply.

3.7.2 I/O output DC characteristics

The figure below provides description of output DC electrical characteristics.

Figure 7. I/O output DC electrical characteristics definition



The following tables provide DC characteristics for bidirectional pads:

- *Table 16* provides output driver characteristics for I/O pads when in WEAK configuration.
- *Table 17* provides output driver characteristics for I/O pads when in MEDIUM configuration.
- *Table 18* provides output driver characteristics for I/O pads when in STRONG configuration.
- *Table 19* provides output driver characteristics for I/O pads when in VERY STRONG configuration.

Note: Driver configuration is controlled by SIUL2_MSCRn registers. It is available within two PBRIDGEA_CLK clock cycles after the associated SIUL2_MSCRn bits have been written.

Table 16 shows the WEAK configuration output buffer electrical characteristics.

Table 16. WEAK configuration output buffer electrical characteristics

Symbol		C	Parameter	Conditions[1]	Value[2]			Unit
					Min	Typ	Max	
R_{OH_W}	CC	P	PMOS output impedance weak configuration	4.5 V < $V_{DD\_HV\_IO}$ < 5.5 V Push pull, I_{OH} < 0.5 mA	—	—	1040	Ω
R_{OL_W}	CC	P	NMOS output impedance weak configuration	4.5 V < $V_{DD\_HV\_IO}$ < 5.5 V Push pull, I_{OL} < 0.5 mA	—	—	1040	Ω
f_{MAX_W}	CC	T	Output frequency weak configuration	C_L = 25 pF[3]	—	—	2	MHz
				C_L = 50 pF[3]	—	—	1	
		D		C_L = 200 pF[3]	—	—	0.25	
t_{TR_W}	CC	T	Transition time output pin weak configuration[4]	C_L = 25 pF, 4.5 V < $V_{DD\_HV\_IO}$ < 5.5 V	40	—	120	ns
				C_L = 50 pF, 4.5 V < $V_{DD\_HV\_IO}$ < 5.5 V	80	—	240	
		D		C_L = 200 pF, 4.5 V < $V_{DD\_HV\_IO}$ < 5.5 V	320	—	820	
				C_L = 25 pF, 3.0 V < $V_{DD\_HV\_IO}$ < 3.6 V[5]	50	—	150	
				C_L = 50 pF, 3.0 V < $V_{DD\_HV\_IO}$ < 3.6 V[5]	100	—	300	
				C_L = 200 pF, 3.0 V < $V_{DD\_HV\_IO}$ < 3.6 V[5]	350	—	1050	
$\lvert t_{SKEW\_W} \rvert$	CC	T	Difference between rise and fall time	—	—	—	25	%
I_{DCMAX_W}	CC	D	Maximum DC current	—	—	—	4	mA
$T_{PHL/PLH}$	CC	D	Propagation delay	C_L = 25 pF, 4.5 V < $V_{DD\_HV\_IO}$ < 5.9 V	—	—	120	ns
				C_L = 25 pF, 3.0 V < $V_{DD\_HV\_IO}$ < 3.6 V	—	—	150	
				C_L = 50 pF, 4.5 V < $V_{DD\_HV\_IO}$ < 5.9 V	—	—	240	
				C_L = 50 pF, 3.0 V < $V_{DD\_HV\_IO}$ < 3.6 V[5]	—	—	300	

1. All VDD_HV_IO conditions for 4.5V to 5.5V are valid for VSIO[VSIO_xx] = 1, and all specifications for 3.0V to 3.6V are valid for VSIO[VSIO_xx] = 0
2. All values need to be confirmed during device validation.
3. C_L is the sum of external capacitance. Device and package capacitances (C_{IN}, defined in *Table 14*) are to be added to calculate total signal capacitance ($C_{TOT} = C_L + C_{IN}$).
4. Transition time maximum value is approximated by the following formula:

   0 pF < C_L < 50 pFt_{TR_W}(ns) = 22 ns + C_L(pF) × 4.4 ns/pF

   50 pF < C_L < 200 pFt_{TR_W}(ns) = 50 ns + C_L(pF) × 3.85 ns/pF
5. Only for $V_{DD\_HV\_IO\_JTAG}$ segment when VSIO[VSIO_IJ] = 0 or $V_{DD\_HV\_IO\_FLEX}$ segment when VSIO[VSIO_IF] = 0.

Table 17 shows the MEDIUM configuration output buffer electrical characteristics.

Table 17. MEDIUM configuration output buffer electrical characteristics

Symbol		C	Parameter	Conditions[1]	Value[2]			Unit
					Min	Typ	Max	
R_{OH_M}	CC	P	PMOS output impedance MEDIUM configuration	4.5 V < $V_{DD\_HV\_IO}$ < 5.5 V Push pull, I_{OH} < 2 mA	—	—	270	Ω
R_{OL_M}	CC	P	NMOS output impedance MEDIUM configuration	4.5 V < $V_{DD\_HV\_IO}$ < 5.5 V Push pull, I_{OL} < 2 mA	—	—	270	Ω
f_{MAX_M}	CC	T	Output frequency MEDIUM configuration	C_L = 25 pF[3]	—	—	12	MHz
				C_L = 50 pF[4]	—	—	6	
		D		C_L = 200 pF[4]	—	—	1.5	
t_{TR_M}	CC	T	Transition time output pin MEDIUM configuration[4]	C_L = 25 pF 4.5 V < $V_{DD\_HV\_IO}$ < 5.5 V	10	—	30	ns
				C_L = 50 pF 4.5 V < $V_{DD\_HV\_IO}$ < 5.5 V	20	—	60	
		D		C_L = 200 pF 4.5 V < $V_{DD\_HV\_IO}$ < 5.5 V	60	—	200	
				C_L = 25 pF, 3.0 V < $V_{DD\_HV\_IO}$ < 3.6 V[5]	12	—	42	
				C_L = 50 pF, 3.0 V < $V_{DD\_HV\_IO}$ < 3.6 V[5]	24	—	86	
				C_L = 200 pF, 3.0 V < $V_{DD\_HV\_IO}$ < 3.6 V[5]	70	—	300	
$\lvert t_{SKEW\_M} \rvert$	CC	T	Difference between rise and fall time	—	—	—	25	%
I_{DCMAX_M}	CC	D	Maximum DC current	—	—	—	4	mA
$T_{PHL/PLH}$	CC	D	Propagation delay	C_L = 25 pF, 4.5 V < $V_{DD\_HV\_IO}$ < 5.9 V	—	—	35	ns
				C_L = 25 pF, 3.0 V < $V_{DD\_HV\_IO}$ < 3.6 V	—	—	42	
				C_L = 50 pF, 4.5 V < $V_{DD\_HV\_IO}$ < 5.9 V	—	—	70	
				C_L = 50 pF, 3.0 V < $V_{DD\_HV\_IO}$ < 3.6 V[5]	—	—	85	

1. All VDD_HV_IO conditions for 4.5V to 5.5V are valid for VSIO[VSIO_xx] = 1, and all specifications for 3.0V to 3.6V are valid for VSIO[VSIO_xx] = 0
2. All values need to be confirmed during device validation.
3. C_L is the sum of external capacitance. Device and package capacitances (C_{IN}, defined in *Table 14*) are to be added to calculate total signal capacitance ($C_{TOT} = C_L + C_{IN}$).
4. Transition time maximum value is approximated by the following formula:

   0 pF < C_L < 50 pFt_{TR_M}(ns) = 5.6 ns + C_L(pF) × 1.11 ns/pF

   50 pF < C_L < 200 pFt_{TR_M}(ns) = 13 ns + C_L(pF) × 0.96 ns/pF

5. Only for $V_{DD\_HV\_IO\_JTAG}$ segment when VSIO[VSIO_IJ] = 0 or $V_{DD\_HV\_IO\_FLEX}$ segment when VSIO[VSIO_IF] = 0

Table 18 shows the STRONG configuration output buffer electrical characteristics.

Table 18. STRONG configuration output buffer electrical characteristics

Symbol		C	Parameter	Conditions[1]	Value[2]			Unit
					Min	Typ	Max	
R_{OH_S}	CC	P	PMOS output impedance STRONG configuration	4.5 V < $V_{DD\_HV\_IO}$ < 5.5 V Push pull, I_{OH} < 8 mA	—	—	70	Ω
R_{OL_S}	CC	P	NMOS output impedance STRONG configuration	4.5 V < $V_{DD\_HV\_IO}$ < 5.5 V Push pull, I_{OL} < 8 mA	—	—	70	Ω
f_{MAX_S}	CC	T	Output frequency STRONG configuration	C_L = 25 pF[3]	—	—	40	MHz
				C_L = 50 pF[4]	—	—	20	
				C_L = 200 pF[4]	—	—	5	
t_{TR_S}	CC	T	Transition time output pin STRONG configuration[4]	C_L = 25 pF 4.5 V < $V_{DD\_HV\_IO}$ < 5.5 V	2.5	—	10	ns
				C_L = 50 pF 4.5 V < $V_{DD\_HV\_IO}$ < 5.5 V	3.5	—	16	
				C_L = 200 pF 4.5 V < $V_{DD\_HV\_IO}$ < 5.5 V	13	—	50	
				C_L = 25 pF, 3.0 V < $V_{DD\_HV\_IO}$ < 3.6 V[5]	4	—	15	
				C_L = 50 pF, 3.0 V < $V_{DD\_HV\_IO}$ < 3.6 V[5]	6	—	27	
				C_L = 200 pF, 3.0 V < $V_{DD\_HV\_IO}$ < 3.6 V[5]	20	—	83	
I_{DCMAX_S}	CC	D	Maximum DC current	—	—	—	10	mA
$\|t_{SKEW\_S}\|$	CC	T	Difference between rise and fall time	—	—	—	25	%
$T_{PHL/PLH}$	CC	D	Propagation delay	C_L = 25 pF, 4.5 V < $V_{DD\_HV\_IO}$ < 5.9 V	—	—	12	ns
				C_L = 25 pF, 3.0 V < $V_{DD\_HV\_IO}$ < 3.6 V	—	—	18	
				C_L = 50 pF, 4.5 V < $V_{DD\_HV\_IO}$ < 5.9 V	—	—	20	
				C_L = 50 pF, 3.0 V < $V_{DD\_HV\_IO}$ < 3.6 V[5]	—	—	36	

1. All VDD_HV_IO conditions for 4.5V to 5.5V are valid for VSIO[VSIO_xx] = 1, and all specifications for 3.0V to 3.6V are valid for VSIO[VSIO_xx] = 0
2. All values need to be confirmed during device validation.

3. C_L is the sum of external capacitance. Device and package capacitances (C_{IN}, defined in *Table 14*) are to be added to calculate total signal capacitance ($C_{TOT} = C_L + C_{IN}$).
4. Transition time maximum value is approximated by the following formula: $t_{TR\_S}(ns) = 4.5\ ns + C_L(pF) \times 0.23\ ns/pF$.
5. Only for $V_{DD\_HV\_IO\_JTAG}$ segment when VSIO[VSIO_IJ] = 0 or $V_{DD\_HV\_IO\_FLEX}$ segment when VSIO[VSIO_IF] = 0

Table 19 shows the VERY STRONG configuration output buffer electrical characteristics.

Table 19. VERY STRONG configuration output buffer electrical characteristics(1)

Symbol		C	Parameter	Conditions(2)	Value(3)			Unit
					Min	Typ	Max	
R_{OH_V}	CC	P	PMOS output impedance VERY STRONG configuration	$V_{DD\_HV\_IO}$ = 5.0 V ± 10%, VSIO[VSIO_xx] = 1, I_{OH} = 8 mA	—	—	60	Ω
		C		$V_{DD\_HV\_IO}$ = 3.3 V ± 10%, VSIO[VSIO_xx] = 0, I_{OH} = 7 mA(4)	—	—	85	
R_{OL_V}	CC	P	NMOS output impedance VERY STRONG configuration	$V_{DD\_HV\_IO}$ = 5.0 V ± 10%, VSIO[VSIO_xx] = 1, I_{OL} = 8 mA	—	—	60	Ω
		C		$V_{DD\_HV\_IO}$ = 3.3 V ± 10%, VSIO[VSIO_xx] = 0, I_{OL} = 7 mA(4)	—	—	85	
f_{MAX_V}	CC	T	Output frequency VERY STRONG configuration	$V_{DD\_HV\_IO}$ = 5.0 V ± 10%, VSIO[VSIO_xx] = 1, C_L = 25 pF(5)	—	—	50	MHz
				$V_{DD\_HV\_IO}$ = 3.3 V ± 10%, VSIO[VSIO_xx] = 1, C_L = 15 pF(4),(5)	—	—	50	
t_{TR_V}	CC	T	10–90% threshold transition time output pin VERY STRONG configuration	$V_{DD\_HV\_IO}$ = 5.0 V ± 10%, VSIO[VSIO_xx] = 1, C_L = 25 pF(5)	1	—	5.3	ns
				$V_{DD\_HV\_IO}$ = 5.0 V ± 10%, VSIO[VSIO_xx] = 1, C_L = 50 pF(5)	2.5	—	12	
				$V_{DD\_HV\_IO}$ = 5.0 V ± 10%, VSIO[VSIO_xx] = 1, C_L = 200 pF(5)	11	—	45	
$t_{TR20\text{-}80}$	CC	D	20–80% threshold transition time(6) output pin VERY STRONG configuration	$V_{DD\_HV\_IO}$ = 5.0 V ± 10%, VSIO[VSIO_xx] = 1, C_L = 25 pF(5)	0.8	—	4	ns
				$V_{DD\_HV\_IO}$ = 3.3 V ± 10%, C_L = 15 pF(5)	1	—	5	
t_{TRTTL}	CC	D	TTL threshold transition time(7) for output pin in VERY STRONG configuration	$V_{DD\_HV\_IO}$ = 3.3 V ± 10%, C_L = 25 pF(5)	1	—	5	ns

Table 19. VERY STRONG configuration output buffer electrical characteristics(1)(Continued)

Symbol		C	Parameter	Conditions(2)	Value(3)			Unit
					Min	Typ	Max	
$\Sigma t_{TR20-80}$	CC	D	Sum of transition time 20–80% output pin VERY STRONG configuration(8)	$V_{DD\_HV\_IO}$ = 5.0 V ± 10%, VSIO[VSIO_xx] = 1, C_L = 25 pF	—	—	9	ns
				$V_{DD\_HV\_IO}$ = 3.3 V ± 10%, C_L = 15 pF(5)	—	—	9	
$\lvert t_{SKEW\_V} \rvert$	CC	T	Difference between rise and fall time at 20–80%	$V_{DD\_HV\_IO}$ = 5.0 V ± 10%, VSIO[VSIO_xx] = 1, C_L = 25 pF(5)	0	—	1	ns
$T_{PHL/PLH}$	CC	D	Propagation delay	C_L = 25 pF, 4.5 V < $V_{DD\_HV\_IO}$ < 5.9 V	—	—	9	ns
				C_L = 25 pF, 3.0 V < $V_{DD\_HV\_IO}$ < 3.6 V	—	—	10.5	
				C_L = 50 pF, 4.5 V < $V_{DD\_HV\_IO}$ < 5.9 V	—	—	15	
				C_L = 50 pF, 3.0 V < $V_{DD\_HV\_IO}$ < 3.6 V	—	—	12	
I_{DCMAX_VS}	CC	D	Maximum DC current	—	—	—	10	mA

1. Refer to FlexRay section for parameter dedicated to this interface.
2. All VDD_HV_IO conditions for 4.5V to 5.5V are valid for VSIO[VSIO_xx] = 1, and all specifications for 3.0V to 3.6V are valid for VSIO[VSIO_xx] = 0.
3. All values need to be confirmed during device validation.
4. Only available on the $V_{DD\_HV\_IO\_JTAG}$ and $V_{DD\_HV\_IO\_FLEX}$ segments.
5. C_L is the sum of external capacitance. Add device and package capacitances (C_{IN}, defined in *Table 14: I/O input DC electrical characteristics*) to calculate total signal capacitance ($C_{TOT} = C_L + C_{IN}$).
6. 20–80% transition time as per FlexRay standard.
7. TTL transition time as for Ethernet standard.
8. For specification per Electrical Physical Layer Specification 3.0.1, see the $dCCTxD_{RISE25}$+$dCCTxD_{FALL25}$ (Sum of Rise and Fall time of TxD signal at the output pin) specification in *Table 58: TxD output characteristics* in *Section 3.17.4.2: TxD*.

3.8 I/O pad current specification

The I/O pads are distributed across the I/O supply segment. Each I/O supply segment is associated to a V_{DD}/V_{SS} supply pair.

Table 20 provides I/O consumption figures.

In order to ensure device reliability, the average current of the I/O on a single segment should remain below the I_{AVGSEG} maximum value.

In order to ensure device functionality, the sum of the dynamic and static currents of the I/O on a single segment should remain below the I_{DYNSEG} maximum value.

Pad mapping on each segment can be optimized using the pad usage information provided in the I/O Signal Description table. The sum of all pad usage ratios within a segment should remain below 100%.

Note: In order to maintain the required input thresholds for the SENT interface, the sum of all I/O pad output percent IR drop as defined in the I/O Signal Description table, must be below 50 %. See the I/O Signal Description attachment.

Note: The SPC574Kxx I/O Signal Description and Input Multiplexing Tables are contained in a Microsoft Excel® workbook file attached to this document. Locate the paperclip symbol on the left side of the PDF window, and click it. Double-click on the Excel file to open it and select the I/O Signal Description Table tab.

Table 20. I/O consumption(1)

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
I_{RMS_SEG}	SR	D	Sum of all the DC I/O current within a supply segment	V_{DD} = 5.0 V ± 10%	—	—	80	mA
				V_{DD} = 3.3 V ± 10%	—	—	80	
I_{RMS_W}	CC	D	RMS I/O current for WEAK configuration	C_L = 25 pF, 2 MHz V_{DD} = 5.0 V ± 10%	—	—	1.1	mA
				C_L = 50 pF, 1 MHz V_{DD} = 5.0 V ± 10%	—	—	1.1	
				C_L = 25 pF, 2 MHz V_{DD} = 3.3 V ± 10%	—	—	0.6	
				C_L = 50 pF, 1 MHz V_{DD} = 3.3 V ± 10%	—	—	0.6	
I_{RMS_M}	CC	D	RMS I/O current for MEDIUM configuration	C_L = 25 pF, 12 MHz V_{DD} = 5.0 V ± 10%	—	—	4.7	mA
				C_L = 50 pF, 6 MHz V_{DD} = 5.0 V ± 10%	—	—	4.8	
				C_L = 25 pF, 12 MHz V_{DD} = 3.3 V ± 10%	—	—	2.6	
				C_L = 50 pF, 6 MHz V_{DD} = 3.3 V ± 10%	—	—	2.7	
I_{RMS_S}	CC	D	RMS I/O current for STRONG configuration	C_L = 25 pF, 50 MHz V_{DD} = 5.0 V ± 10%	—	—	19	mA
				C_L = 50 pF, 25 MHz V_{DD} = 5.0 V ± 10%	—	—	19	
				C_L = 25 pF, 50 MHz V_{DD} = 3.3 V ± 10%	—	—	10	
				C_L = 50 pF, 25 MHz V_{DD} = 3.3 V ± 10%	—	—	10	

Table 20. I/O consumption(1)(Continued)

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
I_{RMS_V}	CC	D	RMS I/O current for VERY STRONG configuration	C_L = 25 pF, 50 MHz, V_{DD} = 5.0V +/- 10%	—	—	22	mA
				C_L = 50 pF, 25 MHz, V_{DD} = 5.0V ± 10%	—	—	22	
				C_L = 25 pF, 50 MHz, V_{DD} = 3.3V ± 10%	—	—	11	
				C_L = 25 pF, 25 MHz, V_{DD} = 3.3V ± 10%	—	—	11	
I_{DYN_SEG}	SR	D	Sum of all the dynamic and DC I/O current within a supply segment	V_{DD} = 5.0 V ± 10%	—	—	195	mA
				V_{DD} = 3.3 V ± 10%	—	—	150	
I_{DYN_W}(2)	CC	D	Dynamic I/O current for WEAK configuration	C_L = 25 pF, V_{DD} = 5.0 V ± 10%	—	—	5.0	mA
				C_L = 50 pF, V_{DD} = 5.0 V ± 10%	—	—	5.1	
				C_L = 25 pF, V_{DD} = 3.3 V ± 10%	—	—	2.2	
				C_L = 50 pF, V_{DD} = 3.3 V ± 10%	—	—	2.3	
I_{DYN_M}	CC	D	Dynamic I/O current for MEDIUM configuration	C_L = 25 pF, V_{DD} = 5.0 V ± 10%	—	—	15	mA
				C_L = 50 pF, V_{DD} = 5.0 V ± 10%	—	—	15.5	
				C_L = 25 pF, V_{DD} = 3.3 V ± 10%	—	—	7.0	
				C_L = 50 pF, V_{DD} = 3.3 V ± 10%	—	—	7.1	
I_{DYN_S}	CC	D	Dynamic I/O current for STRONG configuration	C_L = 25 pF, V_{DD} = 5.0 V ± 10%	—	—	50	mA
				C_L = 50 pF, V_{DD} = 5.0 V ± 10%	—	—	55	
				C_L = 25 pF, V_{DD} = 3.3 V ± 10%	—	—	22	
				C_L = 50 pF, V_{DD} = 3.3 V ± 10%	—	—	25	

Table 20. I/O consumption(1)(Continued)

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
I_{DYN_V}	CC	D	Dynamic I/O current for VERY STRONG configuration	C_L = 25 pF, V_{DD} = 5.0 V ± 10%	—	—	60	mA
				C_L = 50 pF, V_{DD} = 5.0 V ± 10%	—	—	64	
				C_L = 25 pF, V_{DD} = 3.3 V ± 10%	—	—	26	
				C_L = 50 pF, V_{DD} = 3.3 V ± 10%	—	—	29	

1. I/O current consumption specifications for the 4.5 V <= $V_{DD\_HV\_IO}$ <= 5.5 V range are valid for VSIO_[VSIO_xx] = 1, and VSIO[VSIO_xx] = 0 for 3.0 V <= $V_{DD\_HV\_IO}$ <= 3.6 V.
2. Stated maximum values represent peak consumption that lasts only a few ns during I/O transition. When possible (timed output) it is recommended to delay transition between pads by few cycles to reduce noise and consumption.

3.9 Reset pad ($\overline{\text{PORST}}$, $\overline{\text{ESR0}}$) electrical characteristics

The device implements a dedicated bidirectional reset pin ($\overline{\text{PORST}}$).

Note: $\overline{PORST}$ pin does not require active control. It is possible to implement an external pull-up to ensure correct reset exit sequence. Recommended value is 4.7 kΩ.

Figure 8. Start-up reset requirements

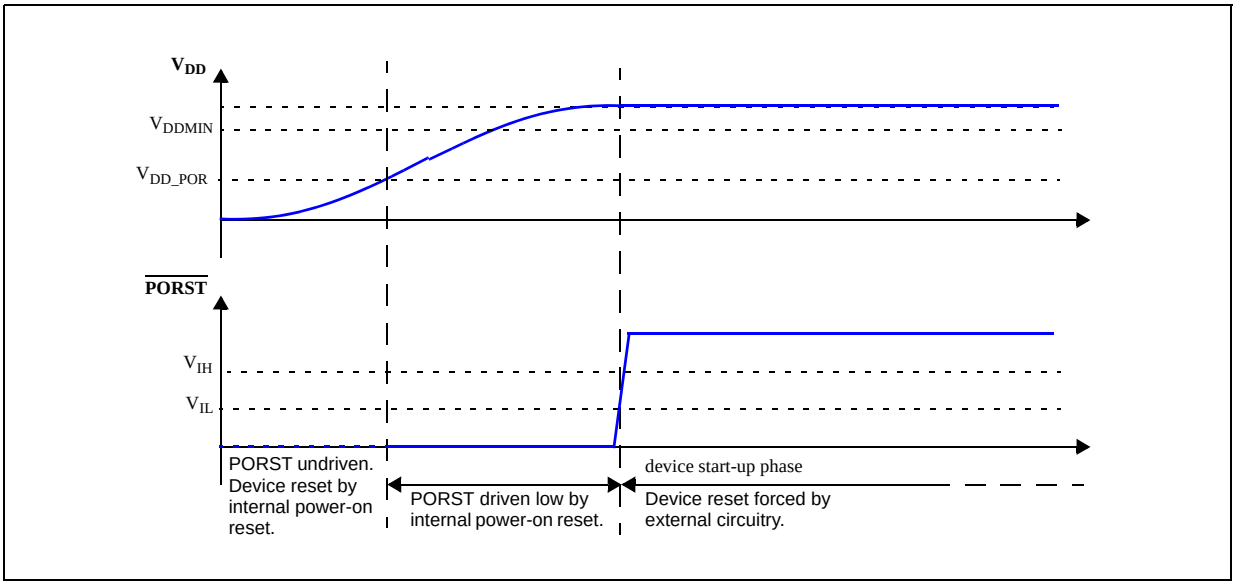


Figure 9 describes device behavior depending on supply signal on $\overline{\text{PORST}}$:

1. $\overline{\text{PORST}}$ low pulse amplitude is too low—it is filtered by input buffer hysteresis. Device remains in current state.
2. $\overline{\text{PORST}}$ low pulse duration is too short—it is filtered by a low pass filter. Device remains in current state.
3. $\overline{\text{PORST}}$ low pulse generates a reset:
   a) $\overline{\text{PORST}}$ low but initially filtered during at least W_{FRST}. Device remains initially in current state.
   b) $\overline{\text{PORST}}$ potentially filtered until W_{NFRST}. Device state is unknown: it may either be reset or remains in current state depending on other factors (temperature, voltage, device).
   c) $\overline{\text{PORST}}$ asserted for longer than W_{NFRST}. Device is under reset.

Figure 9. Noise filtering on reset signal

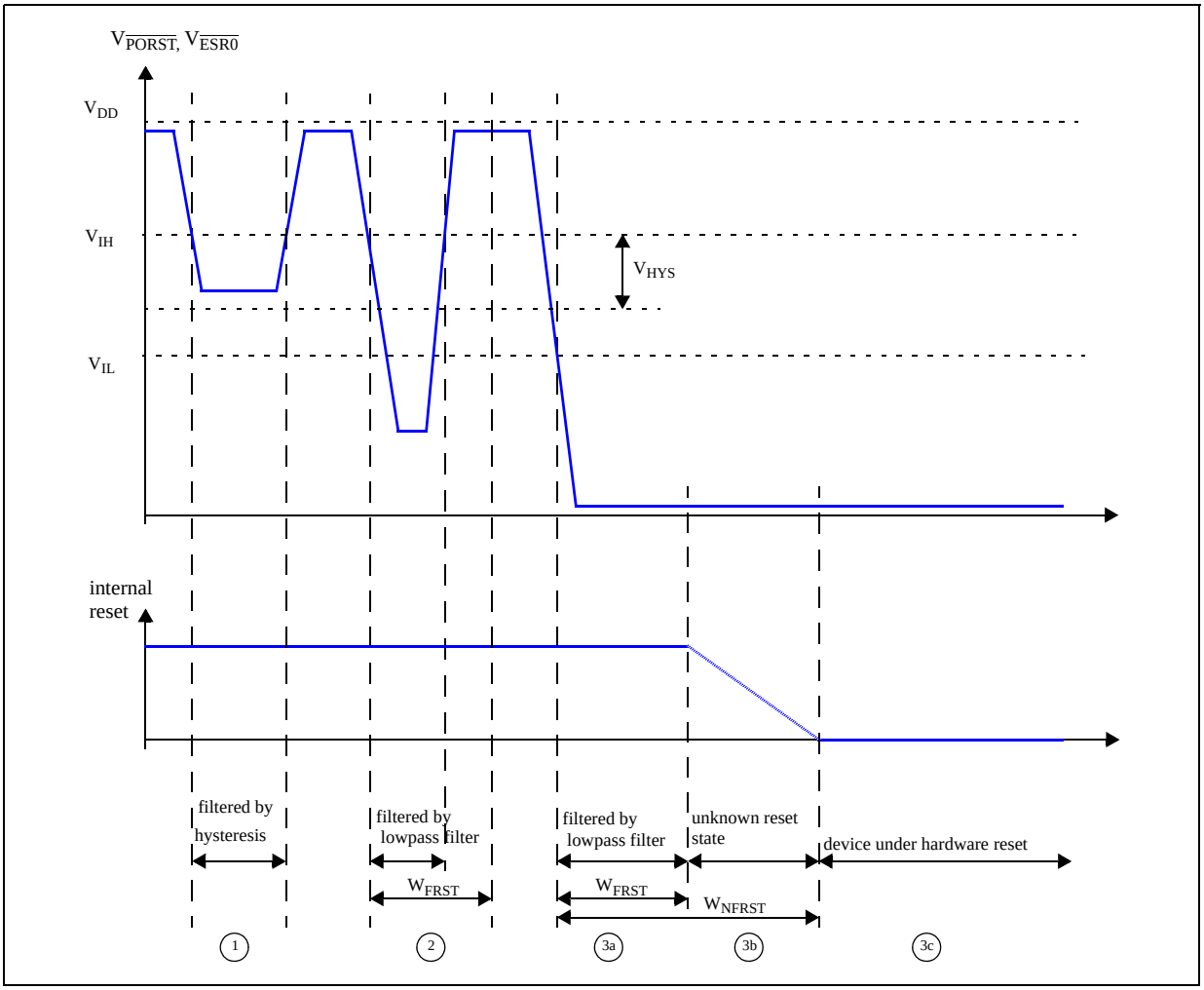


Table 21. Reset electrical characteristics

Symbol			Parameter	Conditions	Value(1)			Unit
					Min	Typ	Max	
V_{IH}	SR	P	Input high level TTL (Schmitt trigger)	—	2.0	—	$V_{DD\_HV\_IO}$ +0.4	V
V_{IL}	SR	P	Input low level TTL (Schmitt trigger)	—	–0.4	—	0.8	V
V_{HYS}	CC	C	Input hysteresis TTL (Schmitt trigger)	—	275	—	—	mV
V_{DD_POR}	CC	D	Minimum supply for strong pull-down activation	—	—	—	1.2	V
I_{OL_R}	CC	P	Strong pull-down current(2)	Device under power-on reset $V_{DD\_HV\_IO} = V_{DD\_POR}$, $V_{OL} = 0.35 * V_{DD\_HV\_IO}$	0.2	—	—	mA
		C		Device under power-on reset 3.0 V < $V_{DD\_HV\_IO}$ < 5.5 V, V_{OL} > 0.9 V	8	—	—	mA
$\lvert I_{WPU} \rvert$	CC	P	Weak pull-up current absolute value	$\overline{ESR0}$ pin $V_{IN} = 0.69 * V_{DD\_HV\_IO}$	23	—	65	µA
		C		$\overline{ESR0}$ pin $V_{IN} = 0.49 * V_{DD\_HV\_IO}$	—	—	82	
$\lvert I_{WPD} \rvert$	CC	P	Weak pull-down current absolute value	$\overline{PORST}$ pin $V_{IN} = 0.69 * V_{DD\_HV\_IO}$	50	—	130	µA
		C		$\overline{PORST}$ pin $V_{IN} = 0.49 * V_{DD\_HV\_IO}$	40	—	—	
W_{FRST}	SR	P	$\overline{PORST}$ and $\overline{ESR0}$ input filtered pulse	—	—	—	500	ns
W_{NFRST}	SR	P	$\overline{PORST}$ and $\overline{ESR0}$ input not filtered pulse	—	2000	—	—	ns
W_{FNMI}	SR	P	ESR1 input filtered pulse	—	—	—	15	ns
W_{NFNMI}	SR	P	ESR1 input not filtered pulse	—	400	—	—	ns

1. An external 4.7 KOhm pull-up resistor is recommended to be used with the PORST and ESR0 pins for fast negation of the signals.
2. I_{OL_R} applies to both PORST and ESR0: Strong pull-down is active on PHASE0 for PORST. Strong pull-down is active on PHASE0, PHASE1, PHASE2, and the beginning of PHASE3 for ESR0.

$\overline{PORST}$ must be connected to an external power-on supply circuitry. Minimum requested circuitry is external pull-up to ensure device can exit reset.

Note: No restrictions exist on reset signal slew rate apart from absolute maximum rating compliance.

3.10 Oscillator and FMPLL

3.10.1 FMPLL

Two frequency-modulated phase-locked loop (FMPLL) modules, the Reference PLL (PLL0) and the System PLL (PLL1) generate the system and auxiliary clocks from the main oscillator driver.

Figure 10. PLL integration

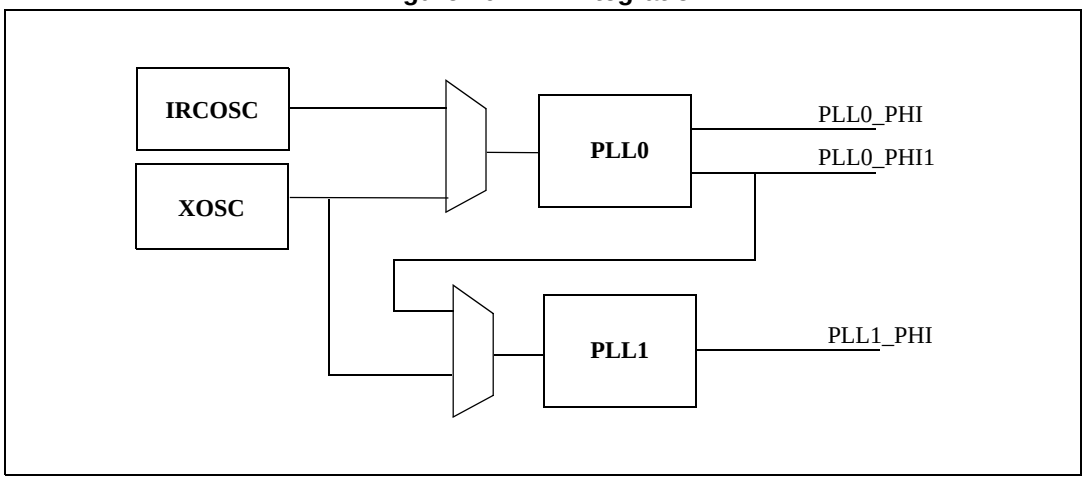


Table 22. PLL0 electrical characteristics

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
f_{PLL0IN}	SR	—	PLL0 input clock[1],[2]	—	8	—	44	MHz
Δ_{PLL0IN}	SR	—	PLL0 input clock duty cycle[1]	—	40	—	60	%
$f_{PLL0VCO}$	CC	P	PLL0 VCO frequency	—	600	—	1250	MHz
$f_{PLL0PHI}$	CC	D	PLL0 clock output frequency on PHI	—	—	—	400	MHz
$f_{PLL0PHI1}$	CC	D	PLL0 clock output frequency on PHI1	—	—	—	78	MHz
$t_{PLL0LOCK}$	CC	P	PLL0 lock time	—	—	—	110	µs
$\lvert\Delta_{PLL0PHI0SPJIT}\rvert$	CC	T	PLL0_PHI0 single period jitter f_{PLL0IN} = 20 MHz (resonator)	$f_{PLL0PHI0}$ = 400 MHz, 6-sigma pk-pk	—	—	200	ps
$\lvert\Delta_{PLL0PHI1SPJIT}\rvert$	CC	T	PLL0_PHI1 single period jitter f_{PLL0IN} = 20 MHz (resonator)	$f_{PLL0PHI1}$ = 40MHz, 6-sigma pk-pk	—	—	300[3]	ps

Table 22. PLL0 electrical characteristics(Continued)

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
$\lvert\Delta_{PLL0LTJIT}\rvert$	CC	T	PLL0 long-term jitter(3) f_{PLL0IN} = 20 MHz (resonator), VCO frequency = 800 MHz	10 periods accumulated jitter (80 MHz equivalent frequency), 6-sigma pk-pk	—	—	± 250	ps
				16 periods accumulated jitter (50 MHz equivalent frequency), 6-sigma pk-pk	—	—	± 300	ps
				long term jitter (< 1 MHz equivalent frequency), 6-sigma pk-pk	—	—	± 500	ps
I_{PLL0}	CC	T	PLL0 consumption	FINE LOCK state	—	—	5	mA
$f_{PLL0FREE}$	CC	D	VCO free running frequency	—	35	—	400	MHz

1. PLL0IN clock retrieved directly from either internal RC oscillator (IRCOSC) or external oscillator (XOSC) clock. Input characteristics are granted when using XOSC.
2. f_{PLL0IN} frequency must be scaled down using PLLDIG_PLL0DV[PREDIV] to ensure PFD input signal is in the range 8 MHz-20 MHz.
3. VDD_LV noise due to application in the range VDD_LV = 1.25 V ± 5%, with frequency below PLL bandwidth (40 KHz) is filtered.

Table 23. PLL1 electrical characteristics

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
f_{PLL1IN}	SR	—	PLL1 input clock(1)	—	38	—	78	MHz
Δ_{PLL1IN}	SR	—	PLL1 input clock duty cycle(1)	—	35	—	65	%
$f_{PLL1VCO}$	CC	P	PLL1 VCO frequency	—	600	—	1250	MHz
$f_{PLL1PHI}$	CC	D	PLL1 output clock frequency on PHI	—	4.762	—	160	MHz
$t_{PLL1LOCK}$	CC	P	PLL1 lock time	—	—	—	100	µs
$f_{PLL1MOD}$	CC	T	PLL1 modulation frequency	—	—	—	250	KHz
$\lvert\delta_{PLL1MOD}\rvert$	CC	T	PLL1 modulation depth (when enabled)	Center spread	0.25	—	2	%
				Down spread	0.5	—	4	%
I_{PLL1}	CC	T	PLL1 consumption	FINE LOCK state	—	—	6	mA
$f_{PLL1FREE}$	CC	D	VCO free running frequency	—	35	—	400	MHz

1. PLL1IN clock retrieved directly from either internal PLL0 or external XOSC clock. Input characteristics are granted when using internal PLL0 or XOSC is used in functional mode.

3.10.2 External oscillator (XOSC)

Table 24. External Oscillator electrical specifications

Symbol		C	Parameter	Conditions		Value		Unit
						Min	Max	
f_{XTAL}	CC	D	Crystal Frequency Range(1)	—		4	8	MHz
				—		>8	20	
				—		>20	40	
t_{cst}	CC	T	Crystal start-up time (2),(3)	T_J = 150 °C		—	5	ms
trec	CC	—	Crystal recovery time(4)	—		—	0.5	ms
V_{IHEXT}	CC	D	EXTAL input high voltage (External Reference)	V_{REF} = 0.28 * $V_{DD\_HV\_IO\_JTAG}$		V_{REF} + 0.6	—	V
V_{ILEXT}	CC	D	EXTAL input low voltage(5)	V_{REF} = 0.28 * $V_{DD\_HV\_IO\_JTAG}$		—	V_{REF} - 0.6	V
C_{S_EXTAL}	CC	T	Total on-chip stray capacitance on EXTAL pin(6)	QFP		6.0	8.0	pF
C_{S_XTAL}	CC	T	Total on-chip stray capacitance on XTAL pin(8)	QFP		6.0	8.0	pF
g_m	CC	P	Oscillator Transconductance	T_J = -40 °C to 150 °C 4.5 V < $V_{DD\_HV\_IO}$ < 5.5 V	$f_{XTAL} \leq$ 8 MHz	2.6	11.0	mA/V
		C			$f_{XTAL} \leq$ 20 MHz	7.9	26.0	
		C			$f_{XTAL} \leq$ 40 MHz	10.4	34.0	
V_{EXTAL}	CC	D	Oscillation Amplitude on the EXTAL pin after startup(7)	T_J = –40 °C to 150 °C		0.5	1.8	V
V_{HYS}	CC	D	Comparator Hysteresis	T_J = 150 °C		0.1	1.0	V
I_{XTAL}	CC	D	XTAL current(8)	T_J = 150 °C		—	14	mA

1. The range is selectable by UTEST miscellaneous DCF clients XOSC_LF_EN and XOSC_EN_40 MHz.
2. This value is determined by the crystal manufacturer and board design.
3. Proper PC board layout procedures must be followed to achieve specifications.
4. Crystal recovery time is the time for the oscillator to settle to the correct frequency after adjustment of the integrated load capacitor value.
5. Applies to an external clock input and not to crystal mode.
6. See crystal manufacturer's specification for recommended load capacitor (C_L) values.The external oscillator requires external load capacitors when operating from 8 MHz to 16 MHz. Account for on-chip stray capacitance (C_{S_EXTAL}/C_{S_XTAL}) and PCB capacitance when selecting a load capacitor value. When operating at 20 MHz/40 MHz, the integrated load capacitor value is selected via S/W to match the crystal manufacturer's specification, while accounting for on-chip and PCB capacitance.
7. Amplitude on the EXTAL pin after startup is determined by the ALC block, i.e., the Automatic Level Control Circuit. The function of the ALC is to provide high drive current during oscillator startup, but reduce current after oscillation in order to reduce power, distortion, and RFI, and to avoid over-driving the crystal. The operating point of the ALC is dependent on the crystal value and loading conditions.
8. I_{XTAL} is the oscillator bias current out of the XTAL pin with both EXTAL and XTAL pins grounded. This is the maximum current during startup of the oscillator. The current after oscillation is typically in the 2-3 mA range and is dependent on the load and series resistance of the crystal. Test circuit is shown in *Figure 12*. The ALC block is the Automatic Level Control Circuit. The function of the ALC is to provide high drive current during oscillator startup, but reduce current after oscillation in order to reduce power, distortion, and RFI, and to avoid overdriving the crystal.

Figure 11. Crystal/Resonator Connections

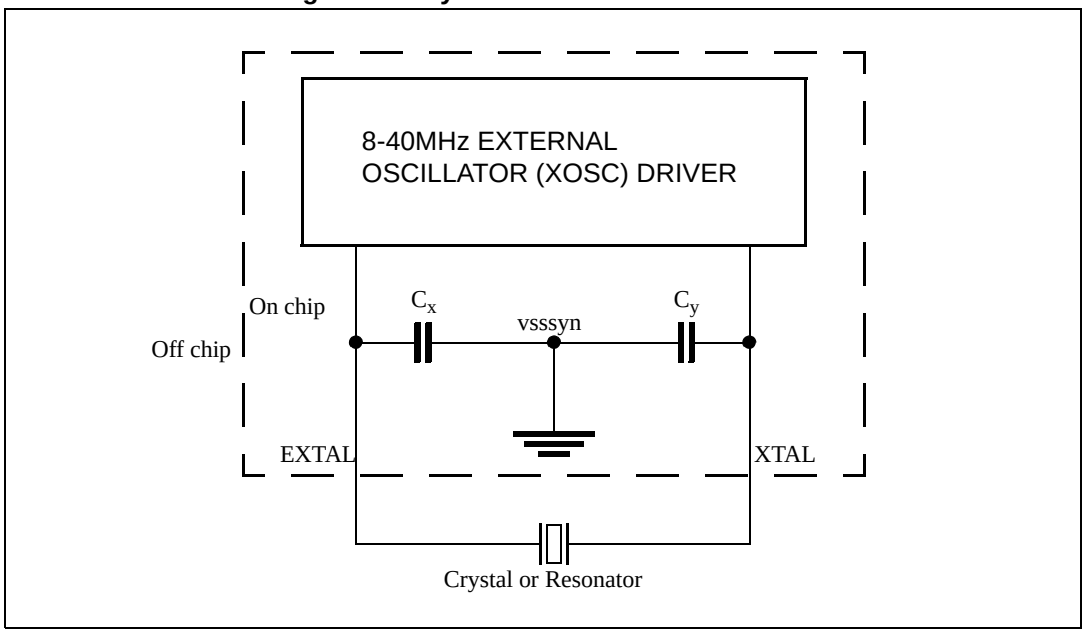


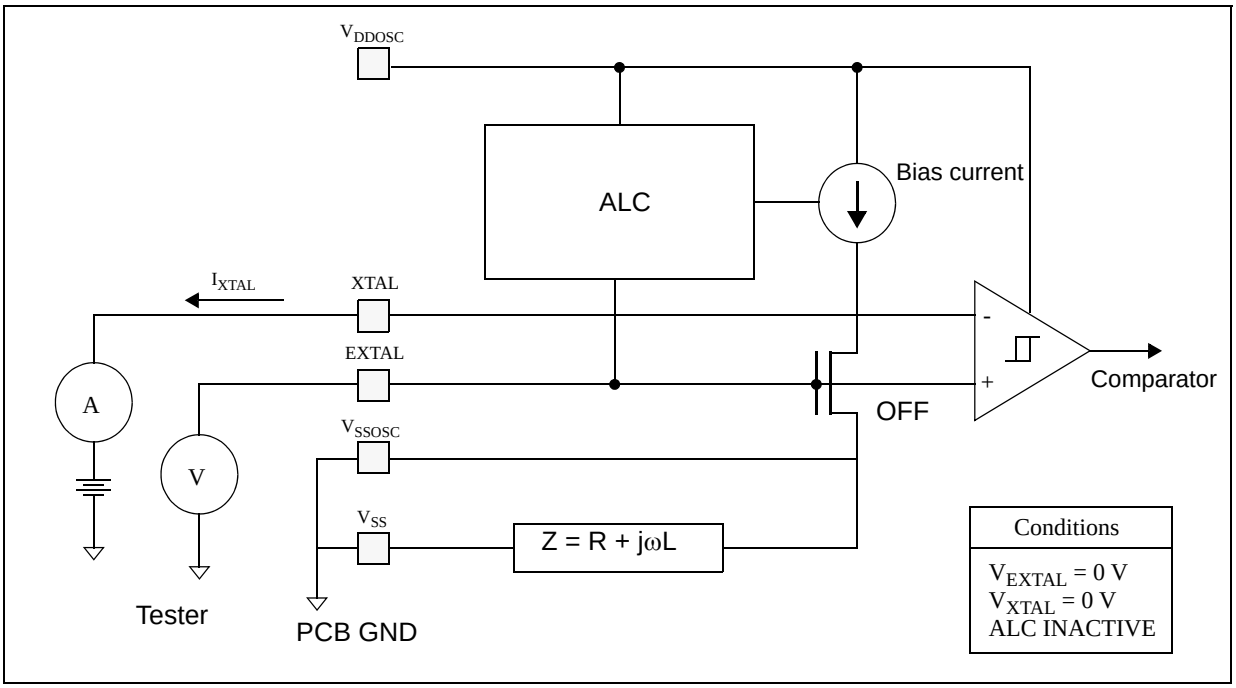
Table 25. Selectable load capacitance

load_cap_sel[4:0] from DCF record	Capacitance offered on EXTAL/XTAL (Cx and Cy)(1),(2) (pF)
00000	1.0
00001	2.0
00010	2.9
00011	3.8
00100	4.8
00101	5.7
00110	6.6
00111	7.5
01000	8.5
01001	9.4
01010	10.3
01011	11.2
01100	12.2
01101	13.1
01110	14.0
01111	15.0
10000–11111(3)	Reserved

1. Values are determined from simulation across process corners and voltage and temperature variation. Capacitance values vary ±12% across process, 0.25% across voltage, and no variation across temperature.

2. Values in this table do not include the die and package capacitances given by Cs_xtal/Cs_extal in *Table 24 (External Oscillator electrical specifications)*.
3. Configurations 10000–11111 should not be used. Configurations 10000–11100 result in same capacitances of configurations 00011–01111. Configurations 11101, 11110, and 11111 select maximum capacitances.

Figure 12. Test circuit



3.10.3 Internal oscillator (IRCOSC)

Table 26. Internal RC oscillator electrical specifications

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
f_{Target}	CC	D	IRCOSC target frequency	—	—	16	—	MHz
δf_{var_noT}	CC	P	IRC frequency variation without temperature compensation	T_J < 150 °C	–8	—	+8	%
δf_{var_T}	CC	T	IRC frequency variation with temperature compensation	T_J < 150 °C	–1.5	—	+1.5	%
δf_{var_SW}	—	T	IRC frequency accuracy after software trimming accuracy(1)	Trimming temperature	–0.5	—	+0.5	%
t_{start_noT}	CC	T	Startup time to reach within f_{var_noT}	Factory trimming already applied	—	—	5	µs
t_{start_T}	CC	T	Startup time to reach within f_{var_T}	Factory trimming already applied	—	—	120	µs

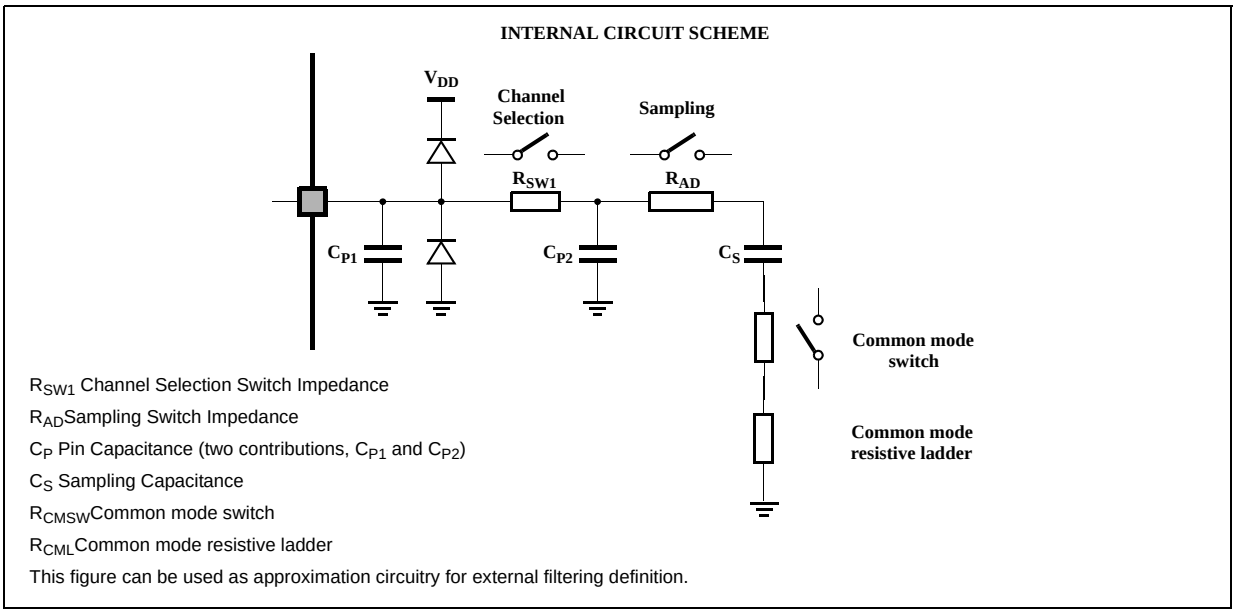
1. The typical user trim step size δf_{TRIM} = 0.35 %.

3.11 ADC specifications

3.11.1 ADC input description

Figure 13 shows the input equivalent circuit for fast SARn channels.

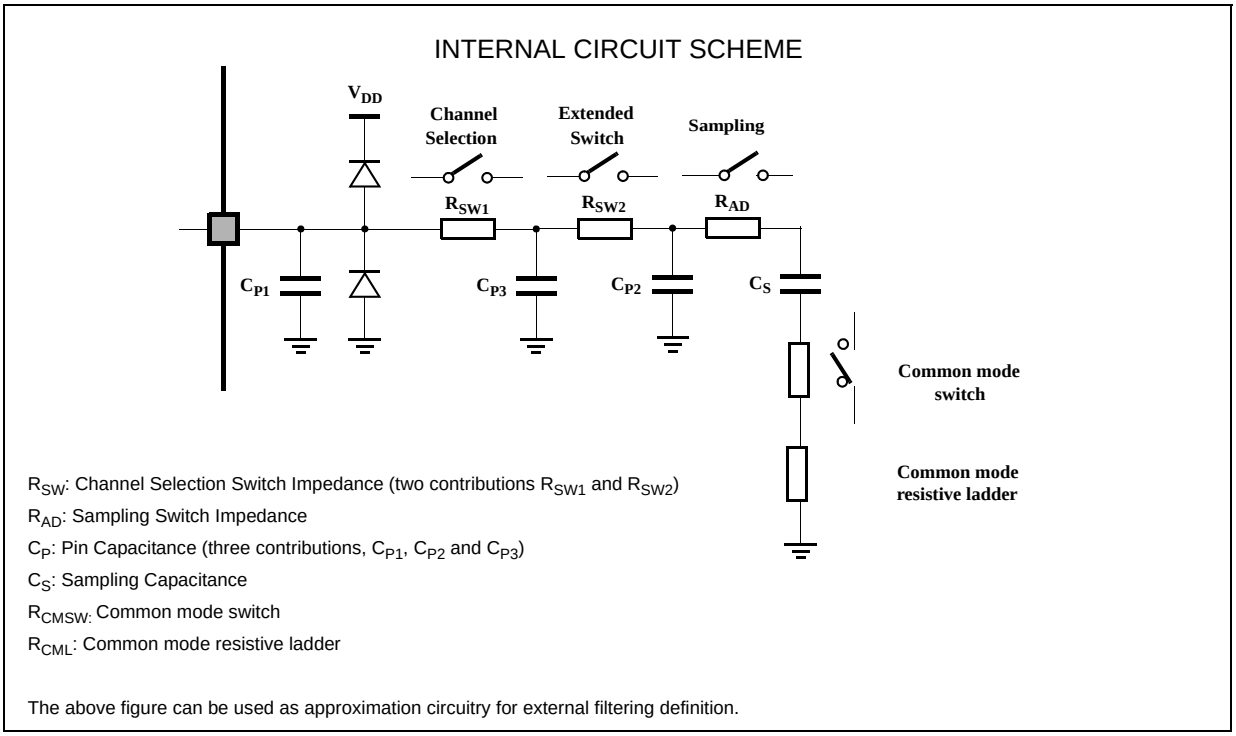
Figure 13. Input equivalent circuit (Fast SARn channels)



R_{SW1} Channel Selection Switch Impedance
R_{AD}Sampling Switch Impedance
C_P Pin Capacitance (two contributions, C_{P1} and C_{P2})
C_S Sampling Capacitance
R_{CMSW}Common mode switch
R_{CML}Common mode resistive ladder
This figure can be used as approximation circuitry for external filtering definition.

Figure 14 shows the input equivalent circuit for SARB channels.

Figure 14. Input equivalent circuit (SARB channels)



R_{SW}: Channel Selection Switch Impedance (two contributions R_{SW1} and R_{SW2})
R_{AD}: Sampling Switch Impedance
C_P: Pin Capacitance (three contributions, C_{P1}, C_{P2} and C_{P3})
C_S: Sampling Capacitance
R_{CMSW}: Common mode switch
R_{CML}: Common mode resistive ladder

The above figure can be used as approximation circuitry for external filtering definition.

Table 27. ADC pin specification(1)

Symbol		C	Parameter	Conditions	Value		Unit
					Min	Max	
I_{LK_INUD}	CC	C	Input leakage current, two ADC channels input with weak pull-up and weak pull-down	T_J < 40 °C, no current injection on adjacent pin	—	70	nA
		C		T_J < 150 °C, no current injection on adjacent pin	—	220	
I_{LK_INUSD}	CC	C	Input leakage current, two ADC channels input with weak pull-up and strong pull-down	T_J < 40 °C, no current injection on adjacent pin	—	80	nA
		C		T_J < 150 °C, no current injection on adjacent pin	—	250	
I_{LK_INREF}	CC	C	Input leakage current, two ADC channels input with weak pull-up and weak pull-down and alternate reference	T_J < 40 °C, no current injection on adjacent pin	—	160	nA
		C		T_J < 150 °C, no current injection on adjacent pin	—	400	
I_{LK_INOUT}	CC	C	Input leakage current, two ADC channels input, GPIO output buffer with weak pull-up and weak pull-down	T_J < 40 °C, no current injection on adjacent pin	—	140	nA
		C		T_J < 150 °C, no current injection on adjacent pin	—	380	
I_{INJ}	CC	T	Injection current on analog input preserving functionality	Applies to any analog pins	–3	3	mA
C_{HV_ADC}	SR	D	$V_{DD\_HV\_ADV}$ external capacitance(2)	—	1	2.2	µF
C_{P1}	CC	D	Pad capacitance	—	0	10	pF
C_{P2}	CC	D	Internal routing capacitance	SARn channels	0	0.5	pF
		D		SARB channels	0	1	
C_{P3}	CC	D	Internal routing capacitance	Only for SARB channels	0	1	pF
C_S	CC	D	SAR ADC sampling capacitance	—	6	8.5	pF
R_{SWn}	CC	D	Analog switches resistance	SARn channels	0	1.1	kΩ
		D		SARB channels	0	1.7	
R_{AD}	CC	D	ADC input analog switches resistance	—	0	0.6	kΩ
R_{CMSW}	CC	D	Common mode switch resistance	—	0	2.6	kΩ
R_{CMRL}	CC	D	Common mode resistive ladder	—	0	3.5	kΩ
R_{SAFEPD}(3)	CC	D	Discharge resistance for AN7/AN35 channels (strong pull-down for safety)	—	0	300	Ω
ΣI_{ADV}	CC	P	ADC pin supply consumption	All SAR and S/D ADC associated to the pin are enabled	—	31	mA
		T		Static consumption (Power-down mode)	—	1	

1. All specifications in this table valid for the full input voltage range for the analog inputs.

2. For noise filtering, add a high frequency bypass capacitance of 0.1 µF between $V_{DD\_HV\_ADV}$ and $V_{SS\_HV\_ADV}$.
3. Safety pull-down is available for port pin PB[5] and PE[14].

3.11.2 SAR ADC electrical specification

The SARn ADCs are 12-bit Successive Approximation Register analog-to-digital converters with full capacitive DAC. The SARn architecture allows input channel multiplexing.

Table 28. SARn ADC electrical specification(1)

Symbol		C	Parameter	Conditions	Value		Unit
					Min	Max	
V_{ALTREF}	SR	C	ADC alternate reference voltage	$V_{ALTREF} < V_{DD\_HV\_IO\_MAIN}$ $V_{ALTREF} < V_{DD\_HV\_ADV}$	4.5	5.5	V
		C			4.0	5.9	
		P		Extended range with reduce TUE $V_{ALTREF} < V_{DD\_HV\_IO\_MAIN}$ $V_{ALTREF} < V_{DD\_HV\_ADV}$	2.0	5.9	
V_{IN}	SR	D	ADC input signal	$0 < V_{IN} < V_{DD\_HV\_IO\_MAIN}$	$V_{SS\_HV\_ADR}$	$V_{DD\_HV\_ADR}$	V
f_{ADCK}	SR	P	Clock frequency	$T_J < 150$ °C	7.5	14.6	MHz
$t_{ADCPRECH}$	SR	T	ADC precharge time	Fast SAR—fast precharge	135	—	ns
				Fast SAR—full precharge	270	—	
				Slow SAR (SARADC_B)—fast precharge	270	—	
				Slow SAR (SARADC_B)—full precharge	540	—	
ΔV_{PRECH}	SR	D	ADC Precharge voltage	Full precharge $V_{PRECH} = V_{DD\_HV\_ADR}/2$ $T_J < 150$ °C	–0.25	0.25	V
		D		Fast precharge $V_{PRECH} = V_{DD\_HV\_ADR}/2$ $T_J < 150$ °C	–0.5	0.5	V
ΔV_{INTREF}	CC	P	Internal reference voltage precision	Applies to all internal reference points ($V_{SS\_HV\_ADR}$, 1/3 * $V_{DD\_HV\_ADR}$, 2/3 * $V_{DD\_HV\_ADR}$, $V_{DD\_HV\_ADR}$)	–0.20	0.20	V
$t_{ADCSAMPLE}$	SR	P	ADC sample time(2)	Fast SAR – 12-bit configuration	0.750	—	µs
		P		Slow SAR (SARADC_B) – 12-bit configuration	1.500	—	
$t_{ADCEVAL}$	SR	P	ADC evaluation time	12-bit configuration (25 clock cycles)	1.712	—	µs

Table 28. SARn ADC electrical specification(1)(Continued)

Symbol		C	Parameter	Conditions	Value		Unit
					Min	Max	
I_{ADCSAR_REFH}(3),(4)	CC	T	ADC high reference current	Dynamic consumption (t_{conv} = 5 µs(5))	—	3.5(6)	µA
				Dynamic consumption (t_{conv} = 2.5 µs6)	—	7	
				Static consumption (Power Down mode)	—	4	
				Bias Current(7)	—	+2	
I_{ADCSAR_REFL}(4)	CC	D	ADC low reference current	Run mode $t_{conv} \geq$ 5 µs $V_{DD\_HV\_ADR}$ <= 5.5 V	—	15	µA
				Run mode t_{conv} = 2.5 µs $V_{DD\_HV\_ADR}$ <= 5.5 V	—	30	
				Power Down mode $V_{DD\_HV\_ADR}$ <= 5.5 V	—	1	
I_{ADV_S}	CC	T	$V_{DD\_HV\_ADV}$ power supply current (each ADC)	Dynamic consumption (t_{conv} = 5 µs)	—	4.0	mA
				Dynamic consumption (t_{conv} = 2.5 µs)	—	4.0	
TUE_{12}	CC	T(8)	Total unadjusted error in 12-bit configuration(9)	T_J < 150 °C, $V_{DD\_HV\_ADV}$ > 4 V, $V_{DD\_HV\_ADR}$ > 4 V	–4	4	LSB (12b)
		P		T_J < 150 °C, $V_{DD\_HV\_ADV}$ > 4 V, $V_{DD\_HV\_ADR}$ > 4 V	–6	6	
		T		T_J < 150 °C, $V_{DD\_HV\_ADV}$ > 4 V, 4 V > $V_{DD\_HV\_ADR}$ > 2 V	–6	6	
		T		T_J < 150 °C, 4 V > $V_{DD\_HV\_ADV}$ > 3.5 V	–12	12	
TUE_{10}	CC	C	Total unadjusted error in 10-bit configuration	T_J < 150 °C, $V_{DD\_HV\_ADV}$ > 4 V $V_{DD\_HV\_ADR}$ > 4 V	–1.5	1.5	LSB (10b)
		C		T_J < 150 °C, $V_{DD\_HV\_ADV}$ > 4 V, 4 V > $V_{DD\_HV\_ADR}$ > 2 V	–2.0	2.0	

Table 28. SARn ADC electrical specification(1)(Continued)

Symbol		C	Parameter	Conditions	Value		Unit
					Min	Max	
ΔTUE_{12}	CC	D	TUE degradation due to $V_{DD\_HV\_ADR}$ offset with respect to $V_{DD\_HV\_ADV}$	$V_{IN} < V_{DD\_HV\_ADV}$ $V_{DD\_HV\_ADR} - V_{DD\_HV\_ADV} \in$ [0:25 mV]	0	0	LSB (12b)
		D		$V_{IN} < V_{DD\_HV\_ADV}$ $V_{DD\_HV\_ADR} - V_{DD\_HV\_ADV} \in$ [25:50 mV]	–2	2	
		D		$V_{IN} < V_{DD\_HV\_ADV}$ $V_{DD\_HV\_ADR} - V_{DD\_HV\_ADV} \in$ [50:75 mV]	–4	4	
		D		$V_{IN} < V_{DD\_HV\_ADV}$ $V_{DD\_HV\_ADR} - V_{DD\_HV\_ADV} \in$ [75:100 mV]	–6	6	
		D		$V_{DD\_HV\_ADV} < V_{IN} <$ $V_{DD\_HV\_ADR}$ $V_{DD\_HV\_ADR} - V_{DD\_HV\_ADV} \in$ [0:25 mV]	–2.5	2.5	
		D		$V_{DD\_HV\_ADV} < V_{IN} <$ $V_{DD\_HV\_ADR}$ $V_{DD\_HV\_ADR} - V_{DD\_HV\_ADV} \in$ [25:50 mV]	–4	4	
		D		$V_{DD\_HV\_ADV} < V_{IN} <$ $V_{DD\_HV\_ADR}$ $V_{DD\_HV\_ADR} - V_{DD\_HV\_ADV} \in$ [50:75 mV]	–7	7	
		D		$V_{DD\_HV\_ADV} < V_{IN} <$ $V_{DD\_HV\_ADR}$ $V_{DD\_HV\_ADR} - V_{DD\_HV\_ADV} \in$ [75:100 mV]	–12	12	

Table 28. SARn ADC electrical specification[1](Continued)

Symbol		C	Parameter	Conditions	Value		Unit
					Min	Max	
ΔTUE_{10}	CC	D	TUE degradation due to $V_{DD\_HV\_ADR}$ offset with respect to $V_{DD\_HV\_ADV}$	$V_{IN} < V_{DD\_HV\_ADV}$ $V_{DD\_HV\_ADR} - V_{DD\_HV\_ADV} \in$ [0:25 mV]	0	0	LSB (10b)
		D		$V_{IN} < V_{DD\_HV\_ADV}$ $V_{DD\_HV\_ADR} - V_{DD\_HV\_ADV} \in$ [25:50 mV]	–0.5	0.5	
		D		$V_{IN} < V_{DD\_HV\_ADV}$ $V_{DD\_HV\_ADR} - V_{DD\_HV\_ADV} \in$ [50:75 mV]	–1	1	
		D		$V_{IN} < V_{DD\_HV\_ADV}$ $V_{DD\_HV\_ADR} - V_{DD\_HV\_ADV} \in$ [75:100 mV]	–1.5	1.5	
		D		$V_{DD\_HV\_ADV} < V_{IN} <$ $V_{DD\_HV\_ADR}$ $V_{DD\_HV\_ADR} - V_{DD\_HV\_ADV} \in$ [0:25 mV]	–1	1	
		D		$V_{DD\_HV\_ADV} < V_{IN} <$ $V_{DD\_HV\_ADR}$ $V_{DD\_HV\_ADR} - V_{DD\_HV\_ADV} \in$ [25:50 mV]	–1	1	
		D		$V_{DD\_HV\_ADV} < V_{IN} <$ $V_{DD\_HV\_ADR}$ $V_{DD\_HV\_ADR} - V_{DD\_HV\_ADV} \in$ [50:75 mV]	–2	2	
		D		$V_{DD\_HV\_ADV} < V_{IN} <$ $V_{DD\_HV\_ADR}$ $V_{DD\_HV\_ADR} - V_{DD\_HV\_ADV} \in$ [75:100 mV]	–3	3	
DNL	CC	P	Differential non-linearity	$V_{DD\_HV\_ADV} > 4$ V $V_{DD\_HV\_ADR} > 4$ V	–1	2	LSB (12b)
ΣI_{ADR_S}	CC	P	ADC pin reference consumption (single pin)[10]	All SAR ADC associated to the pin enabled (t_{conv} = 5 µs)	—	30	µA

1. Functional operating conditions are given in the DC electrical specifications. Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond the listed maxima may affect device reliability or cause permanent damage to the device.
2. Minimum ADC sample times are dependent on adequate charge transfer from the external driving circuit to the internal sample capacitor. The time constant of the entire circuit must allow the sampling capacitor to charge within 1/2 LSB within the sampling window. Please refer to *Figure 13* and *Figure 14* for models of the internal ADC circuit, and the values to use in external RC sizing and calculating the sampling window duration.
3. I_{ADCSAR_REFH} and I_{ADCSAR_REFL} are independent from ADC clock frequency. It depends on conversion rate: consumption is driven by the transfer of charge between internal capacitances during the conversion.
4. Current parameter values are for a single ADC.
5. Total consumption is given by the sum for all ADCs (associated to the reference pin) of their dynamic consumption and their static consumption.
6. I_{ADCSAR_REFH} typical consumption 60 % of maximum value.

7. Extra bias current is present only when BIAS is selected.
8. Extended bench validation performed on 3 samples for each process corner.
9. This parameter is guaranteed by bench validation with a small sample of typical devices, and tested in production to ± 6 LSB.
10. Consumption is given after power-up, when steady state is reached. Extra consumption up to 2 mA may be required during internal circuitry set-up.

3.11.3 S/D ADC electrical specification

The SDn ADCs are Sigma Delta 16-bit analog-to-digital converters with 333 Ksps maximum output rate.

Table 29. SDn ADC electrical specification(1)

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
V_{IN}	SR	P	ADC input signal	—	0	—	$V_{DD\_HV\_ADV}$	V
V_{IN_PK2PK}(2)	SR	D	Input range peak to peak $V_{IN\_PK2PK} = V_{INP}$(3) $- V_{INM}$	Single ended $V_{INM} = V_{SS\_HV\_ADR}$	$V_{DD\_HV\_ADR}$/GAIN			V
		D		Single ended $V_{INM} = 0.5*V_{DD\_HV\_ADR}$ GAIN = 1	$\pm 0.5*V_{DD\_HV\_ADR}$			
		D		Single ended $V_{INM} = 0.5*V_{DD\_HV\_ADR}$ GAIN = 2,4,8,16	$\pm V_{DD\_HV\_ADR}$/GAIN			
		D		Differential, $0 < V_{IN} < V_{DD\_HV\_IO\_MAIN}$	$\pm V_{DD\_HV\_ADR}$/GAIN			
f_{ADCD_M}	SR	P	S/D modulator Input Clock	—	4	14.4	16	MHz
BW_{IN}	SR	D	Input bandwith	SNR = 80 dB f_{ADCD_S} = 150 kHz	0.01	—	50(4)	KHz
		D		SNR = 74 dB f_{ADCD_S} = 333 kHz	0.01	—	111(4)	
f_{ADCD_S}	SR	D	Output conversion rate	$T_J < 150$ °C	—	—	333	ksps
—	CC	D	Oversampling ratio	Internal modulator	24	—	256	—
				External modulator	—	—	256	—
RESOLUTION	CC	D	S/D register resolution(5)	2's complement notation	16			bit
GAIN	SR	D	ADC gain	Defined via ADC_SD[PGA] register. Only integer powers of 2 are valid gain values.	1	—	16	—

Table 29. SDn ADC electrical specification(1)(Continued)

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
$\lvert\delta_{GAIN}\rvert$	CC	C	Absolute value of the ADC gain error(6),(7)	Before calibration (applies to gain setting = 1)	—	—	1.5	%
		D		After calibration, $\Delta V_{DD\_HV\_ADR} < 5\%$ $\Delta V_{DD\_HV\_ADV} < 10\%$ $\Delta T_J < 50$ °C	—	—	5	mV
				After calibration, $\Delta V_{DD\_HV\_ADR} < 5\%$ $\Delta V_{DD\_HV\_ADV} < 10\%$ $\Delta T_J < 100$ °C	—	—	7.5	
				After calibration, $\Delta V_{DD\_HV\_ADR} < 5\%$ $\Delta V_{DD\_HV\_ADV} < 10\%$ $\Delta T_J < 150$ °C	—	—	10	
V_{OFFSET}	CC	P	Input Referred Offset Error(6),(7),(8)	Before calibration (applies to all gain settings – 1, 2, 4, 8, 16)	—	10* (1+1/gain)	20	mV
		D		After calibration, $\Delta V_{DD\_HV\_ADR} < 10\%$ $\Delta T_J < 50$ °C	—	—	5	
				After calibration, $\Delta V_{DD\_HV\_ADV} < 10\%$ $\Delta T_J < 100$ °C			7.5	
				After calibration, $\Delta V_{DD\_HV\_ADV} < 10\%$ $\Delta T_J < 150$ °C	0.5		10	

Table 29. SDn ADC electrical specification(1)(Continued)

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
$SNR_{DIFF150}$(9)	CC	T	Signal to noise ratio in differential mode 150 ksps output rate	$4.5 < V_{DD\_HV\_ADV} < 5.5$(10),(11) $V_{DD\_HV\_ADR} = V_{DD\_HV\_ADV}$ GAIN = 1 $T_J < 150$ °C	80	—	—	dBFS
		T		$4.5 < V_{DD\_HV\_ADV} < 5.5$(10),(11), $V_{DD\_HV\_ADR} = V_{DD\_HV\_ADV}$ GAIN = 2 $T_J < 150$ °C	77	—	—	
		T		$4.5 < V_{DD\_HV\_ADV} < 5.5$(10),(11), $V_{DD\_HV\_ADR} = V_{DD\_HV\_ADV}$ GAIN = 4 $T_J < 150$ °C	74	—	—	
		T		$4.5 < V_{DD\_HV\_ADV} < 5.5$(10),(11) $V_{DD\_HV\_ADR} = V_{DD\_HV\_ADV}$ GAIN = 8 $T_J < 150$ °C	71	—	—	
		D		$4.5 < V_{DD\_HV\_ADV} < 5.5$(10),(11) $V_{DD\_HV\_ADR} = V_{DD\_HV\_ADV}$ GAIN = 16 $T_J < 150$ °C	68	—	—	
$SNR_{DIFF333}$ (12)	CC	T	Signal to noise ratio in differential mode 333 ksps output rate	$4.5 < V_{DD\_HV\_ADV} < 5.5$(10),(11) $V_{DD\_HV\_ADR} = V_{DD\_HV\_ADV}$ GAIN = 1 $T_J < 150$ °C	74	—	—	dBFS
		T		$4.5 < V_{DD\_HV\_ADV} < 5.5$(10),(11) $V_{DD\_HV\_ADR} = V_{DD\_HV\_ADV}$ GAIN = 2 $T_J < 150$ °C	71	—	—	
		T		$4.5 < V_{DD\_HV\_ADV} < 5.5$(10),(11) $V_{DD\_HV\_ADR} = V_{DD\_HV\_ADV}$ GAIN = 4 $T_J < 150$ °C	68	—	—	
		T		$4.5 < V_{DD\_HV\_ADV} < 5.5$(10),(11) $V_{DD\_HV\_ADR} = V_{DD\_HV\_ADV}$ GAIN = 8 $T_J < 150$ °C	65	—	—	
		D		$4.5 < V_{DD\_HV\_ADV} < 5.5$(10),(11) $V_{DD\_HV\_ADR} = V_{DD\_HV\_ADV}$ GAIN = 16 $T_J < 150$ °C	62	—	—	

Table 29. SDn ADC electrical specification[1](Continued)

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
SNR_{SE150}[15]	CC	T	Signal to noise ratio in single ended mode 150 ksps output rate[13]	4.5 < $V_{DD\_HV\_ADV}$ < 5.5[10],[11] $V_{DD\_HV\_ADR}$ = $V_{DD\_HV\_ADV}$ GAIN = 1 T_J < 150 °C	74	—	—	dBFS
		T		4.5 < $V_{DD\_HV\_ADV}$ < 5.5[10],[11] $V_{DD\_HV\_ADR}$ = $V_{DD\_HV\_ADV}$ GAIN = 2 T_J < 150 °C	71	—	—	
				4.5 < $V_{DD\_HV\_ADV}$ < 5.5[10],[11] $V_{DD\_HV\_ADR}$ = $V_{DD\_HV\_ADV}$ GAIN = 4 T_J < 150 °C	68	—	—	
				4.5 < $V_{DD\_HV\_ADV}$ < 5.5[10],[11] $V_{DD\_HV\_ADR}$ = $V_{DD\_HV\_ADV}$ GAIN = 8 T_J < 150 °C	65	—	—	
		D		4.5 < $V_{DD\_HV\_ADV}$ < 5.5[10],[11], $V_{DD\_HV\_ADR}$=$V_{DD\_HV\_ADV}$ GAIN = 16 T_J < 150 °C	62	—	—	
SFDR	CC	P	Spurious free dynamic range	GAIN = 1	60	—	—	dBc
		C		GAIN = 2	60	—	—	
		C		GAIN = 4	60	—	—	
		C		GAIN = 8	60	—	—	
		D		GAIN = 16	60	—	—	
Z_{IN}	CC	D	Input impedance[14]	GAIN = 1, f_{ADCD_M} = 16 MHz	1.2	1.6	1.9	MΩ
				GAIN = 16, f_{ADCD_M} = 16 MHz	0.1	—	—	
R_{BIAS}	CC	D	Bias resistance	—	100	125	160	kΩ
V_{BIAS}	CC	D	Bias voltage	—	—	$V_{DD\_HV\_ADR}/2$	—	V
δV_{BIAS}	CC	D	Bias voltage accuracy	—	–2.5	—	+2.5	%
CMRR	SR	D	Common mode rejection ratio	—	54	—	—	dB
R_{Caaf}	SR	D	Anti-aliasing filter	External series resistance	—	—	20	kΩ
	CC	D		Filter capacitances	180	—	—	pF
$f_{PASSBAND}$	CC	D	Pass band[15]	—	0.01	—	0.333 * f_{ADCD_S}	KHz
δ_{RIPPLE}	CC	D	Pass band ripple[16]	0.333 * f_{ADCD_S}	–1	—	1	%

Table 29. SDn ADC electrical specification(1)(Continued)

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
$F_{rolloff}$	CC	D	Stop band attenuation	[0.5 * f_{ADCD_S}, 1.0 * f_{ADCD_S}]	40	—	—	dB
				[1.0 * f_{ADCD_S}, 1.5 * f_{ADCD_S}]	45	—	—	
				[1.5 * f_{ADCD_S}, 2.0 * f_{ADCD_S}]	50	—	—	
				[2.0 * f_{ADCD_S}, 2.5 * f_{ADCD_S}]	55	—	—	
				[2.5 * f_{ADCD_S}, f_{ADCD_M}/2]	60	—	—	
δ_{GROUP}	CC	D	Group delay	Within pass band – Tclk is f_{ADCD_M} / 2	—	—	—	—
				OSR = 24	—	—	238.5	Tclk
				OSR = 28	—	—	278	
				OSR = 32	—	—	317.5	
				OSR = 36	—	—	357	
				OSR = 40	—	—	396.5	
				OSR = 44	—	—	436	
				OSR = 48	—	—	475.5	
				OSR = 56	—	—	554.5	
				OSR = 64	—	—	633.5	
				OSR = 72	—	—	712.5	
				OSR = 75	—	—	699	
				OSR = 80	—	—	791.5	
				OSR = 88	—	—	870.5	
				OSR = 96	—	—	949.5	
				OSR = 112	—	—	1107.5	
				OSR = 128	—	—	1265.5	
				OSR = 144	—	—	1423.5	
				OSR = 160	—	—	1581.5	
				OSR = 176	—	—	1739.5	
				OSR = 192	—	—	1897.5	
				OSR = 224	—	—	2213.5	
				OSR = 256	—	—	2529.5	
				Distortion within pass band	–0.5/ f_{ADCD_S}	—	+0.5/ f_{ADCD_S}	—
f_{HIGH}	CC	D	High pass filter 3dB frequency	Enabled	—	10e-5* f_{ADCD_S}	—	—

Table 29. SDn ADC electrical specification(1)(Continued)

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
$t_{STARTUP}$	CC	D	Start-up time from power down state	—	—	—	100	µs
$t_{LATENCY}$	CC	D	Latency between input data and converted data when input mux does not change(17)	HPF = ON	—	—	δ_{GROUP} + f_{ADCD_S}	—
				HPF = OFF	—	—	δ_{GROUP}	—
$t_{SETTLING}$	CC	D	Settling time after mux change(18)	Analog inputs are muxed HPF = ON	—	—	2*δ_{GROUP} + 3*f_{ADCD_S}	—
				HPF = OFF	—	—	2*δ_{GROUP} + 2*f_{ADCD_S}	—
$t_{ODRECOVERY}$	CC	D	Overdrive recovery time	After input comes within range from saturation HPF = ON	—	—	2*δ_{GROUP} + f_{ADCD_S}	—
				HPF = OFF	—	—	2*δ_{GROUP}	—
C_{S_D}	CC	D	S/D ADC sampling capacitance after sampling switch(18)	GAIN = 1, 2, 4, 8	—	—	75*GAIN	fF
		D		GAIN = 16	—	—	600	fF
IBIAS	CC	D	Bias consumption	At least 1 ADCD enabled	—	—	3.5	mA
I_{ADV_D}	CC	T	$V_{DD\_HV\_ADV}$ power supply current (each ADC)	ADCD enabled	—	—	3.5	mA
ΣI_{ADR_D}	CC	C	Sum of all ADC reference consumption(19)	ADCD enabled	—	—	30	µA
I_{ADCS/D_REFH}	CC	T	S/D ADC Reference High Current	Dynamic consumption (Conversion)	—	—	3.5	µA
		T		Static consumption (Power-down mode)	—	—	+10	

1. Functional operating conditions are given in the DC electrical specifications. Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond the listed maxima may affect device reliability or cause permanent damage to the device.
2. For input voltage above the maximum and below the clamp voltage of the input pad, there is no latch-up concern, and the signal will only be ‘clipped’.
3. V_{INP} is the input voltage applied to the positive terminal of the SDADC.
4. Maximum input of 166.67 kHz supported with reduced accuracy. See SNR specifications.
5. When using a GAIN setting of 16, the conversion result will always have a value of zero in the least significant bit. The gives an effective resolution of 15 bits.
6. Offset and gain error due to temperature drift can occur in either direction (+/-) for each of the SDADCs on the device.

7. Calibration of gain is possible when gain = 1.
   Offset Calibration should be done with respect to 0.5*$V_{DD\_HV\_ADR}$ for *differential mode* and *single ended mode with negative input=0.5*$V_{DD\_HV\_ADR}$*.
   Offset Calibration should be done with respect to 0 for “single ended mode with negative input=0”.
   Both offset and Gain Calibration is guaranteed for ±5% variation of $V_{DD\_HV\_ADR}$, ±10% variation of $V_{DD\_HV\_ADV}$, and ± 50 °C temperature variation.
8. Conversion offset error must be divided by the applied gain factor (1, 2, 4, 8, or 16) to obtain the actual input referred offset error.
9. This parameter is guaranteed by bench validation with a small sample of devices across process variations, and tested in production to a value of 3 dB less.
10. S/D ADC is functional in the range 3.6 V – 4.5 V, SNR parameter degrades by 3 dB. Degraded SNR value based on simulation.
11. S/D ADC is functional in the range 3.0 – 4.5 V, SNR parameter degrades by 9 dB. Degraded SNR value based on simulation.
12. This parameter is guaranteed by bench validation with a small sample of devices across process variations.
13. This parameter is guaranteed by bench validation with a small sample of devices across process variations.
14. Input impedance is valid over the full input frequency range.Input impedance is calculated in megaohms by the formula 25.6/(Gain * f_{ADCD_M}).
15. SNR values guaranteed only if external noise on the ADC input pin is attenuated by the required SNR value in the frequency range of $f_{ADCD\_M} – f_{ADCD\_S}$ to $f_{ADCD\_M} + f_{ADCD\_S}$, where f_{ADCD_M} is the input sampling frequency, and f_{ADCD_S} is the output sample frequency. A proper external input filter should be used to remove any interfering signals in this frequency range.
16. The ±1% passband ripple specification is equivalent to 20 * $\log_{10}$ (0.99) = 0.087 dB.
17. Propagation of the information from the pin to the register CDR[CDATA] and flags SFR[DFEF], SFR[DFFF] is given by the different modules that need to be crossed: delta/sigma filters, high pass filter, fifo module, clock domain synchronizers. The time elapsed between data availability at pin and internal S/D module registers is given by the below formula:

    REGISTER LATENCY = tLATENCY + 0.5/fADCD_S + 2 (~+1)/fADCD_M + 2(~+1)fPBRIDGEx_CLK

    where fADCD_S is the frequency of the sampling clock, fADCD_M is the frequency of the modulator, and fPBRIDGEx_CLK is the frequency of the peripheral bridge clock feeds to the ADC S/D module. The (~+1) symbol refers to the number of clock cycles uncertainty (from 0 to 1 clock cycle) to be added due to resynchronization of the signal during clock domain crossing.
    Some further latency may be added by the target module (core, DMA, interrupt) controller to process the data received from the ADC S/D module.
18. This capacitance does not include pin capacitance, that can be considered together with external capacitance, before sampling switch.
19. Consumption is given after power-up, when steady state is reached. Extra consumption up to 2 mA may be required during internal circuitry set-up.

3.12 Temperature sensor

The following table describes the temperature sensor electrical characteristics.

Table 30. Temperature sensor electrical characteristics

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
—	CC		Temperature monitoring range	—	–40	—	150	°C
T_{SENS}	CC	T	Sensitivity	—	—	5.18	—	mV/°C
T_{ACC}	CC	C	Accuracy	$T_J < 150$ °C	–3	—	3	°C
I_{TEMP_SENS}	CC	C	$V_{DD\_HV\_ADV}$ power supply current	—	—	—	700	µA

3.13 LVDS Fast Asynchronous Serial Transmission (LFAST) pad electrical characteristics

The LFAST pad electrical characteristics apply to both the SIPI and high-speed debug serial interfaces on the device. The same LVDS pad is used for the Microsecond Channel (MSC) and DSPI LVDS interfaces, with different characteristics given in the following tables.

3.13.1 LFAST interface timing diagrams

Figure 15. LFAST and MSC/DSPI LVDS timing definition

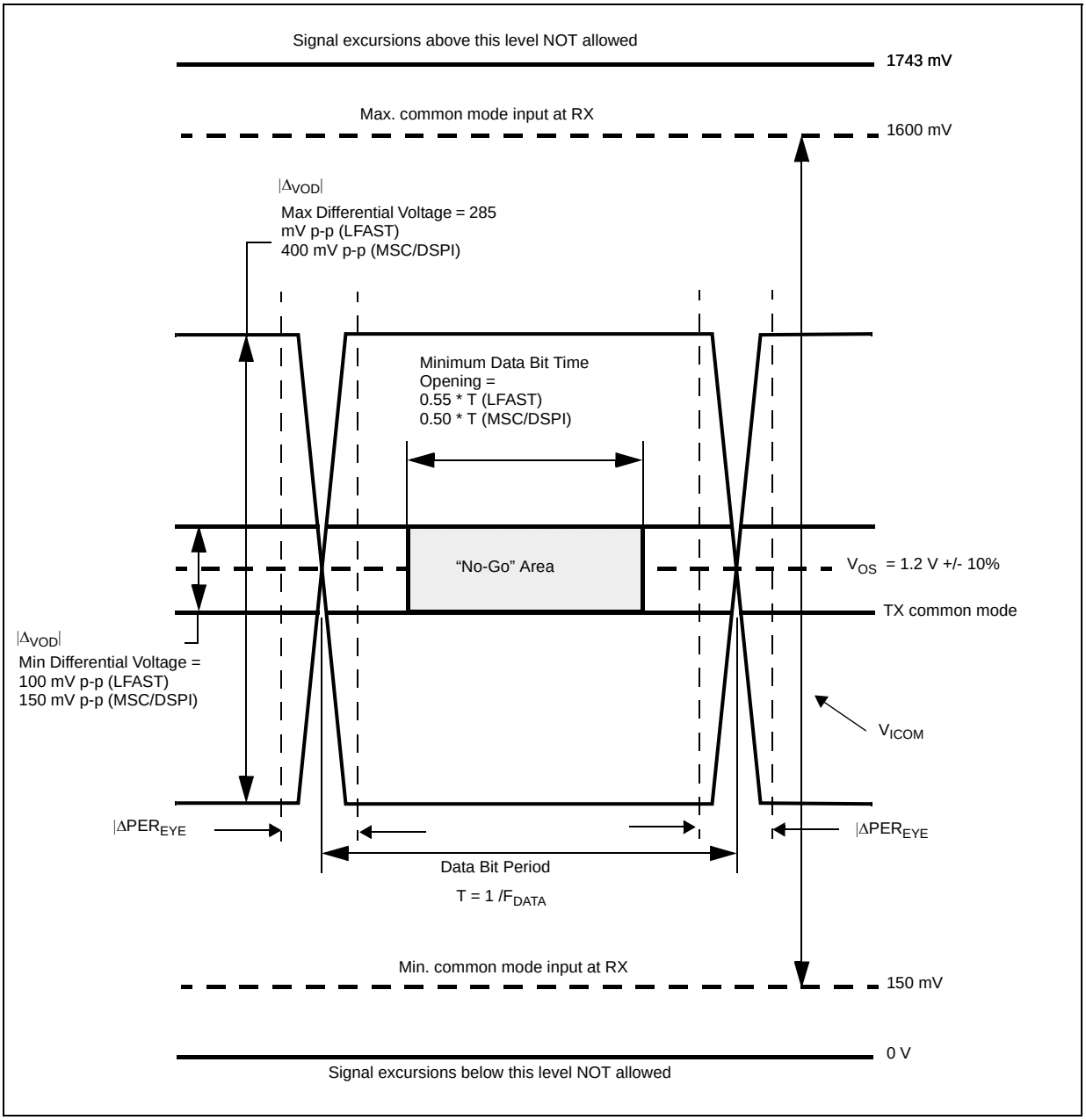


Figure 16. Power-down exit time

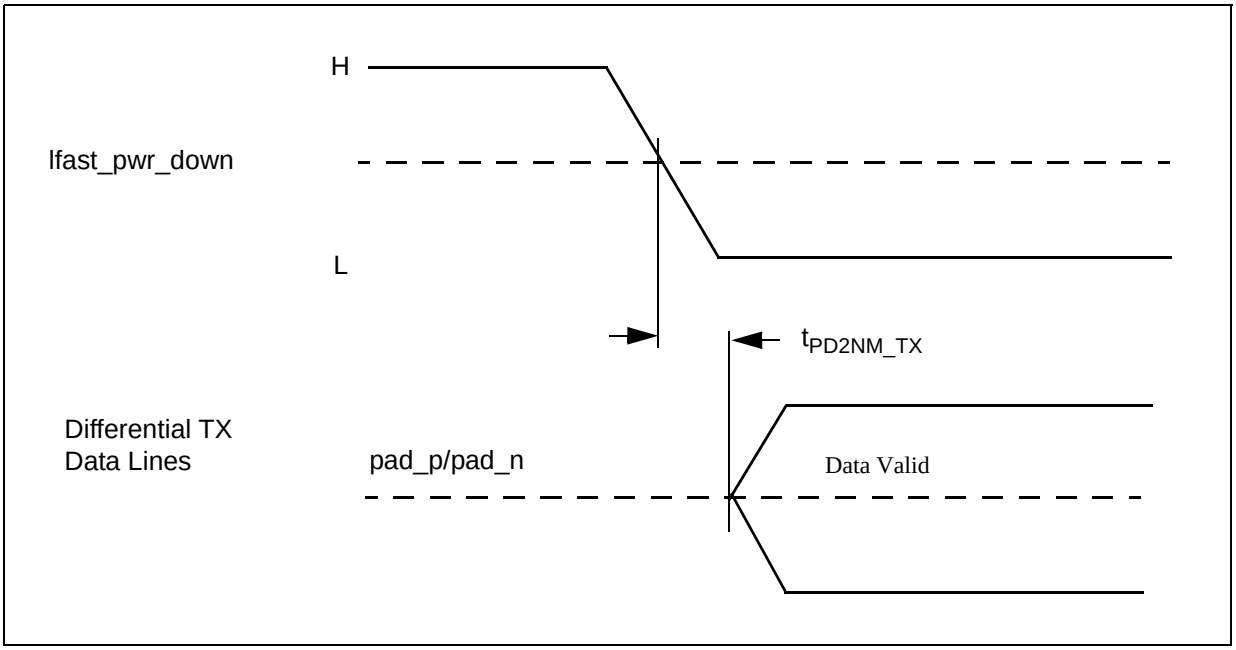
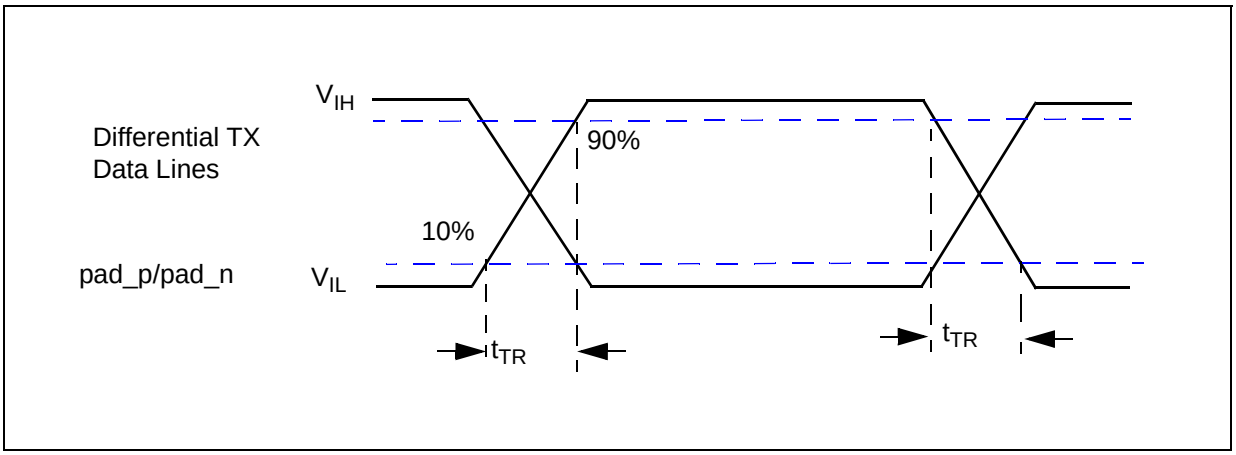


Figure 17. Rise/fall time



3.13.2 LFAST and MSC/DSPI LVDS interface electrical characteristics

The following table contains the electrical characteristics for the LFAST interface.

Table 31. LVDS pad startup and receiver electrical characteristics(1)(2)

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
STARTUP(3),(4)								
t_{STRT_BIAS}	CC	T	Bias current reference startup time(5)	—	—	0.5	4	µs
t_{PD2NM_TX}	CC	T	Transmitter startup time (power down to normal mode)(6)	—	—	0.4	2.75	µs

Table 31. LVDS pad startup and receiver electrical characteristics[1][2](Continued)

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
t_{SM2NM_TX}	CC	T	Transmitter startup time (sleep mode to normal mode)[7]	Not applicable to the MSC/DSPI LVDS pad	—	0.2	0.5	µs
t_{PD2NM_RX}	CC	T	Receiver startup time (power down to normal mode)[8]	—	—	20	40	ns
t_{PD2SM_RX}	CC	T	Receiver startup time (power down to sleep mode)[9]	Not applicable to the MSC/DSPI LVDS pad	—	20	50	ns
I_{LVDS_BIAS}	CC	C	LVDS bias current consumption	Tx or Rx enabled	—	—	0.95	mA
TRANSMISSION LINE CHARACTERISTICS (PCB Track)								
Z_0	SR	D	Transmission line characteristic impedance	—	47.5	50	52.5	Ω
Z_{DIFF}	SR	D	Transmission line differential impedance	—	95	100	105	Ω
RECEIVER								
V_{ICOM}	SR	T	Common mode voltage	—	0.15 (10)	—	1.6[11]	V
$\|\Delta_{VI}\|$	SR	T	Differential input voltage[12]	—	100	—	—	mV
R_{IN}	CC	D	Terminating resistance	$V_{DD\_HV\_IO}$ = 5.0 V ± 10%	80	125	150	Ω
		D		$V_{DD\_HV\_IO}$ = 3.3 V ± 10%	80	115	150	Ω
C_{IN}	CC	D	Differential input capacitance[13]	—	—	3.5	6.0	pF
I_{LVDS_RX}	CC	C	Receiver DC current consumption	Enabled	—	—	0.5	mA

1. The LVDS pad startup and receiver electrical characteristics in this table apply to both the LFAST & High-speed Debug (HSD) LVDS pad, and the MSC/DSPI LVDS pad except where noted in the conditions.
2. All LVDS pad electrical characteristics are valid from –40 °C to 150 °C.
3. All startup times are defined after a 2 peripheral bridge clock delay from writing to the corresponding enable bit in the LVDS control registers (LCR) of the LFAST and High-Speed Debug modules. The value of the LCR bits for the LFAST/HSD modules don't take effect until the corresponding SIUL2 MSCR ODC bits are set to LFAST LVDS mode. Startup times for MSC/DSPI LVDS are defined after 2 peripheral bridge clock delay after selecting MSC/DSPI LVDS in the corresponding SIUL2 MSCR ODC field.
4. Startup times are valid for the maximum external loads CL defined in both the LFAST/HSD and MSC/DSPI transmitter electrical characteristic tables.
5. Bias startup time is defined as the time taken by the current reference block to reach the settling bias current after being enabled.
6. Total transmitter startup time from power down to normal mode is t_{STRT_BIAS} + t_{PD2NM_TX} + 2 peripheral bridge clock periods.
7. Total transmitter startup time from sleep mode to normal mode is t_{SM2NM_TX} + 2 peripheral bridge clock periods. Bias block remains enabled in sleep mode.
8. Total receiver startup time from power down to normal mode is t_{STRT_BIAS} + t_{PD2NM_RX} + 2 peripheral bridge clock periods.
9. Total receiver startup time from power down to sleep mode is t_{PD2SM_RX} + 2 peripheral bridge clock periods. Bias block remains enabled in sleep mode.
10. Absolute min = 0.15 V – (285 mV/2) = 0 V

11. Absolute max = 1.6 V + (285 mV/2) = 1.743 V
12. The LXRXOP[0] bit in the LFAST LVDS Control Register (LCR) must be set to one to ensure proper LFAST receive timing.
13. Total internal capacitance including receiver and termination, co-bonded GPIO pads, and package contributions.

Table 32. LFAST transmitter electrical characteristics(1)(2)

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
f_{DATA}	SR	D	Data rate	—	—	—	320	Mbps
V_{OS}	CC	P	Common mode voltage	—	1.08	—	1.32	V
$\|V_{ODI}\|$	CC	P	Differential output voltage swing (terminated)(3)(4)	—	110	171	285	mV
t_{TR}	CC	T	Rise/Fall time (absolute value of the differential output voltage swing)(3),(4)	—	0.26	—	1.5	ns
C_L	SR	D	External lumped differential load capacitance(3)	$V_{DD\_HV\_IO}$ = 4.5 V	—	—	10.0	pF
				$V_{DD\_HV\_IO}$ = 3.0 V	—	—	8.5	
I_{LVDS_TX}	CC	T	Transmitter DC current consumption	Enabled	—	—	3.2	mA

1. The LFAST and High-Speed Debug LFAST pad electrical characteristics are based on worst case internal capacitance values shown in *Figure 18*.
2. All LFAST and High-Speed Debug LVDS pad electrical characteristics are valid from –40 °C to 150 °C.
3. Valid for maximum data rate f_{DATA}. Value given is the capacitance on each terminal of the differential pair, as shown in *Figure 18*.
4. Valid for maximum external load C_L.

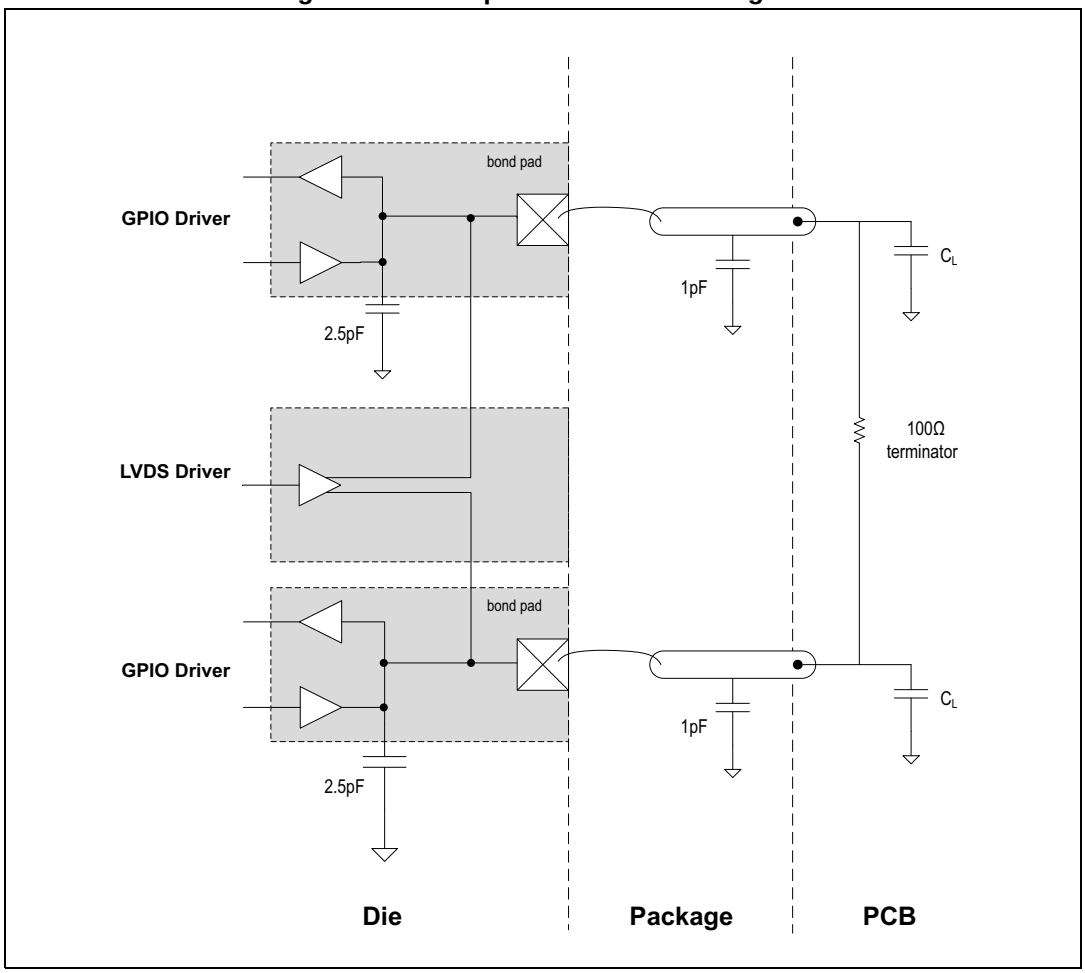
Table 33. MSC/DSPI LVDS transmitter electrical characteristics (1)(2)

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
Data Rate								
f_{DATA}	SR	D	Data rate	—	—	—	80	Mbps
V_{OS}	CC	P	Common mode voltage	—	1.08	—	1.32	V
$\|V_{ODI}\|$	CC	P	Differential output voltage swing (terminated)(3)(4)	—	150	214	400	mV
t_{TR}	CC	T	Rise/Fall time (absolute value of the differential output voltage swing)(3),(4)	—	0.8	—	4.0	ns
C_L	SR	D	External lumped differential load capacitance(3)	$V_{DD\_HV\_IO}$ = 4.5 V	—	—	50	pF
				$V_{DD\_HV\_IO}$ = 3.0 V	—	—	39	
I_{LVDS_TX}	CC	T	Transmitter DC current consumption	Enabled	—	—	4.0	mA

1. The MSC and DSPI LVDS pad electrical characteristics are based on the application circuit and typical worst case internal capacitance values given in *Figure 18*.
2. All MSC and DSPI LVDS pad electrical characteristics are valid from –40 °C to 150 °C.

3. Valid for maximum data rate f_{DATA}. Value given is the capacitance on each terminal of the differential pair, as shown in *Figure 18*.
4. Valid for maximum external load C_L.

Figure 18. LVDS pad external load diagram



3.13.3 LFAST PLL electrical characteristics

The following table contains the electrical characteristics for the LFAST PLL.

Table 34. LFAST PLL electrical characteristics(1)

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Nominal	Max	
f_{RF_REF}	SR	D	PLL reference clock frequency	—	10	—	26	MHz
ERR_{REF}	CC	D	PLL input reference clock frequency error	—	–1	—	1	%
DC_{REF}	CC	D	PLL input reference clock duty cycle	—	45	—	55	%

Table 34. LFAST PLL electrical characteristics[1](Continued)

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Nominal	Max	
PN	CC	D	Integrated phase noise (single side band)	f_{RF_REF} = 20 MHz	—	—	–58	dBc
		D		f_{RF_REF} = 10 MHz	—	—	–64	
f_{VCO}	CC	D	PLL VCO frequency	—	—	640[2]	—	MHz
t_{LOCK}	CC	D	PLL phase lock[3]	—	—	—	40	µs
ΔPER_{REF}	SR	T	Input reference clock jitter (peak to peak)	Single period, f_{RF_REF} = 10 MHz	—	—	300	ps
		T		Long term, f_{RF_REF} = 10 MHz	–500	—	500	ps
ΔPER_{EYE}	CC	T	Output Eye Jitter (peak to peak)[4]	—	—	—	400	ps

1. The specifications in this table apply to both the interprocessor bus and debug LFAST interfaces.
2. The 640 MHz frequency is achieved with a 10 MHz or 20 MHz reference clock. With a 26 MHz reference, the VCO frequency is 624 MHz. PLL lock with 640 MHz VCO frequency guaranteed by production testing.
3. The time from the PLL enable bit register write to the start of phase locks is maximum 2 clock cycles of the peripheral bridge clock that is connected to the PLL on the device.
4. Measured at the transmitter output across a 100 Ohm termination resistor on a device evaluation board. See *Figure 18*.

3.14 Aurora LVDS electrical characteristics

The following table describes the Aurora LVDS electrical characteristics.

Note: The Aurora interface is AC coupled, so there is no common-mode voltage specification.

Table 35. Aurora LVDS electrical characteristics[1][2]

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
Transmitter								
F_{TX}	CC	D	Transmit Data Rate	—	—	—	1.25	Gbps
$\lvert\Delta V_{OD\_LVDS}\rvert$	CC	P	Differential output voltage swing (terminated)[3]	—	400	600	800	mV
t_{TR_LVDS}	CC	T	Rise/Fall time (10%–90% of swing)	—	60	—	—	ps
$R_{V\_L\_Tx}$	SR	D	Differential Terminating resistance	—	81	100	120	W
T_{Loss}	CC	D	Transmission Line Loss due to loading effects	—	—	—	6[4]	dB
Transmission line characteristics (PCB track)								
L_{LINE}	SR	D	Transmission line length	—	—	—	20	cm
Z_{LINE}	SR	D	Transmission line characteristic impedance	—	45	50	55	W
C_{ac_clk}	SR	D	Clock Receive Pin External AC Coupling Capacitance	Values are nominal, valid for +/– 50% tolerance	100	—	270	pF

Table 35. Aurora LVDS electrical characteristics(1)(2)(Continued)

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
C_{ac_tx}	SR	D	Transmit Lane External AC Coupling Capacitance	Values are nominal, valid for +/– 50% tolerance	250	—	2000	pF
Receiver								
F_{RX}	CC	D	Receive Clock Rate	T_J = 150 °C	—	—	1.25	Gbps
$\|\Delta V_{I\_L}\|$	SR	T	Differential input voltage (peak to peak)	—	200	—	1000	mV
$R_{V\_L\_Rx}$	CC	D	Differential Terminating resistance	—	81	100	120	W

1. All Aurora electrical characteristics are valid from –40 °C to 150 °C, except where noted.
2. All specifications valid for maximum transmit data rate F_{TX}.
3. The minimum value of 400 mV is only valid for differential terminating resistance (R_{V_L}) = 99 Ohm to 101 ohm. The differential output voltage swing tracks with the value of R_{V_L}.
4. Transmission line loss maximum value is specified for the maximum drive level of the Aurora transmit pad.

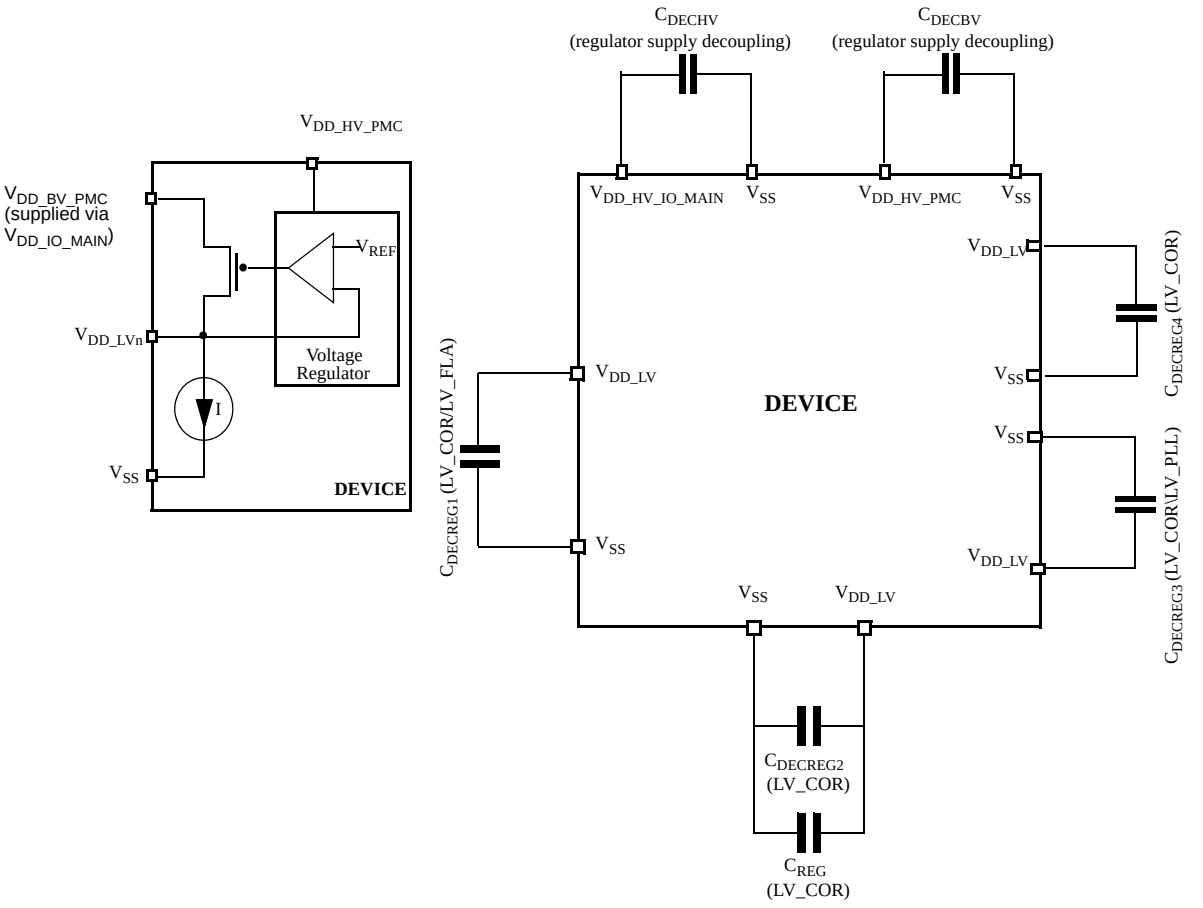
3.15 Power management: PMC, POR/LVD, sequencing

The power management module monitors the different power supplies as well as generating the required internal supplies. The power management module is supplied by the $V_{DD\_HV\_PMC}$ supply, with redundant voltage references and monitors guaranteeing safe operation.

3.15.1 Power management integration

Use the integration scheme provided below to ensure proper device function.

Figure 19. Voltage regulator capacitance connection



Note: The pins positions correspond to the pins positions in the pins package.

The internal voltage regulator requires external capacitance (C_{REGn}) to be connected to the device to provide a stable low voltage digital supply to the device. Placed capacitances on the board as near as possible to the associated pins and limit the serial inductance of the board to less than 5 nH.

Place a decoupling capacitor between each V_{DD_LV} supply pin and V_{SS} ground plane to ensure stable voltage. Place the capacitor as near as possible to the V_{DD_LV} supply pin.

3.15.2 Main voltage regulator electrical characteristics

The device implements an internal voltage regulator to generate the low voltage core supply V_{DD_LV} from the high voltage ballast supply $V_{DD\_BV\_PMC}$, internally connected to $V_{DD\_HV\_IO\_MAIN}$ supply. The regulator itself is supplied by $V_{DD\_HV\_PMC}$. Both high voltage supplies are common with $V_{DD\_HV\_IO}$.

Note: Refer to JPC5744M_IO_Signal.xls table for details regarding power connectivity.

The following supplies are involved:

- HV—High voltage external power supply for voltage regulator module. This must be provided externally through $V_{DD\_HV\_PMC}/V_{DD\_HV\_IO\_MAIN}$ power pin.
- BV—High voltage external power supply for internal ballast module. This must be provided externally through $V_{DD\_HV\_PMC}/V_{DD\_HV\_IO\_MAIN}$ power pins.
- LV—Low voltage internal power supply for core, PLL and Flash digital logic. This is generated by the internal voltage regulator but provided externally to allow connection to a stability capacitor. It is further split into three main domains to ensure noise isolation between critical LV modules:
  - LV_COR—Low voltage supply for the core. It is also used to provide supply LV_PLL through double bonding.
  - LV_FLA—Low voltage supply for code flash module. It is supplied with dedicated ballast and shorted to LV_COR through double bonding.
  - LV_PLL—Low voltage supply for PLL0. It is shorted to LV_COR through double bonding.

Table 36. Device Power Supply Integration

Symbol		C	Parameter	Conditions[1]	Value[2]			Unit
					Min	Typ	Max	
C_{REG}	SR	D	Internal voltage regulator stability external capacitance	—	1.3	2[3]	—	µF
R_{REG}	SR	D	Stability capacitor equivalent serial resistance	Total resistance including board track	—	—	50	mΩ
$C_{DECREGn}$	SR	D	Internal voltage regulator decoupling external capacitance	V_{DD_LV}/V_{SS} pair	30	100	—	nF
$R_{DECREGn}$	SR	D	Stability capacitor equivalent serial resistance	—	—	—	50	mΩ
C_{DECBV}	SR	D	Relay capacitance for ballast power-up	—	3	4[4]	—	µF
C_{DECHV}	SR	D	Decoupling capacitance regulator supply	$V_{DD\_HV\_IO\_MAIN}/V_{SS}$ pair	30	100	—	nF
V_{MREG}	CC	P	Main regulator output voltage	Before trimming	1.14	1.28	1.4[5]	V
		P		After trimming	1.14	1.28	1.32	
IDD_{MREG}	SR	P	Main regulator current provided to V_{DD_LV} domain	—	—	—	350	mA
IDD_{CLAMP}	CC	D	Main regulator rush current sinked from VDD_HV_IO_MAIN domain during VDD_LV external capacitance loading	Power-up condition	200	—	1500	mA
ΔIDD_{MREG}	SR	T	Main regulator current variation	20 µs observation window	–60	—	60	mA
$I_{MREGINT}$	CC	D	Main regulator current consumption	I_{MREG} = 300 mA	—	—	3.5	mA
		D		I_{MREG} = 0 mA	—	—	2.2	

Table 36. Device Power Supply Integration(Continued)

Symbol		C	Parameter	Conditions[1]	Value[2]			Unit
					Min	Typ	Max	
C_{DECFLA}	SR	D	Decoupling capacitance for flash supply	$V_{DD\_HV\_FLA}$/VSS pair	100	220	—	nF
C_{HV_ADC}	SR	D	$V_{DD\_HV\_ADV}$ external capacitance[6]		1	2.2	—	µF

1. V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 / 125 °C, unless otherwise specified.
2. All values need to be confirmed during device validation.
3. Recommended X7R or X5R ceramic –35 % / +20 % variation across process, temperature, voltage and after aging.
4. Recommended X7R or X5R ceramic –35 % / +20 % variation across process, temperature, voltage and after aging.
5. At power-up condition before trimming.
6. For noise filtering, add a high frequency bypass capacitance of 0.1 µF between $V_{DD\_HV\_ADV}$ and $V_{SS\_HV\_ADV}$.

3.15.3 Device voltage monitoring

The LVD/HVDs and their associated levels for the device are given in the following table. The figure below illustrates the workings of voltage monitoring threshold.

Figure 20. Voltage monitor threshold definition

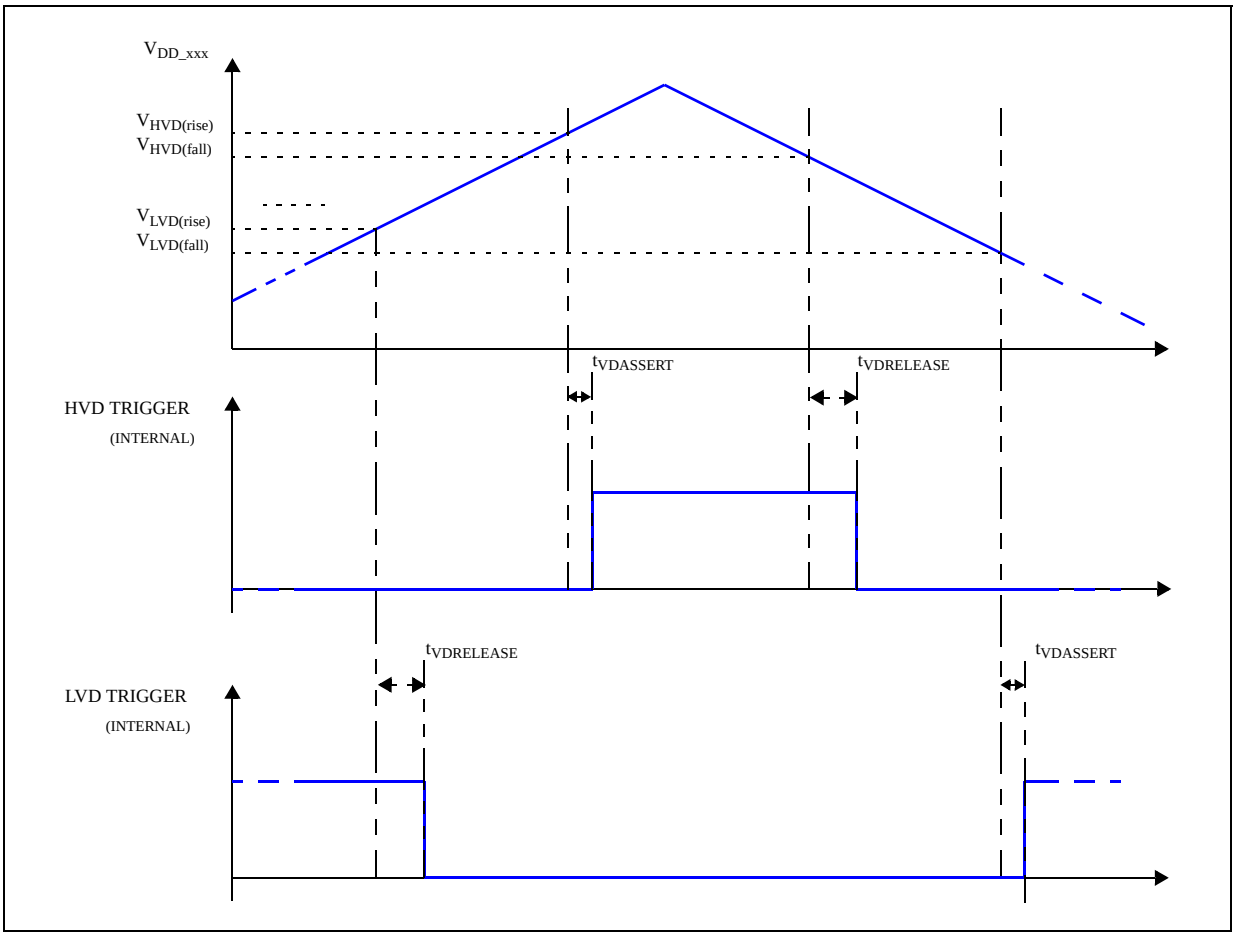


Table 37. Voltage monitor electrical characteristics(1)

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
V_{PORUP_LV}(2)	CC	D	LV supply power on reset threshold[	Rising voltage (power up)	1040	—	1180	mV
		P		Falling voltage (power down)(3)	960	—	1100	
				Hysteresis on power-up	50	—	—	
V_{LVD096}	CC	P	LV internal(4) supply low voltage monitoring	See note (5)	960	—	1100	mV
V_{LVD108}	CC	P	Core LV internal(4) supply low voltage monitoring	See note(6)	1080	—	1170	mV
V_{LVD112}	CC	P	LV external(7) supply low voltage monitoring	See note (5)	1110	—	1180	mV
V_{HVD140}	CC	P	LV external(7) supply high voltage monitoring	See note (8)	1320	—	1420	mV
VHVD145	CC	P	LV external(7) supply high voltage monitoring	See note (8)	1390	—	1480	mV
V_{PORUP_HV}(2)	CC	P	HV supply power on reset threshold(9)	Rising voltage (power up) on PMC/IO Main supply	2850	—	3210	mV
				Rising voltage (power up) on IO JTAG and Osc supply	2680	—	2980	
				Rising voltage (power up) on ADC supply	2870	—	3182	
				Falling voltage (power down)(10)	2710	—	3000	
				Hysteresis on power up(11)	150	—	—	
V_{POR240}	CC	P	HV supply power-on reset voltage monitoring	Rising voltage	2420	—	2780	mV
				Falling voltage	2400	—	2760	
V_{LVD270}	CC	P	HV supply low voltage monitoring	Rising voltage	2750	—	3000	mV
				Falling voltage	2700	—	2950	
V_{LVD295}	CC	P	ADC supply low voltage monitoring	Rising voltage	—	—	3120	mV
				Falling voltage	2920	—	3100	
V_{LVD400}	CC	P	HV supply low voltage monitoring	Rising voltage	4110	—	4410	mV
				Falling voltage	3970	—	4270	
V_{HVD600}	CC	P	HV supply high voltage monitoring	Rising voltage	5560	—	5960	mV
				Falling voltage	5500	—	5900	

Table 37. Voltage monitor electrical characteristics[1](Continued)

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
$t_{VDASSERT}$	CC	D	Voltage detector threshold crossing assertion	—	0.1	—	2	µs
$t_{VDRELEASE}$	CC	D	Voltage detector threshold crossing de-assertion	—	5	—	20	µs

1. For V_{DD_LV} levels, a maximum of 30 mV IR drop is incurred from the pin to all sinks on the die. For other LVD, the IR drop is estimated by multiplying the supply current by 0.5 Ω.
2. V_{PORUP_LV} and V_{PORUP_HV} threshold are untrimmed values before completion of the power-up sequence. All other LVD/HVD thresholds are provided after trimming.
3. Assume all of LVDs on LV supplies disabled.
4. LV internal supply levels are measured on device internal supply grid after internal voltage drop.
5. LVD is released after $t_{VDRELEASE}$ temporization when *upper* threshold is crossed, LVD is asserted $t_{VDASSERT}$ after detection when *lower* threshold is crossed.
6. This is combination of LVD108_C, P, and F. Min is from min value of LVD108_F, and P which is the lowest one. Max is the max value of LVD108_C which is the highest one of three.
7. LV external supply levels are measured on the die side of the package bond wire after package voltage drop.
8. HVD is released after $t_{VDRELEASE}$ temporization when *lower* threshold is crossed, HVD is asserted $t_{VDASSERT}$ after detection when *upper* threshold is crossed. HVD140 does not cause reset.
9. This supply also needs to be below 5472 mV (untrimmed HVD600 min).
10. Untrimmed LVD300_A will be asserted first on power down.
11. Hysteresis is implemented only between the VDD_HV_IO_MAIN High voltage Supplies and the ADC high voltage supply. When these two supplies are shorted together, the hysteresis is as is shown in *Table 37*. If the supplies are not shorted (VDD_IO_MAIN and ADC high voltage supply), then there will be no hysteresis on the high voltage supplies.

3.15.4 Power up/down sequencing

The following table shows the constraints and relationships for the different power supplies.

Table 38. Device supply relation during power-up/power-down sequence

		Supply 2[1]					
		V_{DD_LV}	$V_{DD\_HV\_IO\_JTAG}$/ $V_{DD\_HV\_IO\_FLEX}$	$V_{DD\_HV\_IO}$	$V_{DD\_HV\_ADV}$	$V_{DD\_HV\_ADR}$	ALTREFn[2]
Supply 1[1]	V_{DD_LV}						
	$V_{DD\_HV\_IO\_JTAG}$/ $V_{DD\_HV\_IO\_FLEX}$						
	$V_{DD\_HV\_IO}$						
	$V_{DD\_HV\_ADV}$						
	$V_{DD\_HV\_ADR}$				5 mA		
	ALTREFn			10 mA[3]	10 mA[3]		

1. Red cells: Supply 1 (row) can exceed Supply 2 (column), granted that external circuitry ensures current flowing from supply1 is less than absolute maximum rating current value provided.
2. ALTREFn are the alternate references for the ADC that can be used in place of the default reference ($V_{DD\_HV\_ADR\_*}$). They are SARB.ALTREF and SAR2.ALTREF.

3. ADC performance is not guaranteed when ALTREFn, and $V_{DD\_HV\_ADR}$ supplies are above $V_{DD\_HV\_IO}$/$V_{DD\_HV\_ADV}$.

During power-up, all functional terminals are maintained in a known state as described in the following table.

Table 39. Functional terminals state during power-up and reset

TERMINAL type(1)	POWER-UP(2) pad state	RESET pad state	DEFAULT pad state(3)	Comments
PORST	Strong pull-down(4)	Weak pull-down	Weak pull-down	Power-on reset pad
ESR0(5)	Strong pull-down	Strong pull-down	Weak pull-up	Functional reset pad
ESR1	Weak pull-up	Weak pull-up	Weak pull-up	—
TEST_MODE	Weak pull-down	Weak pull-down(6)	Weak pull-down(6)	—
GPIO	Weak pull-up(4)	Weak pull-up	Weak pull-up	—
ANALOG	High impedance	High impedance	High impedance	—
ERROR[0]	High impedance	High impedance	High impedance	During functional reset, pad state can be overridden by FCCU
TRST	High impedance	Weak pull-down	Weak pull-down	—
TCK	High impedance	Weak pull-down	Weak pull-down	—
TMS	Weak pull-up	Weak pull-up	Weak pull-up	—
TDI	Weak pull-up	Weak pull-up	Weak pull-up	—
TDO	High impedance	High impedance	High impedance	—

1. Refer to pinout information for terminal type.
2. POWER-UP state is guaranteed from $V_{DD\_HV\_IO} > V_{DD\_POR}$ and maintained until supply crosses the power-on reset thresholds V_{PORUP_LV} for LV supply and V_{PORUP_HV} for high voltage supply.
3. Before software configuration.
4. Pull-down and pull-up strengths are provided in *Table 15 (I/O pull-up/pull-down DC electrical characteristics)*
5. Unlike ESR0, ESR1 is provided as a normal GPIO and implements weak pull-up during power-up.
6. An internal pull-down is implemented on the TESTMODE pin to prevent the device from entering test mode if the package TESTMODE pin is not connected. It is recommended to connect the TESTMODE pin to $V_{SS\_HV\_IO}$ on the board for maximum robustness, but not required. The value of TESTMODE is latched at the negation of reset and has no affect afterward. The device will not exit functional reset with the TESTMODE pin asserted during power-up. The TESTMODE pin can be connected externally directly to ground without any other components.

3.16 Flash memory electrical characteristics

Table 40 shows the estimated Program/Erase characteristics.

Table 40. Flash memory program and erase specifications (1)

Symbol	Characteristics(2)	Value									Unit
		Typ(3)	C	Initial max			Typical end of life(4)	Lifetime max(5)		C	
				25 °C(6)	All temp (7)	C		< 1 k cycles	≤ 250 K cycles		
$t_{dwprogram}$	Double Word (64 bits) program time [Packaged part]	34	C	100	—	—	55	500		C	µs
$t_{pprogram}$	Page (256 bits) program time	60	C	200	—	—	108	1000		C	µs
$t_{pprogrameep}$	Page (256 bits) program time EEPROM (partition 2) [Packaged part]	69	C	220	—	—	124	1000		C	µs
$t_{qprogram}$	Quad Page (1024 bits) program time	204	C	1040	1200	P	850	2000		C	µs
$t_{qprogrameep}$	Quad Page (1024 bits) program time EEPROM (partition 2) [Packaged part]	234	C	1140	1320	P	978	2000		C	µs
$t_{16kpperase}$	16 KB block pre-program and erase time	150	C	1000	1000	P	330	5000	—	C	ms
$t_{32kpperase}$	32 KB block pre-program and erase time	200	C	1000	1000	P	440	5000	—	C	ms
$t_{64kpperase}$	64 KB block pre-program and erase time	300	C	1000	1000	P	660	5000	—	C	ms
$t_{256kpperase}$	256 KB block pre-program and erase time	900	C	2000	3000	P	1100	15000	—	C	ms
$t_{16kprogram}$	16 KB block program time	27	C	45	50	P	40	1000	—	C	ms
$t_{32kprogram}$	32 KB block program time	54	C	90	100	P	80	2000	—	C	ms
$t_{64kprogram}$	64 KB block program time	108	C	175	200	P	169	4000	—	C	ms
$t_{256kprogram}$	256 KB block program time	432	C	700	850	P	634	17000	—	C	ms
$t_{16kprogrameep}$	Program 16 KB EEPROM (partition 2) [Packaged part]	31	C	52	58	P	64	1000		C	ms
$t_{16keraseeep}$	Erase 16 KB EEPROM (partition 2) [Packaged part]	160	C	1000	1000	P	500	5000		C	ms
t_{tr}	Program rate(8)	1.73	C	2.24	3.40	C	1.9	—		C	s/MB
t_{pr}	Erase rate(8)	4.0	C	8.0	12.0	C	4.4	—		C	s/MB
$t_{ffprogram}$	Full flash programming time(9)	5	C	20	30	P	5.8	32	—	C	s
$t_{fferase}$	Full flash erasing time(9)	13	C	26	30	P	14.2	40	—	C	s
t_{ESRT}	Erase suspend request rate(10)	5.5	T	—	—	—	—	—		—	ms
t_{PSRT}	Program suspend request rate(10)	20	T	—	—	—	—	—		—	µs
t_{PSUS}	Program suspend latency(11)	—	—	—	—	—	—	10		T	µs

Table 40. Flash memory program and erase specifications (1)

Symbol	Characteristics(2)	Value									Unit
		Typ(3)	C	Initial max			Typical end of life(4)	Lifetime max(5)		C	
				25 °C(6)	All temp (7)	C		< 1 k cycles	≤ 250 K cycles		
t_{ESUS}	Erase suspend latency(11)	—	—	—	—	—	—	20		T	µs
t_{AIC0S}	Array Integrity Check (2.5 MB, sequential)(12)	25	T	—	—	—	—	—	—	—	ms
$t_{AIC256KS}$	Array Integrity Check (256 KB, sequential)(12)	2.5	T	—	—	—	—	—	—	—	ms
t_{AIC0P}	Array Integrity Check (2.5 MB, proprietary)(12)	2.5	T	—	—	—	—	—	—	—	s
t_{MR0S}	Margin Read (2.5 MB, sequential)(12)	125	T	—	—	—	—	—	—	—	ms
$t_{MR256KS}$	Margin Read (256 KB, sequential)(12)	12.5	T	—	—	—	—	—	—	—	ms

1. Characteristics are valid both for Data Flash and Code Flash, unless specified in the characteristics column.
2. Actual hardware programming times; this does not include software overhead.
3. Typical program and erase times assume nominal supply values and operation at 25 °C. All times are subject to change pending device characterization.
4. Typical End of Life program and erase times represent the median performance and assume nominal supply values. Typical End of Life program and erase values may be used for throughput calculations. These values are characteristic, but not tested.
5. Lifetime maximum program & erase times apply across the voltages and temperatures and occur after the specified number of program/erase cycles. These maximum values are characterized but not tested or guaranteed.
6. Initial factory condition: < 100 program/erase cycles, 20 °C < T_J < 30 °C junction temperature, and nominal (± 2%) supply voltages. These values are verified at production testing.
7. Initial maximum “All temp” program and erase times provide guidance for time-out limits used in the factory and apply for less than or equal to 100 program or erase cycles, –40 °C < T_J < 150 °C junction temperature, and nominal (± 2%) supply voltages. These values are verified at production testing.
8. Rate computed based on 256 K sectors.
9. Only code sectors, not including EEPROM.
10. Time between suspend resume and next suspend. Value stated actually represents minimum value specification.
11. Timings guaranteed by design.
12. AIC is done using system clock, thus all timing is dependant on system frequency and number of wait states. Timing in the table is calculated at max frequency.

Table 41. Flash memory Life Specification

Symbol	Characteristics(1)	Value				Unit
		Min	C	Typ	C	
N_{CER16K}	16 KB CODE Flash endurance	10	—	100	—	kcycles
N_{CER32K}	32 KB CODE Flash endurance	10	—	100	—	kcycles
N_{CER64K}	64 KB CODE Flash endurance	10	—	100	—	kcycles

Table 41. Flash memory Life Specification

Symbol	Characteristics[1]	Value				Unit
		Min	C	Typ	C	
$N_{CER256K}$	256 KB CODE Flash endurance	1	—	100	—	kcycles
N_{DER16K}	16 KB EEPROM Flash endurance	250	—	—	—	kcycles
t_{DR1k}	Minimum data retention Blocks with 0 - 1,000 P/E cycles	20	—	—	—	Years
t_{DR10k}	Minimum data retention Blocks with 1,001 - 10,000 P/E cycles	20	—	—	—	Years
t_{DR250k}	Minimum data retention Blocks with 10,001 - 250,000 P/E cycles	10	—	—	—	Years

1. Program and erase cycles supported across specified temperature specs.

3.16.1 Flash read wait state and address pipeline control settings

Table 42 describes the recommended RWSC settings at various operating frequencies based on specified intrinsic flash access times of the Flash array at 150 °C.

Table 42. Flash memory RWSC configuration

Platform Frequency	Minimum RWSC settings
0 – 25 MHz	0
25 – 50 MHz	1
50 – 80 MHz	2
80 – 110 MHz	3
110 – 140 MHz	4
140 – 160 MHz	5

3.17 AC specifications

3.17.1 Debug and calibration interface timing

3.17.1.1 JTAG interface timing

Table 43. JTAG pin AC electrical characteristics(1)(2)

#	Symbol		C	Characteristic	Value		Unit
					Min	Max	
1	t_{JCYC}	CC	D	TCK cycle time	100	—	ns
2	t_{JDC}	CC	T	TCK clock pulse width	40	60	%
3	$t_{TCKRISE}$	CC	D	TCK rise and fall times (40%–70%)	—	3	ns
4	t_{TMSS}, t_{TDIS}	CC	D	TMS, TDI data setup time	5	—	ns
5	t_{TMSH}, t_{TDIH}	CC	D	TMS, TDI data hold time	5	—	ns
6	t_{TDOV}	CC	D	TCK low to TDO data valid	—	15(3)	ns
7	t_{TDOI}	CC	D	TCK low to TDO data invalid	0	—	ns
8	t_{TDOHZ}	CC	D	TCK low to TDO high impedance	—	15	ns
9	t_{JCMPPW}	CC	D	JCOMP assertion time	100	—	ns
10	t_{JCMPS}	CC	D	JCOMP setup time to TCK low	40	—	ns
11	t_{BSDV}	CC	D	TCK falling edge to output valid	—	600(4)	ns
12	t_{BSDVZ}	CC	D	TCK falling edge to output valid out of high impedance	—	600	ns
13	t_{BSDHZ}	CC	D	TCK falling edge to output high impedance	—	600	ns
14	t_{BSDST}	CC	D	Boundary scan input valid to TCK rising edge	15	—	ns
15	t_{BSDHT}	CC	D	TCK rising edge to boundary scan input invalid	15	—	ns

1. These specifications apply to JTAG boundary scan only. See *Table 44* for functional specifications.
2. JTAG timing specified at $V_{DD\_HV\_IO\_JTAG}$ = 4.0 V to 5.5 V, and maximum loading per pad type as specified in the I/O section of the data sheet.
3. Timing includes TCK pad delay, clock tree delay, logic delay and TDO output pad delay.
4. Applies to all pins, limited by pad slew rate. Refer to IO delay and transition specification and add 20 ns for JTAG delay.

Figure 21. JTAG test clock input timing

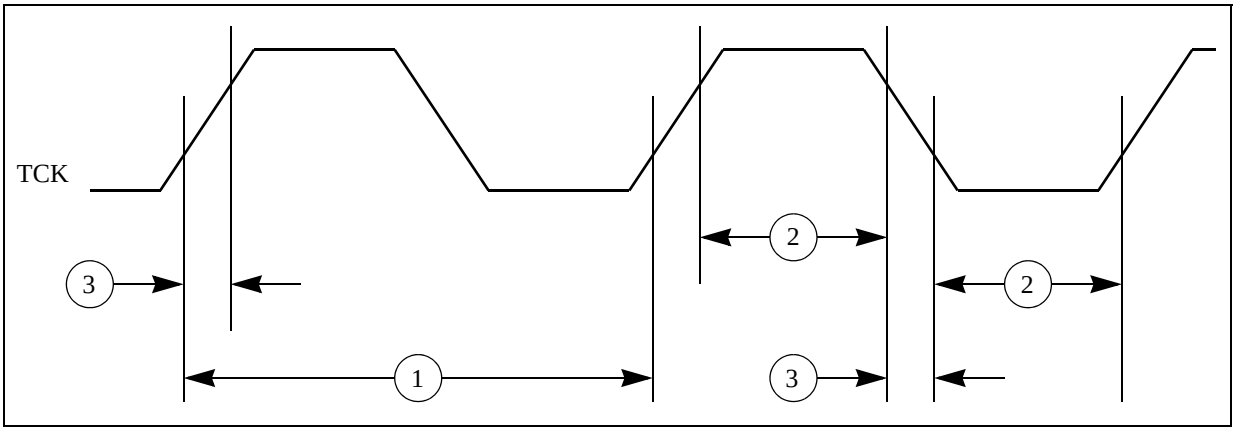


Figure 22. JTAG test access port timing

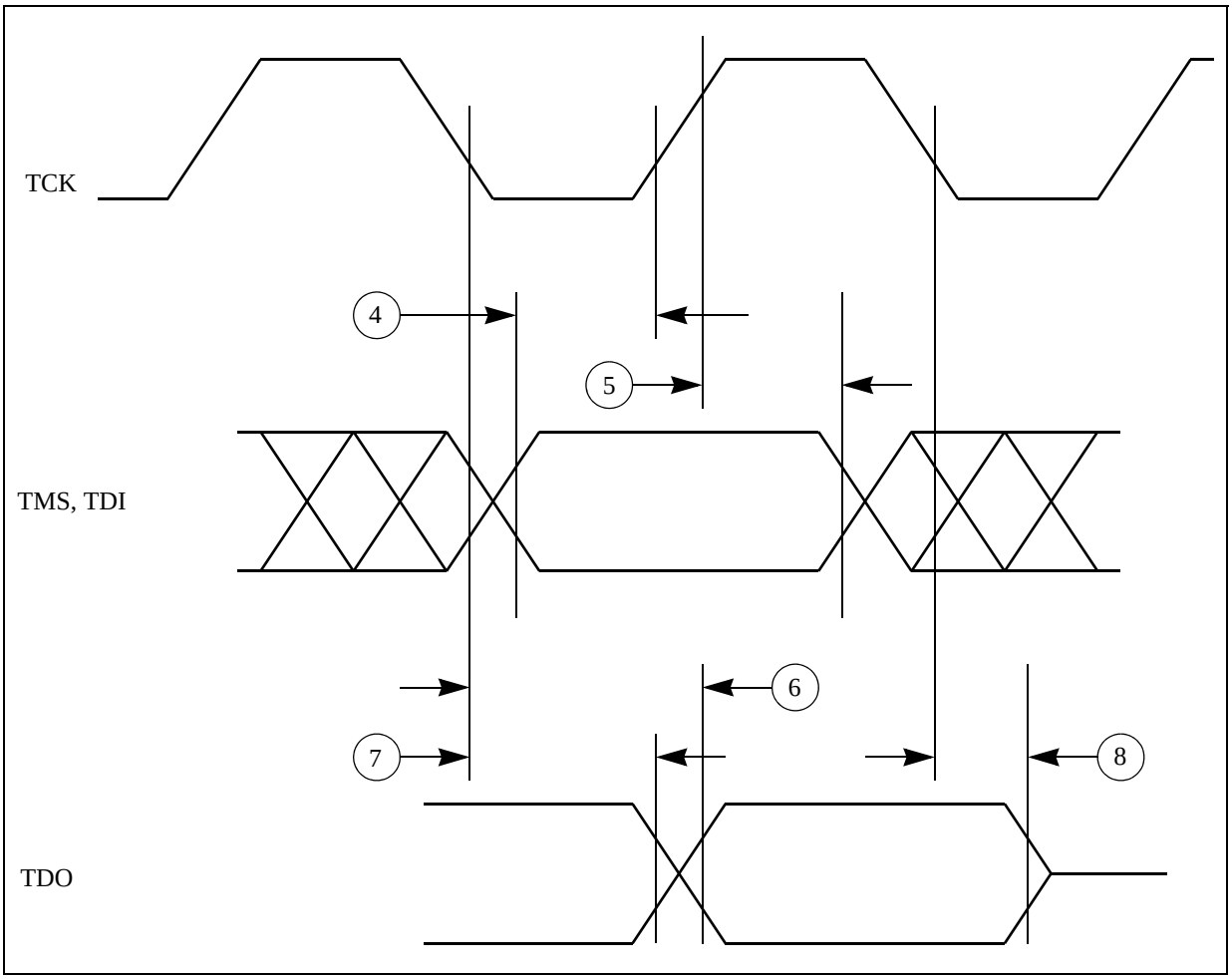


Figure 23. JTAG JCOMP timing

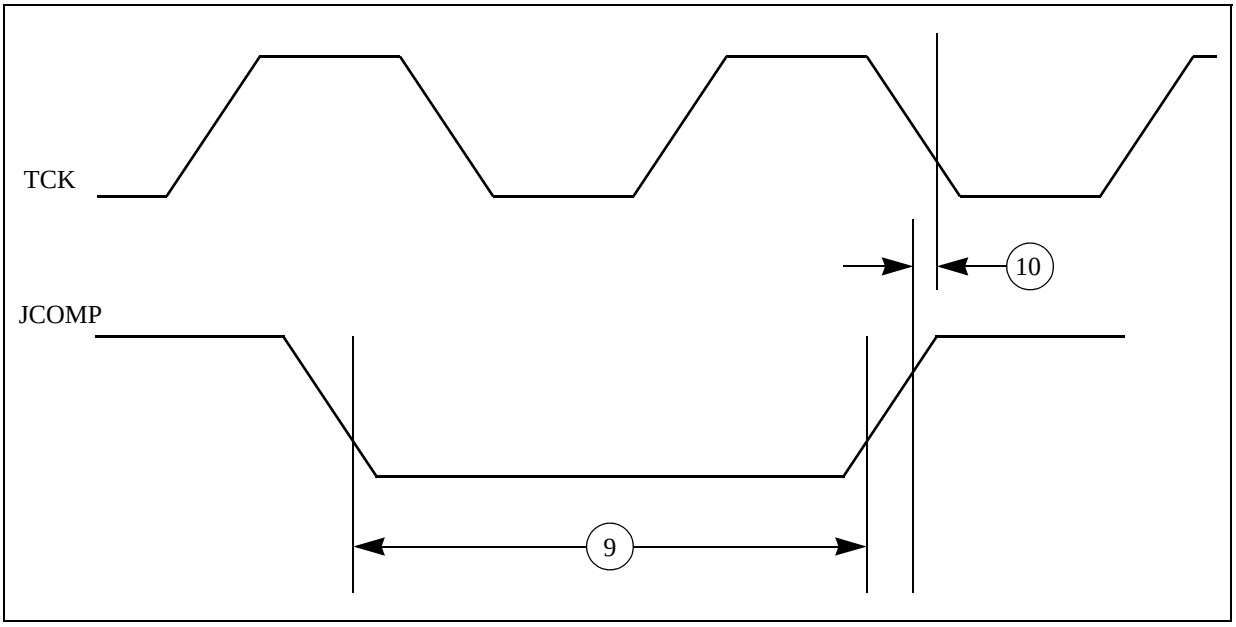
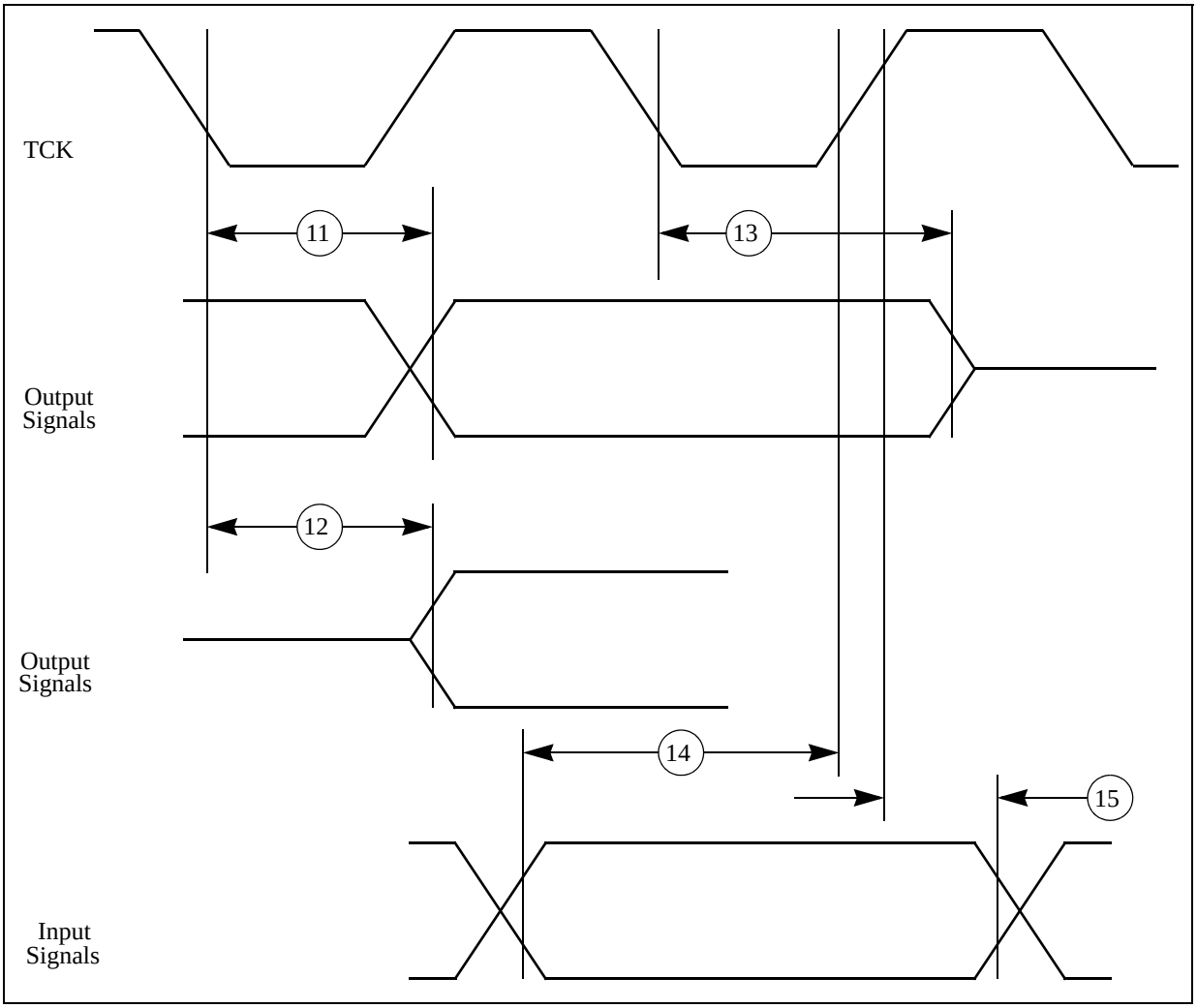


Figure 24. JTAG boundary scan timing



3.17.1.2 Nexus interface timing

Table 44. Nexus debug port timing(1)

#	Symbol		C	Characteristic	Value		Unit
					Min	Max	
7	t_{EVTIPW}	CC	P	$\overline{EVTI}$ pulse width	4	—	t_{CYC}(2)
8	t_{EVTOPW}	CC	P	$\overline{EVTO}$ pulse width	40	—	ns
9	t_{TCYC}	CC	D	TCK cycle time	2(3), (4)	—	t_{CYC}(2)
9	t_{TCYC}	CC	D	Absolute minimum TCK cycle time(5) (TDO sampled on posedge of TCK)	40(6)	—	ns
11(7)	t_{NTDIS}	CC	D	TDI/TDIC data setup time	5	—	ns
12	t_{NTDIH}	CC	D	TDI/TDIC data hold time	5	—	ns

Table 44. Nexus debug port timing(1)(Continued)

#	Symbol		C	Characteristic	Value		Unit
					Min	Max	
13(8)	t_{NTMSS}	CC	D	TMS/TMSC data setup time	5	—	ns
14	t_{NTMSH}	CC	D	TMS/TMSC data hold time	5	—	ns
15(9)	—	CC	D	TDO/TDOC propagation delay from falling edge of TCK(10)	—	16	ns
16	—	CC	D	TDO/TDOC hold time with respect to TCK falling edge (minimum TDO/TDOC propagation delay)	2.25	—	ns

1. Nexus timing specified at $V_{DD\_HV\_IO\_JTAG}$ = 4.0 V to 5.5 V, and maximum loading per pad type as specified in the I/O section of the data sheet.
2. t_{CYC} is system clock period.
3. Achieving the absolute minimum TCK cycle time may require a maximum clock speed (system frequency / 8) that is less than the maximum functional capability of the design (system frequency / 4) depending on the actual peripheral frequency being used. To ensure proper operation TCK frequency should be set to the peripheral frequency divided by a number greater than or equal to that specified here.
4. This is a functionally allowable feature. However, it may be limited by the maximum frequency specified by the Absolute minimum TCK period specification.
5. This timing applies to TDI/TDIC, TDO/TDOC, TMS/TMSC pins; however, actual frequency is limited by pad type for EXTEST instructions. Refer to pad specification for allowed transition frequency.
6. This may require a maximum clock speed (system frequency / 8) that is less than the maximum functional capability of the design (system frequency / 4) depending on the actual system frequency being used.
7. TDIC represents the TDI bit frame of the scan packet in compact JTAG 2-wire mode.
8. TMSC represents the TMS bit frame of the scan packet in compact JTAG 2-wire mode.
9. TDOC represents the TDO bit frame of the scan packet in compact JTAG 2-wire mode.
10. Timing includes TCK pad delay, clock tree delay, logic delay and TDO/TDOC output pad delay.

Figure 25. Nexus event trigger and test clock timings

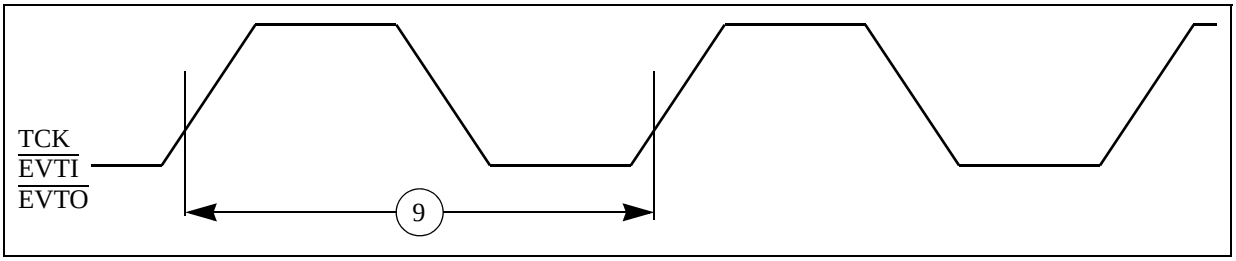
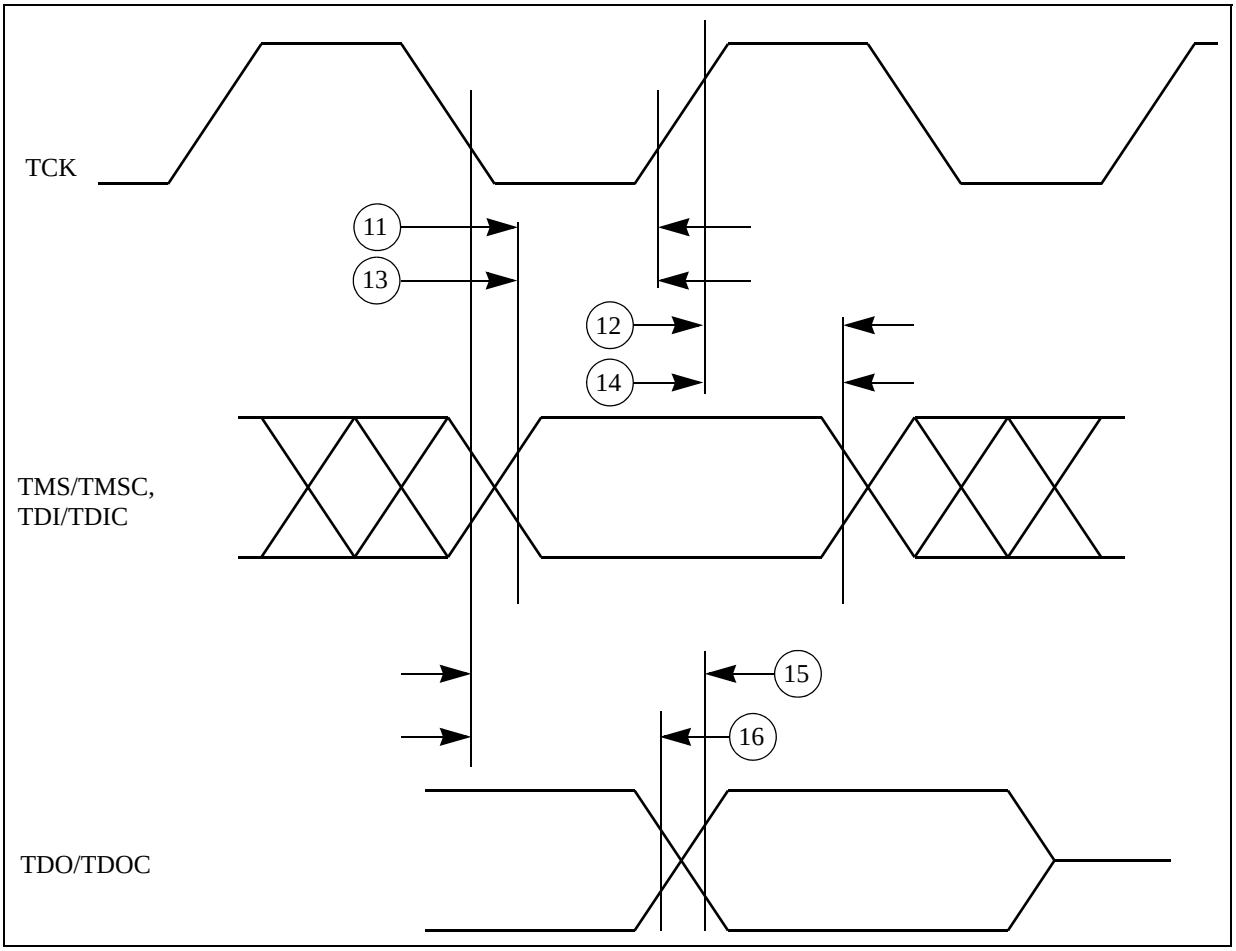


Figure 26. Nexus TDI/TDIC, TMS/TMSC, TDO/TDOC timing



3.17.1.3 Aurora LVDS interface timing

Table 45. Aurora LVDS interface timing specifications

Symbol		C	Parameter	Value			Unit
				Min	Typ	Max	
Data Rate							
—	SR	T	Data rate	—	—	1250	Mbps
STARTUP							
t_{STRT_BIAS}	CC	T	Bias startup time(1)	—	—	5	µs
t_{STRT_TX}	CC	T	Transmitter startup time(2)	—	—	5	µs
t_{STRT_RX}	CC	T	Receiver startup time(3)	—	—	4	µs

1. Startup time is defined as the time taken by LVDS current reference block for settling bias current after its pwr_down (power down) has been deasserted. LVDS functionality is guaranteed only after the startup time.
2. Startup time is defined as the time taken by LVDS transmitter for settling after its pwr_down (power down) has been deasserted. Here it is assumed that current reference is already stable (see Bias start-up time). LVDS functionality is guaranteed only after the startup time.

3. Startup time is defined as the time taken by LVDS receiver for settling after its pwr_down (power down) has been deasserted. Here it is assumed that current reference is already stable (see Bias start-up time). LVDS functionality is guaranteed only after the startup time.

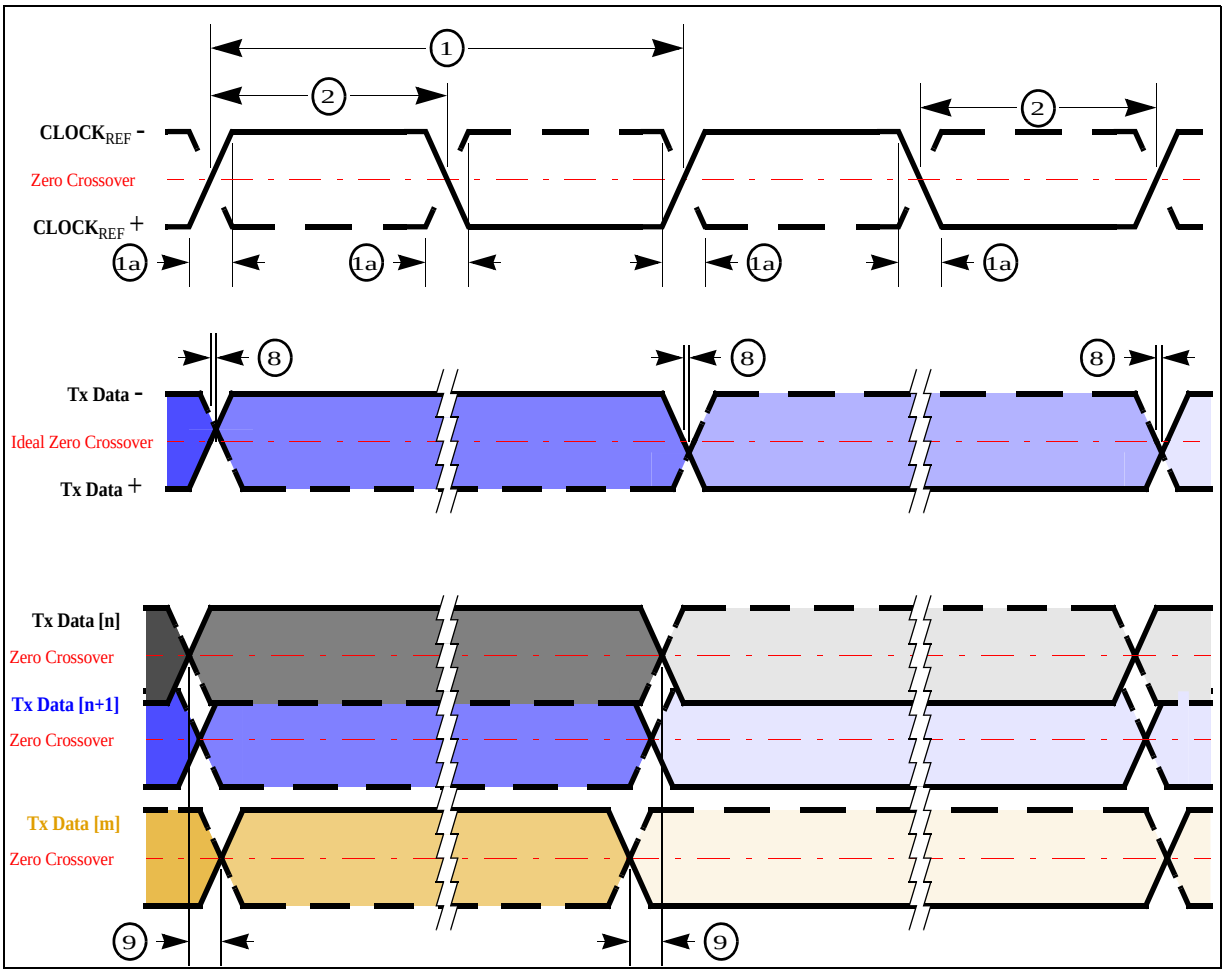
3.17.1.4 Aurora debug port timing

Table 46. Aurora debug port timing

#	Symbol		C	Characteristic		Value		Unit
						Min	Max	
1	t_{REFCLK}	CC	T	Reference clock frequency		625	1250	MHz
1a	t_{MCYC}	CC	T	Reference clock rise/fall time		—	400	ps
2	t_{RCDC}	CC	D	Reference clock duty cycle		45	55	%
3	J_{RC}	CC	D	Reference clock jitter		—	40	ps
4	$t_{STABILITY}$	CC	D	Reference clock stability		50	—	PPM
5	BER	CC	D	Bit error rate		—	10^{-12}	—
6	J_D	SR	D	Transmit lane deterministic jitter		—	0.17	OUI
7	J_T	SR	D	Transmit lane total jitter		—	0.35	OUI
8	S_O	CC	T	Differential output skew		—	20	ps
9	S_{MO}	CC	T	Lane to lane output skew		—	1000	ps
10	OUI	CC	D	Aurora lane unit interval(1)	625 Mbps	1600	1600	ps
			D		1.25 Gbps	800	800	

1. ± 100 PPM

Figure 27. Aurora timings



3.17.2 DSPI timing with CMOS and LVDS[a] pads

DSPI channel frequency support is shown in *Table 47*. Timing specifications are shown in *Table 48*, *Table 49*, *Table 50*, *Table 51* and *Table 52*.

Table 47. DSPI channel frequency support

DSPI use mode		Max usable frequency (MHz)[1],[2]
CMOS (Master mode)	Full duplex – Classic timing (*Table 48*)	17
	Full duplex – Modified timing (*Table 49*)	30
	Output only mode (SCK/SOUT/PCS) (*Table 48* and *Table 49*)	30
	Output only mode TSB mode (SCK/SOUT/PCS) (*Table 52*)	30

a. DSPI in TSB mode with LVDS pads can be used to implement Micro Second Channel bus protocol.

Table 47. DSPI channel frequency support(Continued)

DSPI use mode		Max usable frequency (MHz)[1],[2]
LVDS (Master mode)	Full duplex – Modified timing (*Table 50*)	33
	Output only mode TSB mode (SCK/SOUT/PCS) (*Table 51*)	40
CMOS Slave mode	Full duplex (*Table 53*)	16

1. Maximum usable frequency can be achieved if used with fastest configuration of the highest drive pads.
2. Maximum usable frequency does not take into account external device propagation delay.

3.17.2.1 DSPI master mode full duplex timing with CMOS and LVDS pads

3.17.2.1.1 DSPI CMOS Master Mode – Classic Timing

Table 48. DSPI CMOS master classic timing (full duplex and output only) – MTFE = 0, CPHA = 0 or 1[1]

#	Symbol		C	Characteristic	Condition		Value[2]		Unit
					Pad drive[3]	Load (C_L)	Min	Max	
1	t_{SCK}	CC	D	SCK cycle time	SCK drive strength				
					Very strong	25 pF	33.0	—	ns
					Strong	50 pF	80.0	—	
					Medium	50 pF	200.0	—	
2	t_{CSC}	CC	D	PCS to SCK delay	SCK and PCS drive strength				
					Very strong	25 pF	$(N^{(4)} \times t_{SYS}^{(5)}) - 16$	—	ns
					Strong	50 pF	$(N^{(4)} \times t_{SYS}^{(5)}) - 16$	—	
					Medium	50 pF	$(N^{(4)} \times t_{SYS}^{(5)}) - 16$	—	
					PCS medium and SCK strong	PCS = 50 pF SCK = 50 pF	$(N^{(4)} \times t_{SYS}^{(5)}) - 29$	—	
3	t_{ASC}	CC	D	After SCK delay	SCK and PCS drive strength				
					Very strong	PCS = 0 pF SCK = 50 pF	$(M^{(6)} \times t_{SYS}^{(5)}) - 35$	—	ns
					Strong	PCS = 0 pF SCK = 50 pF	$(M^{(6)} \times t_{SYS}^{(5)}) - 35$	—	
					Medium	PCS = 0 pF SCK = 50 pF	$(M^{(6)} \times t_{SYS}^{(5)}) - 35$	—	
					PCS medium and SCK strong	PCS = 0 pF SCK = 50 pF	$(M^{(6)} \times t_{SYS}^{(5)}) - 35$	—	

Table 48. DSPI CMOS master classic timing (full duplex and output only) – MTFE = 0, CPHA = 0 or 1[1](Continued)

#	Symbol		C	Characteristic	Condition		Value[2]		Unit
					Pad drive[3]	Load (C_L)	Min	Max	
4	t_{SDC}	CC	D	SCK duty cycle[7]	SCK drive strength				
					Very strong	0 pF	$^1/_2t_{SCK} - 2$	$^1/_2t_{SCK} + 2$	ns
					Strong	0 pF	$^1/_2t_{SCK} - 2$	$^1/_2t_{SCK} + 2$	
					Medium	0 pF	$^1/_2t_{SCK} - 5$	$^1/_2t_{SCK} + 5$	
PCS strobe timing									
5	t_{PCSC}	CC	D	PCSx to $\overline{PCSS}$ time[8]	PCS and PCSS drive strength				
					Strong	25 pF	16.0	—	ns
6	t_{PASC}	CC	D	$\overline{PCSS}$ to PCSx time[8]	PCS and PCSS drive strength				
					Strong	25 pF	16.0	—	ns
SIN setup time									
7	t_{SUI}	CC	D	SIN setup time to SCK[9]	SCK drive strength				
					Very strong	25 pF	25.0	—	ns
					Strong	50 pF	31.0	—	
					Medium	50 pF	52.0	—	
SIN hold time									
8	t_{HI}	CC	D	SIN hold time from SCK[9]	SCK drive strength				
					Very strong	0 pF	–1.0	—	ns
					Strong	0 pF	–1.0	—	
					Medium	0 pF	–1.0	—	
SOUT data valid time (after SCK edge)									
9	t_{SUO}	CC	D	SOUT data valid time from SCK[10]	SOUT and SCK drive strength				
					Very strong	25 pF	—	7.0	ns
					Strong	50 pF	—	8.0	
					Medium	50 pF	—	16.0	
SOUT data hold time (after SCK edge)									
10	t_{HO}	CC	D	SOUT data hold time after SCK[10]	SOUT and SCK drive strength				
					Very strong	25 pF	–7.7	—	ns
					Strong	50 pF	–11.0	—	
					Medium	50 pF	–15.0	—	

1. All output timing is worst case and includes the mismatching of rise and fall times of the output pads.
2. All timing values for output signals in this table are measured to 50% of the output voltage.
3. Timing is guaranteed to same drive capabilities for all signals, mixing of pad drives may reduce operating speeds and may cause incorrect operation.

4. N is the number of clock cycles added to time between PCS assertion and SCK assertion and is software programmable using DSPI_CTARx[PSSCK] and DSPI_CTARx[CSSCK]. The minimum value is 2 cycles unless TSB mode or Continuous SCK clock mode is selected, in which case, N is automatically set to 0 clock cycles (PCS and SCK are driven by the same edge of DSPI_CLKn).
5. t_{SYS} is the period of DSPI_CLKn clock, the input clock to the DSPI module. Maximum frequency is 100 MHz (min t_{SYS} = 10 ns).
6. M is the number of clock cycles added to time between SCK negation and PCS negation and is software programmable using DSPI_CTARx[PASC] and DSPI_CTARx[ASC]. The minimum value is 2 cycles unless TSB mode or Continuous SCK clock mode is selected, in which case, M is automatically set to 0 clock cycles (PCS and SCK are driven by the same edge of DSPI_CLKn).
7. t_{SDC} is only valid for even divide ratios. For odd divide ratios the fundamental duty cycle is not 50:50. For these odd divide ratios cases, the absolute spec number is applied as jitter/uncertainty to the nominal high time and low time.
8. PCSx and PCSS using same pad configuration.
9. Input timing assumes an input slew rate of 1 ns (10% – 90%) and uses TTL / Automotive voltage thresholds.
10. SOUT Data Valid and Data hold are independent of load capacitance if SCK and SOUT load capacitances are the same value.

Figure 28. DSPI CMOS master mode – classic timing, CPHA = 0

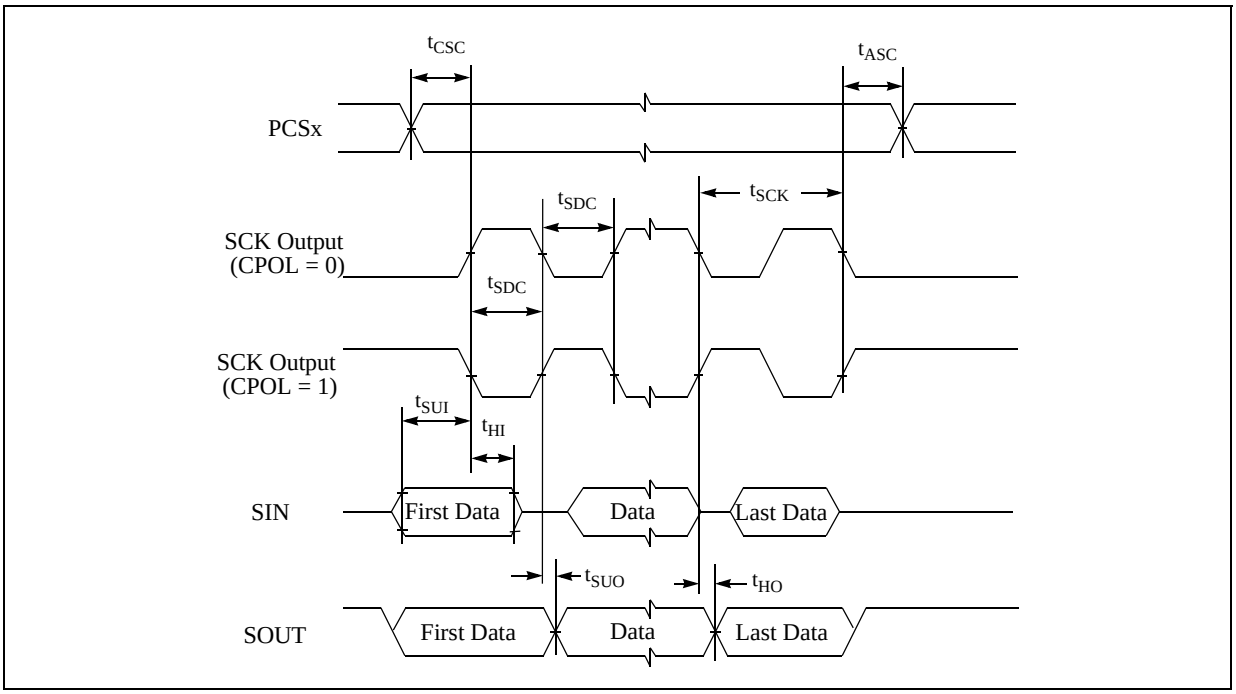


Figure 29. DSPI CMOS master mode – classic timing, CPHA = 1

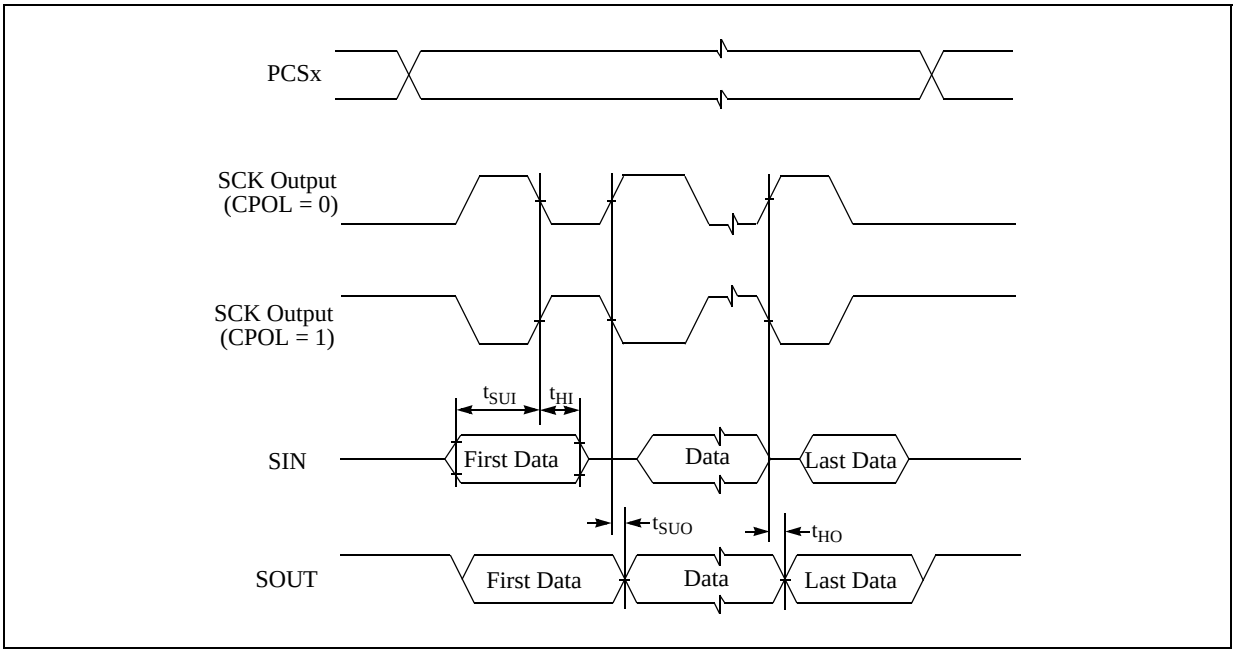
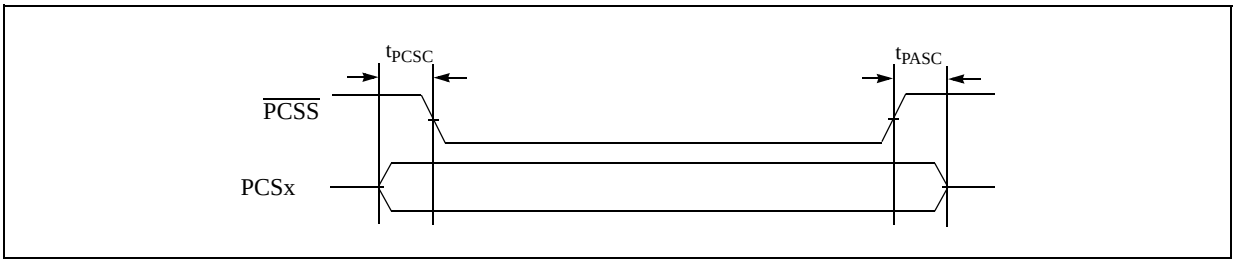


Figure 30. DSPI PCS strobe ($\overline{\text{PCSS}}$) timing (master mode)



3.17.2.1.2 DSPI CMOS Master Mode – Modified Timing

Table 49. DSPI CMOS master modified timing (full duplex and output only) – MTFE = 1, CPHA = 0 or 1(1)

#	Symbol		C	Characteristic	Condition		Value(2)		Unit
					Pad drive(3)	Load (C_L)	Min	Max	
1	t_{SCK}	CC	D	SCK cycle time	SCK drive strength				
					Very strong	25 pF	33.0	—	ns
					Strong	50 pF	80.0	—	
					Medium	50 pF	200.0	—	

Table 49. DSPI CMOS master modified timing (full duplex and output only) – MTFE = 1, CPHA = 0 or 1[1](Continued)

#	Symbol		C	Characteristic	Condition		Value[2]		Unit
					Pad drive[3]	Load (C_L)	Min	Max	
2	t_{CSC}	CC	D	PCS to SCK delay	SCK and PCS drive strength				
					Very strong	25 pF	($N^{(4)}$ × $t_{SYS}^{(5)}$) – 16	—	ns
					Strong	50 pF	($N^{(4)}$ × $t_{SYS}^{(5)}$) – 16	—	
					Medium	50 pF	($N^{(4)}$ × $t_{SYS}^{(5)}$) – 16	—	
					PCS medium and SCK strong	PCS = 50 pF SCK = 50 pF	($N^{(4)}$ × $t_{SYS}^{(5)}$) – 29	—	
3	t_{ASC}	CC	D	After SCK delay	SCK and PCS drive strength				
					Very strong	PCS = 0 pF SCK = 50 pF	($M^{(6)}$ × $t_{SYS}^{(5)}$) – 35	—	ns
					Strong	PCS = 0 pF SCK = 50 pF	($M^{(6)}$ × $t_{SYS}^{(5)}$) – 35	—	
					Medium	PCS = 0 pF SCK = 50 pF	($M^{(6)}$ × $t_{SYS}^{(5)}$) – 35	—	
					PCS medium and SCK strong	PCS = 0 pF SCK = 50 pF	($M^{(6)}$ × $t_{SYS}^{(5)}$) – 35	—	
4	t_{SDC}	CC	D	SCK duty cycle[7]	SCK drive strength				
					Very strong	0 pF	$^1/_2t_{SCK}$ – 2	$^1/_2t_{SCK}$ + 2	ns
					Strong	0 pF	$^1/_2t_{SCK}$ – 2	$^1/_2t_{SCK}$ + 2	
					Medium	0 pF	$^1/_2t_{SCK}$ – 5	$^1/_2t_{SCK}$ + 5	
PCS strobe timing									
5	t_{PCSC}	CC	D	PCSx to $\overline{\text{PCSS}}$ time[8]	PCS and PCSS drive strength				
					Strong	25 pF	16.0	—	ns
6	t_{PASC}	CC	D	$\overline{\text{PCSS}}$ to PCSx time[8]	PCS and PCSS drive strength				
					Strong	25 pF	16.0	—	ns
SIN setup time									

Table 49. DSPI CMOS master modified timing (full duplex and output only) – MTFE = 1, CPHA = 0 or 1[1](Continued)

#	Symbol		C	Characteristic	Condition		Value[2]		Unit
					Pad drive[3]	Load (C_L)	Min	Max	
7	t_{SUI}	CC	D	SIN setup time to SCK CPHA = 0[9]	SCK drive strength				
					Very strong	25 pF	25 – (P[10] × t_{SYS}[5])	—	ns
					Strong	50 pF	31 – (P[10] × t_{SYS}[5])	—	
					Medium	50 pF	52 – (P[10] × t_{SYS}[5])	—	
				SIN setup time to SCK CPHA = 1[9]	SCK drive strength				
					Very strong	25 pF	25.0	—	ns
					Strong	50 pF	31.0	—	
					Medium	50 pF	52.0	—	
SIN hold time									
8	t_{HI}	CC	D	SIN hold time from SCK CPHA = 0[9]	SCK drive strength				
					Very strong	0 pF	– 1 + (P[9] × t_{SYS}[4])	—	ns
					Strong	0 pF	– 1 + (P[9] × t_{SYS}[4])	—	
					Medium	0 pF	– 1 + (P[9] × t_{SYS}[4])	—	
				SIN hold time from SCK CPHA = 1[9]	SCK drive strength				
					Very strong	0 pF	–1.0	—	ns
					Strong	0 pF	–1.0	—	
					Medium	0 pF	–1.0	—	
SOUT data valid time (after SCK edge)									
9	t_{SUO}	CC	D	SOUT data valid time from SCK CPHA = 0[10]	SOUT and SCK drive strength				
					Very strong	25 pF	—	7.0 + t_{SYS}[5]	ns
					Strong	50 pF	—	8.0 + t_{SYS}[5]	
					Medium	50 pF	—	16.0 + t_{SYS}[5]	
				SOUT data valid time from SCK CPHA = 1[10]	SOUT and SCK drive strength				
					Very strong	25 pF	—	7.0	ns
					Strong	50 pF	—	8.0	
					Medium	50 pF	—	16.0	

Table 49. DSPI CMOS master modified timing (full duplex and output only) – MTFE = 1, CPHA = 0 or 1(1)(Continued)

#	Symbol	C	Characteristic	Condition		Value(2)		Unit
				Pad drive(3)	Load (C_L)	Min	Max	
SOUT data hold time (after SCK edge)								
10	t_{HO}	CC	D	SOUT data hold time after SCK CPHA = 0(11)	SOUT and SCK drive strength			
					Very strong	25 pF	–7.7 + t_{SYS}(5)	—	ns
					Strong	50 pF	–11.0 + t_{SYS}(5)	—	
					Medium	50 pF	–15.0 + t_{SYS}(5)	—	
				SOUT data hold time after SCK CPHA = 1(11)	SOUT and SCK drive strength			
					Very strong	25 pF	–7.7	—	ns
					Strong	50 pF	–11.0	—	
					Medium	50 pF	–15.0	—	

1. All output timing is worst case and includes the mismatching of rise and fall times of the output pads.
2. All timing values for output signals in this table are measured to 50% of the output voltage.
3. Timing is guaranteed to same drive capabilities for all signals, mixing of pad drives may reduce operating speeds and may cause incorrect operation.
4. N is the number of clock cycles added to time between PCS assertion and SCK assertion and is software programmable using DSPI_CTARx[PSSCK] and DSPI_CTARx[CSSCK]. The minimum value is 2 cycles unless TSB mode or Continuous SCK clock mode is selected, in which case, N is automatically set to 0 clock cycles (PCS and SCK are driven by the same edge of DSPI_CLKn).
5. t_{SYS} is the period of DSPI_CLKn clock, the input clock to the DSPI module. Maximum frequency is 100 MHz (min t_{SYS} = 10 ns).
6. M is the number of clock cycles added to time between SCK negation and PCS negation and is software programmable using DSPI_CTARx[PASC] and DSPI_CTARx[ASC]. The minimum value is 2 cycles unless TSB mode or Continuous SCK clock mode is selected, in which case, M is automatically set to 0 clock cycles (PCS and SCK are driven by the same edge of DSPI_CLKn).
7. t_{SDC} is only valid for even divide ratios. For odd divide ratios the fundamental duty cycle is not 50:50. For these odd divide ratios cases, the absolute spec number is applied as jitter/uncertainty to the nominal high time and low time.
8. PCSx and PCSS using same pad configuration.
9. Input timing assumes an input slew rate of 1 ns (10% – 90%) and uses TTL / Automotive voltage thresholds.
10. P is the number of clock cycles added to delay the DSPI input sample point and is software programmable using DSPI_MCR[SMPL_PT]. The value must be 0, 1 or 2. If the baud rate divide ratio is /2 or /3, this value is automatically set to 1.
11. SOUT Data Valid and Data hold are independent of load capacitance if SCK and SOUT load capacitances are the same value.

Figure 31. DSPI CMOS master mode – modified timing, CPHA = 0

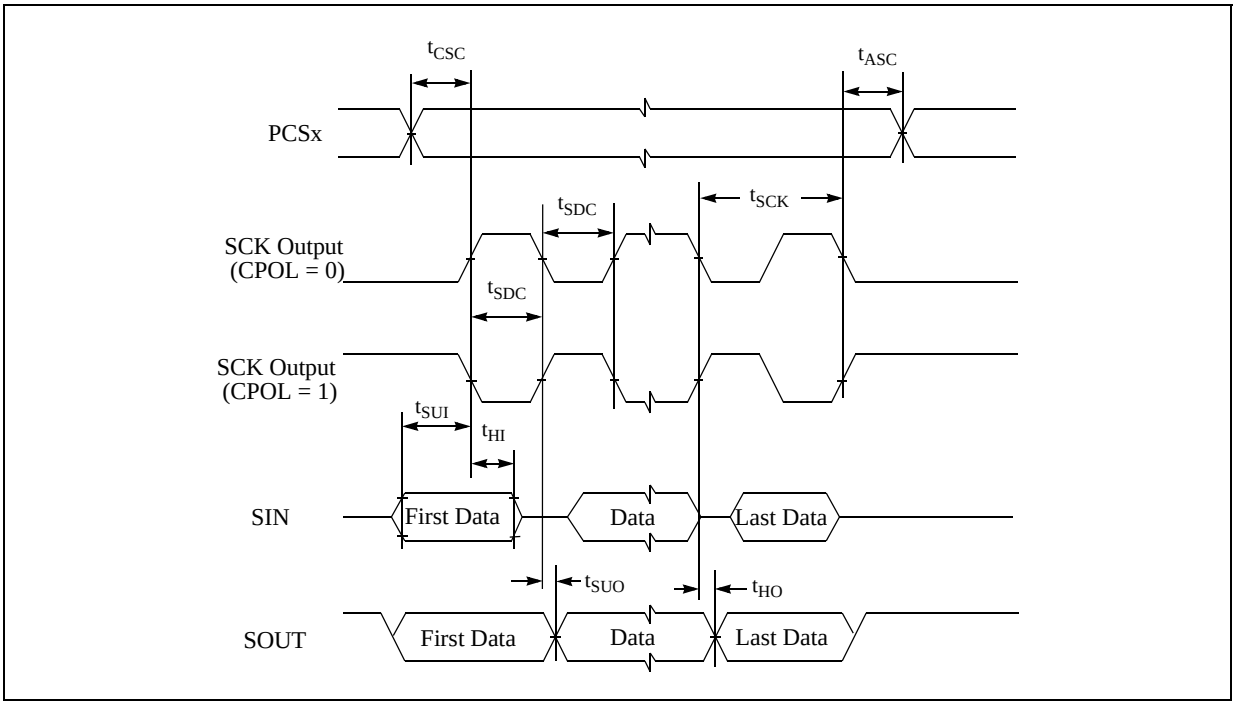


Figure 32. DSPI CMOS master mode – modified timing, CPHA = 1

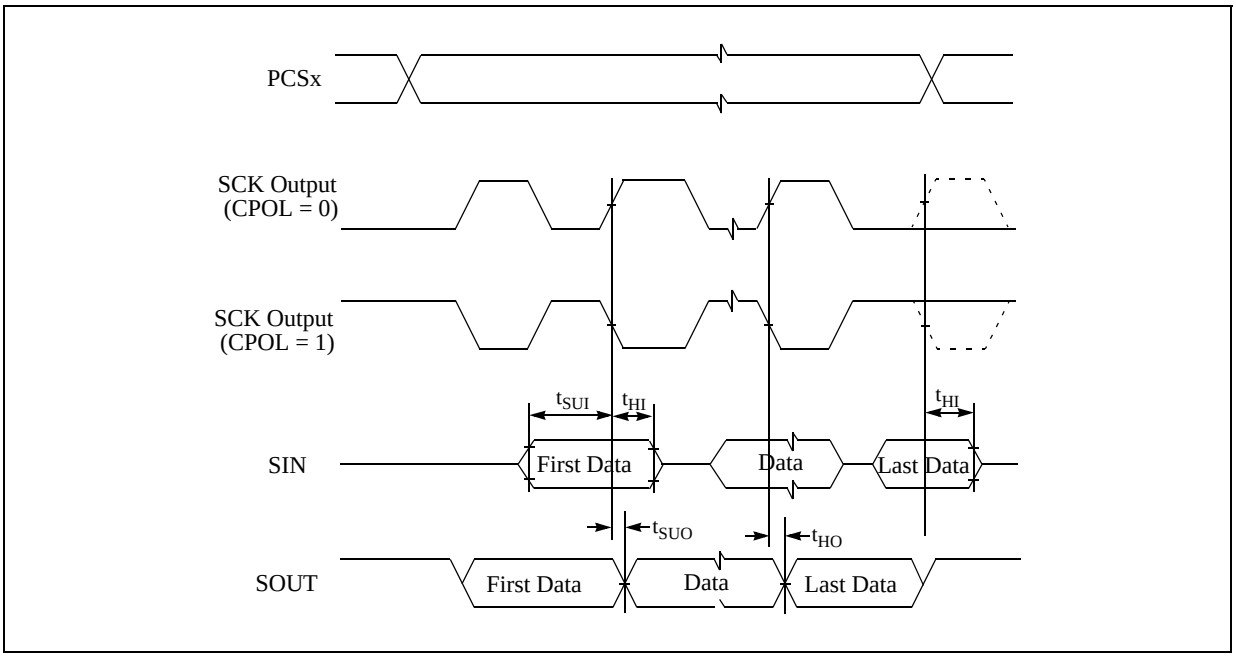
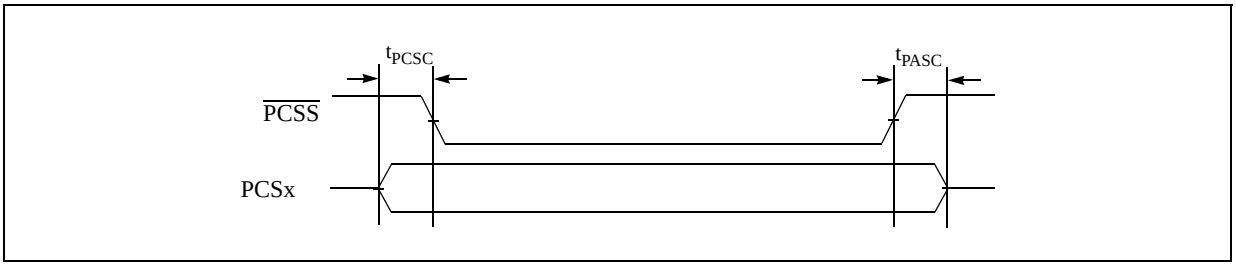


Figure 33. DSPI PCS strobe ($\overline{PCSS}$) timing (master mode)



3.17.2.1.3 DSPI LVDS Master Mode – Modified Timing

Table 50. DSPI LVDS master timing – full duplex – modified transfer format (MTFE = 1), CPHA = 0 or 1

#	Symbol		C	Characteristic	Condition		Value(1)		Unit
					Pad drive	Load	Min	Max	
1	t_{SCK}	CC	D	SCK cycle time	LVDS	15 pF to 25 pF differential	30.0	—	ns
2	t_{CSC}	CC	D	PCS to SCK delay (LVDS SCK)	PCS drive strength				
					Very strong	25 pF	$(N^{(2)} \times t_{SYS}^{(3)}) - 10$	—	ns
					Strong	50 pF	$(N^{(2)} \times t_{SYS}^{(3)}) - 10$	—	ns
					Medium	50 pF	$(N^{(2)} \times t_{SYS}^{(3)}) - 32$	—	ns
3	t_{ASC}	CC	D	After SCK delay (LVDS SCK)	Very strong	PCS = 0 pF SCK = 25 pF	$(M^{(4)} \times t_{SYS}^{(3)}) - 8$	—	ns
					Strong	PCS = 0 pF SCK = 25 pF	$(M^{(4)} \times t_{SYS}^{(3)}) - 8$	—	ns
					Medium	PCS = 0 pF SCK = 25 pF	$(M^{(4)} \times t_{SYS}^{(3)}) - 8$	—	ns
4	t_{SDC}	CC	D	SCK duty cycle(5)	LVDS	15 pF to 25 pF differential	$^1/_2t_{SCK} - 2$	$^1/_2t_{SCK} + 2$	ns
7	t_{SUI}	CC	D	SIN setup time					
				SIN setup time to SCK CPHA = 0(6)	SCK drive strength				
					LVDS	15 pF to 25 pF differential	$23 - (P^{(7)} \times t_{SYS}^{(3)})$	—	ns
				SIN setup time to SCK CPHA = 1(6)	SCK drive strength				
					LVDS	15 pF to 25 pF differential	23	—	ns

Table 50. DSPI LVDS master timing – full duplex – modified transfer format (MTFE = 1), CPHA = 0 or 1(Continued)

#	Symbol		C	Characteristic	Condition		Value[1]		Unit
					Pad drive	Load	Min	Max	
8	t_{HI}	CC	D	SIN Hold Time					
				SIN hold time from SCK CPHA = 0[6]	SCK drive strength				
					LVDS	0 pF differential	– 1 + ($P^{(7)}$ × $t_{SYS}^{(3)}$)	—	ns
				SIN hold time from SCK CPHA = 1[6]	SCK drive strength				
					LVDS	0 pF differential	–1	—	ns
9	t_{SUO}	CC	D	SOUT data valid time (after SCK edge)					
				SOUT data valid time from SCK CPHA = 0[8]	SOUT and SCK drive strength				
					LVDS	15 pF to 25 pF differential	—	7.0 + $t_{SYS}^{(3)}$	ns
				SOUT data valid time from SCK CPHA = 1[8]	SOUT and SCK drive strength				
					LVDS	15 pF to 25 pF differential	—	7.0	ns
10	t_{HO}	CC	D	SOUT data hold time (after SCK edge)					
				SOUT data hold time after SCK CPHA = 0[8]	SOUT and SCK drive strength				
					LVDS	15 pF to 25 pF differential	–7.5 + $t_{SYS}^{(3)}$	—	ns
				SOUT data hold time after SCK CPHA = 1[8]	SOUT and SCK drive strength				
					LVDS	15 pF to 25 pF differential	–7.5	—	ns

1. All timing values for output signals in this table are measured to 50% of the output voltage.
2. N is the number of clock cycles added to time between PCS assertion and SCK assertion and is software programmable using DSPI_CTARx[PSSCK] and DSPI_CTARx[CSSCK]. The minimum value is 2 cycles unless TSB mode or Continuous SCK clock mode is selected, in which case, N is automatically set to 0 clock cycles (PCS and SCK are driven by the same edge of DSPI_CLKn).
3. t_{SYS} is the period of DSPI_CLKn clock, the input clock to the DSPI module. Maximum frequency is 100 MHz (min t_{SYS} = 10 ns).
4. M is the number of clock cycles added to time between SCK negation and PCS negation and is software programmable using DSPI_CTARx[PASC] and DSPI_CTARx[ASC]. The minimum value is 2 cycles unless TSB mode or Continuous SCK clock mode is selected, in which case, M is automatically set to 0 clock cycles (PCS and SCK are driven by the same edge of DSPI_CLKn).
5. t_{SDC} is only valid for even divide ratios. For odd divide ratios the fundamental duty cycle is not 50:50. For these odd divide ratios cases, the absolute spec number is applied as jitter/uncertainty to the nominal high time and low time.
6. Input timing assumes an input slew rate of 1 ns (10% – 90%) and LVDS differential voltage = ±100 mV.
7. P is the number of clock cycles added to delay the DSPI input sample point and is software programmable using DSPI_MCR[SMPL_PT]. The value must be 0, 1 or 2. If the baud rate divide ratio is /2 or /3, this value is automatically set to 1.
8. SOUT Data Valid and Data hold are independent of load capacitance if SCK and SOUT load capacitances are the same value.

Figure 34. DSPI LVDS master mode – modified timing, CPHA = 0

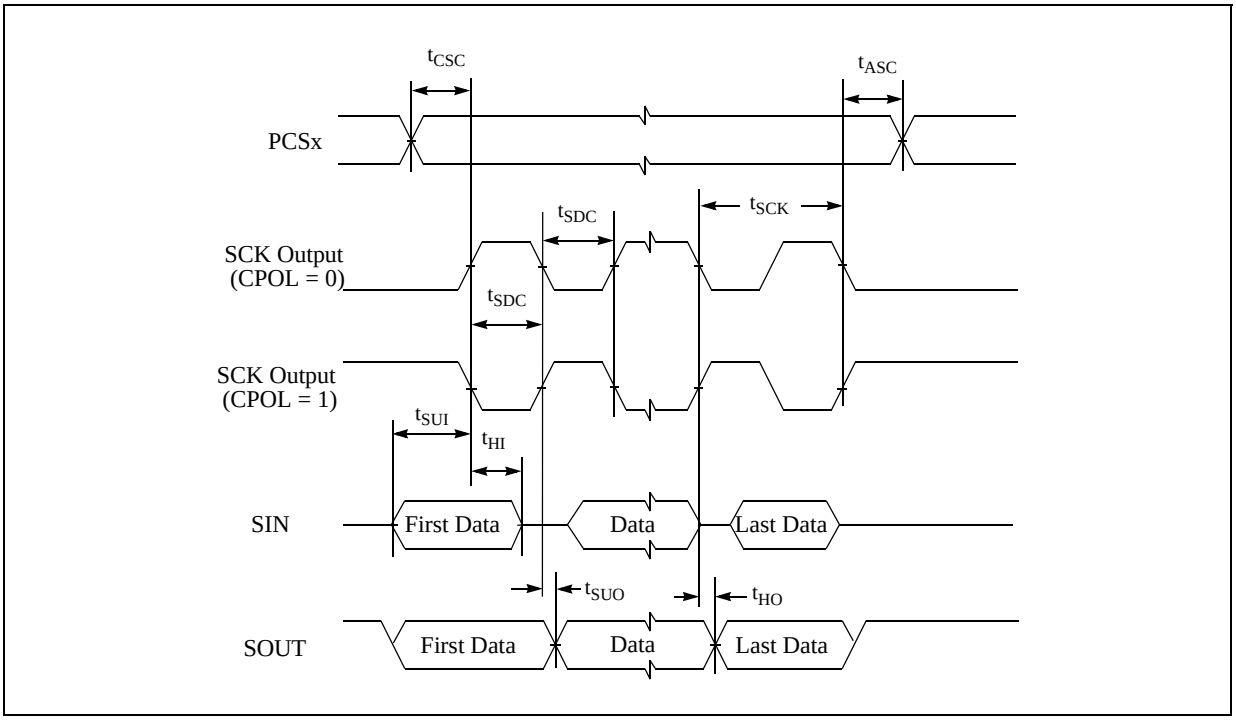
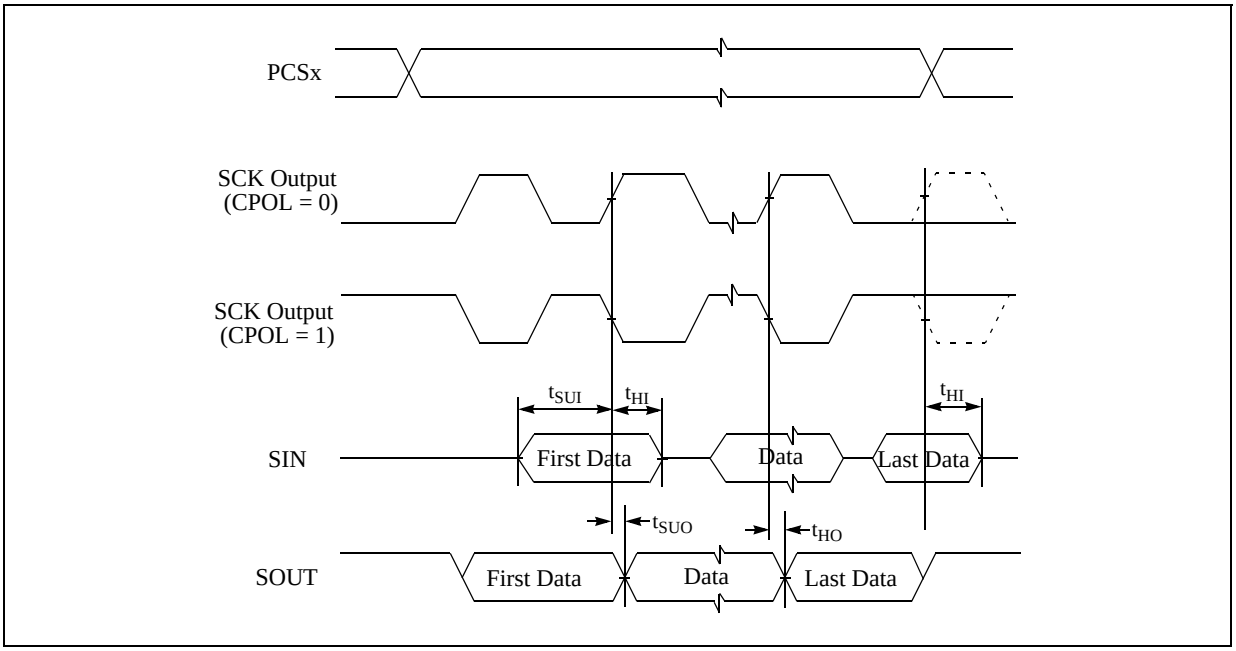


Figure 35. DSPI LVDS master mode – modified timing, CPHA = 1



3.17.2.1.4 DSPI Master Mode – Output Only

Table 51. DSPI LVDS master timing – output only – timed serial bus mode TSB = 1 or ITSB = 1, CPOL = 0 or 1, continuous SCK clock(1)(2)

#	Symbol		C	Characteristic	Condition		Value		Unit
					Pad drive	Load	Min	Max	
1	t_{SCK}	CC	D	SCK cycle time	LVDS	15 pF to 50 pF differential	25.0	—	ns
2	t_{CSV}	CC	D	PCS valid after SCK(3) (SCK with 50 pF differential load cap.)	Very strong	25 pF	—	6.0	ns
					Strong	50 pF	—	10.5	ns
3	t_{CSH}	CC	D	PCS hold after SCK(3) (SCK with 50 pF differential load cap.)	Very strong	0 pF	–4.0	—	ns
					Strong	0 pF	–4.0	—	ns
4	t_{SDC}	CC	D	SCK duty cycle (SCK with 50 pF differential load cap.)	LVDS	15 pF to 50 pF differential	$^1/_2t_{SCK} - 2$	$^1/_2t_{SCK} + 2$	ns
SOUT data valid time (after SCK edge)									
5	t_{SUO}	CC	D	SOUT data valid time from SCK(4)	SOUT and SCK drive strength				
					LVDS	15 pF to 50 pF differential	—	3.5	ns
SOUT data hold time (after SCK edge)									
6	t_{HO}	CC	D	SOUT data hold time after SCK(4)	SOUT and SCK drive strength				
					LVDS	15 pF to 50 pF differential	–3.5	—	ns

1. All DSPI timing specifications apply to pins when using LVDS pads for SCK and SOUT and CMOS pad for PCS with pad driver strength as defined. Timing may degrade for weaker output drivers.
2. TSB = 1 or ITSB = 1 automatically selects MTFE = 1 and CPHA = 1.
3. With TSB mode or Continuous SCK clock mode selected, PCS and SCK are driven by the same edge of DSPI_CLKn. This timing value is due to pad delays and signal propagation delays.
4. SOUT Data Valid and Data hold are independent of load capacitance if SCK and SOUT load capacitances are the same value.

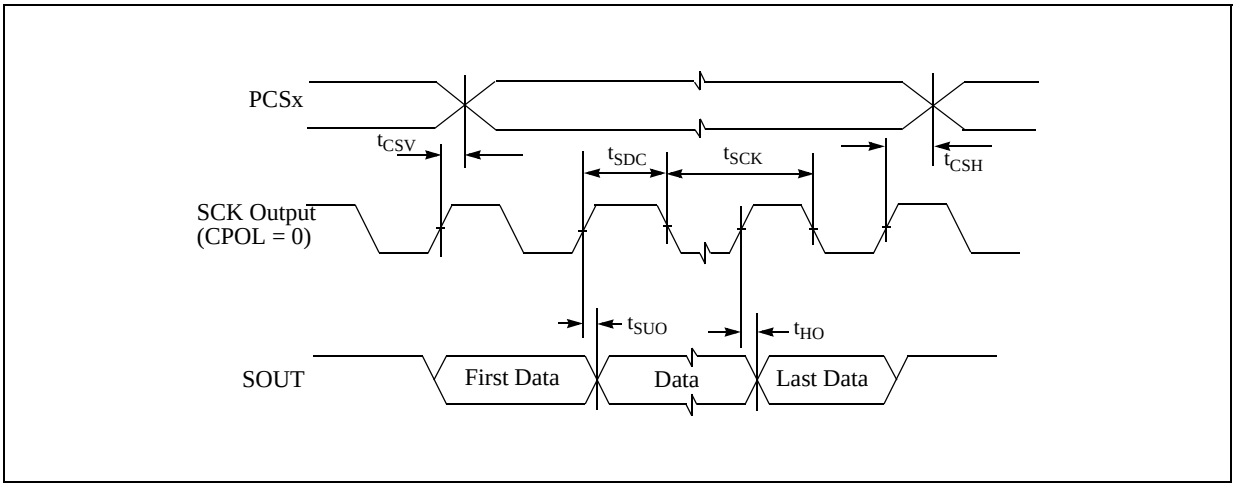
Table 52. DSPI CMOS master timing – output only – timed serial bus mode TSB = 1 or ITSB = 1, CPOL = 0 or 1, continuous SCK clock(1)(2)

#	Symbol		C	Characteristic	Condition		Value(3)		Unit
					Pad drive(4)	Load (C_L)	Min	Max	
1	t_{SCK}	CC	D	SCK cycle time	SCK drive strength				
					Very strong	25 pF	33.0	—	ns
					Strong	50 pF	80.0	—	ns
					Medium	50 pF	200.0	—	ns
2	t_{CSV}	CC	D	PCS valid after SCK(5)	SCK and PCS drive strength				
					Very strong	25 pF	7	—	ns
					Strong	50 pF	8	—	ns
					Medium	50 pF	16	—	ns
					PCS medium and SCK strong	PCS = 50 pF SCK = 50 pF	29	—	ns
3	t_{CSH}	CC	D	PCS hold after SCK(5)	SCK and PCS drive strength				
					Very strong	PCS = 0 pF SCK = 50 pF	–14	—	ns
					Strong	PCS = 0 pF SCK = 50 pF	–14	—	ns
					Medium	PCS = 0 pF SCK = 50 pF	–33	—	ns
					PCS medium and SCK strong	PCS = 0 pF SCK = 50 pF	–35	—	ns
4	t_{SDC}	CC	D	SCK duty cycle(6)	SCK drive strength				
					Very strong	0 pF	$^1/_2t_{SCK} - 2$	$^1/_2t_{SCK} + 2$	ns
					Strong	0 pF	$^1/_2t_{SCK} - 2$	$^1/_2t_{SCK} + 2$	ns
					Medium	0 pF	$^1/_2t_{SCK} - 5$	$^1/_2t_{SCK} + 5$	ns
SOUT data valid time (after SCK edge)									
9	t_{SUO}	CC	D	SOUT data valid time from SCK CPHA = 1(7)	SOUT and SCK drive strength				
					Very strong	25 pF	—	7.0	ns
					Strong	50 pF	—	8.0	ns
					Medium	50 pF	—	16.0	ns
SOUT data hold time (after SCK edge)									
10	t_{HO}	CC	D	SOUT data hold time after SCK CPHA = 1(7)	SOUT and SCK drive strength				
					Very strong	25 pF	–7.7	—	ns
					Strong	50 pF	–11.0	—	ns
					Medium	50 pF	–15.0	—	ns

1. TSB = 1 or ITSB = 1 automatically selects MTFE = 1 and CPHA = 1.

2. All output timing is worst case and includes the mismatching of rise and fall times of the output pads.
3. All timing values for output signals in this table are measured to 50% of the output voltage.
4. Timing is guaranteed to same drive capabilities for all signals, mixing of pad drives may reduce operating speeds and may cause incorrect operation.
5. With TSB mode or Continuous SCK clock mode selected, PCS and SCK are driven by the same edge of DSPI_CLKn. This timing value is due to pad delays and signal propagation delays.
6. t_{SDC} is only valid for even divide ratios. For odd divide ratios the fundamental duty cycle is not 50:50. For these odd divide ratios cases, the absolute spec number is applied as jitter/uncertainty to the nominal high time and low time.
7. SOUT Data Valid and Data hold are independent of load capacitance if SCK and SOUT load capacitances are the same value.

Figure 36. DSPI LVDS and CMOS master timing – output only – modified transfer format MTFE = 1, CHPA = 1



3.17.2.2 Slave Mode timing

Table 53. DSPI CMOS Slave timing - Modified Transfer Format (MTFE = 0/1)(1)

#	Symbol		C	Characteristic	Condition		Min	Max	Unit
					Pad Drive	Load			
1	t_{SCK}	CC	D	SCK Cycle Time(2)	—	—	62	—	ns
2	t_{CSC}	SR	D	$\overline{SS}$ to SCK Delay(2)	—	—	16	—	ns
3	t_{ASC}	SR	D	SCK to $\overline{SS}$ Delay(2)	—	—	16	—	ns
4	t_{SDC}		D	SCK Duty Cycle(2)	—	—	30	—	ns
5	t_A	CC	D	Slave Access Time(2),(3),(4) ($\overline{SS}$ active to SOUT driven)	Very Strong	25 pF	—	50	ns
					Strong	50 pF	—	50	ns
					Medium	50 pF	—	60	ns
6	t_{DIS}	CC	D	Slave SOUT Disable Time(2),(3),(4) ($\overline{SS}$ inactive to SOUT High-Z or invalid)	Very Strong	25 pF	—	5	ns
					Strong	50 pF	—	5	ns
					Medium	50 pF	—	10	ns

Table 53. DSPI CMOS Slave timing - Modified Transfer Format (MTFE = 0/1)(1)(Continued)

#	Symbol		C	Characteristic	Condition		Min	Max	Unit
					Pad Drive	Load			
9	t_{SUI}	CC	D	Data Setup Time for Inputs(2)	—	—	10	—	ns
10	t_{HI}	CC	D	Data Hold Time for Inputs(2)	—	—	10	—	ns
11	t_{SUO}	CC	D	SOUT Valid Time(2),(3),(4) (after SCK edge)	Very Strong	25 pF	—	30	ns
					Strong	50 pF	—	30	ns
					Medium	50 pF	—	50	ns
12	t_{HO}	CC	D	SOUT Hold Time(2),(3),(4) (after SCK edge)	Very Strong	25 pF	2.5	—	ns
					Strong	50 pF	2.5	—	ns
					Medium	50 pF	2.5	—	ns

1. DSPI slave operation is only supported for a single master and single slave on the device. Timing is valid for that case only.
2. Input timing assumes an input slew rate of 1 ns (10% - 90%) and uses TTL / Automotive voltage thresholds.
3. All timing values for output signals in this table, are measured to 50% of the output voltage.
4. All output timing is worst case and includes the mismatching of rise and fall times of the output pads.

3.17.3 FEC timing

The FEC provides RMII in the eLQFP176 and FusionQuad® packages. RMII signals can be configured for either CMOS or TTL signal levels compatible with devices operating at either 5.0 V or 3.3 V.

3.17.3.1 RMII serial management channel timing (MDIO and MDC)

The FEC functions correctly with a maximum MDC frequency of 2.5 MHz.

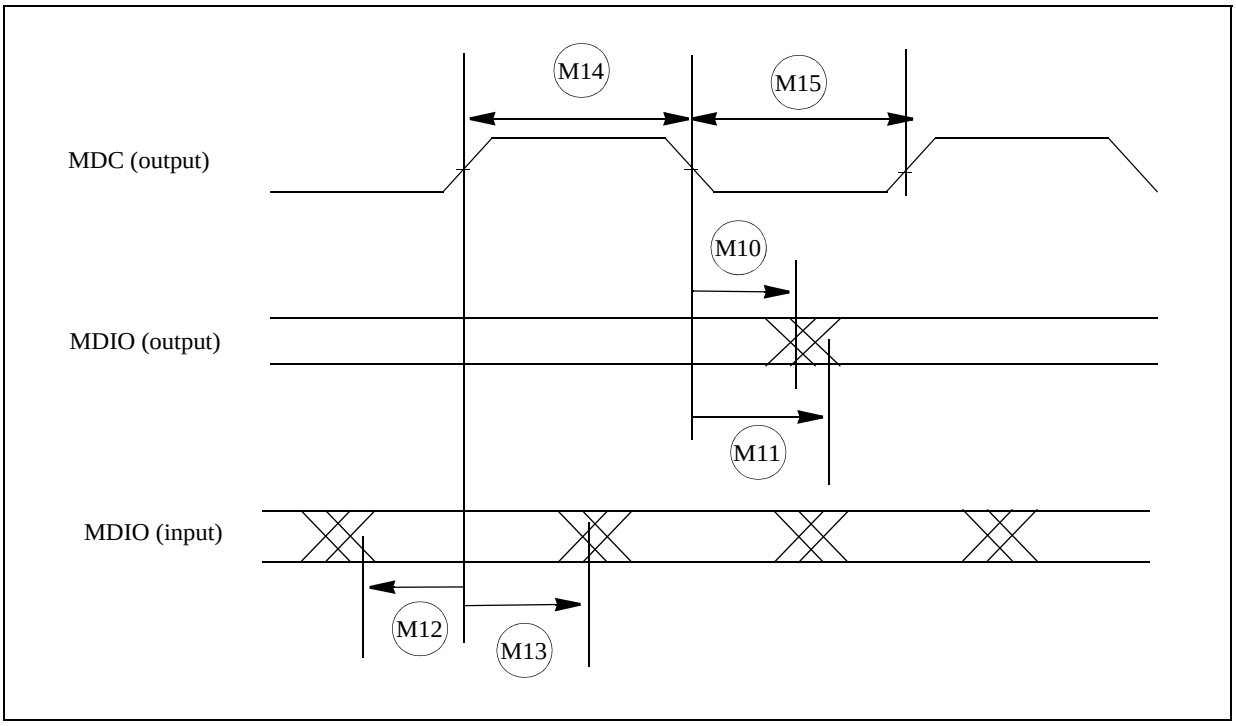
Table 54. RMII serial management channel timing(1)(2)

Symbol		C	Characteristic	Value(3)		Unit
				Min	Max	
M10	CC	D	MDC falling edge to MDIO output invalid (minimum propagation delay)	-10	—	ns
M11	CC	D	MDC falling edge to MDIO output valid (max prop delay)	—	25	ns
M12	CC	D	MDIO (input) to MDC rising edge setup	10	—	ns
M13	CC	D	MDIO (input) to MDC rising edge hold	10	—	ns
M14	CC	D	MDC pulse width high	40%	60%	MDC period
M15	CC	D	MDC pulse width low	40%	60%	MDC period

1. All timing specifications are referenced from MDC = 1.4 V (TTL levels) to the valid input and output levels, 0.8 V and 2.0 V (TTL levels). For 5 V operation, timing is referenced from MDC = 50% to 2.2 V/3.5 V input and output levels.
2. RMII timing is valid only up to a maximum of 150 ^{o}C junction temperature.

3. Output parameters are valid for C_L = 25 pF, where C_L is the external load to the device. The internal package capacitance is accounted for, and need not be subtracted from the 25 pF value. Care should be taken to align external load on MDIO and MDC.

Figure 37. RMII serial management channel timing diagram



3.17.3.2 RMII receive signal timing (RXD[1:0], CRS_DV)

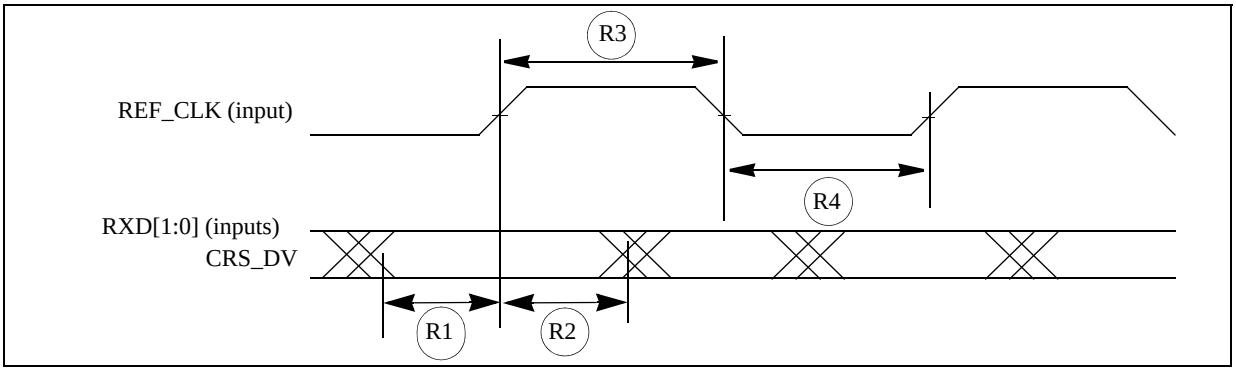
The receiver functions correctly up to a REF_CLK maximum frequency of 50 MHz +1%. There is no minimum frequency requirement. The system clock frequency must be at least equal to or greater than the RX_CLK frequency, which is half that of the REF_CLK frequency.

Table 55. RMII receive signal timing(1)(2)

Symbol		C	Characteristic	Value		Unit
				Min	Max	
R1	CC	D	RXD[1:0], CRS_DV to REF_CLK setup	4	—	ns
R2	CC	D	REF_CLK to RXD[1:0], CRS_DV hold	2	—	ns
R3	CC	D	REF_CLK pulse width high	35%	65%	REF_CLK period
R4	CC	D	REF_CLK pulse width low	35%	65%	REF_CLK period

1. All timing specifications are referenced from REF_CLK = 1.4 V to the valid input levels, 0.8 V and 2.0 V.
2. RMII timing is valid only up to a maximum of 150 ^{o}C junction temperature.

Figure 38. RMII receive signal timing diagram



3.17.3.3 RMII transmit signal timing (TXD[1:0], TX_EN)

The transmitter functions correctly up to a REF_CLK maximum frequency of 50 MHz + 1%. There is no minimum frequency requirement. The system clock frequency must be at least equal to or greater than the TX_CLK frequency, which is half that of the REF_CLK frequency.

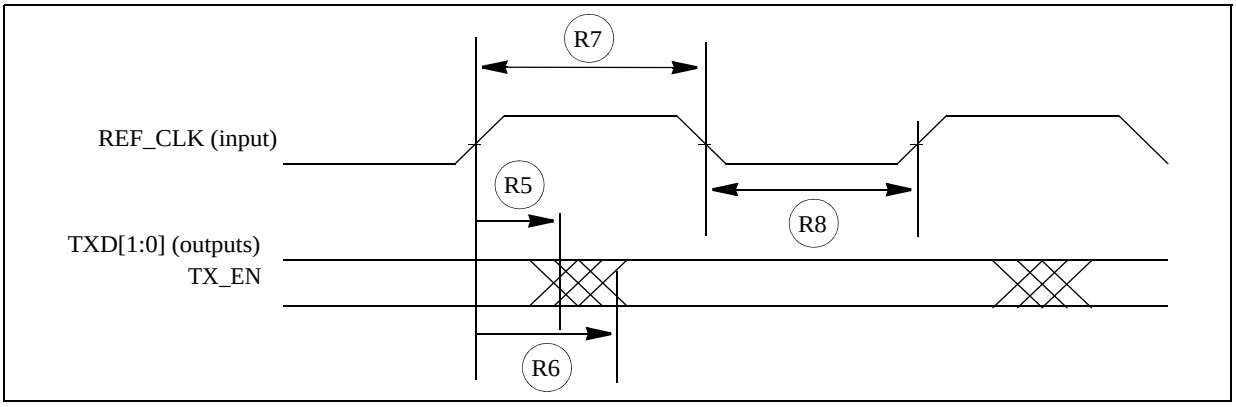
The transmit outputs (TXD[1:0], TX_EN) can be programmed to transition from either the rising or falling edge of REF_CLK, and the timing is the same in either case. This options allows the use of non-compliant RMII PHYs.

Table 56. RMII transmit signal timing(1)(2)

Symbol		C	Characteristic	Value(3)		Unit
				Min	Max	
R5	CC	D	REF_CLK to TXD[1:0], TX_EN invalid	2	—	ns
R6	CC	D	REF_CLK to TXD[1:0], TX_EN valid	—	16	ns
R7	CC	D	REF_CLK pulse width high	35%	65%	REF_CLK period
R8	CC	D	REF_CLK pulse width low	35%	65%	REF_CLK period

1. RMII timing is valid only up to a maximum of 150 ^{o}C junction temperature.
2. CL = 25pF, VDD_HV_IO_FLEX = 3.3V +/- 5% and CMOS levels are required for the REF_CLK input. For CL = 15pF, VDD_HV_IO_FLEX = 3.3V +/- 10%, CMOS or TTL levels for the REF_CLK input.
3. C_L is the external load to the device. The internal package capacitance is accounted for, and does not need to be subtracted from the 25 pF value.

Figure 39. RMII transmit signal timing diagram



3.17.4 FlexRay timing

This section provides the FlexRay Interface timing characteristics for the input and output signals.

These are recommended numbers as per the FlexRay EPL v3.0 specification, and subject to change per the final timing analysis of the device.

3.17.4.1 TxEN

Figure 40. TxEN signal

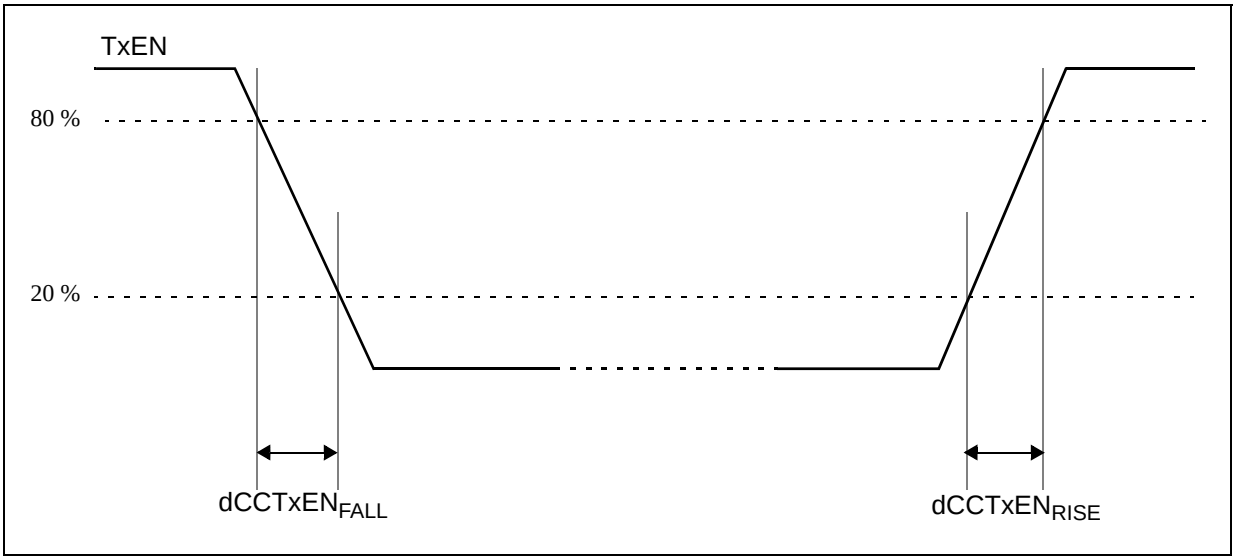


Table 57. TxEN output characteristics(1)

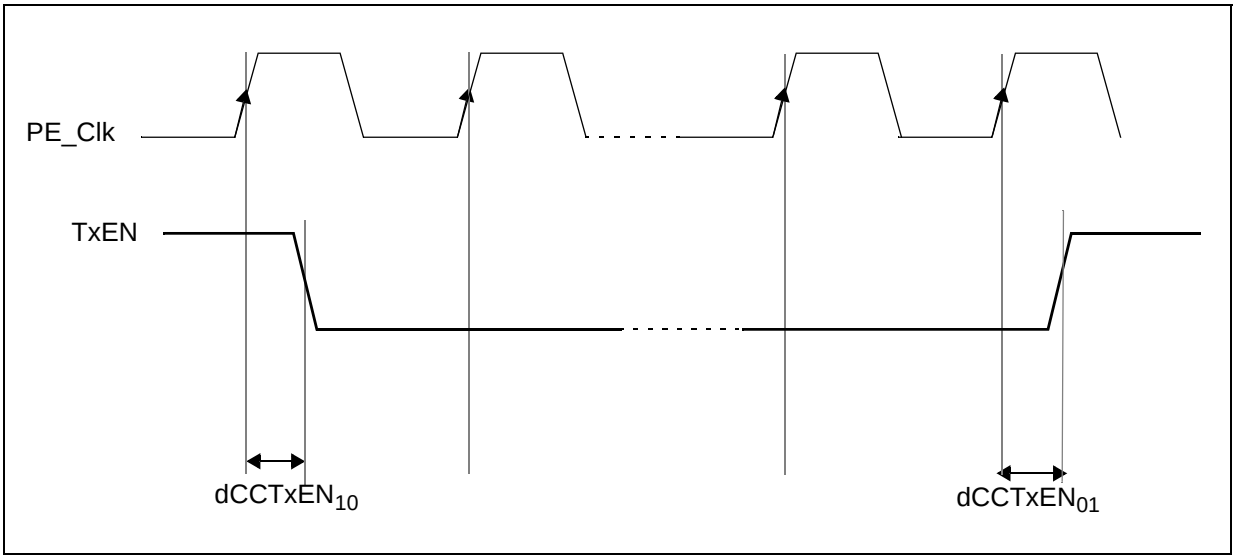
Symbol		C	Characteristic	Value		Unit
				Min	Max	
dCCTxEN$_{RISE25}$	CC	D	Rise time of TxEN signal at CC	—	9	ns
dCCTxEN$_{FALL25}$	CC	D	Fall time of TxEN signal at CC	—	9	ns

Table 57. TxEN output characteristics(1)(Continued)

Symbol		C	Characteristic	Value		Unit
				Min	Max	
$dCCTxEN_{01}$	CC	D	Sum of delay between Clk to Q of the last FF and the final output buffer, rising edge	—	25	ns
$dCCTxEN_{10}$	CC	D	Sum of delay between Clk to Q of the last FF and the final output buffer, falling edge	—	25	ns

1. TxEN pin load maximum 25 pF

Figure 41. TxEN signal propagation delays



3.17.4.2 TxD

Figure 42. TxD signal

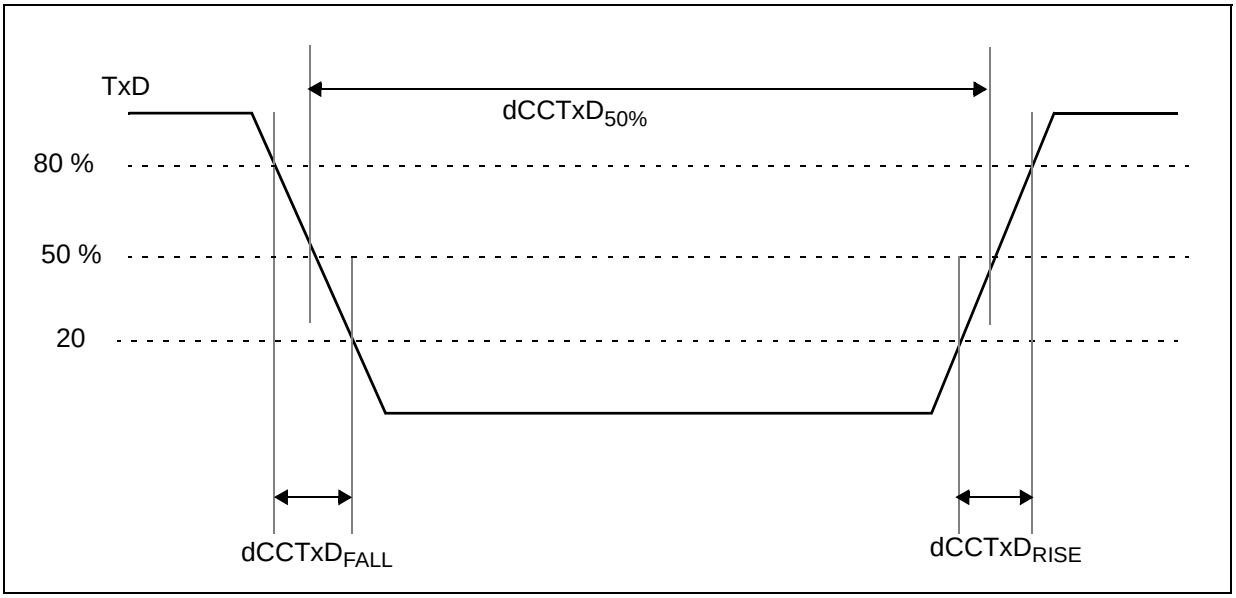
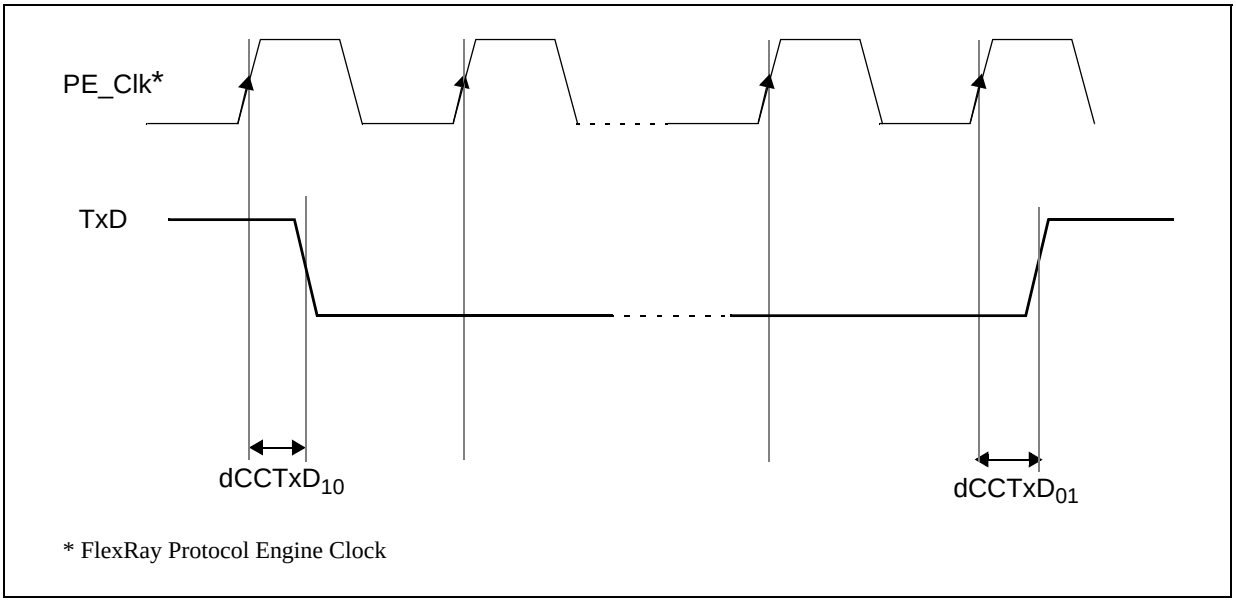


Table 58. TxD output characteristics(1)(2)

Symbol		C	Characteristic	Value		Unit
				Min	Max	
dCCTxAsym	CC	D	Asymmetry of sending CC at 25 pF load (= $dCCTxD_{50\%}$ – 100 ns)	–2.45	2.45	ns
$dCCTxD_{RISE25}$+$dCCTxD_{FALL25}$	CC	D	Sum of Rise and Fall time of TxD signal at the output pin(3),(4)	—	9(5)	ns
		D		—	9(6)	
$dCCTxD_{01}$	CC	D	Sum of delay between Clk to Q of the last FF and the final output buffer, rising edge	—	25	ns
$dCCTxD_{10}$	CC	D	Sum of delay between Clk to Q of the last FF and the final output buffer, falling edge	—	25	ns

1. TxD pin load maximum 25 pF.
2. Specifications valid according to FlexRay EPL 3.0.1 standard with 20%–80% levels and a 10pF load at the end of a 50 Ohm, 1 ns stripline. Please refer to the Very Strong I/O pad specifications.
3. Pad configured as VERY STRONG.
4. Sum of transition time simulation is performed according to Electrical Physical Layer Specification 3.0.1 and the entire temperature range of the device has been taken into account.
5. $V_{DD\_HV\_IO}$ = 5.0 V ± 10%, Transmission line Z = 50 ohms, t_{delay} = 1 ns, C_L = 10 pF
6. $V_{DD\_HV\_IO}$ = 3.3 V ± 10%, Transmission line Z = 50 ohms, t_{delay} = 0.6 ns, C_L = 10 pF

Figure 43. TxD Signal propagation delays



3.17.4.3 RxD

Table 59. RxD input characteristics(1)

Symbol		C	Characteristic	Value		Unit
				Min	Max	
C_CCRxD	CC	D	Input capacitance on RxD pin	—	7	pF
uCCLogic_1	CC	D	Threshold for detecting logic high	35	70	%
uCCLogic_0	CC	D	Threshold for detecting logic low	30	65	%
$dCCRxD_{01}$	CC	D	Sum of delay from actual input to the D input of the first FF, rising edge	—	10	ns
$dCCRxD_{10}$	CC	D	Sum of delay from actual input to the D input of the first FF, falling edge	—	10	ns
dCCRxAsymAccept15	CC	D	Acceptance of asymmetry at receiving CC with 15 pF load	–31.5	44	ns
dCCRxAsymAccept25	CC	D	Acceptance of asymmetry at receiving CC with 25 pF load	–30.5	43	ns

1. FlexRay RxD timing is valid for CMOS input levels, hysteresis disabled, and $4.5\ V \le V_{DD\_HV\_IO} \le 5.5\ V$.

3.17.5 PSI5 timing

The following table describes the PSI5 timing.

Table 60. PSI5 timing

Symbol		C	Parameter	Value		Unit
				Min	Max	
t_{MSG_DLY}	CC	D	Delay from last bit of frame (CRC0) to assertion of new message received interrupt	—	3	µs
t_{SYNC_DLY}	CC	D	Delay from internal sync pulse to sync pulse trigger at the SDOUT_PSI5_n pin	—	2	µs
t_{MSG_JIT}	CC	D	Delay jitter from last bit of frame (CRC0) to assertion of new message received interrupt	—	1	cycles(1)
t_{SYNC_JIT}	CC	D	Delay jitter from internal sync pulse to sync pulse trigger at the SDOUT_PSI5_n pin	—	±(1 PSI5_1µs_CLK + 1 PBRIDGEn_CLK)	cycles

1. Measured in PSI5 clock cycles (PBRIDGEn_CLK on the device). Minimum PSI5 clock period is 20 ns.

3.17.6 UART timing

UART channel frequency support is shown in the following table.

Table 61. UART frequency support

LINFlexD clock frequency LIN_CLK (MHz)	Oversampling rate	Voting scheme	Max usable frequency (Mbaud)
80	16	3:1 majority voting	5
	8		10
	6	Limited voting on one sample with configurable sampling point	13.33
	5		16
	4		20
100	16	3:1 majority voting	6.25
	8		12.5
	6	Limited voting on one sample with configurable sampling point	16.67
	5		20
	4		25

3.17.7 I²C timing

The I²C AC timing specifications are provided in the following tables.

Table 62. I²C input timing specifications — SCL and SDA(1)

No.	Symbol		C	Parameter	Value		Unit
					Min	Max	
1	—	CC	D	Start condition hold time	2	—	PER_CLK Cycle(2)
2	—	CC	D	Clock low time	8	—	PER_CLK Cycle

Table 62. I²C input timing specifications — SCL and SDA(1)(Continued)

No.	Symbol		C	Parameter	Value		Unit
					Min	Max	
3	—	CC	D	Bus free time between Start and Stop condition	4.7	—	µs
4	—	CC	D	Data hold time	0.0	—	ns
5	—	CC	D	Clock high time	4	—	PER_CLK Cycle
6	—	CC	D	Data setup time	0.0	—	ns
7	—	CC	D	Start condition setup time (for repeated start condition only)	2	—	PER_CLK Cycle
8	—	CC	D	Stop condition setup time	2	—	PER_CLK Cycle

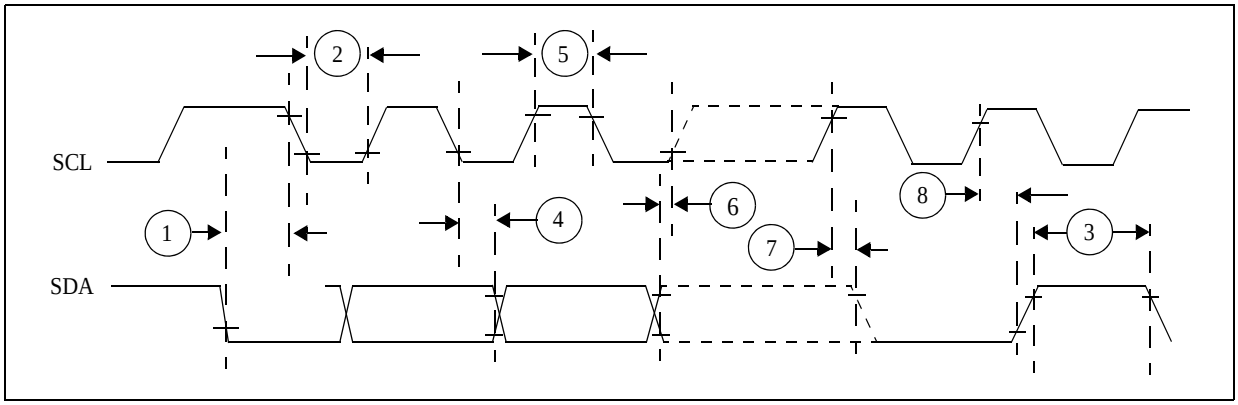
1. I²C input timing is valid for Automotive and TTL inputs levels, hysteresis enabled, and an input edge rate no slower than 1 ns (10% – 90%).
2. PER_CLK is the SoC peripheral clock, which drives the I²C BIU and module clock inputs. See the Clocking chapter in the device reference manual for more detail.

Table 63. I²C output timing specifications — SCL and SDA(1)(2)(3)(4)

No.	Symbol		C	Parameter	Value		Unit
					Min	Max	
1	—	CC	D	Start condition hold time	6	—	PER_CLK Cycle(5)
2	—	CC	D	Clock low time	10	—	PER_CLK Cycle
3	—	CC	D	Bus free time between Start and Stop condition	4.7	—	µs
4	—	CC	D	Data hold time	7	—	PER_CLK Cycle
5	—	CC	D	Clock high time	10	—	PER_CLK Cycle
6	—	CC	D	Data setup time	2	—	PER_CLK Cycle
7	—	CC	D	Start condition setup time (for repeated start condition only)	20	—	PER_CLK Cycle
8	—	CC	D	Stop condition setup time	10	—	PER_CLK Cycle

1. All output timing is worst case and includes the mismatching of rise and fall times of the output pads.
2. Output parameters are valid for C_L = 25 pF, where C_L is the external load to the device (lumped). The internal package capacitance is accounted for, and does not need to be subtracted from the 25 pF value.
3. Timing is guaranteed to same drive capabilities for all signals, mixing of pad drives may reduce operating speedsand may cause incorrect operation.
4. Programming the IBFD register (I²C bus Frequency Divider) with the maximum frequency results in the minimum output timings listed. The I²C interface is designed to scale the data transition time, moving it to the middle of the SCL low period. The actual position is affected by the pre-scale and division values programmed in the IBC field of the IBFD register.
5. PER_CLK is the SoC peripheral clock, which drives the I²C BIU and module clock inputs. See the Clocking chapter in the device reference manual for more detail.

Figure 44. I²C input/output timing



3.17.8 GPIO delay timing

The GPIO delay timing specification is provided in the following table.

Table 64. GPIO delay timing

Symbol		C	Parameter	Value		Unit
				Min	Max	
IO_delay	CC	D	Delay from MSCR bit update to pad function enable	5	25	ns

4 Package characteristics

The following table lists the case numbers for each available package for the device.

Table 65. Package case numbers

Package Type	Device Type	Package reference
eTQFP144	Production	7386636
FQ172	Emulation	8153717
eLQFP176	Production	8391697
FQ216	Emulation	8338897

4.1 ECOPACK®

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

4.2 eTQFP144 case drawing

Figure 45. eTQFP144 – STMicroelectronics package mechanical drawing (1 of 2)

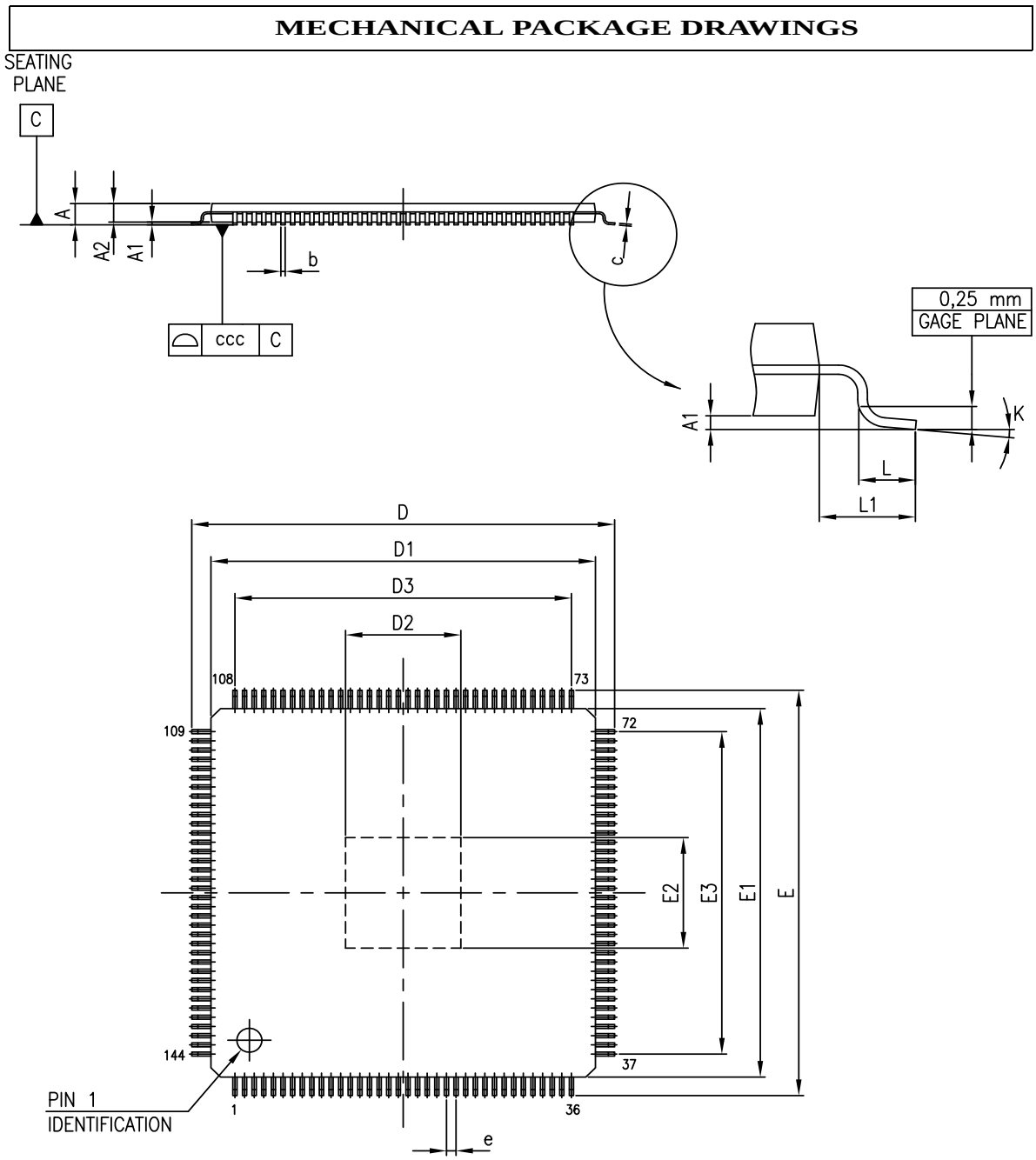


Figure 46. eTQFP144 – STMicroelectronics package mechanical drawing (2 of 2)

Symbol	Dimensions					
	Millimeters			Inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	—	—	1.20	—	—	0.047
A1	0.05	—	0.15	0.002	—	0.006
A2	0.95	1.00	1.05	0.037	0.039	0.041
b	0.17	0.22	0.27	0.007	0.009	0.011
c	0.09	—	0.20	0.004	—	0.008
D	21.80	22.00	22.20	0.858	0.866	0.874
D1	19.80	20.00	20.20	0.780	0.787	0.795
D2[2]	—	7.35	—	—	0.289	—
D3	—	17.50	—	—	0.689	—
E	21.80	22.00	22.20	0.858	0.866	0.874
E1	19.80	20.00	20.20	0.780	0.787	0.795
E2	—	7.35	—	—	0.289	—
E3[2]	—	17.50	—	—	0.689	—
e	—	0.50	—	—	0.020	—
L[3]	0.45	0.60	0.75	0.018	0.024	0.030
L1	—	1.00	—	—	0.039	—
k	0.0°	3.5°	7.0°	0.0°	3.5°	7.0°
ccc[4]	0.08			0.003		

1. Values in inches are converted from millimeters (mm) and rounded to four decimal digits.
2. The size of exposed pad is variable depending of leadframe design pad size.
3. L dimension is measured at gauge plane at 0.25 above the seating plane.
4. Tolerance

4.3 eLQFP176 case drawing

Figure 47. eLQFP176 – STMicroelectronics package mechanical drawing (1 of 2)

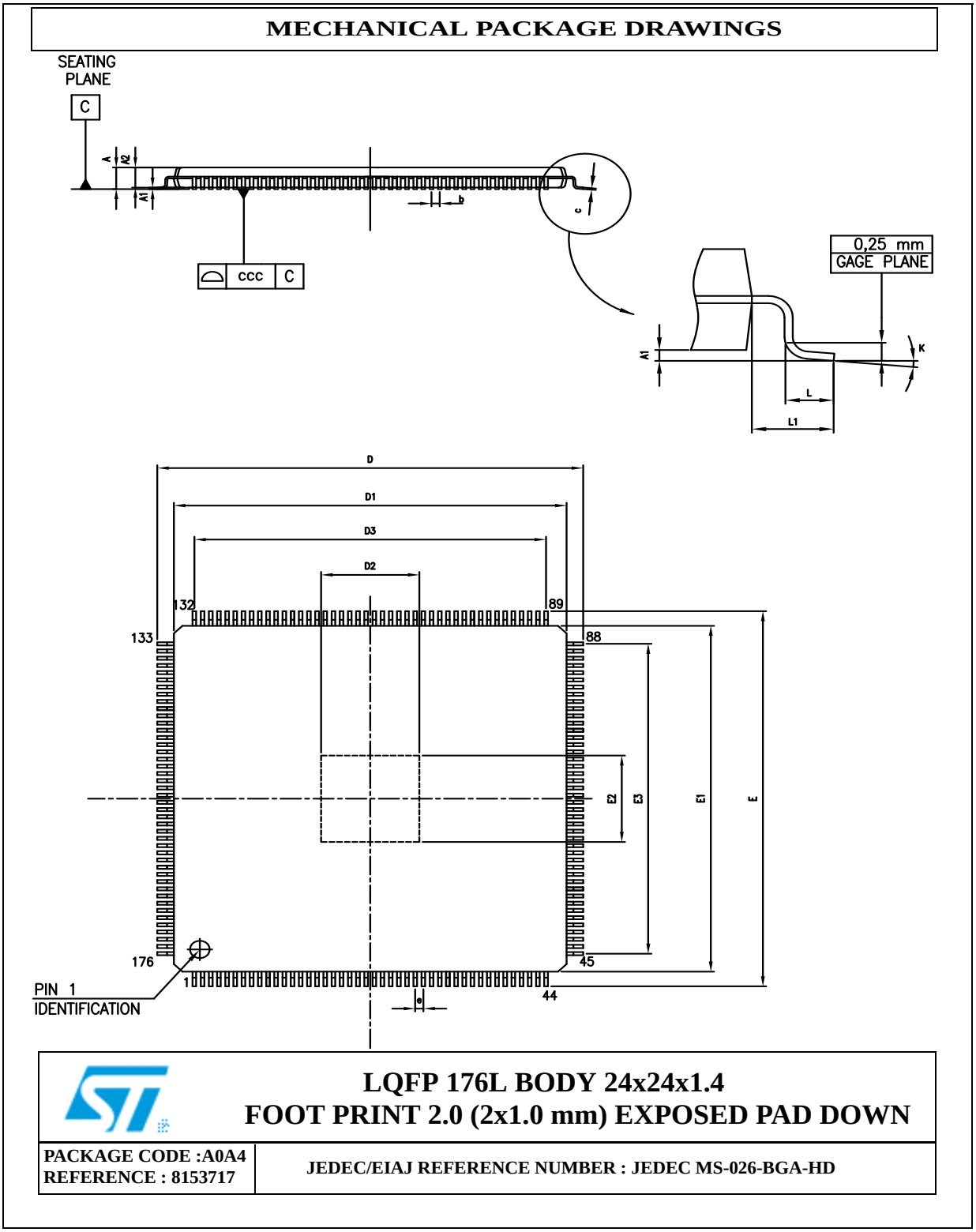


Figure 48. eLQFP176 – STMicroelectronics package mechanical drawing (2 of 2)

Symbol	Dimensions					
	Millimeters			Inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	—	—	1.60	—	—	0.063
A1	0.05	—	0.15	0.002	—	0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
b	0.17	0.22	0.27	0.007	0.009	0.011
c	0.09	—	0.20	0.004	—	0.008
D	25.80	26.00	26.20	1.016	1.024	1.032
D1	23.90	24.00	24.10	0.941	0.945	0.949
D2[2]	—	7.35	—	—	0.289	—
D3	—	21.500	—	—	0.847	—
E	25.80	26.00	26.20	1.016	1.024	1.032
E1	23.90	24.00	24.10	0.941	0.945	0.949
E2[2]	—	7.35	—	—	0.289	—
E3	—	21.50	—	—	0.847	—
e	—	0.50	—	—	0.020	—
L[3]	0.45	0.60	0.75	0.018	0.024	0.030
L1	—	1.00	—	—	0.039	—
k	0.0°	3.5°	7.0°	0.0°	3.5°	7.0°
ccc[4]	0.080			0.003		

1. Values in inches are converted from millimeters (mm) and rounded to four decimal digits.
2. The size of exposed pad is variable depending of leadframe design pad size.
3. L dimension is measured at gauge plane at 0.25 above the seating plane.
4. Tolerance

4.4 FusionQuad® case drawing

Figure 49. FusionQuad® QFP172 package mechanical drawing (1 of 2)

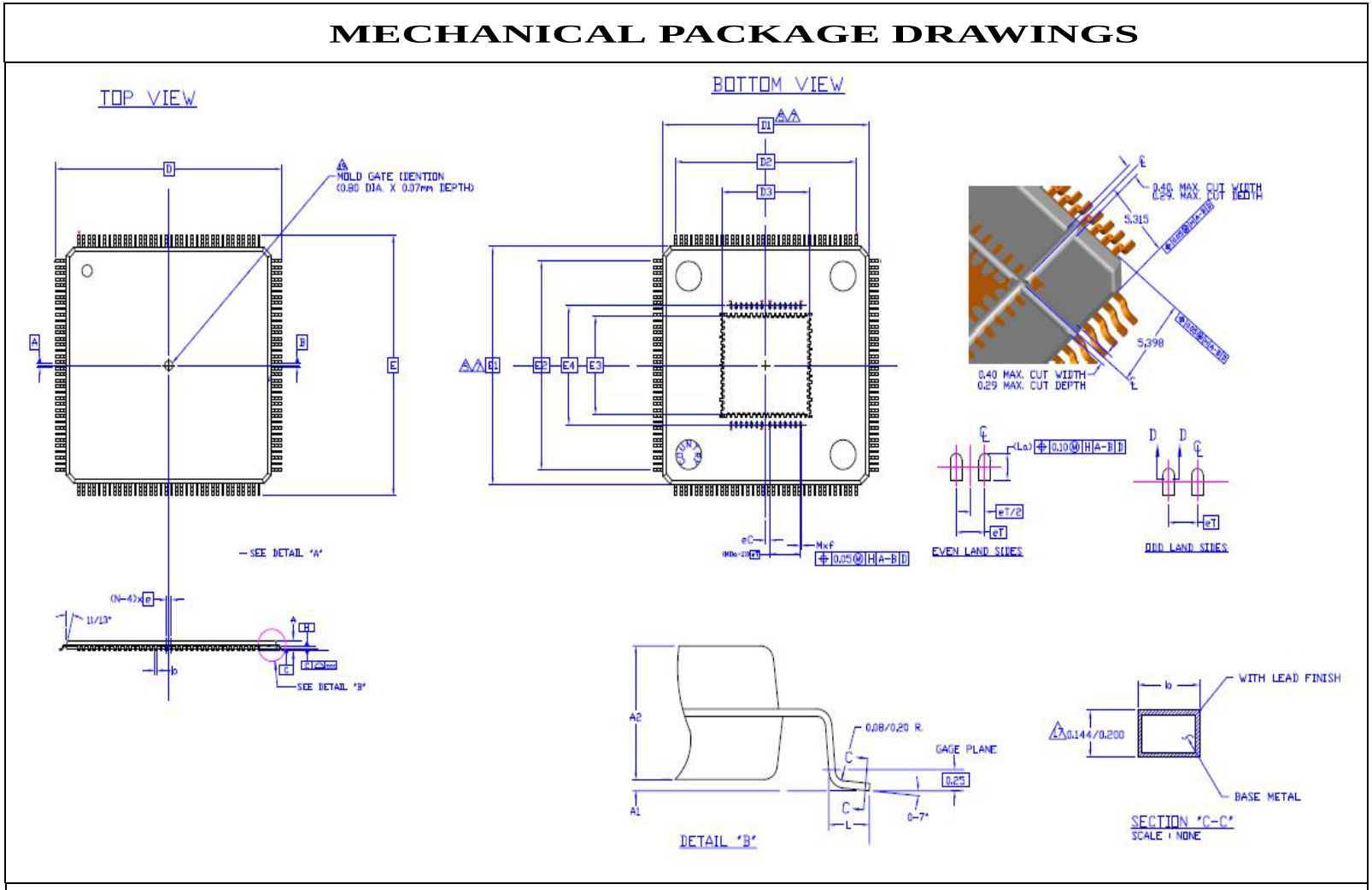


Figure 50. FusionQuad® QFP172 package mechanical drawing (2 of 2)

MECHANICAL OUTLINE ASSEMBLY

NOTES:

1. ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5-1982.
2. DATUM PLANE H LOCATED AT MOLD PARTING LINE AND COINCIDENT WITH LEAD, WHERE LEAD EXITS PLASTIC BODY AT BOTTOM OF PARTING LINE.
3. DATUMS A–B AND D TO BE DETERMINED AT CENTERLINE BETWEEN LEADS WHERE LEADS EXIT PLASTIC BODY AT DATUM PLANE H.
4. TO BE DETERMINED AT SEATING PLANE C.
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION IS 0.254 MM ON D1 AND E1 DIMENSIONS.
6. 'N' IS THE NUMBER OF TERMINALS FOR PERIPHERAL LEADS, AND 'M' IS THE NUMBER OF TERMINALS FOR BOTTOM LANDS ON BOTTOM SURFACE OF PACKAGE BODY. THE BOTTOM LANDS ARE IDENTIFIED BY ALPHANUMERICS | A1~A#.
7. THESE DIMENSIONS TO BE DETERMINED AT DATUM PLANE H.
8. THE TOP OF PACKAGE MAY BE SMALLER THAN THE BOTTOM OF PACKAGE BY 0.15 MM.
9. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 MM TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT.
10. CONTROLLING DIMENSION | MILLIMETERS.
11. MAXIMUM ALLOWABLE DIE THICKNESS TO BE ASSEMBLED IN THIS PACKAGE FAMILY IS 0.38 MM.
12. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.
13. DIMENSIONS D2 AND E2 REPRESENT THE SIZE OF THE EXPOSED PAD. THE ACTUAL DIMENSIONS ARE DETERMINED BY EACH INDIVIDUAL LEADFRAME DRAWING. THE EXPOSED PAD SIZE TOLERANCE IS 0.10 MAX.
14. EXPOSED PAD SHALL BE COPLANAR WITH BOTTOM OF PACKAGE WITHIN 0.05 MM.
15. UNILATERAL COPLANARITY ZONE APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
16. MECHANICAL CONNECT TABS ARE COUNTED FOR GROUND (VSS) SIGNAL PINS. THOSE ARE INCLUDED INTO PACKAGE TOTAL PIN COUNTS.
17. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 MM AND 0.25 MM FROM THE LEAD TIP.
18. THESE DIMENSIONS APPLY TO ALL 4 SYMMETRIC LOCATIONS.
19. GATE PROTRUSION HEIGHT OR CHIP OUT DEPTH | 0.049 MM MAX

ALL DIMENSIONS IN MILLIMETERS

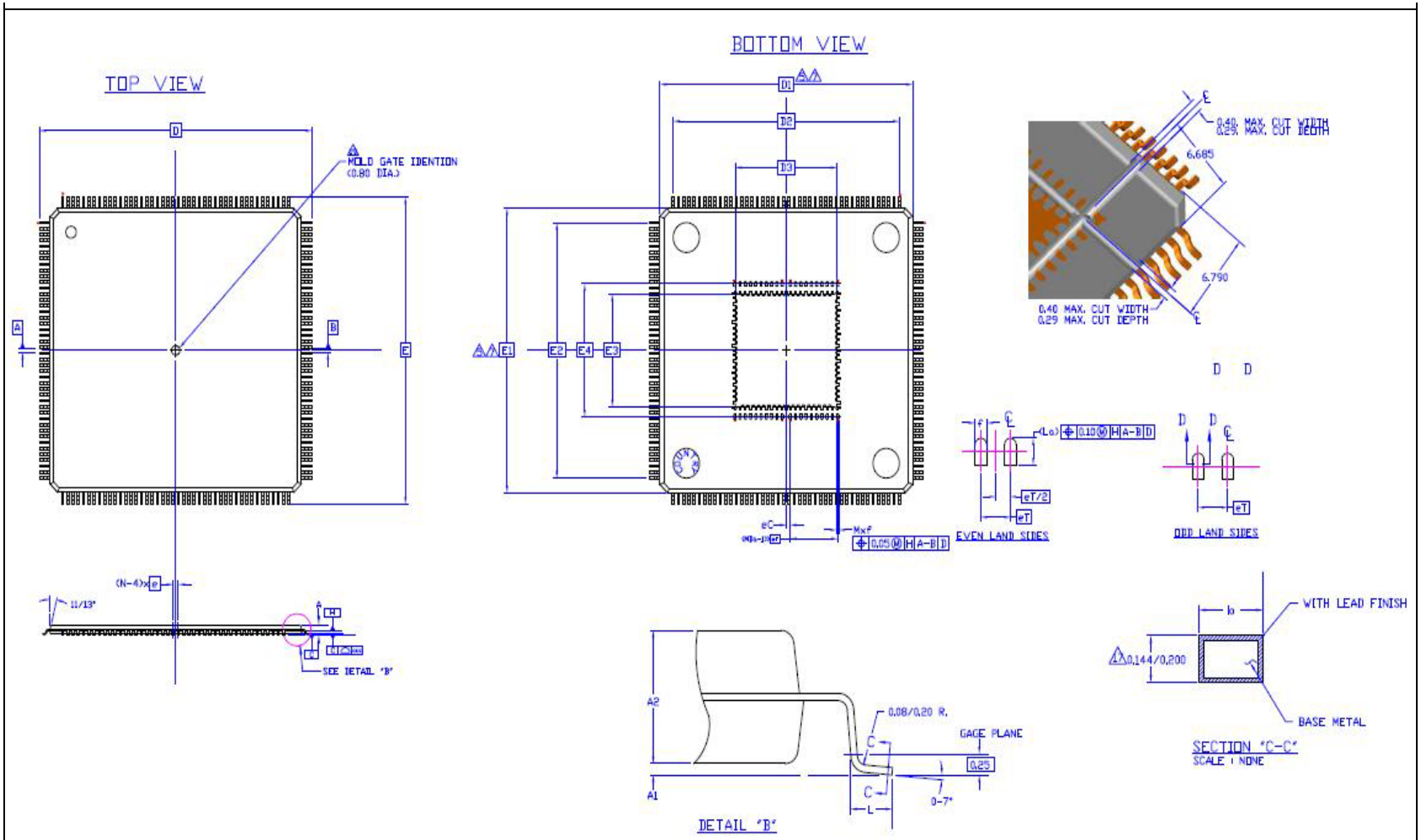
VARIATIONS				
SYMBOL	FUSION			NOTE
	MIN	NOM	MAX	
A	—	—	1.20	
A1	0.05	0.10	0.15	
A2	0.95	1.00	1.05	
A3	–0.05	0.00	0.05	
A4		0.152 REF		
D		22.00 BSC		4
D1		20.00 BSC		5
D2		17.50 BSC		
D3	8.32	8.42	8.52	
E		22.00 BSC		4
E1		20.00 BSC		5
E2		17.50 BSC		
E3	8.20	8.30	9.40	
E4		10.00 REF		
L	0.45	0.60	0.75	
N		144		6
e		0.50 BSC		
b	0.17	0.22	0.27	
c.c.c		0.08		
d.d.d		0.08		

PITCH VARIATIONS				
SYMBOL	FUSION			NOTE
	MIN	NOM	MAX	
eT		0.50 BSC		
eC		0.39 BSC		18
M		28		6
La	0.30	0.40	0.50	
f	0.17	0.22	0.27	
999	—	0.08	—	

THE FusionQuad PACKAGE IS A REGISTERED TRADEMARK OF AMKOR TECHNOLOGIES.

THE FusionQuad PACKAGE IS ASSEMBLED BY AMKOR TECHNOLOGIES.

Figure 51. FusionQuad® QFP216 package mechanical drawing (1 of 2)



FusionQuad® 176+40L 24x24x1.0 0.5 mm Pitch

PACKAGE CODE: A0HX
REFERENCE : 8338897

Figure 52. FusionQuad® QFP216 package mechanical drawing (2 of 2)

MECHANICAL OUTLINE ASSEMBLY

NOTES:

1. ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5-1982.
2. DATUM PLANE H LOCATED AT MOLD PARTING LINE AND COINCIDENT WITH LEAD, WHERE LEAD EXITS PLASTIC BODY AT BOTTOM OF PARTING LINE.
3. DATUMS A–B AND D TO BE DETERMINED AT CENTERLINE BETWEEN LEADS WHERE LEADS EXIT PLASTIC BODY AT DATUM PLANE H.
4. TO BE DETERMINED AT SEATING PLANE C.
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION IS 0.254 MM ON D1 AND E1 DIMENSIONS.
6. 'N' IS THE NUMBER OF TERMINALS FOR PERIPHERAL LEADS, AND 'M' IS THE NUMBER OF TERMINALS FOR BOTTOM LANDS ON BOTTOM SURFACE OF PACKAGE BODY. THE BOTTOM LANDS ARE IDENTIFIED BY ALPHANUMERICS | A1~A#.
7. THESE DIMENSIONS TO BE DETERMINED AT DATUM PLANE H.
8. THE TOP OF PACKAGE MAY BE SMALLER THAN THE BOTTOM OF PACKAGE BY 0.15 MM.
9. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 MM TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT.
10. CONTROLLING DIMENSION | MILLIMETERS.
11. MAXIMUM ALLOWABLE DIE THICKNESS TO BE ASSEMBLED IN THIS PACKAGE FAMILY IS 0.38 MM.
12. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.
13. DIMENSIONS D2 AND E2 REPRESENT THE SIZE OF THE EXPOSED PAD. THE ACTUAL DIMENSIONS ARE DETERMINED BY EACH INDIVIDUAL LEADFRAME DRAWING. THE EXPOSED PAD SIZE TOLERANCE IS 0.10 MAX.
14. EXPOSED PAD SHALL BE COPLANAR WITH BOTTOM OF PACKAGE WITHIN 0.05 MM.
15. UNILATERAL COPLANARITY ZONE APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
16. MECHANICAL CONNECT TABS ARE COUNTED FOR GROUND (VSS) SIGNAL PINS. THOSE ARE INCLUDED INTO PACKAGE TOTAL PIN COUNTS.
17. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 MM AND 0.25 MM FROM THE LEAD TIP.
18. THESE DIMENSIONS APPLY TO ALL 4 SYMMETRIC LOCATIONS.

ALL DIMENSIONS IN MILLIMETERS

VARIATIONS				
SYMBOL	FUSION			NOTE
	MIN	NOM	MAX	
A	—	—	1.20	
A1	0.00	0.051	0.10	
A2	0.95	1.00	1.05	
D		26.00 BSC		4
D1		24.00 BSC		5
D2		17.50 BSC		
D3	9.58	9.68	9.78	
E		26.00 BSC		4
E1		24.00 BSC		5
E2		21.00 BSC		
E3	9.40	9.50	9.60	
E4		11.20 REF		
L	0.45	0.60	0.75	
N		176		6
e		0.50 BSC		
b	0.17	0.22	0.27	
c.c.c		0.08		
d.d.d		0.08		

PITCH VARIATIONS				
SYMBOL	FUSION			NOTE
	MIN	NOM	MAX	
eT		0.50 BSC		
eC		0.39 BSC		18
M		40		6
La	0.30	0.40	0.50	
f	0.17	0.22	0.27	
999	—	0.08	—	

THE FusionQuad PACKAGE IS A REGISTERED TRADEMARK OF AMKOR TECHNOLOGIES.

THE FusionQuad PACKAGE IS ASSEMBLED BY AMKOR TECHNOLOGIES.

4.5 Thermal characteristics

The following tables describe the thermal characteristics of the device.

Table 66. Thermal characteristics for eTQFP144(1)

Symbol		C	Parameter	Conditions	Value		Unit
					Min	Max	
$R_{\theta JA}$	CC	D	Junction-to-ambient, natural convection(2)	Four layer board—2s2p	26	29	°C/W
$R_{\theta JMA}$	CC	D	Junction-to-moving-air, ambient(2)	At 200 ft./min., four layer board—2s2p	19	23	°C/W
$R_{\theta JB}$	CC	D	Junction-to-board(3)	—	12	16	°C/W
$R_{\theta JCtop}$	CC	D	Junction-to-case top(4)	—	10	13	°C/W
$R_{\theta JCbottom}$	CC	D	Junction-to-case bottom(5)	—	1.5	4	°C/W
Ψ_{JT}	CC	D	Junction-to-package top(6)	Natural convection	3	5	°C/W
P_d	CC	D	Device power dissipation	Maximum power and voltage condition	—	2	W

1. The lower number in the ranges specified in the ‘Value’ column are based on simulation; actual data may vary in the given range. The specified characteristics are subject to change per final device design and characterization. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per JEDEC JESD51-6 with the board (JESD51-7) horizontal.
3. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
4. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
5. Thermal resistance between the die and the solder pad on the bottom of the package based on simulation without any interface resistance.
6. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2.

Table 67. Thermal characteristics for eLQFP176[1]

Symbol		C	Parameter	Conditions	Value		Unit
					Min	Max	
$R_{\theta JA}$	CC	D	Junction-to-ambient, natural convection[2]	Four layer board—2s2p	25	28	°C/W
$R_{\theta JMA}$	CC	D	Junction-to-moving-air, ambient[2]	At 200 ft./min., four layer board—2s2p	18	22	°C/W
$R_{\theta JB}$	CC	D	Junction-to-board[3]	—	12	16	°C/W
$R_{\theta JCtop}$	CC	D	Junction-to-case top[4]	—	12	15	°C/W
$R_{\theta JCbottom}$	CC	D	Junction-to-case bottom[5]	—	1.5	3.5	°C/W
Ψ_{JT}	CC	D	Junction-to-package top[6]	Natural convection	3	4.5	°C/W
P_d	CC	D	Device power dissipation	Maximum power and voltage condition	—	2	W

1. The lower number in the ranges specified in the 'Value' column are based on simulation; actual data may vary in the given range. The specified characteristics are subject to change per final device design and characterization. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per JEDEC JESD51-6 with the board (JESD51-7) horizontal.
3. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
4. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
5. Thermal resistance between the die and the solder pad on the bottom of the package based on simulation without any interface resistance.
6. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2.

4.5.1 General notes for specifications at maximum junction temperature

An estimation of the chip junction temperature, T_J, can be obtained from the equation:

Equation 1 $T_J = T_A + (R_{\theta JA} * P_D)$

where:

T_A = ambient temperature for the package (°C)

$R_{\theta JA}$ = junction-to-ambient thermal resistance (°C/W)

P_D = power dissipation in the package (W)

The thermal resistance values used are based on the JEDEC JESD51 series of standards to provide consistent values for estimations and comparisons. The difference between the values determined for the single-layer (1s) board compared to a four-layer board that has two signal layers, a power and a ground plane (2s2p), demonstrate that the effective thermal resistance is not a constant. The thermal resistance depends on the:

- Construction of the application board (number of planes)
- Effective size of the board which cools the component
- Quality of the thermal and electrical connections to the planes
- Power dissipated by adjacent components

Connect all the ground and power balls to the respective planes with one via per ball. Using fewer vias to connect the package to the planes reduces the thermal performance. Thinner planes also reduce the thermal performance. When the clearance between the vias leave the planes virtually disconnected, the thermal performance is also greatly reduced.

As a general rule, the value obtained on a single-layer board is within the normal range for the tightly packed printed circuit board. The value obtained on a board with the internal planes is usually within the normal range if the application board has:

- One oz. (35 micron nominal thickness) internal planes
- Components are well separated
- Overall power dissipation on the board is less than 0.02 W/cm^2

The thermal performance of any component depends on the power dissipation of the surrounding components. In addition, the ambient temperature varies widely within the application. For many natural convection and especially closed box applications, the board temperature at the perimeter (edge) of the package is approximately the same as the local air temperature near the device. Specifying the local ambient conditions explicitly as the board temperature provides a more precise description of the local ambient conditions that determine the temperature of the device.

At a known board temperature, the junction temperature is estimated using the following equation:

Equation 2 $T_J = T_B + (R_{\theta JB} * P_D)$

where:

T_B = board temperature for the package perimeter (°C)

$R_{\theta JB}$ = junction-to-board thermal resistance (°C/W) per JESD51-8

P_D = power dissipation in the package (W)

When the heat loss from the package case to the air does not factor into the calculation, the junction temperature is predictable if the application board is similar to the thermal test condition, with the component soldered to a board with internal planes.

The thermal resistance is expressed as the sum of a junction-to-case thermal resistance plus a case-to-ambient thermal resistance:

Equation 3 $R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$

where:

$R_{\theta JA}$ = junction-to-ambient thermal resistance (°C/W)

$R_{\theta JC}$ = junction-to-case thermal resistance (°C/W)

$R_{\theta CA}$ = case to ambient thermal resistance (°C/W)

$R_{\theta JC}$ is device related and is not affected by other factors. The thermal environment can be controlled to change the case-to-ambient thermal resistance, $R_{\theta CA}$. For example, change the air flow around the device, add a heat sink, change the mounting arrangement on the printed circuit board, or change the thermal dissipation on the printed circuit board surrounding the device. This description is most useful for packages with heat sinks where 90% of the heat flow is through the case to heat sink to ambient. For most packages, a better model is required.

A more accurate two-resistor thermal model can be constructed from the junction-to-board thermal resistance and the junction-to-case thermal resistance. The junction-to-case

thermal resistance describes when using a heat sink or where a substantial amount of heat is dissipated from the top of the package. The junction-to-board thermal resistance describes the thermal performance when most of the heat is conducted to the printed circuit board. This model can be used to generate simple estimations and for computational fluid dynamics (CFD) thermal models. More accurate compact Flotherm models can be generated upon request.

To determine the junction temperature of the device in the application on a prototype board, use the thermal characterization parameter (Ψ_{JT}) to determine the junction temperature by measuring the temperature at the top center of the package case using the following equation:

Equation 4 $T_J = T_T + (\Psi_{JT} \times P_D)$

where:

T_T = thermocouple temperature on top of the package (°C)

Ψ_{JT} = thermal characterization parameter (°C/W)

P_D = power dissipation in the package (W)

The thermal characterization parameter is measured in compliance with the JESD51-2 specification using a 40-gauge type T thermocouple epoxied to the top center of the package case. Position the thermocouple so that the thermocouple junction rests on the package. Place a small amount of epoxy on the thermocouple junction and approximately 1 mm of wire extending from the junction. Place the thermocouple wire flat against the package case to avoid measurement errors caused by the cooling effects of the thermocouple wire.

When board temperature is perfectly defined below the device, it is possible to use the thermal characterization parameter (Ψ_{JPB}) to determine the junction temperature by measuring the temperature at the bottom center of the package case (exposed pad) using the following equation:

Equation 5 $T_J = T_B + (\Psi_{JPB} \times P_D)$

where:

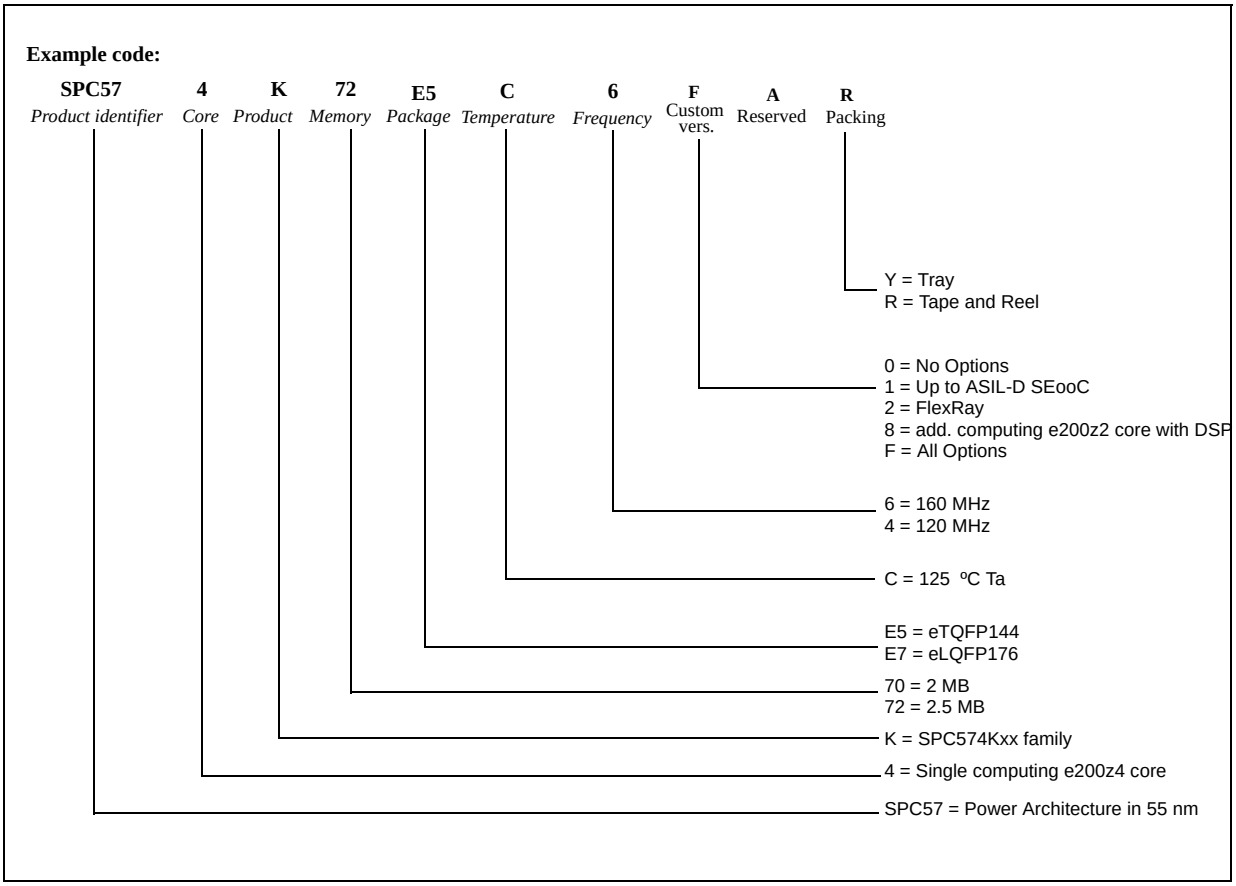
T_B= thermocouple temperature on bottom of the package (°C)

Ψ_{PB}= thermal characterization parameter (°C/W)

P_D = power dissipation in the package (W)

5 Ordering information

Figure 53. Product code structure



6 Revision history

Table 69. Document revision history

Date	Revision	Changes
28-Oct-2011	1	Initial release
17-Sep-2012	2	Document updated after Initial application and customer feedbacks. Editorial and formatting changes are made throughout the document.
03-Feb-2014	3	Document updated after initial silicon validation and characterization feedbacks.
17-Apr-2015	4	Document updated after major silicon review – first validation and characterization feedbacks.
22-Jul-2015	5	Document updated after major silicon review – final validation and characterization feedbacks.