SN65LVDS324 1080p60 Image Sensor Receiver

1 Features

- Bridges the Interface Between Video Image Sensors and Processors
- Receives Aptina HiSPi™, Panasonic LVDS, or Sony LVDS Parallel; Outputs 1.8V CMOS with 10/12/14/16 Bits at 18.5 MHz to 162 MHz
- SubLVDS Inputs Support Up To:
  - Sony LVDS parallel:
    - 10-bpp: 1620 Mbps
    - 12-bpp: 1944 Mbps
  - Panasonic LVDS:
    - 1-channel 4-lane 12-bpp: 972 Mbps
    - 1-channel 4-lane 16-bpp: 1296 Mbps
    - 2-channel 2-port 12-bpp: 486 Mbps per channel
    - 2-channel 2-port 16-bpp: 6408 Mbps per channel
  - Aptina HiSPi:
    - 1-channel 4-lane 14bpp: 1134Mbps
    - 1-channel 2-lane 12bpp: 594 Mbps

  648Mbps
- Integrated 100-Ω Differential Input Termination
- Test Image Generation Feature
- Compatible with TI OMAP™ and DaVinci™ Including DM385, DM8127, DM36x, and DMVA
- Low Power 1.8 V CMOS Process
- Configurable Output Conventions
- Packaged in 4.5 x 7mm BGA

2 Applications

- Surveillance Cameras
- Machine Vision
- Video Conferencing
- Gesture Recognition

3 Description

The SN65LVDS324 is a SubLVDS deserializer that recovers words, detects sync codes, multiplies the input DDR clock by a ratio, and outputs parallel CMOS 1.8 V data on the rising clock edge. It bridges the video stream interface between HD image sensors made by leading manufacturers, to a format that common processors can accept. The supported pixel frequency is 18.5 MHz to 162 MHz — suitable for resolutions from VGA to 1080p60.

Four high-level modes are supported:
Aptina 1-Channel 4-Lane, Aptina 1-Channel 2-Lane, Panasonic 2-Channel 2-Port, and Sony LVDS Parallel. Each supports 10/12/14/16 bit sub-modes, according to Table 1. Each mode also has a configurable allowable frequency range, as specified by Table 3 register PLL_CFG.

The SN65LVDS324 is configured through its I^2C-programmable registers. This volatile memory must be written after power up. Configuration options include the MSB/LSB output order, sync polarity convention, data slew rate, and two output timing modes (long-setup or clock-centered), for wider compatibility with different processors and software. The TESTMODE_VIDEO feature is designed to assist engineering development. The max allowable frame size is 8191 x 8191.

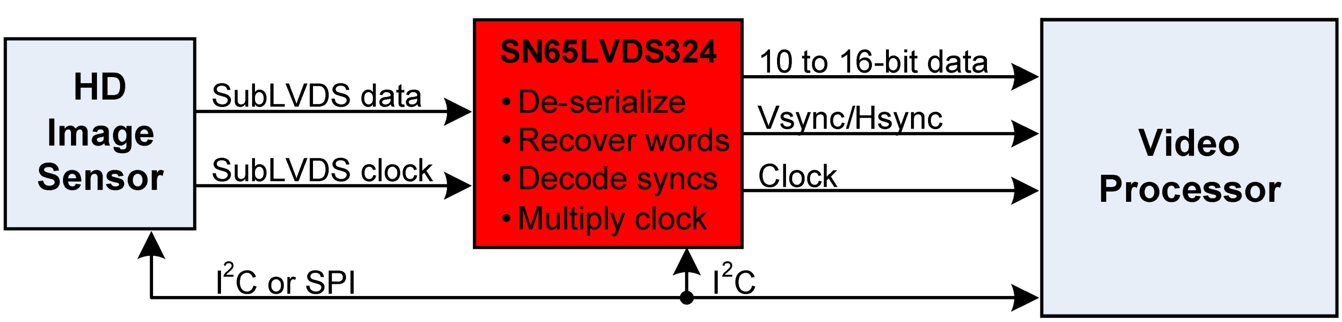
With integrated differential input termination, and a footprint of 4.5 x 7mm, the SN65LVDS324 provides a differentiated solution with optimized form, function, and cost. It operates through an ambient temperature range of –40°C to 85°C.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN65LVDS324	BGA (60)	4.50 mm × 7.00 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

4 General System Diagram



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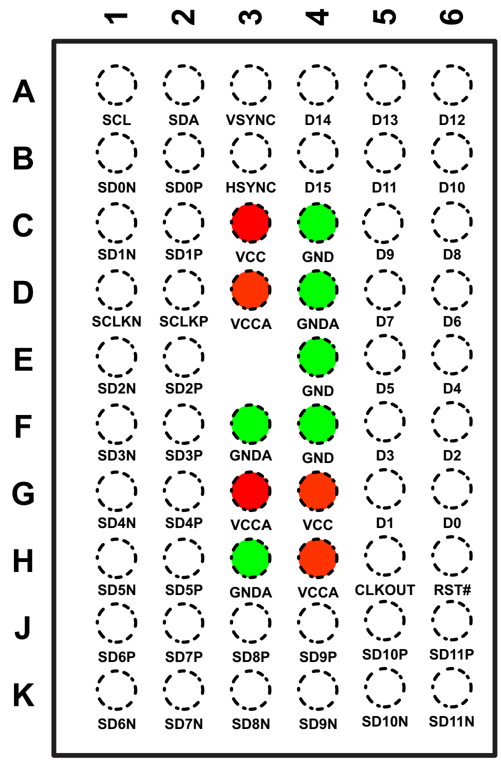
5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (November 2012) to Revision A	Page
• Added items to Features list	1
• Changed from "IP Network Cameras" to "Surveillance Cameras"	1
• Added Device Information table, Feature Description section, Device Functional Modes, Application and Implementation section, Power Supply Recommendations section, Layout section, Device and Documentation Support section, and Mechanical, Packaging, and Orderable Information section	1
• Added jitter specs t_j, R_j and D_j to Recommended Operating Conditions.	4
• Added NOTE: before Figure 10 and Figure 11.	9

6 Pin Configuration and Functions

**ZQL Package
60 Bumps
(Top View)**



Pin Functions

PIN		DESCRIPTION
SIGNAL	I/O	
SD[11:0]P/N	SubLVDS Input (Failsafe)	SubLVDS Input Data Lanes with 100Ω differential termination. In the 2-Channel 2-Port configurations, SD2P/N is used as Channel 2 clock. See Table 1 for sensor SubLVDS signal mapping per configuration.
SCLKP/N		SubLVDS Input Clock. In 2-Channel 2-Port mode, this input is the Channel 1 clock.
D[15:0]	CMOS Output	Parallel Output Pixel Data. Pixel data outputs beyond the pixel data width configuration are driven low.
CLKOUT		Parallel Output Clock.
HSYNC		Parallel Output Horizontal Sync.
VSYNC		Parallel Output Vertical Sync.
SCL	CMOS Input (Failsafe)	Local I^2C Programming Interface Clock Signal.
$\overline{RST}$		Logic Reset. Active when Low.
SDA	CMOS Input/Output (Failsafe)	Local I^2C Programming Interface Data Signal.
GNDA	Power Supply	Reference Ground for Analog Circuits.
VCCA		1.8V Power Supply for Analog Circuits.
GND		Reference Ground for Digital Circuits.
VCC		1.8V Power Supply for Digital Circuits.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
Supply Voltage	V_{CCA}, V_{CC}	–0.3	2.175	V
Input Voltage	All Input Terminals	–0.5	2.175	V
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±4000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{CCA}	Power supply; analog circuits		1.65	1.8	1.95	V
V_{CC}	Power supply; digital circuits		1.65	1.8	1.95	V
$V_{CCn(PP)}$	Power supply voltage noise	f_{NOISE} < 1MHz			100	mV
		f_{NOISE} > 1MHz			40	
$\|V_{ID}\|$	Magnitude of differential input voltage; see Figure 1		90		350	mV
V_{CM}	Input common mode voltage; see Figure 1	CSR 0A[6] = 0	100		650	mV
		CSR 0A[6] = 1	550		1200	
V_{CM}	Peak to peak input common mode voltage variation; see Figure 2				50	mV
V_{IN_DC}	SubLVDS receiver input voltage range				1400	mV
V_{ID_OS}	Differential input voltage overshoot/undershoot; see Figure 3				20%	
T_A	Operating free-air temperature		–40		85	°C
T_{CASE}	Case temperature				101	°C
f_{I2C}	Local I^2C interface operating frequency				400	kHz
f_{CLK}	SubLVDS input clock (SCLKP/N) frequency		18.5		324	MHz
t_{SETUP}	SubLVDS data setup time to SCLKP/N transition; see Figure 4	LVDS Parallel modes	1500			ps
		All other modes	350			
t_{HOLD}	SubLVDS data hold time after SCLKP/N transition; see Figure 4	LVDS Parallel modes	1500			ps
		All other modes	350			
t_{DUTCLK}	SubLVDS CLK input clock duty cycle		45%		55%	
C_L	Parallel output load capacitance(1)			5	6	pF
t_j	CLKOUT total jitter	Peak to peak			190	ps
R_j	Residual jitter				8	
D_j	Deterministic jitter				80	

(1) The SN65LVDS324 supports up to 10pF parallel output load capacitance under test conditions.

7.4 Thermal Information

THERMAL METRIC(1)		SN65LVDS324 ZQL	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	73.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	30.6	
$R_{\theta JB}$	Junction-to-board thermal resistance	37.7	
ψ_{JT}	Junction-to-top characterization parameter	1.3	
ψ_{JB}	Junction-to-board characterization parameter	36.9	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	125	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

7.5 DC Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
V_{THL}	Low-level differential input voltage threshold	$V_{SD[11:0]P} – V_{SD[11:0]N}$, $V_{SCLKP} – V_{SCLKN}$	–40			mV
V_{THH}	High-level differential input voltage threshold				40	mV
V_{IL}	Low-level control signal input voltage	SCL, SDA			0.3×V_{CC}	V
V_{IH}	High-level control signal input voltage	SCL, SDA	0.7×V_{CC}			V
V_{OH}	High-level output voltage	I_{OH} = –2 mA	1.3			V
V_{OL}	Low-level output voltage	I_{OL} = 2 mA			0.4	V
I_{OS}	Short circuit output current	Output V_{OH} driving GND short	–35			mA
I_{LEAK}	Failsafe input leakage current	V_{CC} = 0; $V_{CC(PIN)}$ =1.8 V			10	µA
I_{IH}	High level input current	SDA, SCL			5	µA
I_{IL}	Low level input current				5	µA
I_{CC}	Active current(2) (3)	LVDS Parallel 1080p60		89	125	mA
		2-Channel 2-Port 1080p60 1-Channel 4-Lane 1080p60		83	120	
		1-Channel 2-Lane 720p60		74	100	
R_{DIFF}	Differential termination resistance		80	100	125	Ω
R_{RST}	Reset input resistance		120	150	180	kΩ
C_{IN}	Input pin capacitance			1.5		pF

(1) All typical values are at V_{CC} = 1.8V and T_A = 25°C
(2) V_{CC} = 1.95V; T_A = 0°C; C_L = 6pF; Worst case test pattern
(3) V_{CC} = 1.8V; T_A = 25°C; C_L = 5pF; Typical power test pattern

7.6 Switching Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP[(1)]	MAX	UNIT
F_{CLKOUT}	CLKOUT frequency	C_L = 6 pF	18.5		162	MHz
t_{del}	Data valid to CLKOUT↑ (see Figure 5)	C_L = 6 pF; CSR 09[3] = 1	1.5			ns
		C_L = 6 pF; CSR 09[3] = 0	3.8			
t_{pd}	CLKOUT↑ to data switching (see Figure 5)	C_L = 6 pF; CSR 09[3] = 1	1.5			ns
		C_L = 6 pF; CSR 09[3] = 0	0.2			
t_{en}	Enable time, $\overline{RST}$ ↑ to output valid and CLKOUT meets electrical specifications	F_{CLKOUT} = 148.5 MHz, See Figure 6			2	ms
t_r	Rise transition time, output (20% to 80%)	C_L = 6 pF, CSR 0A[5:4] = 10	450	750	1300	ps
t_f	Fall transition time, output (80% to 20%)	C_L = 6 pF, CSR 0A[5:4] = 10	450	750	1300	
t_{dc}	CLKOUT duty cycle		45%		55%	

(1) All typical values are at V_{CC} = 1.8V and T_A = 25°C.

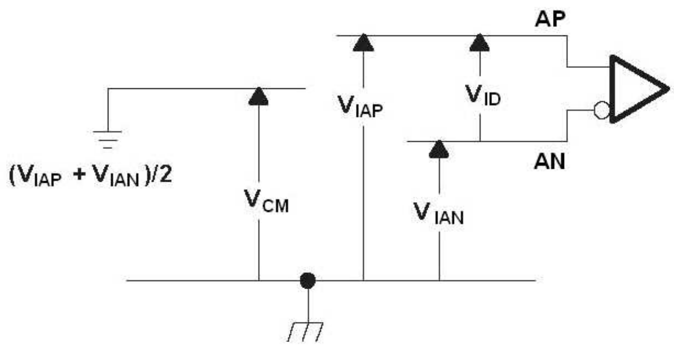


Figure 1. SubLVDS Input Voltage Definitions

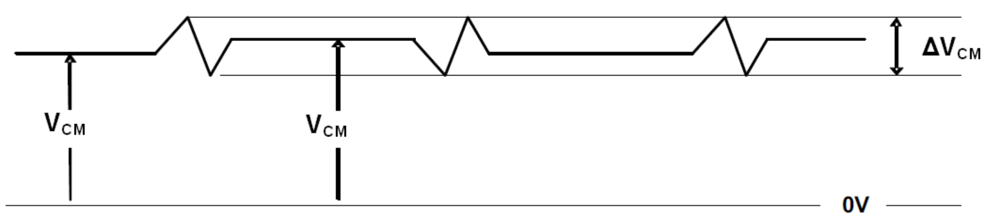


Figure 2. SubLVDS Delta Common Mode Input Voltage Definition

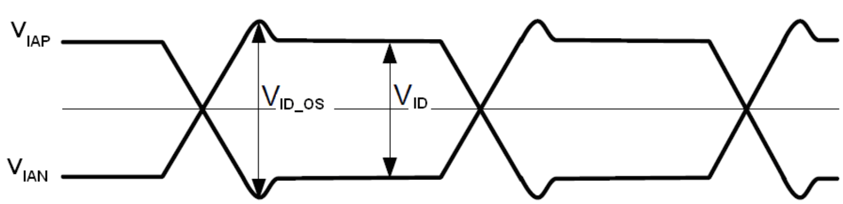


Figure 3. V_{ID} Overshoot Definition

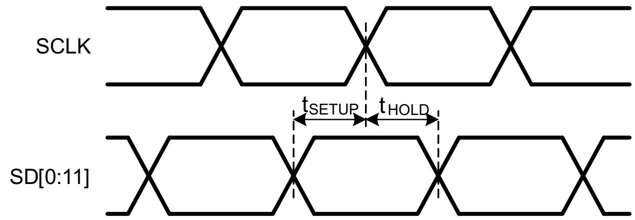


Figure 4. SubLVDS Timing Definitions

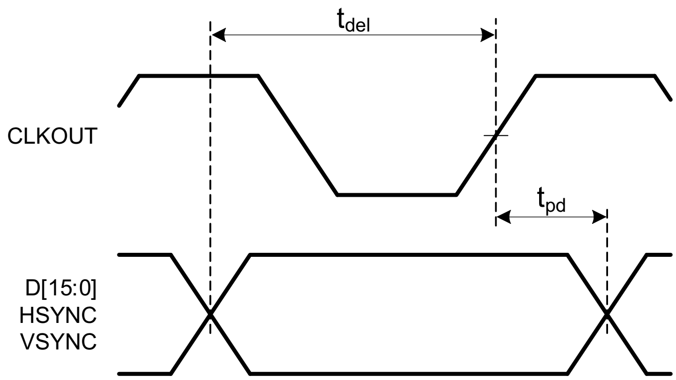


Figure 5. CMOS Output Timing Waveforms

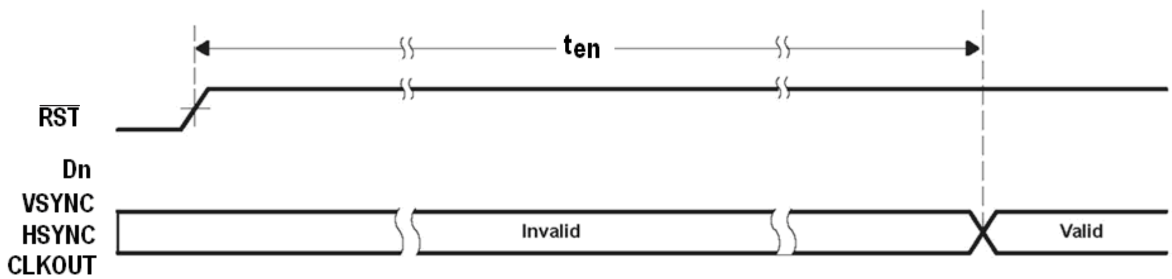


Figure 6. Device Enable Waveforms

7.7 Typical Characteristics

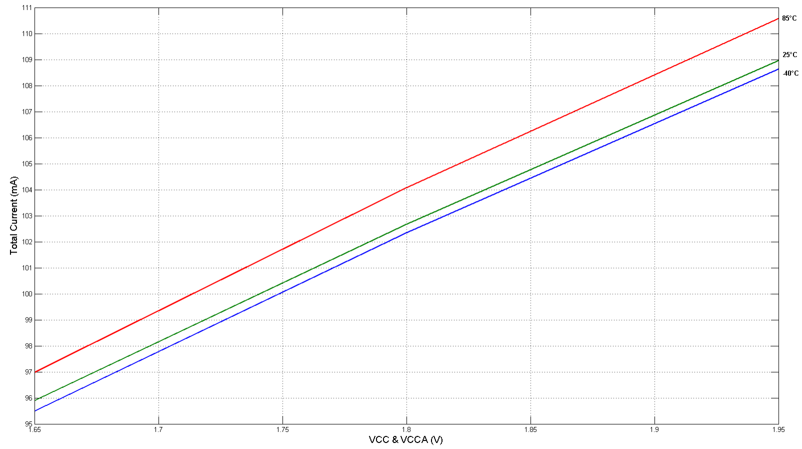


Figure 7. SN65LVDS324 Power Consumption - Sony LVDS Parallel Mode

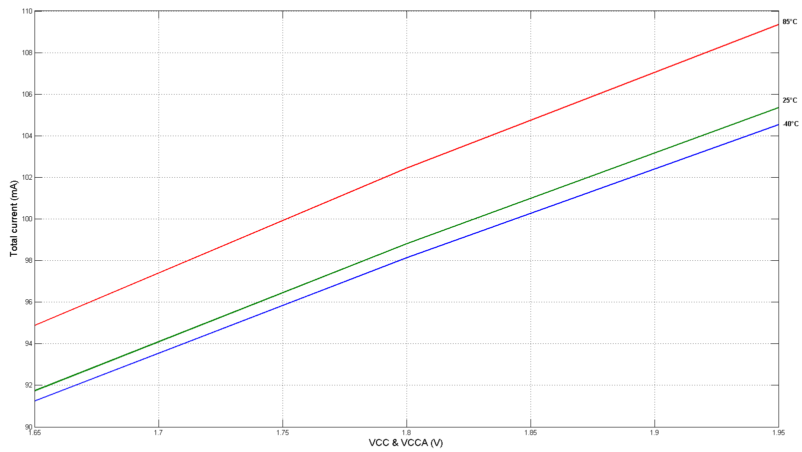


Figure 8. SN65LVDS324 Power Consumption - Panasonic LVDS Mode

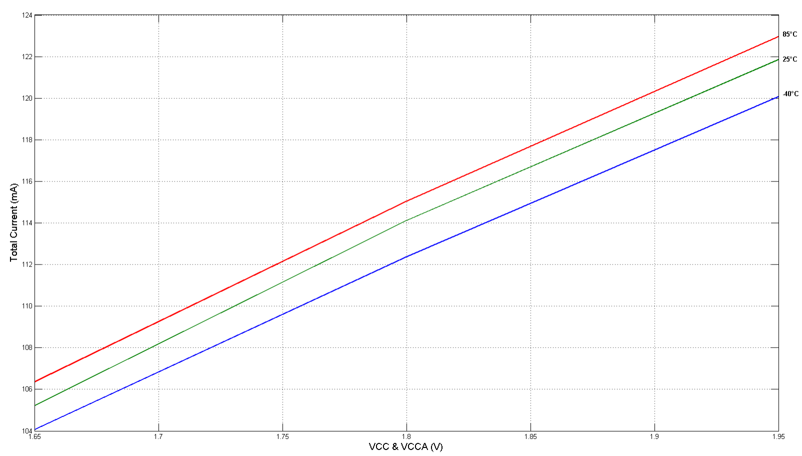


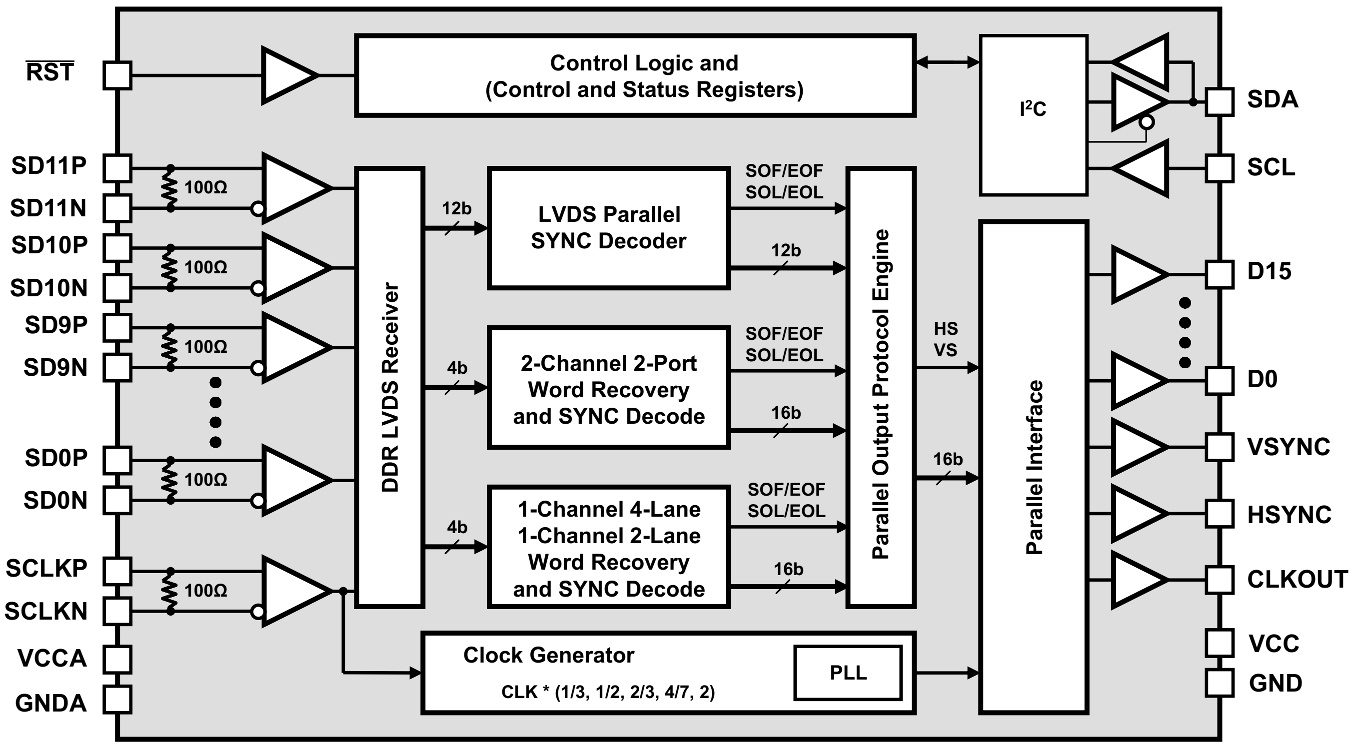
Figure 9. SN65LVDS324 Power Consumption - Aptina HiSPi Mode

8 Detailed Description

8.1 Overview

The SN65LVDS324 is a SubLVDS deserializer that recovers words, detects sync codes, multiplies the input DDR clock by a ratio, and outputs parallel CMOS 1.8 V data on the rising clock edge. It bridges the video stream interface between HD image sensors made by leading manufacturers, to a format that common processors can accept. The supported pixel frequency is 18.5 MHz to 162 MHz (suitable for resolutions from VGA to 1080p60).

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Reset Implementation

When $\overline{RST}$ is Low, the PLL is disabled, the SubLVDS inputs are disabled, and all outputs drive either V_{OH} or V_{OL} with no toggling. It is critical to transition the $\overline{RST}$ input from a low to high level after the V_{CC} supply has reached the minimum recommended operating voltage. This is achieved by an external capacitor connected between $\overline{RST}$ and GND, and/or by a control signal to the $\overline{RST}$ input. Both implementations are shown, Figure 10 and Figure 11:

NOTE

After the $\overline{RST}$ signal has been de-asserted and any time the Sub-LVDS input clock is removed and re-applied, write to I2C Register 0x28 a value of 0x03 for proper operation.

Feature Description (continued)

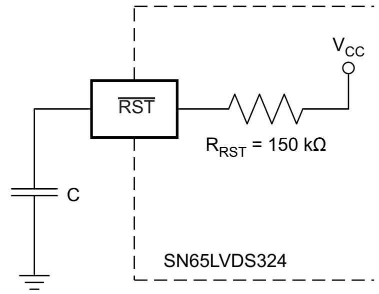


Figure 10. External Capacitor Controlled RST

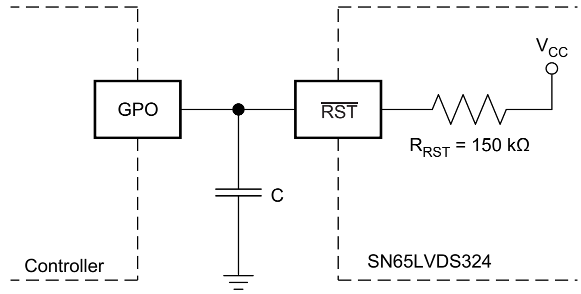


Figure 11. RST Input from Active Controller

8.4 Device Functional Modes

Table 1. SN65LVDS324 Modes, Common Frequencies, and Signals Used(1)(2)

SENSOR_CFG (CSR 09[2:0])	SubLVDS Interface Mode	Bits Per Pixel	Target Video	Target SCLK Frequency (MHz)	Target PLL_CFG (CSR 0A[1:0])	Target CLKOUT Frequency (MHz)	SCLK	SD [0:1]	SD2	SD [3:4]	SD [5:9]	SD [10:11]
000	Sony LVDS Parallel	10	1080p 60fps	74.25	10	148.5	Sensor Clock	GND	X[2]	X[3:4]	X[5:9]	X[10:11]
001		12						X[0:1]				
010	Panasonic 2-Channel 2-Port	12		222.75	10		Sensor Ch1 Clock	Ch1 X[0:1]	Sensor Ch2 Clock	Ch2 X[0:1]	GND	GND
011		16		297	11							
100	Aptina 1-Channel 4-Lane	12		222.75	10		Sensor Clock	X[0:1]	X[2]	X[3], GND		
110		16		297	11							
101		14	720p 60fps	129.9375	00	74.25						
111	Aptina 1-Channel 2-Lane	12		222.75	10				GND	GND		

(1) X[0:11] represent the connected sensor's LVDS data lanes.
(2) GND represents a connection to the system reference ground.

8.4.1 Aptina Mode Specifics

Only the Streaming-SP HiSPi mode is supported. If "FLR" and "CRC" are in the data stream, the SN65LVDS324 will transmit them. "IDL" cannot match a sync code or be all-zero.

8.4.2 VSYNC and HSYNC Output Timing

Figure 12 describes the horizontal and vertical blanking periods, and how they generally relate to the VSYNC and HSYNC outputs. The SN65LVDS324 asserts VSYNC (driven high) by default, and drives VSYNC high for at least one CLKOUT cycle at the beginning of each video frame. The SN65LVDS324 sensor interface logic determines the beginning of an active video frame by sensor-dependent methods.

There may be certain VSYNC and HSYNC operating requirements in the video processing pipeline in the DSP, such as a required number of vertical blanking lines, requirements for horizontal sync during vertical blanking, or requirements for data patterns during blanking times, special requirements for still image capture, etc. Systems that utilize SN65LVDS324 are required to configure the sensor to meet the vertical blanking and horizontal blanking requirements set by DSP video processing pipeline; these limitations shall be met by the sensor and not by SN65LVDS324 logic.

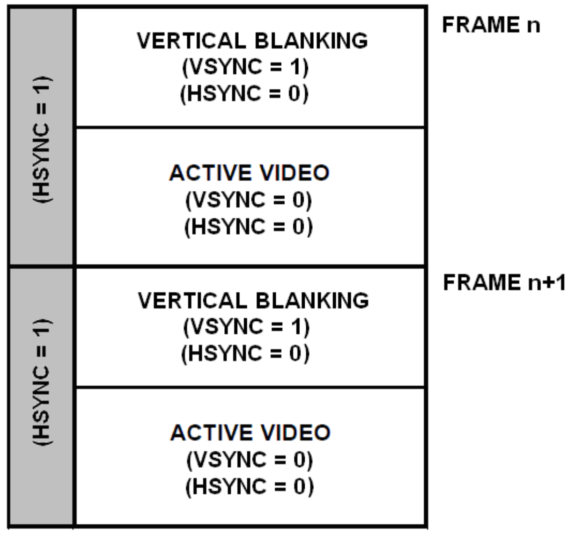


Figure 12. VSYNC and HSYNC Output Relation to Active Video Frames

HSYNC is asserted (driven high) by default. HSYNC is driven low during the active video data stream transfer, as illustrated in Figure 13. HSYNC may be de-asserted (driven low) while VSYNC is asserted or de-asserted.

As shown in Figure 13, the HSYNC output is generally asserted following an EOL (End of Line) indication from the image sensor, and de-asserted (driven low) following a SOL (Start of Line) indication. Figure 13 further illustrates the data expected on the output interface during blanking periods.

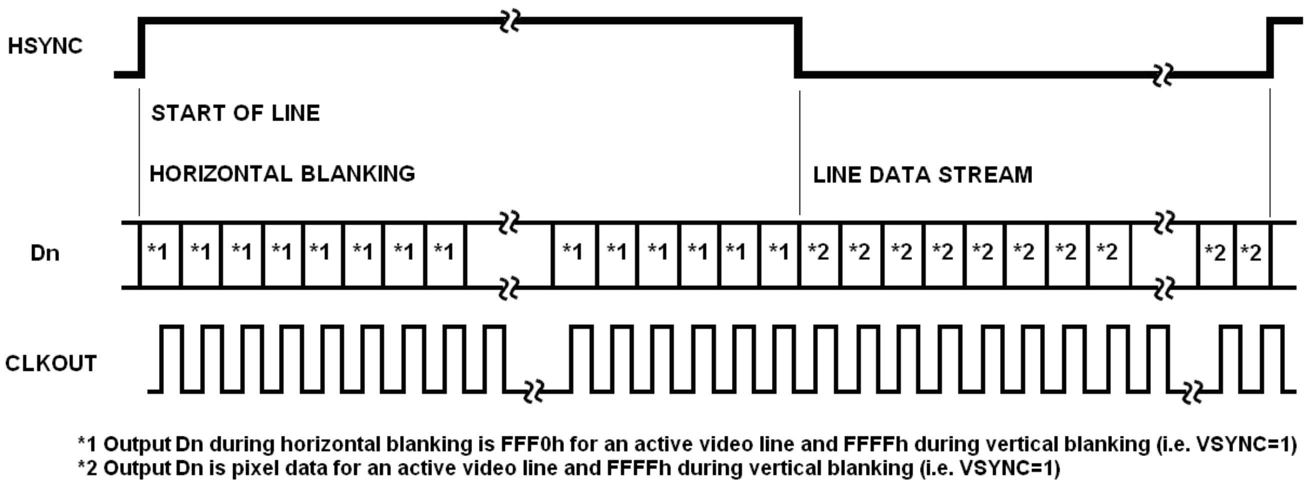


Figure 13. HSYNC Output Relation to Line Data Stream

NOTE

The SN65LVDS324 overrides the fixed patterns illustrated in Figure 13 (FFF0h and FFFFh as shown by notes *1 and *2) when line data is received from the sensor during blanking periods.

8.5 Register Maps

8.5.1 Local I²C Interface Overview

The SCL and SDA terminals are used for I²C clock and I²C data, respectively. The SN65LVDS324 I²C interface conforms to the two-wire serial interface defined by the I²C Bus Specification, Version 2.1 (January 2000), and supports standard mode transfers up to 400 kbps.

The device address byte is the first byte received following the START condition from the master device. The 7 bit device address for SN65LVDS324 is factory preset to 7'b0101101 (0x2D). Table 2 clarifies the SN65LVDS324 target address.

Table 2. SN65LVDS324 I²C Target Address Description

SN65LVDS324 I²C TARGET Address(1)							
Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (W/R)
0	1	0	1	1	0	1	0/1

(1) When ADDR=1, Address Cycle is 0x5A (Write) and 0x5B (Read)

The following procedure is followed to write to the SN65LVDS324 I²C registers:

1. The master initiates a write operation by generating a start condition (S), followed by the SN65LVDS324 7-bit address and a zero-value "W/R" bit to indicate a write cycle.
2. The SN65LVDS324 acknowledges the address cycle.
3. The master presents the sub-address (I²C register within SN65LVDS324) to be written, consisting of one byte of data, MSB-first.
4. The SN65LVDS324 acknowledges the sub-address cycle.
5. The master presents the first byte of data to be written to the I²C register.
6. The SN65LVDS324 acknowledges the byte transfer.
7. The master may continue presenting additional bytes of data to be written, with each byte transfer completing with an acknowledge from the SN65LVDS324.
8. The master terminates the write operation by generating a stop condition (P).

The following procedure is followed to read the SN65LVDS324 I²C registers:

1. The master initiates a read operation by generating a start condition (S), followed by the SN65LVDS324 7-bit address and a one-value "W/R" bit to indicate a read cycle.
2. The SN65LVDS324 acknowledges the address cycle.
3. The SN65LVDS324 transmit the contents of the memory registers MSB-first starting at the last address specified.
4. The SN65LVDS324 will wait for either an acknowledge (ACK) or a not-acknowledge (NACK) from the master after each byte transfer; the I²C master acknowledges reception of each data byte transfer.
5. If an ACK is received, the SN65LVDS324 transmits the next byte of data.
6. The master terminates the read operation by generating a stop condition (P).

8.5.2 Control and Status Registers Overview

CSR's are accessible through the local I^2C interface. See Table 3 for SN65LVDS324 CSR descriptions. Reads from reserved fields not described return zeros, and writes are ignored.

CSR's "SENSOR_CFG" and "PLL_CFG" must be set before the input clock (SCLK) is applied.

Table 3. SN65LVDS324 CSR Bit Field Definitions

ADDRESS	BIT(S)	DESCRIPTION	ACCESS (1)
0x00 – 0x07	7:0	DEVICE_ID Returns a string of ASCII characters "LVDS324" preceded by one space character. Addresses 0x00 - 0x07 = {0x20, 0x4C, 0x56, 0x44, 0x53, 0x33, 0x32, 0x34}	R
0x08	7:0	DEVICE_REV Device revision; returns 0x01	R
0x09	7	SOFT_RESET This bit automatically clears when set to '1' and returns zeros when read. When set, the device is reset to the default condition.	RW
	6	TESTMODE_VIDEO When enabled, the device outputs a known color pattern with SCLK applied. The pattern is 128 lines of red, 128 of green, and 128 of blue, repeated. CSR addresses 0B, 0C, 0D, and 0E set the active image area, while addresses 1F, 20, 21, and 22 set the entire frame including blanking. SENSOR_CFG and PLL_CFG control the bpp, PLL multiplier, and PLL range. The CLKOUT frequency directly scales the frame rate; for the default 2250x1100 frame, a CLKOUT frequency of 148.5MHz causes 60fps. 0 – Disabled (default) 1 – Enabled	RW
	5	LSB_FIRST_OUTPUT 0 – Output data is MSB first; D[15:0] output represents MSB at D0 1 – Output data is LSB first; D[15:0] output represents LSB at D0 (default)	RW
	4	SYNC_ACTIVE_HIGH 0 – VSYNC and HSYNC are output low during blanking periods 1 – VSYNC and HSYNC are output high during blanking periods (default)	RW
	3	CLK_CENTERED_TIMING 0 – Output timing accommodates long setup time receivers [e.g. DaVinci] (default) 1 – Outputs are clock-centered for relatively matched setup/hold receivers [e.g. OMAP]	RW
	2:0	SENSOR_CFG This field shall be written to configure the sensor interface per Table 1. 000 – LVDS Parallel 10bpp mode (default) 001 – LVDS Parallel 12bpp mode 010 – 2-Channel 2-Port 12bpp mode 011 – 2-Channel 2-Port 16bpp mode 100 – 1-Channel 4-Lane 12bpp mode 101 – 1-Channel 4-Lane 14bpp mode 110 – 1-Channel 4-Lane 16bpp mode 111 – 1-Channel 2-Lane 12bpp mode	RW

(1) R = Read Only; RW = Read/Write (only reads return undetermined values)

Table 3. SN65LVDS324 CSR Bit Field Definitions (continued)

<table>
<tr><th>ADDRESS</th><th>BIT(S)</th><th>DESCRIPTION</th><th>ACCESS (1)</th></tr>
<tr><td rowspan="4">0x0A</td><td>7</td><td>CLKOUT_PLL_LOCK
0 – Output pixel clock PLL not locked
1 – Output pixel clock PLL locked</td><td>R</td></tr>
<tr><td>6</td><td>VCM_MODE
0 – Selects Low common mode voltage range
1 – Selects High common mode voltage range (default)</td><td>RW</td></tr>
<tr><td>5:4</td><td>D_SLEW_RATE
Controls the rise and fall time for D[15:0].
00 – Slowest; sets to 50% of the baseline speed
01 – Slower; sets to 75% of the baseline speed
10 – Baseline (default)
11 – Fastest; sets to 150% of the baseline speed</td><td>RW</td></tr>
<tr><td>1:0</td><td>PLL_CFG
This field sets the allowable SCLK frequency range, based on the mode set by SENSOR_CFG. The register defaults to 10 (and 01 for the 14bpp mode).

LVDS Parallel 10/12bpp (PLL Multiplier = 2)
00 – SCLK = 18.5 to 33MHz, CLKOUT = 37 to 66MHz
01 – SCLK = 31 to 60MHz, CLKOUT = 62 to 120MHz
10 – SCLK = 58 to 81MHz, CLKOUT = 116 to 162MHz
11 – Reserved

2-Channel 2-Port 12bpp and 1-Channel 4-Lane 12bpp (PLL Multiplier = 2/3)
00 – SCLK = 55.5 to 99MHz, CLKOUT = 37 to 66MHz
01 – SCLK = 97 to 180MHz, CLKOUT = 64.7 to 120MHz
10 – SCLK = 178 to 243MHz, CLKOUT = 118.7 to 162MHz
11 – Reserved

2-Channel 2-Port 16bpp and 1-Channel 4-Lane 16bpp (PLL Multiplier = ½)
00 – SCLK = 74 to 120MHz, CLKOUT = 37 to 60MHz
01 – SCLK = 118 to 180MHz, CLKOUT = 59 to 90MHz
10 – SCLK = 178 to 222MHz, CLKOUT = 89 to 111MHz
11 – SCLK = 220 to 324MHz, CLKOUT = 110 to 162MHz

1-Channel 4-Lane 14bpp (PLL Multiplier = 4/7)
00 – SCLK = 120 to 220MHz, CLKOUT = 68.6 to 125.7MHz
01 – SCLK = 218 to 283.5MHz, CLKOUT = 124.6 to 162MHz
10 – Reserved
11 – Reserved

1-Channel 2-Lane 12bpp (PLL Multiplier = 1/3)
00 – SCLK = 55.5 to 99MHz, CLKOUT = 18.5 to 33MHz
01 – SCLK = 97 to 180MHz, CLKOUT = 32.3 to 60MHz
10 – SCLK = 178 to 297MHz, CLKOUT = 59.3 to 99MHz
11 – Reserved</td><td>RW</td></tr>
</table>

Table 3. SN65LVDS324 CSR Bit Field Definitions (continued)

ADDRESS	BIT(S)	DESCRIPTION	ACCESS (1)
0x0B	4:0	FRAME_WIDTH_MSB The width of the active area; this field is the high order byte. The default is 1920 (0x**07**80), and this field's default is 0x07. The max width is 8191. When TESTMODE_VIDEO is disabled, this field is only used to set SENSOR_SPECIFIC registers that flag window size errors.	RW
0x0C	7:0	FRAME_WIDTH_LSB The width of the active area; this field is the low order byte. The default is 1920 (0x07**80**), and this field's default is 0x80. The max width is 8191. When TESTMODE_VIDEO is disabled, this field is only used to set SENSOR_SPECIFIC registers that flag window size errors.	RW
0x0D	4:0	FRAME_HEIGHT_MSB The height of the active area; this field is the high order byte. The default is 1080 (0x**04**38), and this field's default is 0x04. The max height is 8191. When TESTMODE_VIDEO is disabled, this field is only used to set SENSOR_SPECIFIC registers that flag window size errors. In LVDS Parallel modes, the height must include all lines between SAV-Valid and EAV-Valid.	RW
0x0E	7:0	FRAME_HEIGHT_LSB The height of the active area; this field is the low order byte. The default is 1080 (0x04**38**), and this field's default is 0x38. The max height is 8191. When TESTMODE_VIDEO is disabled, this field is only used to set SENSOR_SPECIFIC registers that flag window size errors. In LVDS Parallel modes, the height must include all lines between SAV-Valid and EAV-Valid.	RW
0x0F – 0x1E	7:0	SENSOR_SPECIFIC These are sensor-specific status registers, and depend on SENSOR_CFG. They are further described by Table 4 through Table 6.	RW
0x1F	4:0	TESTMODE_WIDTH_MSB Applies only when TESTMODE_VIDEO is enabled, and configurable up to 8191 pixels. This field controls the high order byte of the frame width including blanking; the default is 2250 (0x08CA), and this field's default is 0x08. For 720p, a width of 1500 (0x**05**DC) facilitates 60fps with 74.25MHz.	RW
0x20	7:0	TESTMODE_WIDTH_LSB Applies only when TESTMODE_VIDEO is enabled, and configurable up to 8191 pixels. This field controls the low order byte of the frame width including blanking; the default is 2250 (0x08**CA**), and this field's default is 0xCA. For 720p, a width of 1500 (0x05**DC**) facilitates 60fps with 74.25MHz.	RW
0x21	4:0	TESTMODE_HEIGHT_MSB Applies only when TESTMODE_VIDEO is enabled, and configurable up to 8191 pixels. This field controls the high order byte of the frame height including blanking; the default is 1100 (0x**04**4C), and this field's default is 0x04. For 720p, a height of 825 (0x**03**39) facilitates 60fps with 74.25MHz.	RW
0x22	7:0	TESTMODE_ HEIGHT_LSB Applies only when TESTMODE_VIDEO is enabled, and configurable up to 8191 pixels. This field controls the low order byte of the frame height including blanking; the default is 1100 (0x04**4C**), and this field's default is 0x4C. For 720p, a height of 825 (0x03**39**) facilitates 60fps with 74.25MHz.	RW
0x23 – 0x30	7:0	RESERVED These registers are reserved for factory test. Do not write to them.	RW

Table 4. Sensor-Specific Registers for Aptina Modes

ADDRESS	BIT(S)	DESCRIPTION	ACCESS(1)
0x0F	6	FILLER_EN 0 – FLR codes are not used in data stream 1 – FLR codes are used in data stream (default)	RW
	5	CRC_EN 0 – CRC is not used in the data stream 1 – CRC is used in the data stream (default)	RW
0x10	7	CLEAR_STATUS When a '1' is written to this field, the status bits in 0x10 and 0x11 are cleared, and this bit is auto-cleared to a zero value (always returns zero when read)	W
	3	CRC_ERR_LANE3 0 – No checksum error detected (default) 1 – Checksum error detected Note: Bits in registers 0x10 and 0x11 are latched and cleared only when the CLEAR_STATUS field is written.	R
	2	CRC_ERR_LANE2; same bit function as CRC_ERR_LANE3 but applied to LANE 2.	R
	1	CRC_ERR_LANE1; same bit function as CRC_ERR_LANE3 but applied to LANE 1.	R
	0	CRC_ERR_LANE0; same bit function as CRC_ERR_LANE3 but applied to LANE 0.	R
0x11	5	UNKNOWN_SYNC_CODE 0 – No unexpected sync code (default) 1 – Sync code (final word of sync_code) does not match a defined type	R
	4	SOF_ERR 0 – No SOF error occurred (default) 1 – SOF was detected when it was unexpected	R
	3	SOL_ERR 0 – No SOL error occurred (default) 1 – SOL was detected when it was unexpected	R
	2	SOV_ERR 0 – No SOV error occurred (default) 1 – SOV was detected when it was unexpected	R

(1) R = Read Only; RW = Read/Write; W = Write Only (reads return undetermined values)

Table 5. Sensor-Specific Registers for Panasonic Modes

ADDRESS	BIT(S)	DESCRIPTION	ACCESS(1)
0x0F	7:0	Reserved.	R
0x10	7	CLEAR_STATUS When a '1' is written to this field, the status bits in 0x11 are cleared, and this bit is auto-cleared to a zero value (always returns zero when read)	W
0x11	7	FRAME_SIZE_ERROR 0 – Start up sequence has not identified a frame size error, decode window applied. 1 – Start up sequence identified a frame size error, decode window is not applied	R
	5	UNKNOWN_SYNC_CODE When set to'1', sync code (final word of sync_code) does not match a defined type	R
	4	SOF_ERR When set to '1', SOF was detected when it was unexpected per the decode window.	R
	3	SOL_ERR When set to '1', SOL was detected when it was unexpected per the decode window.	R
	1	EOF_ERR When set to '1', EOF was detected when it was unexpected per the decode window.	R
	0	EOL_ERR When set to '1', EOL was detected when it was unexpected per the decode window.	R

(1) R = Read Only; W = Write Only

Table 6. Sensor-Specific Registers for Sony Modes

ADDRESS	BIT(S)	DESCRIPTION	ACCESS(1)
0x0F	7:0	Reserved.	R
0x10	7	CLEAR_STATUS When a '1' is written to this field, the status bits in 0x11 are cleared, and this bit is auto-cleared to a zero value (always returns zero when read)	W
0x11	7	FRAME_SIZE_ERROR 0 – Start up sequence has not identified a frame size error, decode window applied. 1 – Start up sequence identified a frame size error, decode window is not applied	R
	5	UNKNOWN_SYNC_CODE When set to '1', sync code (final word of sync_code) does not match a defined type	R
	4	SAV_VALID_ERR When set to '1', SAV (Valid Line) was unexpectedly detected per the decode window.	R
	3	SAV_INVALID_ERR When set to '1', SAV (Invalid Line) was unexpectedly detected per the decode window.	R
	1	EAV_VALID_ERR When set to '1', EAV (Valid Line) was unexpectedly detected per the decode window.	R
	0	EAV_INVALID_ERR When set to '1', EAV (Invalid Line) was unexpectedly detected per the decode window.	R

(1) R = Read Only; W = Write Only (reads return undetermined values)

9 Application and Implementation

9.1 Application Information

The SN65LVDS324 offers several operating modes, as described in this section. The typical mode of 1080p60 involves a 148.5MHz output clock.

The parallel output video interface provides up to 16-bits of data per pixel, a vertical synchronization signal (VSYNC), and a horizontal synchronization signal (HSYNC) that are all synchronous to the output clock, CLKOUT. VSYNC and HSYNC are by default logically active high, and output a high logic level during blanking periods.

The following application diagrams illustrate each high-level typical configuration given in Table 1.

9.2 Typical Application

9.2.1 Sony LVDS Parallel 10-Bit Mode

Figure 14 illustrates the LVDS Parallel 10-bit mode for 1080p60 operation.

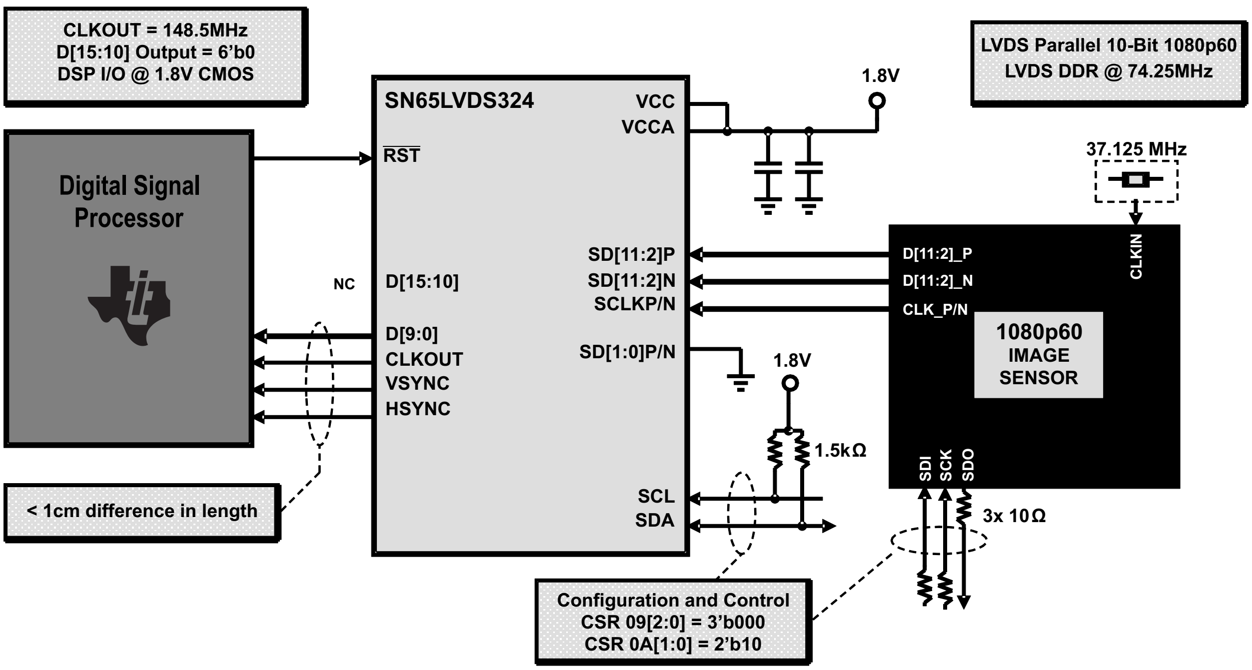


Figure 14. LVDS Parallel 10bpp Application

Typical Application (continued)

9.2.2 Design Requirements

- T_A Operating free-air temperature –40°C to 85 °C
- VCCA Analog Power supply 1.65 V – 1.95 V
- VCC Digital Power supply 1.65 V – 1.95 V
- |VID| Magnitude of differential input voltage 90 – 350 mV
- VCM Input common mode voltage (CSR 0A[6]=0) 100 650 mV (CSR 0A[6]=1) 550 1200 mV
- Peak to peak input VCM variation 50 mV
- VIN_DC SubLVDS receiver input voltage range 1400 mV
- VID_OS Differential VIN overshoot/undershoot 20%
- fCLK SubLVDS input clock (SCLKP/N) frequency 18.5 – 324 MHz
- SubLVDS input clock Maximum jitter specs
  - Total Jitter (Tj): 190ps
  - Random Jitter (Rj): 8ps
  - Deterministic Jitter (Dj): 80ps

9.2.3 Detailed Design Procedure

In this configuration, the image sensor transmits 10-bit video with a DDR reference clock operating at 74.25 MHz. The SN65LVDS324 provides a 2x PLL to convert the 74.25 MHz SubLVDS input to a 148.5 MHz pixel clock output (CLKOUT) for the 10-bit output interface.

An SPI-like serial bus is used to configure and control the sensor in this typical application example. The DSP shall properly configure the sensor to the particular target application, which may involve setting the electrical interface and optical gain settings.

The SN65LVDS324 identifies sync codes from the data stream to identify vertical and horizontal sync conditions, and sets the outputs HSYNC and VSYNC appropriately.

9.2.4 Panasonic 2-Channel 2-Port 12-Bit Mode

Figure 15 illustrates the 1080p60 2-Channel 2-Port 12-bit operating mode.

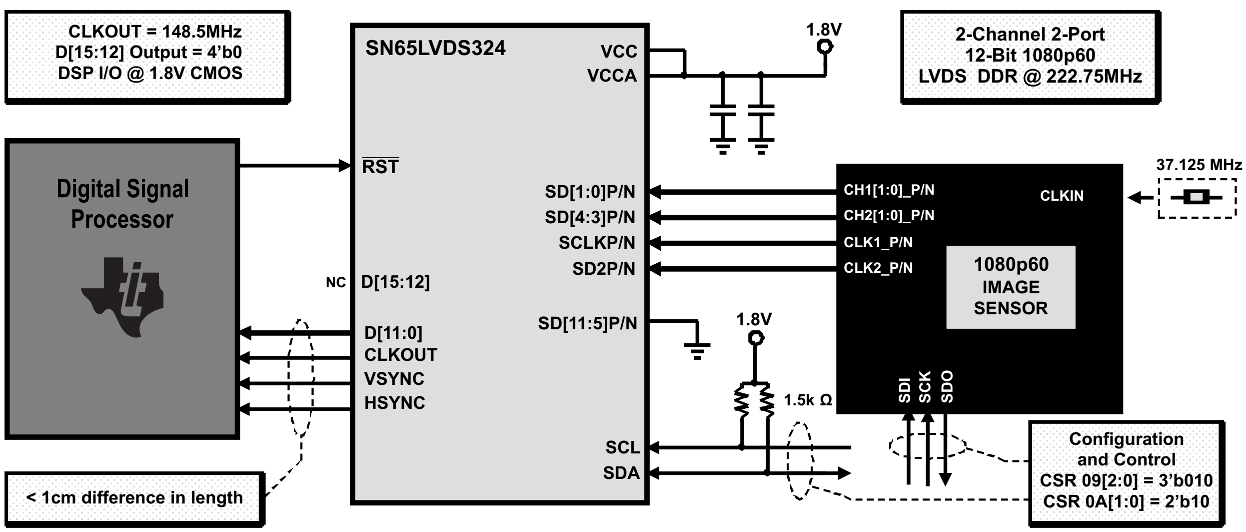


Figure 15. 2-Channel 2-Port 12bpp Application

The channel 2 clock is **not** guaranteed to be synchronous with channel 1; the SN65LVDS324 Word Alignment function provides the data synchronization between channel 1 and channel 2. If the sensor output is dual-frame WDR, the SN65LVDS324 transmits the data for both frames.

Typical Application (continued)

9.2.5 Panasonic 2-Channel 2-Port 16-bit Mode

Figure 16 illustrates the 16-bit color 1080p60 2-Channel 2-Port operating mode.

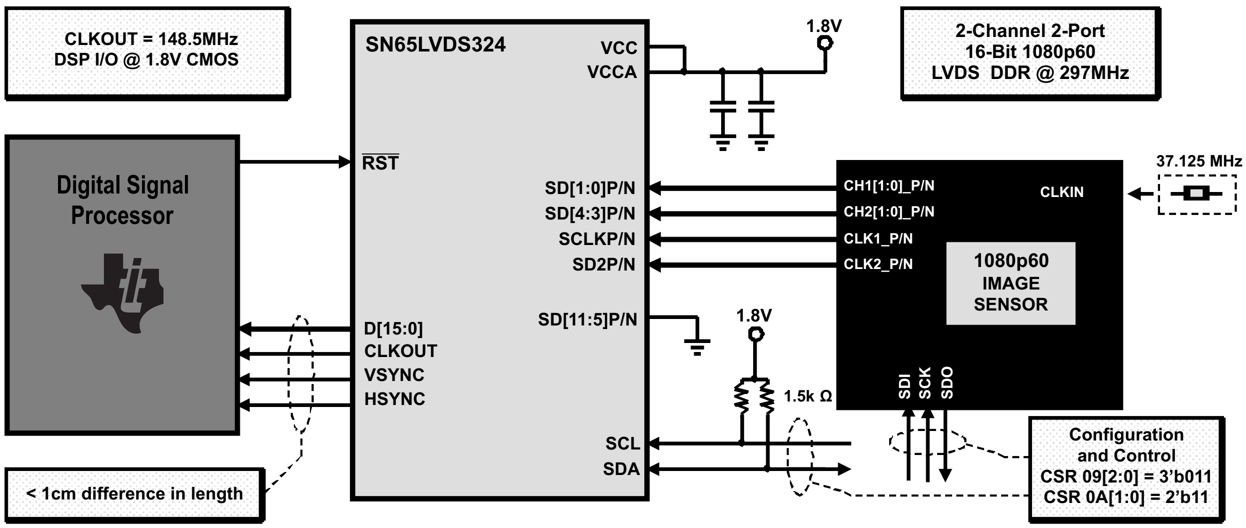


Figure 16. 2-Channel 2-Port 16bpp Application

9.2.6 Aptina 1-Channel 4-Lane 12-bit Mode

Figure 17 illustrates the 1080p60 1-Channel 4-Lane 12-bit per pixel operating mode with an image sensor pixel clock frequency is 148.5MHz (222.75 MHz SubLVDS clock frequency). In this configuration, the SN65LVDS324 outputs the parallel pixel clock (CLKOUT) at 148.5 MHz by implementing a PLL operating with a 2/3 multiplier from the SubLVDS clock input (SCLKP/N).

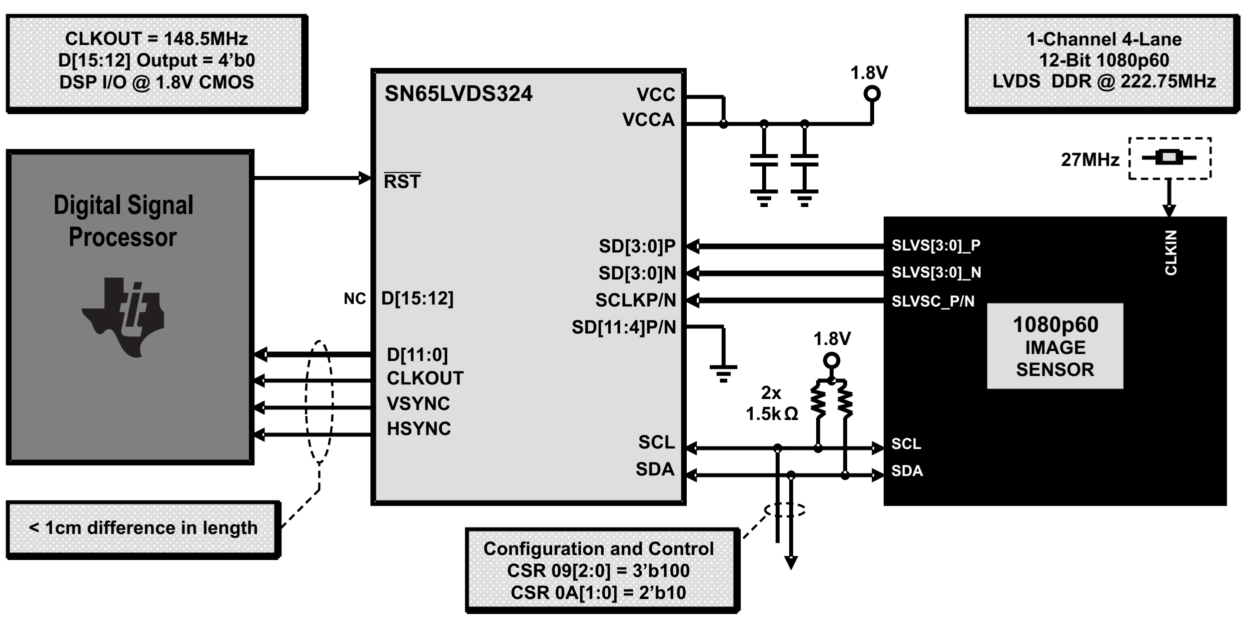


Figure 17. 1-Channel 4-Lane 12bpp Application

Typical Application (continued)

9.2.7 Aptina 1-Channel 4-Lane 14-bit Mode

Figure 18 illustrates the 1080p60 1-Channel 4-Lane 14-bit per pixel operating mode. Some image sensors utilize a compression method in 14-bit mode that communicates compressed data in 14 bits per pixel that can be expanded to 16 or 20 bits per pixel by the DSP video processing pipeline.

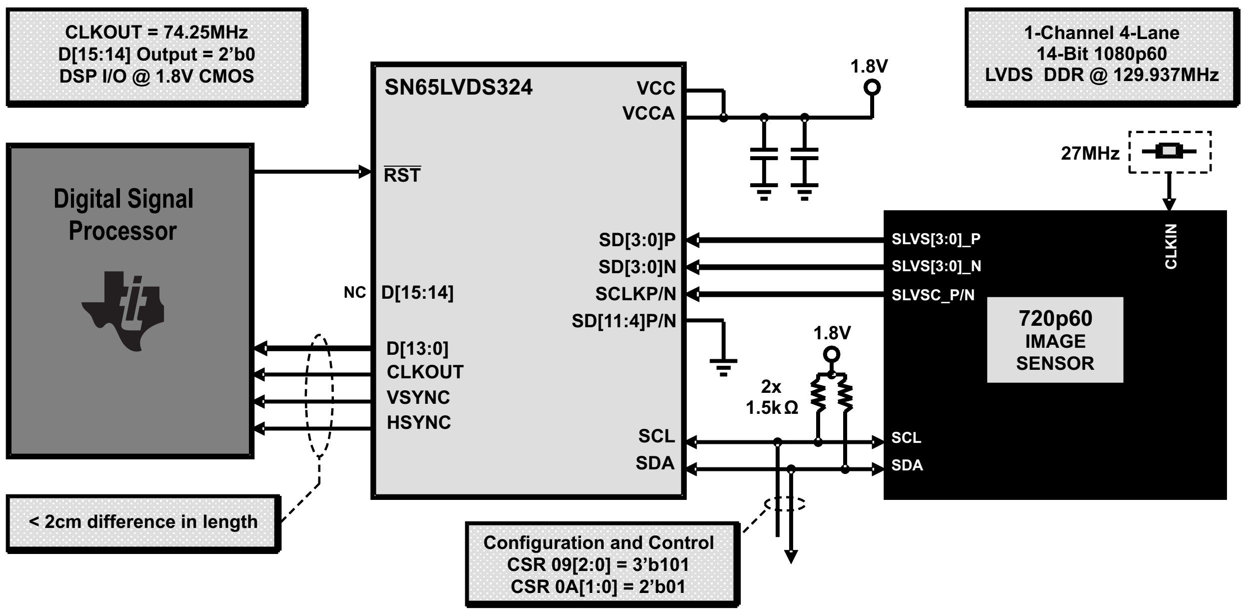


Figure 18. 1-Channel 4-Lane 14bpp Application

9.2.8 Aptina 1-Channel 4-Lane 16-bit Mode

Figure 19 illustrates the 1080p60 1-Channel 4-Lane 16-bit per pixel operating mode.

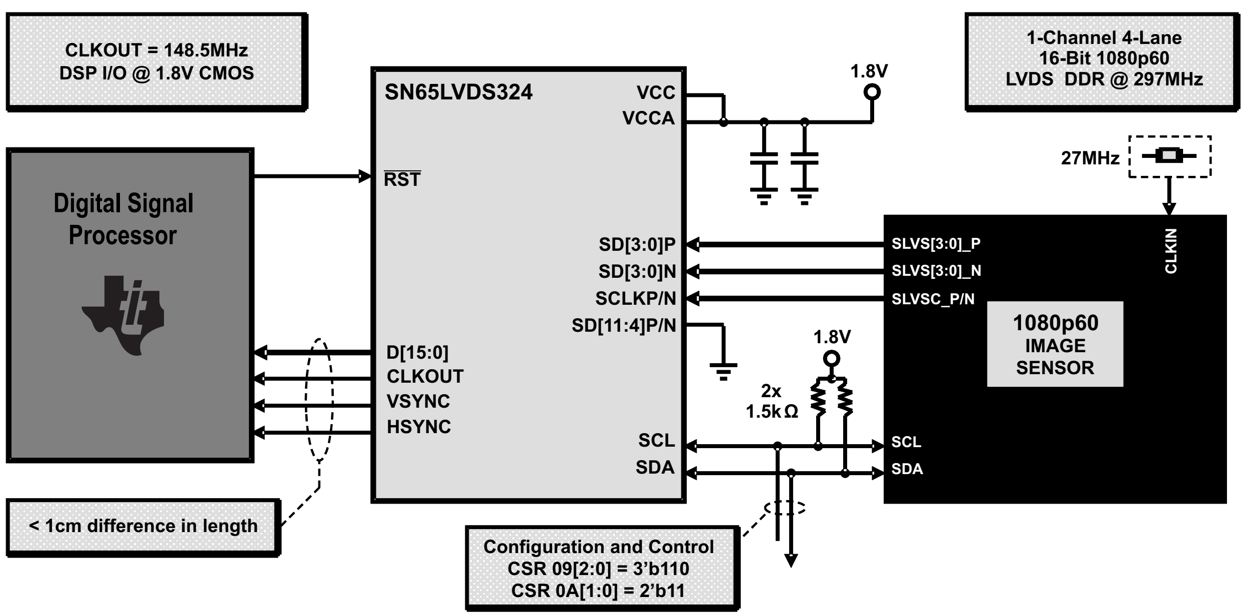


Figure 19. 1-Channel 4-Lane 16bpp Application

Typical Application (continued)

9.2.9 Aptina 1-Channel 2-Lane 12-bit Mode

Figure 20 illustrates the 720p60 1-Channel 2-Lane 12-bit per pixel operating mode.

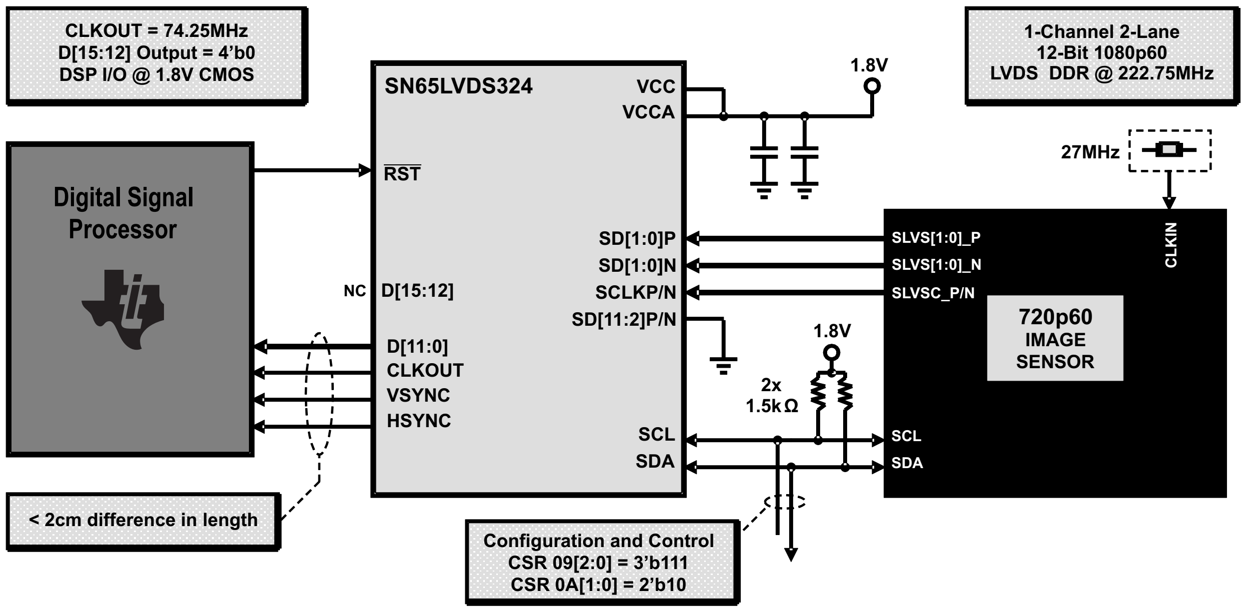


Figure 20. 1-Channel 2-Lane 12bpp Application

10 Power Supply Recommendations

10.1 Decoupling Recommendations

To minimize the power supply noise floor, provide good decoupling near the SN65LVDS324 power pins. The use of four ceramic capacitors (2x 0.01 µF and 2x 0.1 µF) provides good performance. At the very least, it is recommended to install one 0.1 µF and one 0.01 µF capacitor near the SN65LVDS324. To avoid large current loops and trace inductance, the trace length between decoupling capacitors and device power inputs pins must be minimized. Placing the capacitor underneath the SN65LVDS324 on the bottom of the PCB is often a good choice.

11 Layout

11.1 Layout Guidelines

SN65LVDS324 layout example, Figure 21, shows how the SN65LVDS324 should be placed with respect of the IMX136 and how to route the LVDS parallel lanes.

- Use 45 degree bends(chamfered corners),instead of right-angle(90°) bends. Right-angle bends increase the effective trace width, which changes the differential trace impedance creating large discontinuities. A 45° bends is seen as a smaller discontinuity.
- Place passive components within the signal path, such as source-matching resistors or ac-coupling capacitors, next to each other. Routing as in case a)creates wider trace spacing than in b),the resulting discontinuity, however, is limited to a far narrower area.
- When routing traces next to a via or between an array of vias, make sure that the via clearance section does not interrupt the path of the return current on the ground plane below.
- Avoid metal layers and traces underneath or between the pads off the connectors for better impedance matching.
- Use solid power and ground planes for 100-Ω impedance control and minimum power noise.
- For a multi-layer PCB, it is recommended to keep one common GND layer underneath the device and connect all ground terminals directly to this plane. For 100-Ω differential impedance, use the smallest trace spacing possible, which is usually specified by the PCB vendor.
- Keep the trace length as short as possible to minimize attenuation.
- Place bulk capacitors(i.e.10 µF) close to power sources, such as voltage regulators or where the power is supplied to the PCB.
- Reduce intra-pair skew in a differential trace by introducing small meandering corrections at the point of mismatch.
- When routing around an object, route both trace of a pair in parallel. Splitting the traces changes the line-to-line spacing, thus causing the differential impedance to change and discontinuities to occur.

11.2 Layout Example

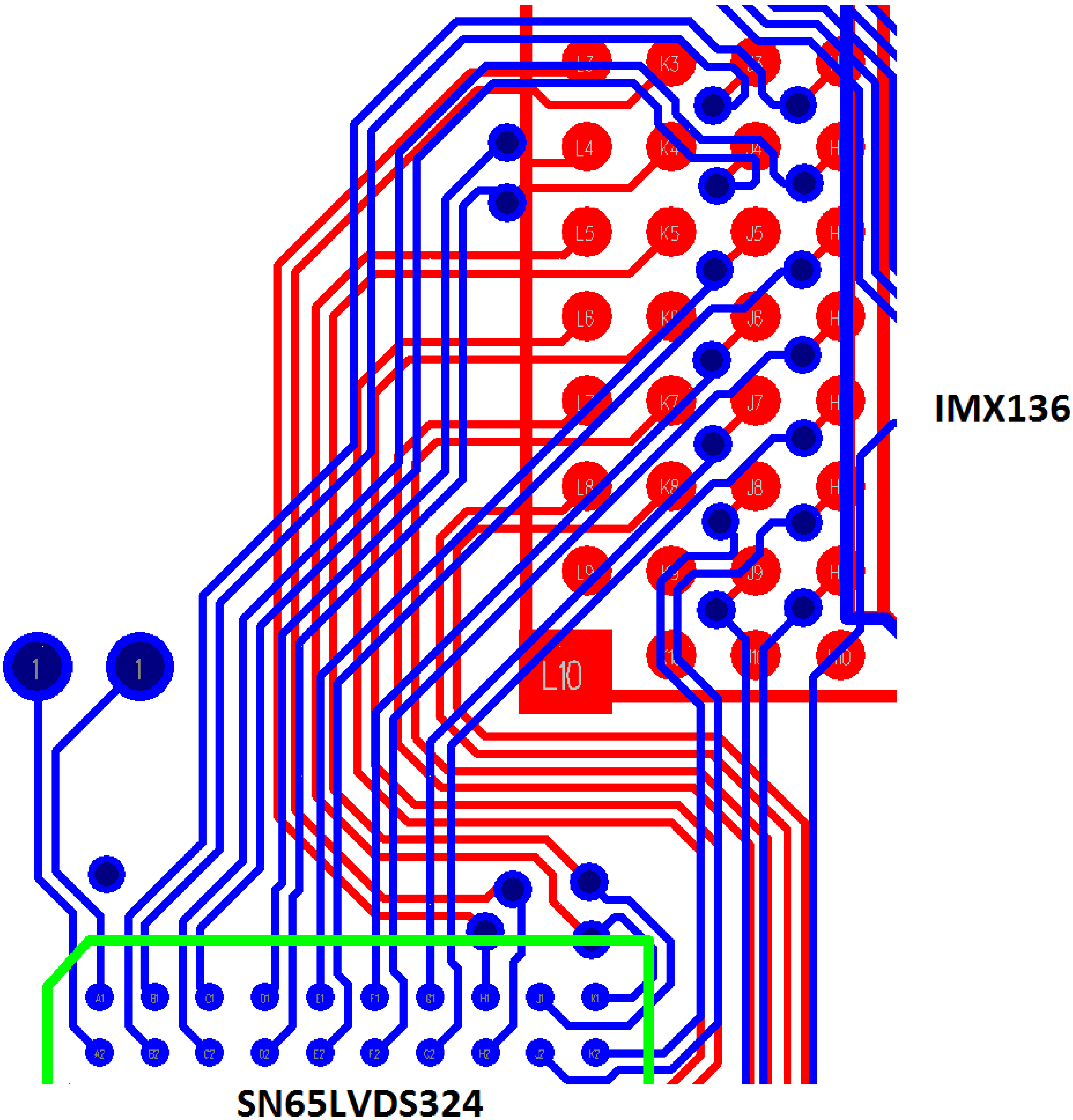


Figure 21. Layout Example

12 Device and Documentation Support

12.1 Trademarks

OMAP, DaVinci are trademarks of Texas Instruments.
HiSPi is a trademark of Aptina.

12.2 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.3 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN65LVDS324ZQLR	ACTIVE	BGA MICROSTAR JUNIOR	ZQL	59	1000	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR	-40 to 85	LVDS324	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

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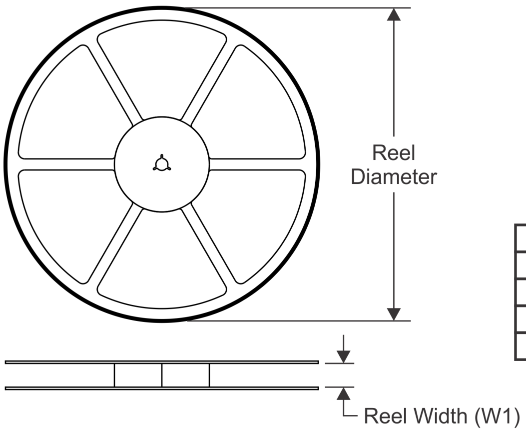
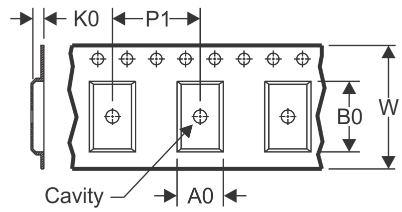
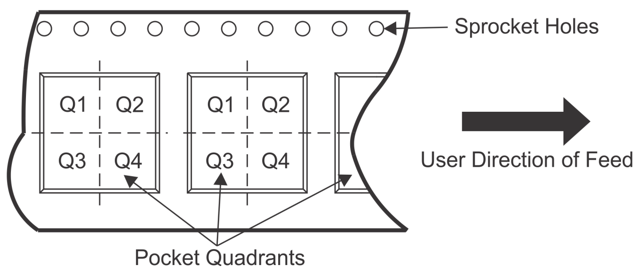
TAPE AND REEL INFORMATION





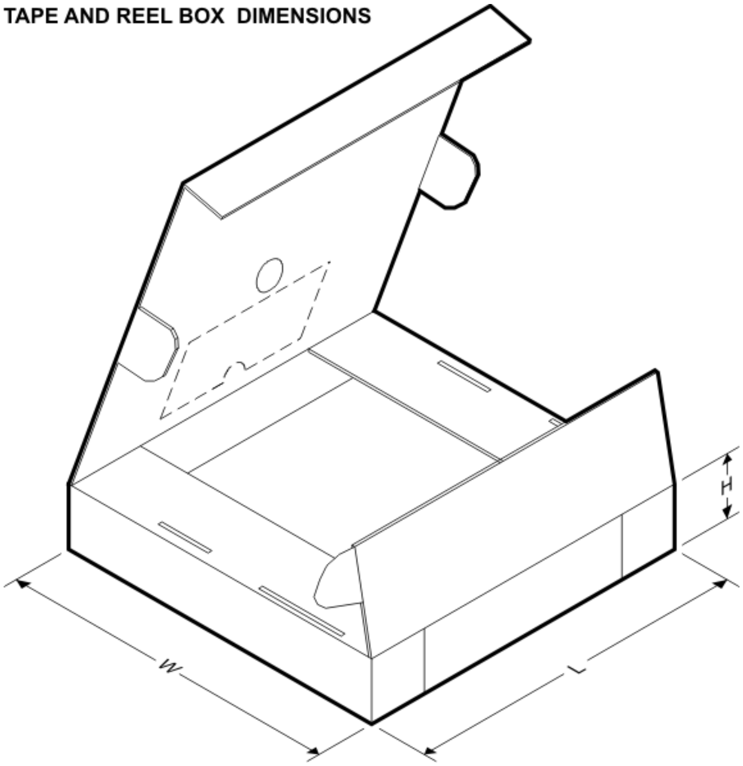
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65LVDS324ZQLR	BGA MICROSTAR JUNIOR	ZQL	59	1000	330.0	16.4	4.8	7.3	1.5	8.0	16.0	Q1

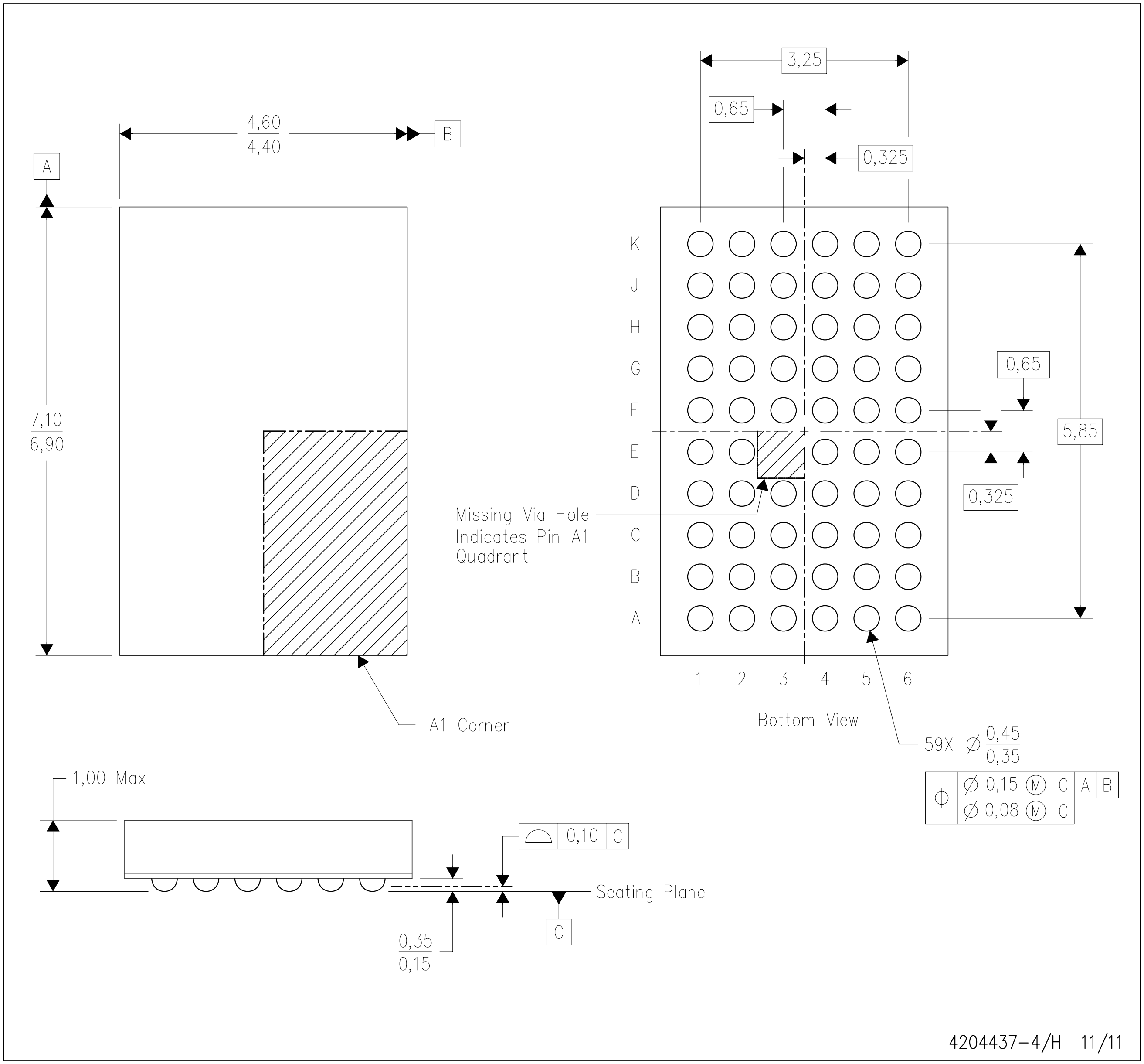
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65LVDS324ZQLR	BGA MICROSTAR JUNIOR	ZQL	59	1000	336.6	336.6	31.8

ZQL (R–PBGA–N59) PLASTIC BALL GRID ARRAY



NOTES:

A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.

B. This drawing is subject to change without notice.

C. Falls within JEDEC MO–285 variation BA–2.

D. This package is Pb–free.

MicroStar Junior is a trademark of Texas Instruments

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