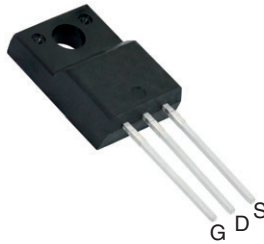


## E Series Power MOSFET

**Thin-Lead TO-220 FULLPAK**


N-Channel MOSFET

### FEATURES

- 4<sup>th</sup> generation E series technology
- Low figure-of-merit (FOM)  $R_{on} \times Q_g$
- Low effective capacitance ( $C_{o(er)}$ )
- Reduced switching and conduction losses
- Avalanche energy rated (UIS)
- Material categorization: for definitions of compliance please see [www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)


**RoHS**  
 COMPLIANT  
 HALOGEN  
**FREE**

### APPLICATIONS

- Server and telecom power supplies
- Switch mode power supplies (SMPS)
- Power factor correction power supplies (PFC)
- Lighting
  - High-intensity discharge (HID)
  - Fluorescent ballast lighting
- Industrial
  - Welding
  - Induction heating
  - Motor drives
  - Battery chargers
  - Solar (PV inverters)

### PRODUCT SUMMARY

|   |                 |       |
|---|-----------------|-------|
| $V_{DS}$ (V) at $T_J$ max.              | 650             |       |
| $R_{DS(on)}$ typ. ( $\Omega$ ) at 25 °C | $V_{GS} = 10$ V | 0.086 |
| $Q_g$ max. (nC)                         | 50              |       |
| $Q_{gs}$ (nC)                           | 13              |       |
| $Q_{gd}$ (nC)                           | 10              |       |
| Configuration                           | Single          |       |

### ORDERING INFORMATION

|                                 |                          |
|---------------------------------|--------------------------|
| Package                         | Thin-Lead TO-220 FULLPAK |
| Lead (Pb)-free and halogen-free | SiHA100N60E-GE3          |

### ABSOLUTE MAXIMUM RATINGS ( $T_C = 25$ °C, unless otherwise noted)


| PARAMETER   | SYMBOL           | LIMIT          | UNIT |
|---|------------------|----------------|------|
| Drain-source voltage                                      | $V_{DS}$         | 600            | V    |
| Gate-source voltage                                       | $V_{GS}$         | $\pm 30$       |      |
| Continuous drain current ( $T_J = 150$ °C) <sup>e</sup>   | $V_{GS}$ at 10 V | $T_C = 25$ °C  | A    |
|   |                  | $T_C = 100$ °C |      |
| Pulsed drain current <sup>a</sup>                         | $I_{DM}$         | 73             |      |
| Linear derating factor                                    |                  | 0.28           | W/°C |
| Single pulse avalanche energy <sup>b</sup>                | $E_{AS}$         | 226            | mJ   |
| Maximum power dissipation                                 | $P_D$            | 35             | W    |
| Operating junction and storage temperature range          | $T_J, T_{stg}$   | -55 to +150    | °C   |
| Drain-source voltage slope                                | dv/dt            | $T_J = 125$ °C | V/ns |
| Reverse diode dv/dt <sup>d</sup>                          |                  |                |      |
| Soldering recommendations (peak temperature) <sup>c</sup> | For 10 s         | 260            | °C   |
| Mounting torque, M3 screw                                 |                  | 0.6            | Nm   |

#### Notes

- Repetitive rating; pulse width limited by maximum junction temperature
- $V_{DD} = 120$  V, starting  $T_J = 25$  °C,  $L = 28.2$  mH,  $R_g = 25$   $\Omega$ ,  $I_{AS} = 4.0$  A
- 1.6 mm from case
- $I_{SD} \leq I_D$ ,  $di/dt = 100$  A/ $\mu$ s, starting  $T_J = 25$  °C
- Limited by maximum junction temperature



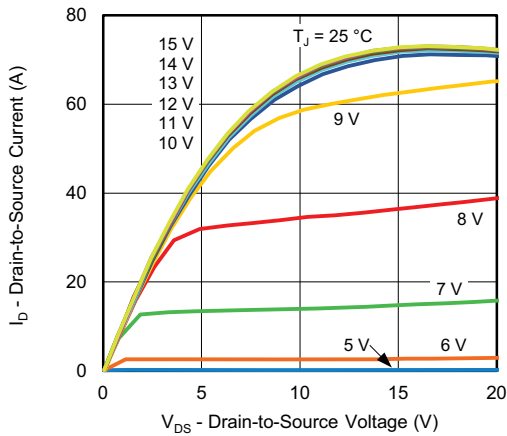
| THERMAL RESISTANCE RATINGS       |                   |      |      |      |
|----------------------------------|-------------------|------|------|------|
| PARAMETER                        | SYMBOL            | TYP. | MAX. | UNIT |
| Maximum junction-to-ambient      | R <sub>thJA</sub> | -    | 65   | °C/W |
| Maximum junction-to-case (drain) | R <sub>thJC</sub> | -    | 3.6  |      |

| SPECIFICATIONS (T <sub>J</sub> = 25 °C, unless otherwise noted) |                                  |   |  |      |       |       |      |
|---|----------------------------------|---|--|------|-------|-------|------|
| PARAMETER   | SYMBOL                           | TEST CONDITIONS   |  | MIN. | TYP.  | MAX.  | UNIT |
| <b>Static</b>   |                                  |   |  |      |       |       |      |
| Drain-source breakdown voltage                                  | V <sub>DS</sub>                  | V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250 μA  |  | 600  | -     | -     | V    |
| V <sub>DS</sub> temperature coefficient                         | ΔV <sub>DS</sub> /T <sub>J</sub> | Reference to 25 °C, I <sub>D</sub> = 1 mA   |  | -    | 0.73  | -     | V/°C |
| Gate-source threshold voltage (N)                               | V <sub>GS(th)</sub>              | V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA   |  | 3.0  | -     | 5.0   | V    |
| Gate-source leakage   | I <sub>GSS</sub>                 | V <sub>GS</sub> = ± 20 V  |  | -    | -     | ± 100 | nA   |
|   |                                  | V <sub>GS</sub> = ± 30 V  |  | -    | -     | ± 1   | μA   |
| Zero gate voltage drain current                                 | I <sub>DSS</sub>                 | V <sub>DS</sub> = 600 V, V <sub>GS</sub> = 0 V  |  | -    | -     | 1     | μA   |
|   |                                  | V <sub>DS</sub> = 480 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 125 °C   |  | -    | -     | 10    |      |
| Drain-source on-state resistance                                | R <sub>DS(on)</sub>              | V <sub>GS</sub> = 10 V  | I <sub>D</sub> = 13 A                          | -    | 0.086 | 0.1   | Ω    |
| Forward transconductance <sup>a</sup>                           | g <sub>fs</sub>                  | V <sub>DS</sub> = 8 V, I <sub>D</sub> = 13 A  |  | -    | 11    | -     | S    |
| <b>Dynamic</b>  |                                  |   |  |      |       |       |      |
| Input capacitance   | C <sub>iSS</sub>                 | V <sub>GS</sub> = 0 V,<br>V <sub>DS</sub> = 100 V,<br>f = 1 MHz   |  | -    | 1851  | -     | pF   |
| Output capacitance  | C <sub>oss</sub>                 |   |  | -    | 84    | -     |      |
| Reverse transfer capacitance                                    | C <sub>rSS</sub>                 |   |  | -    | 5     | -     |      |
| Effective output capacitance, energy related <sup>a</sup>       | C <sub>o(er)</sub>               |   |  | -    | 64    | -     |      |
| Effective output capacitance, time related <sup>b</sup>         | C <sub>o(tr)</sub>               | V <sub>DS</sub> = 0 V to 480 V, V <sub>GS</sub> = 0 V   |  | -    | 407   | -     |      |
| Total gate charge   | Q <sub>g</sub>                   | V <sub>GS</sub> = 10 V  | I <sub>D</sub> = 13 A, V <sub>DS</sub> = 480 V | -    | 33    | 50    | nC   |
| Gate-source charge  | Q <sub>gs</sub>                  |   |  | -    | 13    | -     |      |
| Gate-drain charge   | Q <sub>gd</sub>                  |   |  | -    | 10    | -     |      |
| Turn-on delay time  | t <sub>d(on)</sub>               | V <sub>DD</sub> = 480 V, I <sub>D</sub> = 13 A,<br>V <sub>GS</sub> = 10 V, R <sub>g</sub> = 9.1 Ω   |  | -    | 21    | 42    | ns   |
| Rise time   | t <sub>r</sub>                   |   |  | -    | 34    | 68    |      |
| Turn-off delay time   | t <sub>d(off)</sub>              |   |  | -    | 33    | 66    |      |
| Fall time   | t <sub>f</sub>                   |   |  | -    | 20    | 40    |      |
| Gate input resistance   | R <sub>g</sub>                   | f = 1 MHz, open drain   |  | 0.3  | 0.7   | 1.4   | Ω    |
| <b>Drain-Source Body Diode Characteristics</b>                  |                                  |   |  |      |       |       |      |
| Continuous source-drain diode current                           | I <sub>S</sub>                   | MOSFET symbol showing the integral reverse p - n junction diode  |  | -    | -     | 30    | A    |
| Pulsed diode forward current                                    | I <sub>SM</sub>                  |   |  | -    | -     | 73    |      |
| Diode forward voltage   | V <sub>SD</sub>                  | T <sub>J</sub> = 25 °C, I <sub>S</sub> = 13 A, V <sub>GS</sub> = 0 V  |  | -    | -     | 1.2   | V    |
| Reverse recovery time   | t <sub>rr</sub>                  | T <sub>J</sub> = 25 °C, I <sub>F</sub> = I <sub>S</sub> = 13 A,<br>di/dt = 100 A/μs, V <sub>R</sub> = 25 V  |  | -    | 358   | 716   | ns   |
| Reverse recovery charge   | Q <sub>rr</sub>                  |   |  | -    | 5.1   | 10.2  | μC   |
| Reverse recovery current  | I <sub>RRM</sub>                 |   |  | -    | 24    | -     | A    |

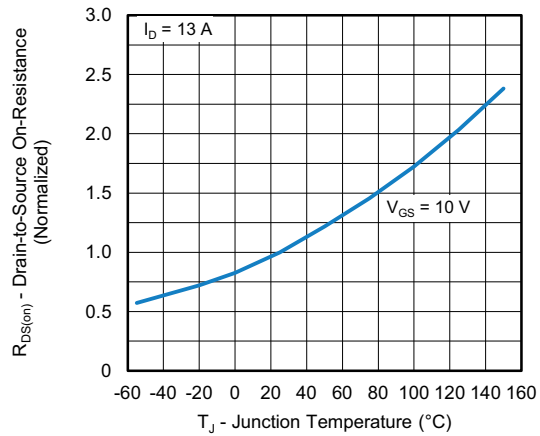
**Notes**

- f. C<sub>oss(er)</sub> is a fixed capacitance that gives the same energy as C<sub>oss</sub> while V<sub>DS</sub> is rising from 0 % to 80 % V<sub>DSS</sub>
- g. C<sub>oss(tr)</sub> is a fixed capacitance that gives the same charging time as C<sub>oss</sub> while V<sub>DS</sub> is rising from 0 % to 80 % V<sub>DSS</sub>

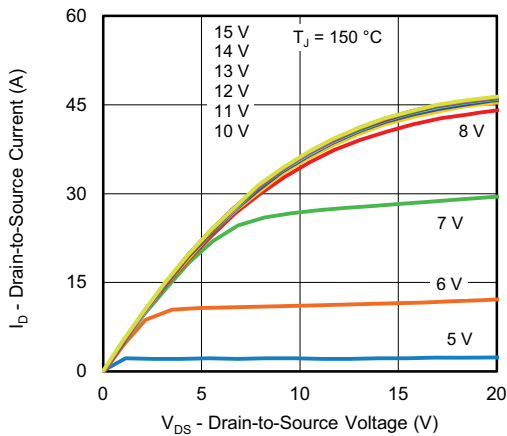
**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



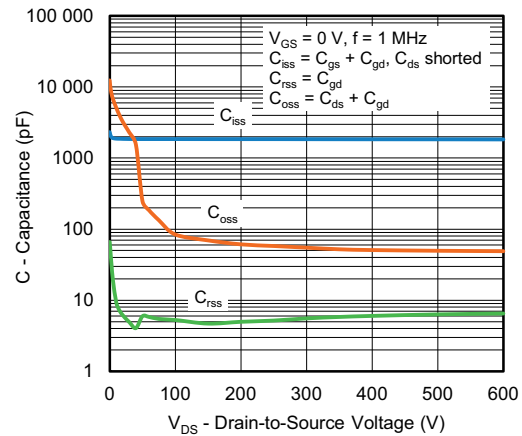
**Fig. 1 - Typical Output Characteristics**



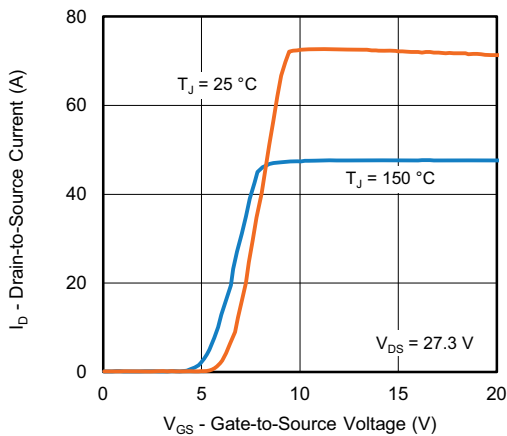
**Fig. 4 - Normalized On-Resistance vs. Temperature**



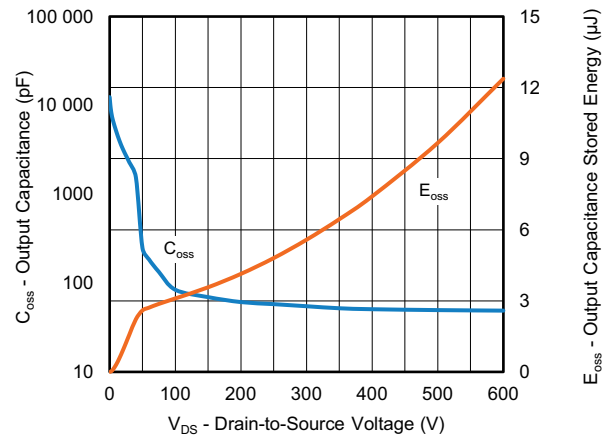
**Fig. 2 - Typical Output Characteristics**



**Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage**



**Fig. 3 - Typical Transfer Characteristics**



**Fig. 6 - C<sub>oss</sub> and E<sub>oss</sub> vs. V<sub>DS</sub>**

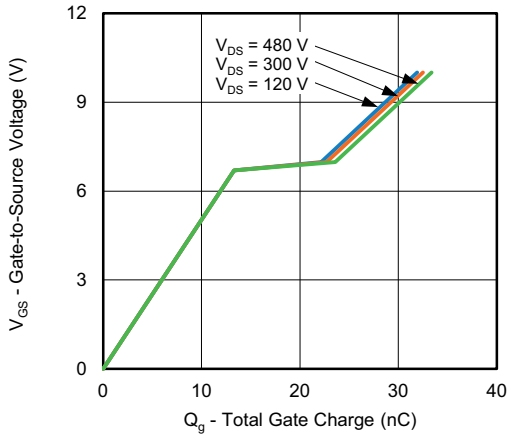


Fig. 7 - Typical Gate Charge vs. Gate-to-Source Voltage

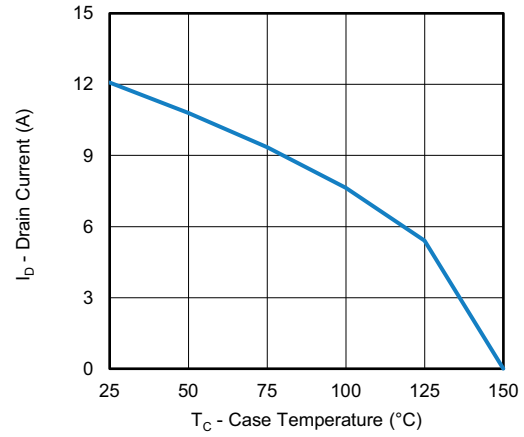


Fig. 10 - Maximum Drain Current vs. Case Temperature

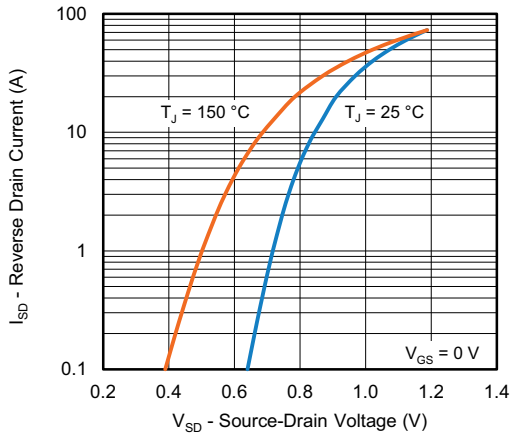


Fig. 8 - Typical Source-Drain Diode Forward Voltage

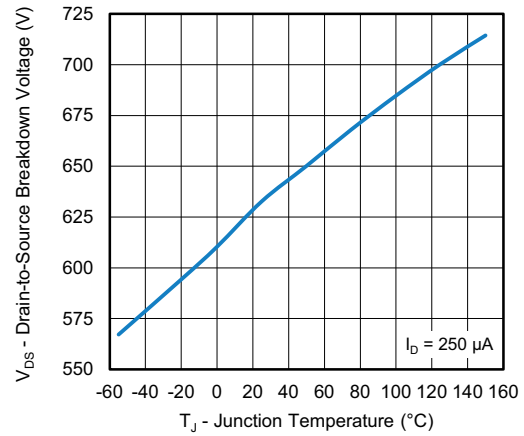


Fig. 11 - Temperature vs. Drain-to-Source Voltage

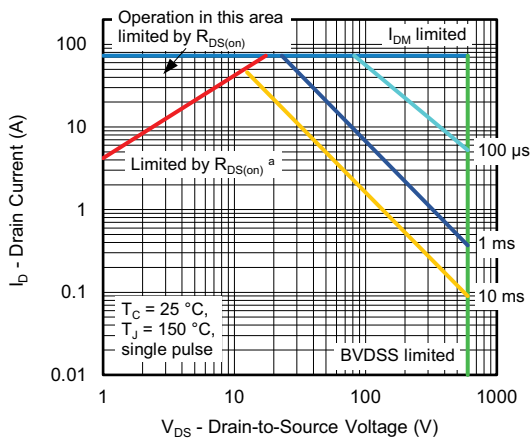


Fig. 9 - Maximum Safe Operating Area

**Note**

h.  $V_{GS} >$  minimum  $V_{GS}$  at which  $R_{DS(on)}$  is specified

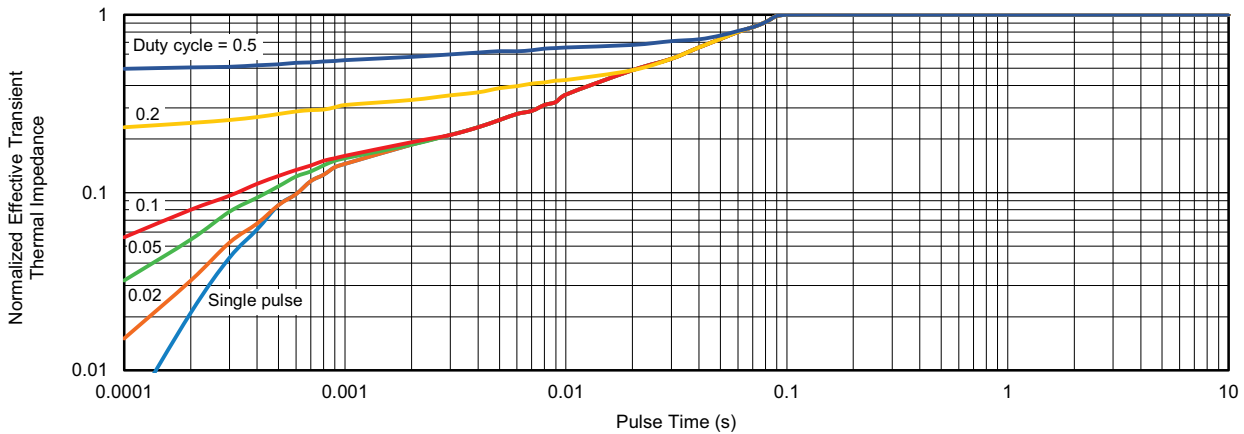


Fig. 12 - Normalized Transient Thermal Impedance, Junction-to-Case

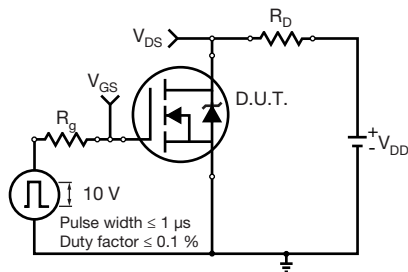


Fig. 13 - Switching Time Test Circuit

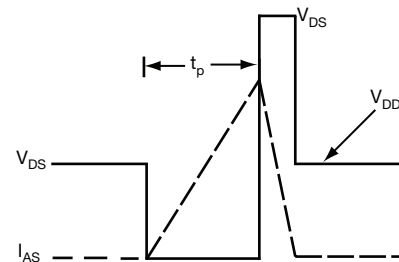


Fig. 16 - Unclamped Inductive Waveforms

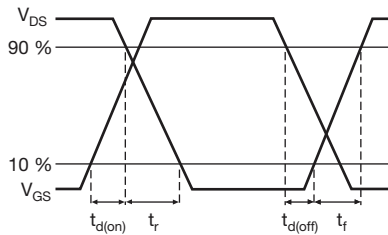


Fig. 14 - Switching Time Waveforms

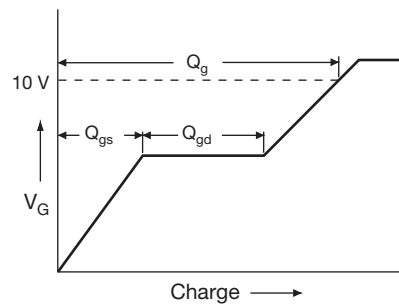


Fig. 17 - Basic Gate Charge Waveform

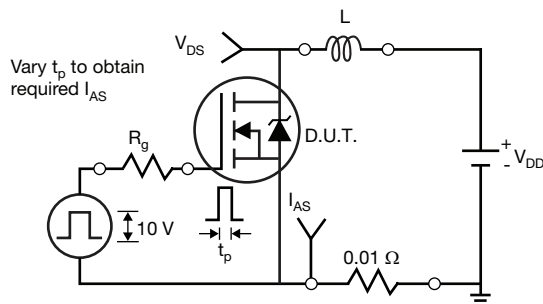


Fig. 15 - Unclamped Inductive Test Circuit

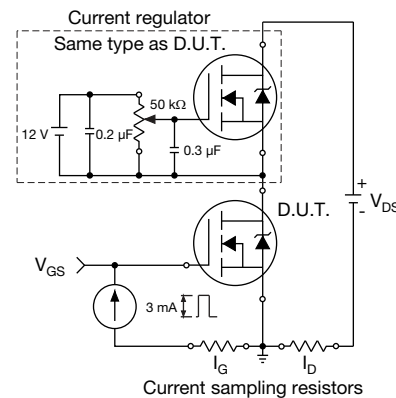
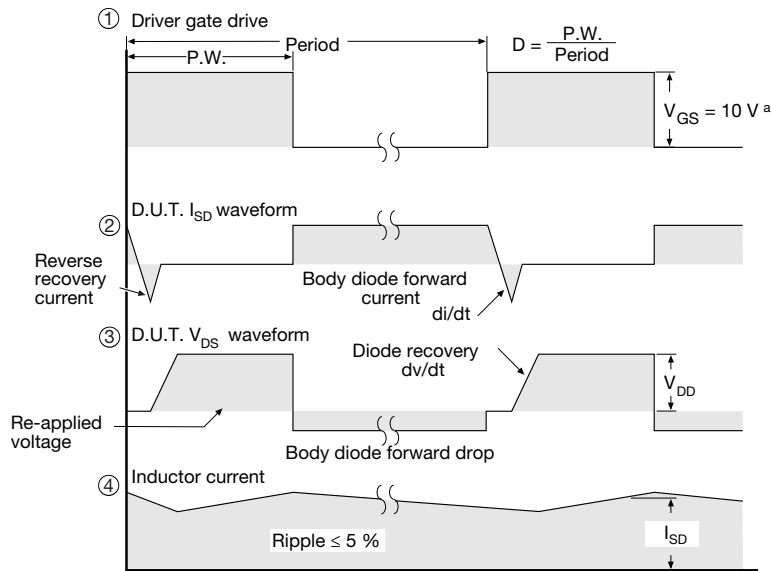
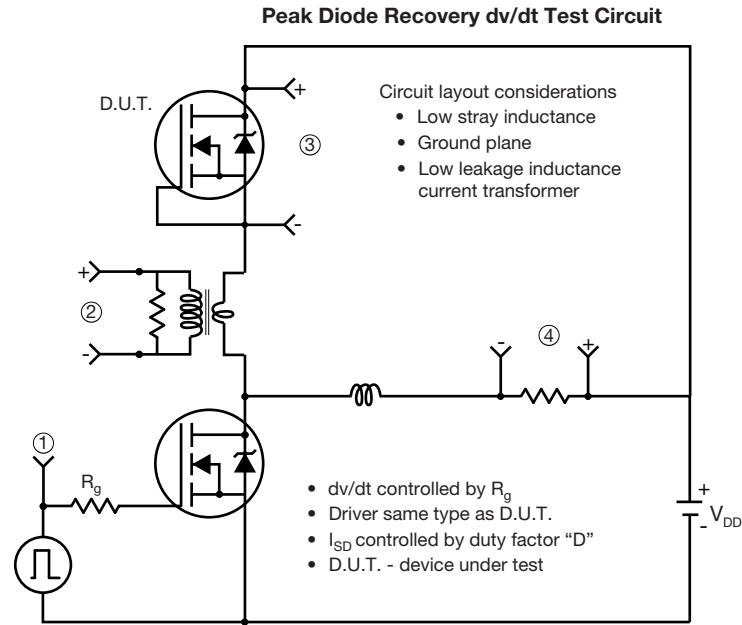


Fig. 18 - Gate Charge Test Circuit



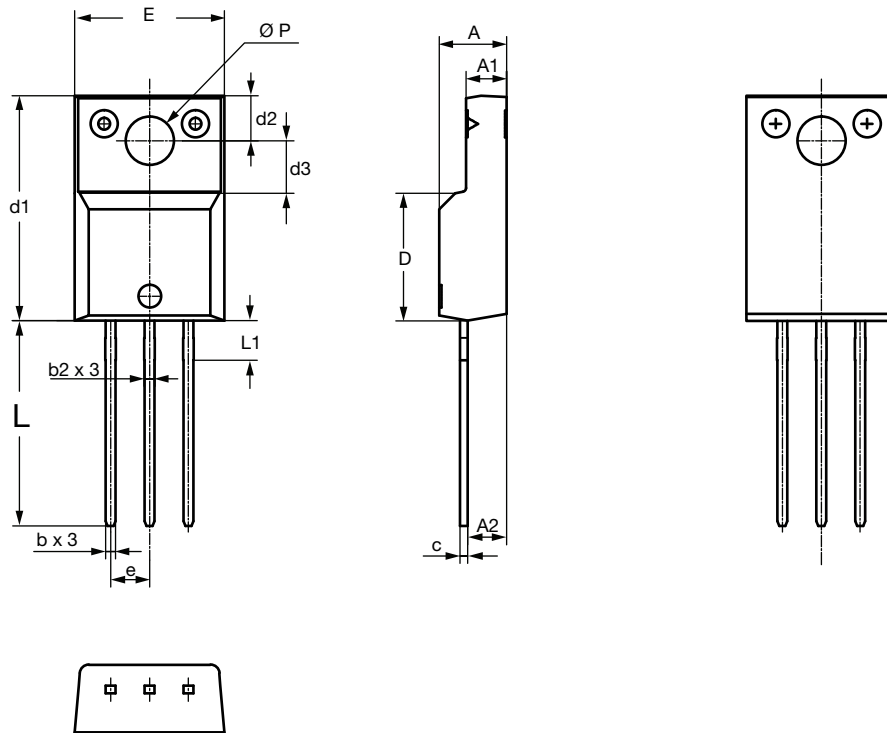
**Note**  
 a.  $V_{GS} = 5 V$  for logic level devices

**Fig. 19 - For N-Channel**

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### TO-220 FULLPAK Thin Lead



| SYMBOL          | DIMENSIONS  |       |        |       |
|-----------------|-------------|-------|--------|-------|
|                 | MILLIMETERS |       | INCHES |       |
|                 | MIN.        | MAX.  | MIN.   | MAX.  |
| A               | 4.30        | 4.70  | 0.169  | 0.185 |
| A1              | 2.50        | 2.90  | 0.098  | 0.114 |
| A2              | 2.40        | 2.80  | 0.094  | 0.110 |
| b               | 0.60        | 0.80  | 0.024  | 0.031 |
| b2              | 0.60        | 0.90  | 0.024  | 0.035 |
| c               | -           | 0.60  | -      | 0.024 |
| D               | 8.30        | 8.70  | 0.327  | 0.342 |
| d1              | 14.70       | 15.30 | 0.579  | 0.602 |
| d2              | 2.90        | 3.10  | 0.114  | 0.122 |
| d3              | 3.30        | 3.70  | 0.130  | 0.146 |
| E               | 9.70        | 10.30 | 0.382  | 0.406 |
| e               | 2.50        | 2.70  | 0.098  | 0.106 |
| L               | 13.40       | 13.80 | 0.528  | 0.543 |
| L1              | 1.00        | 2.80  | 0.039  | 0.110 |
| $\varnothing P$ | 3.00        | 3.40  | 0.118  | 0.134 |

ECN: E20-0684-Rev. D, 28-Dec-2020  
DWG: 6021



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