Si8650/51/52/55 数据表

低功耗五信道数字隔离器

Silicon Labs 的超低功耗数字隔离器系列属于 CMOS 设备，与传统的隔离技术相比，在数据速率、传送延时、功率、尺寸、可靠性和外部 BOM 等方面具有显著优势。这些产品的运行参数能在宽广的温度范围和整个设备使用寿命期间保持稳定，实现轻松设计和高度一致的性能。所有设备版本都具有施密特触发器输入，噪声抗扰度高，且仅需 VDD 旁路电容器。

支持高达 150 Mbps 的数据速率，且所有设备都可实现低于 10 ns 的传送延时。启用输入提供单点控制，可用于启用和禁用输出驱动。订购选项包括可选择的隔离额定值（1.0 kV、2.5 kV、3.75 kV 和 5 kV）和可选择的故障保护工作模式，以控制功率损耗期间的默认输出状态。所有 >1 kV_{RMS} 的产品都符合 UL、CSA、VDE 和 CQC 认证，宽体封装的产品支持最高 5 kV_{RMS} 的强化绝缘。

应用

- 工业自动化系统
- 医疗电子设备
- 混合动力汽车
- 隔离的开关模式电源
- 隔离的 ADC、DAC
- 电机控制
- 电源逆变器
- 通信系统

安全法规认证

- UL 1577 认证
  - 1 分钟内最大 5000 V_{RMS}
- CSA component notice 5A 认证
  - IEC 60950-1、62368-1、60601-1（强化绝缘）
- VDE 认证合规
  - VDE 0884-10
  - EN60950-1（强化绝缘）
- CQC 认证
  - GB4943.1

主要特点

- 高速运行
  - 直流至 150 Mbps
- 不需要启动初始化
- 宽广的工作电压范围
  - 2.5 – 5.5 V
- 高达 5000 V_{RMS} 的隔离
- 60 年的使用寿命（额定工作电压下）
- 高电磁抗扰度
- 超低功耗（典型）
  - 5 V 运行
    - 1 Mbps 时每信道 1.6 mA
    - 100 Mbps 时每信道 5.5 mA
  - 2.5 V 运行
    - 1 Mbps 时每信道 1.5 mA
    - 100 Mbps 时每信道 3.5 mA
- 带有 ENABLE 的三态输出
- 施密特触发器输入
- 可选故障保护模式
  - 默认高或低输出（订购选项）
- 精确定时（典型）
  - 10 ns 传送延时
  - 1.5 ns 脉冲宽度失真
  - 0.5 ns 信道-信道偏移
  - 2 ns 传送延时偏移
  - 5 ns 最小脉冲宽度
- 瞬态抗扰度 50 kV/µs
- AEC-Q100 认证
- 宽广的工作温度范围：
  - – 40 至 125 ° C
- 符合 RoHS 的封装
  - SOIC-16 宽体
  - SOIC-16 窄体
  - QSOP-16

1. Ordering Guide

Table 1.1. Ordering Guide for Valid OPNs[1, 2, 3]

Ordering Part Number (OPN)	Number of Inputs VDD1 Side	Number of Inputs VDD2 Side	Max Data Rate (Mbps)	Default Output State	Isolation rating (kV)	Temp (°C)	Package
QSOP-16 Packages							
Si8650BB-B-IU	5	0	150	Low	2.5	–40 to 125 °C	QSOP-16
Si8650EB-B-IU	5	0	150	High	2.5	–40 to 125 °C	QSOP-16
Si8651BB-B-IU	4	1	150	Low	2.5	–40 to 125 °C	QSOP-16
Si8651EB-B-IU	4	1	150	High	2.5	-40 to 125˚C	QSOP-16
Si8652BB-B-IU	3	2	150	Low	2.5	-40 to 125˚C	QSOP-16
Si8652EB-B-IU	3	2	150	High	2.5	-40 to 125˚C	QSOP-16
Si8655BA-B-IU	5	0	150	Low	1.0	–40 to 125 °C	QSOP-16
Si8655BA-C-IU	5	0	150	Low	1.0	–40 to 125 °C	QSOP-16
SOIC-16 Packages							
Si8650BB-B-IS1	5	0	150	Low	2.5	–40 to 125 °C	NB SOIC-16
Si8650BD-B-IS	5	0	150	Low	5.0	–40 to 125 °C	WB SOIC-16
Si8650EC-B-IS1	5	0	150	High	3.75	–40 to 125 °C	NB SOIC-16
Si8650ED-B-IS	5	0	150	High	5.0	–40 to 125 °C	WB SOIC-16
Si8651BB-B-IS1	4	1	150	Low	2.5	–40 to 125 °C	NB SOIC-16
Si8651BC-B-IS1	4	1	150	Low	3.75	–40 to 125 °C	NB SOIC-16
Si8651BD-B-IS	4	1	150	Low	5.0	–40 to 125 °C	WB SOIC-16
Si8651EC-B-IS1	4	1	150	High	3.75	–40 to 125 °C	NB SOIC-16
Si8651ED-B-IS	4	1	150	High	5.0	–40 to 125 °C	WB SOIC-16
Si8652BB-B-IS1	3	2	150	Low	2.5	–40 to 125 °C	NB SOIC-16
Si8652BC-B-IS1	3	2	150	Low	3.75	–40 to 125 °C	NB SOIC-16
Si8652BD-B-IS	3	2	150	Low	5.0	–40 to 125 °C	WB SOIC-16
Si8652EC-B-IS1	3	2	150	High	3.75	–40 to 125 °C	NB SOIC-16
Si8652ED-B-IS	3	2	150	High	5.0	–40 to 125 °C	WB SOIC-16
Si8655BA-B-IS	5	0	150	Low	1.0	–40 to 125 °C	WB SOIC-16
Si8655BB-B-IS1	5	0	150	Low	2.5	–40 to 125 °C	NB SOIC-16
Si8655BD-B-IS	5	0	150	Low	5.0	–40 to 125 °C	WB SOIC-16

Notes:

1. All packages are RoHS-compliant with peak reflow temperatures of 260 °C according to the JEDEC industry standard classifications and peak solder temperatures.
2. “Si” and “SI” are used interchangeably.
3. An "R" at the end of the part number denotes tape and reel packaging option.

Table of Contents

2. Functional Description

2.1 Theory of Operation

The operation of an Si865x channel is analogous to that of an opto coupler, except an RF carrier is modulated instead of light. This simple architecture provides a robust isolated data path and requires no special considerations or initialization at start-up. A simplified block diagram for a single Si865x channel is shown in the figure below.

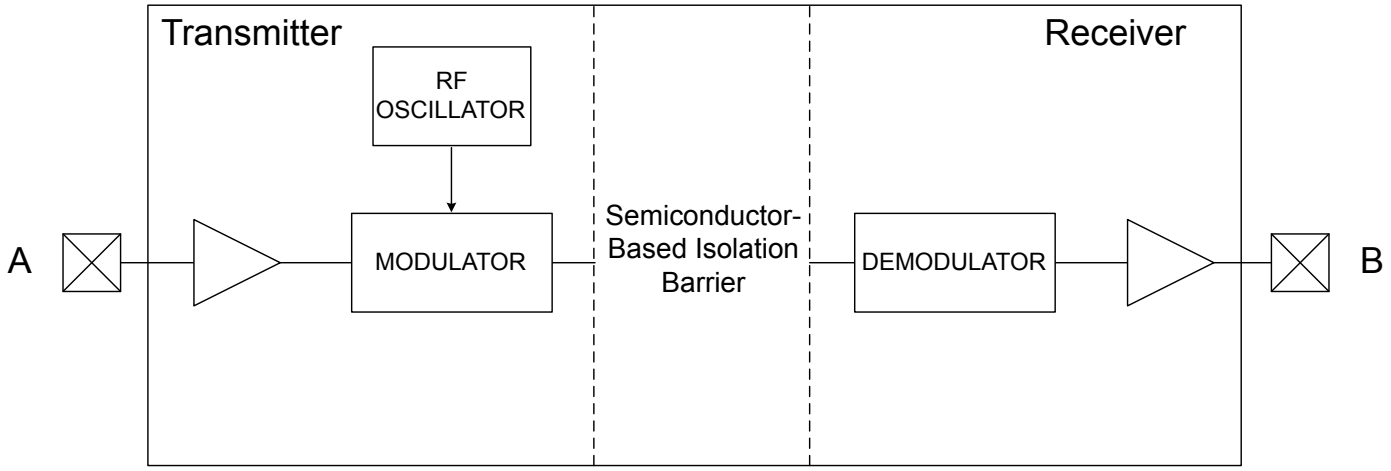


Figure 2.1. Simplified Channel Diagram

A channel consists of an RF Transmitter and RF Receiver separated by a semiconductor-based isolation barrier. Referring to the Transmitter, input A modulates the carrier provided by an RF oscillator using on/off keying. The Receiver contains a demodulator that decodes the input state according to its RF energy content and applies the result to output B via the output driver. This RF on/off keying scheme is superior to pulse code schemes as it provides best-in-class noise immunity, low power consumption, and better immunity to magnetic fields. See the figure below for more details.

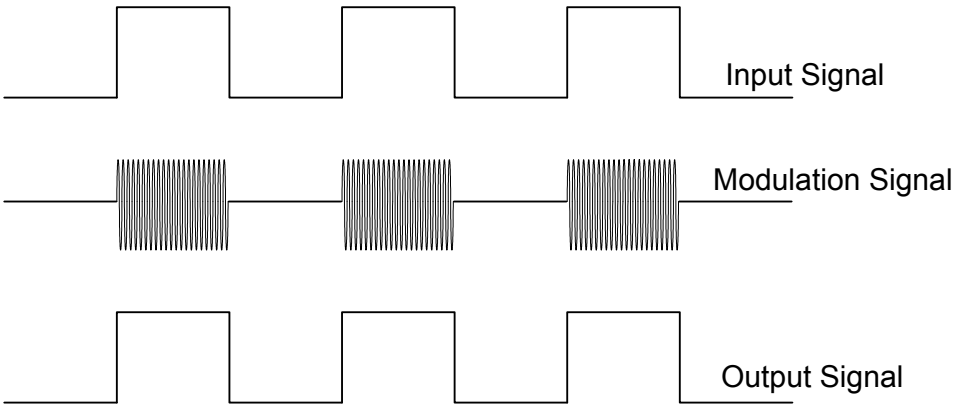


Figure 2.2. Modulation Scheme

2.2 Eye Diagram

The figure below illustrates an eye-diagram taken on an Si8650. For the data source, the test used an Anritsu (MP1763C) Pulse Pattern Generator set to 1000 ns/div. The output of the generator's clock and data from an Si8650 were captured on an oscilloscope. The results illustrate that data integrity was maintained even at the high data rate of 150 Mbps. The results also show that 2 ns pulse width distortion and 350 ps peak jitter were exhibited.

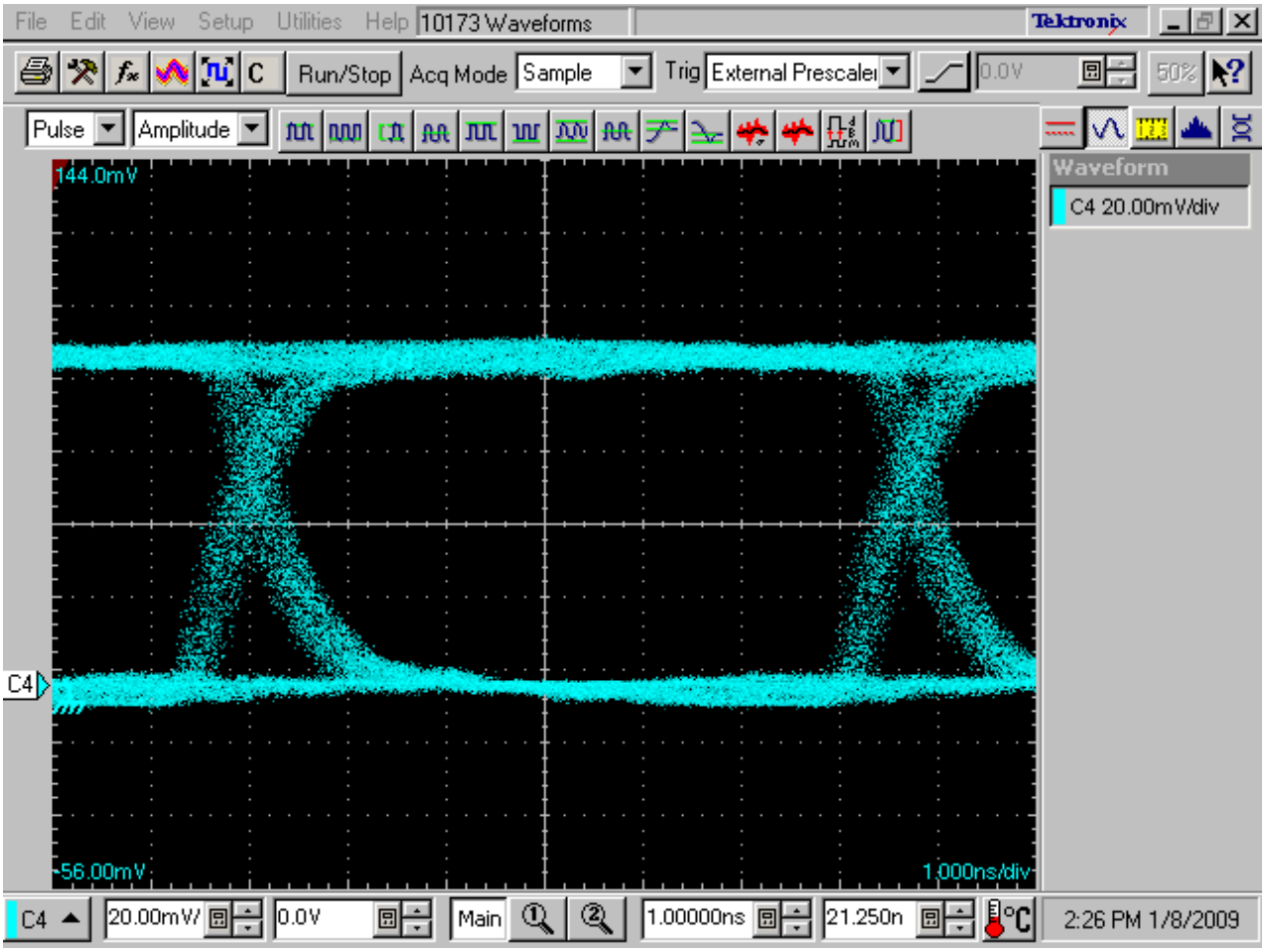


Figure 2.3. Eye Diagram

3. Device Operation

Device behavior during start-up, normal operation, and shutdown is shown in Figure 3.1 Device Behavior during Normal Operation on page 8, where UVLO+ and UVLO- are the positive-going and negative-going thresholds respectively. Refer to the table below to determine outputs when power supply (VDD) is not present. Additionally, refer to the table on the following page for logic conditions when enable pins are used.

Table 3.1. Si865x Logic Operation

V_I Input [1,2]	EN Input [1,2,3,4]	VDDI State [1,5,6]	VDDO State [1,5,6]	V_O Output [1,2]	Comments
H	H or NC	P	P	H	Enabled, normal operation.
L	H or NC	P	P	L	
X [7]	L	P	P	Hi-Z [8]	Disabled.
X [7]	H or NC	UP	P	L [9] H [9]	Upon transition of VDDI from unpowered to powered, V_O returns to the same state as V_I in less than 1 µs.
X [7]	L	UP	P	Hi-Z [8]	Disabled.
X [7]	X [7]	P	UP	Undetermined	Upon transition of VDDO from unpowered to powered, V_O returns to the same state as V_I within 1 µs, if EN is in either the H or NC state. Upon transition of VDDO from unpowered to powered, V_O returns to Hi-Z within 1 µs if EN is L.

Notes:

1. VDDI and VDDO are the input and output power supplies. V_I and V_O are the respective input and output terminals. EN is the enable control input located on the same output side.
2. X = not applicable; H = Logic High; L = Logic Low; Hi-Z = High Impedance.
3. It is recommended that the enable inputs be connected to an external logic high or low level when the Si865x is operating in noisy environments.
4. No Connect (NC) replaces EN1 on Si8650. No Connects are not internally connected and can be left floating, tied to VDD, or tied to GND.
5. “Powered” state (P) is defined as 2.5 V < VDD < 5.5 V.
6. “Unpowered” state (UP) is defined as VDD = 0 V.
7. Note that an I/O can power the die for a given side through an internal diode if its source has adequate current.
8. When using the enable pin (EN) function, the output pin state is driven into a high-impedance state when the EN pin is disabled (EN = 0).
9. See 1. Ordering Guide for details. This is the selectable fail-safe operating mode (ordering option). Some devices have default output state = H, and some have default output state = L, depending on the ordering part number (OPN). For default high devices, the data channels have pull-ups on inputs/outputs. For default low devices, the data channels have pull-downs on inputs/outputs.

Table 3.2. Enable Input Truth [1]

P/N	EN1 [1,2]	EN2 [1,2]	Operation
Si8650	—	H	Outputs B1, B2, B3, B4, B5 are enabled and follow input state.
	—	L	Outputs B1, B2, B3, B4, B5 are disabled and Logic Low or in high impedance state. [3]
Si8651	H	X	Output A5 enabled and follow input state.
	L	X	Output A5 disabled and in high impedance state. [3]
	X	H	Outputs B1, B2, B3, B4 are enabled and follow input state.
	X	L	Outputs B1, B2, B3, B4 are disabled and in high impedance state. [3]
Si8652	H	X	Outputs A4 and A5 are enabled and follow input state.
	L	X	Outputs A4 and A5 are disabled and in high impedance state. [3]
	X	H	Outputs B1, B2, B3 are enabled and follow input state.
	X	L	Outputs B1, B2, B3 are disabled and in high impedance state. [3]
Si8655	—	—	Outputs B1, B2, B3, B4, B5 are enabled and follow input state.

Notes:

1. Enable inputs EN1 and EN2 can be used for multiplexing, for clock sync, or other output control. These inputs are internally pulled-up to local VDD by a 2 µA current source allowing them to be connected to an external logic level (high or low) or left floating. To minimize noise coupling, do not connect circuit traces to EN1 or EN2 if they are left floating. If EN1, EN2 are unused, it is recommended they be connected to an external logic level, especially if the Si865x is operating in a noisy environment.
2. X = not applicable; H = Logic High; L = Logic Low.
3. When using the enable pin (EN) function, the output pin state is driven into a high-impedance state when the EN pin is disabled (EN = 0).

3.1 Device Startup

Outputs are held low during powerup until VDD is above the UVLO threshold for time period tSTART. Following this, the outputs follow the states of inputs.

3.2 Undervoltage Lockout

Undervoltage Lockout (UVLO) is provided to prevent erroneous operation during device startup and shutdown or when VDD is below its specified operating circuits range. Both Side A and Side B each have their own undervoltage lockout monitors. Each side can enter or exit UVLO independently. For example, Side A unconditionally enters UVLO when V_{DD1} falls below $V_{DD1(UVLO-)}$ and exits UVLO when V_{DD1} rises above $V_{DD1(UVLO+)}$. Side B operates the same as Side A with respect to its V_{DD2} supply.

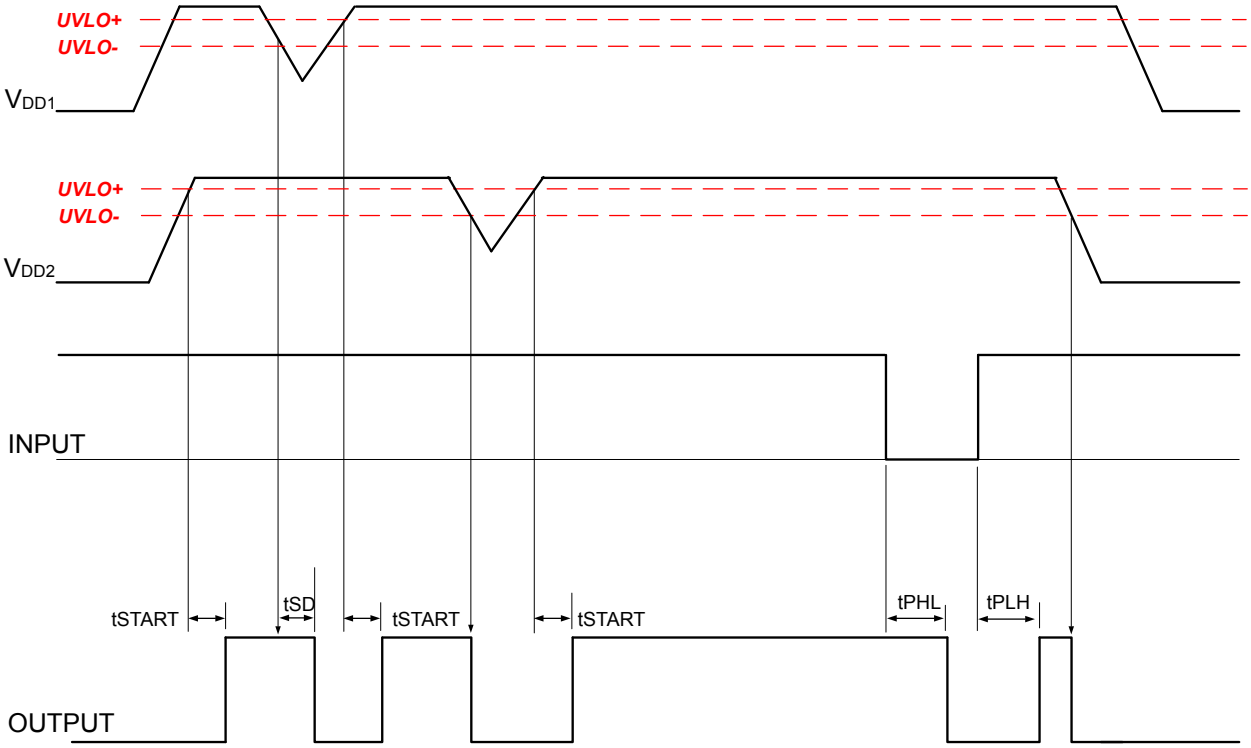


Figure 3.1. Device Behavior during Normal Operation

3.3 Layout Recommendations

To ensure safety in the end user application, high voltage circuits (i.e., circuits with >30 V_{AC}) must be physically separated from the safety extra-low voltage circuits (SELV is a circuit with <30 V_{AC}) by a certain distance (creepage/clearance). If a component, such as a digital isolator, straddles this isolation barrier, it must meet those creepage/clearance requirements and also provide a sufficiently large high-voltage breakdown protection rating (commonly referred to as working voltage protection). Table 4.5 Regulatory Information [1] on page 21 and 4. Electrical Specifications detail the working voltage and creepage/clearance capabilities of the Si86xx. These tables also detail the component standards (UL1577, IEC60747, CSA 5A), which are readily accepted by certification bodies to provide proof for end-system specifications requirements. Refer to the end-system specification (61010-1, 60950-1, 60601-1, etc.) requirements before starting any design that uses a digital isolator.

3.3.1 Supply Bypass

The Si865x family requires a 0.1 µF bypass capacitor between V_{DD1} and GND1 and V_{DD2} and GND2. The capacitor should be placed as close as possible to the package. To enhance the robustness of a design, the user may also include resistors (50–300 Ω) in series with the inputs and outputs if the system is excessively noisy.

3.3.2 Output Pin Termination

The nominal output impedance of an isolator driver channel is approximately 50 Ω, ±40%, which is a combination of the value of the on-chip series termination resistor and channel resistance of the output driver FET. When driving loads where transmission line effects will be a factor, output pins should be appropriately terminated with controlled impedance PCB traces.

3.4 Fail-Safe Operating Mode

Si86xx devices feature a selectable (by ordering option) mode whereby the default output state (when the input supply is unpowered) can either be a logic high or logic low when the output supply is powered. See Table 3.1 Si865x Logic Operation on page 6 and 1. Ordering Guide for more information.

3.5 Typical Performance Characteristics

The typical performance characteristics depicted in the following diagrams are for information purposes only. Refer to Table 4.2 Electrical Characteristics on page 11 through Table 4.4 Electrical Characteristics on page 18 for actual specification limits.

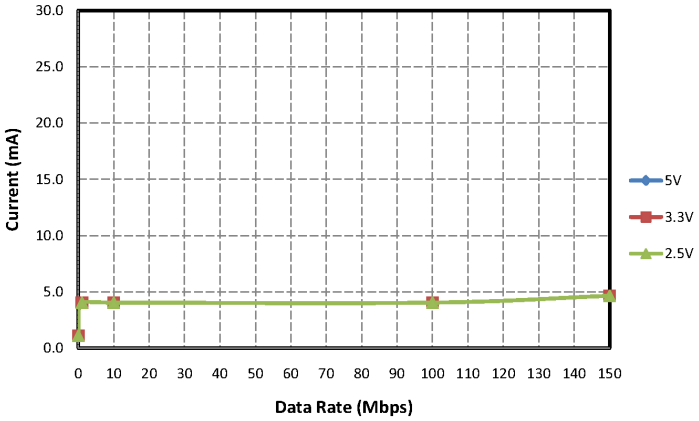


Figure 3.2. Si8650/55 Typical V_{DD1} Supply Current vs. Data Rate 5, 3.3, and 2.5 V Operation

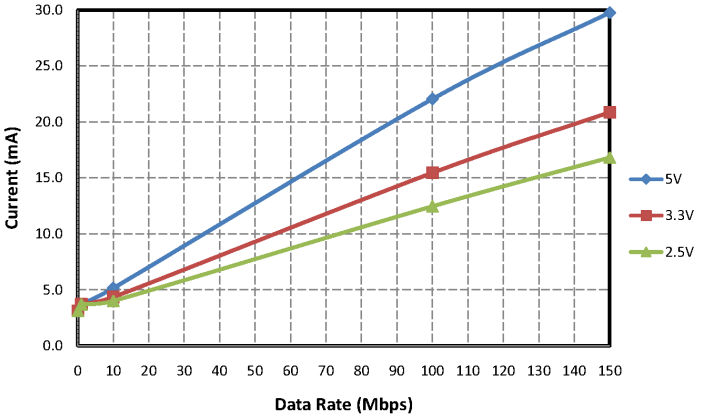


Figure 3.3. Si8650/55 Typical V_{DD2} Supply Current vs. Data Rate 5, 3.3, and 2.5 V Operation (15 pF Load)

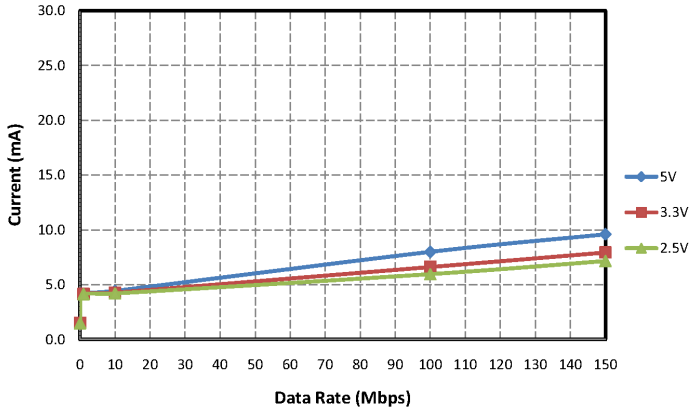


Figure 3.4. Si8651 Typical V_{DD1} Supply Current vs. Data Rate 5, 3.3, and 2.5 V Operation (15 pF Load)

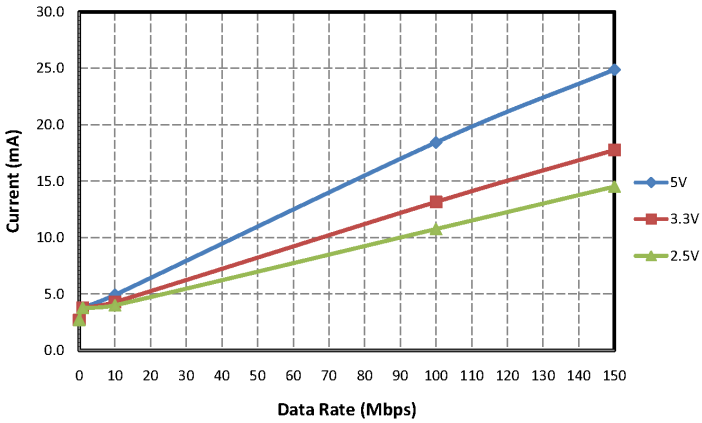


Figure 3.5. Si8651 Typical V_{DD2} Supply Current vs. Data Rate 5, 3.3, and 2.5 V Operation (15 pF Load)

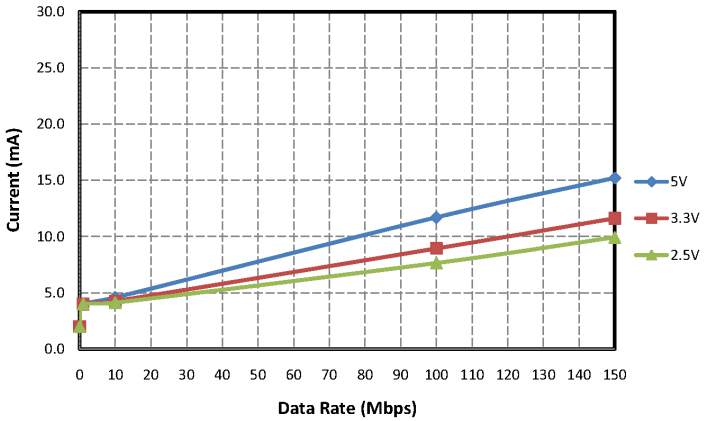


Figure 3.6. Si8652 Typical V_{DD1} Supply Current vs. Data Rate 5, 3.3, and 2.5 V Operation (15 pF Load)

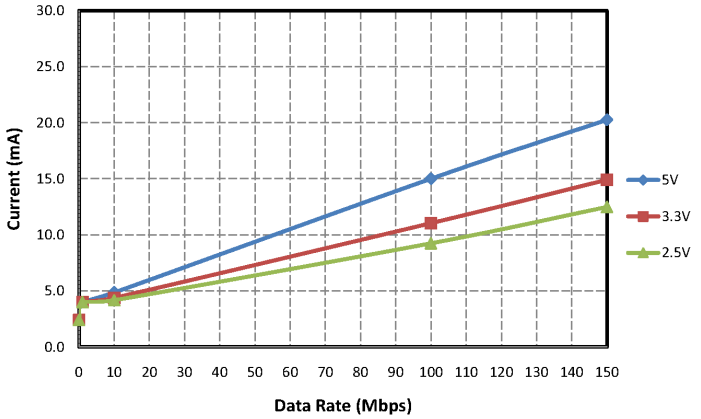


Figure 3.7. Si8652 Typical V_{DD2} Supply Current vs. Data Rate 5, 3.3, and 2.5 V Operation (15 pF Load)

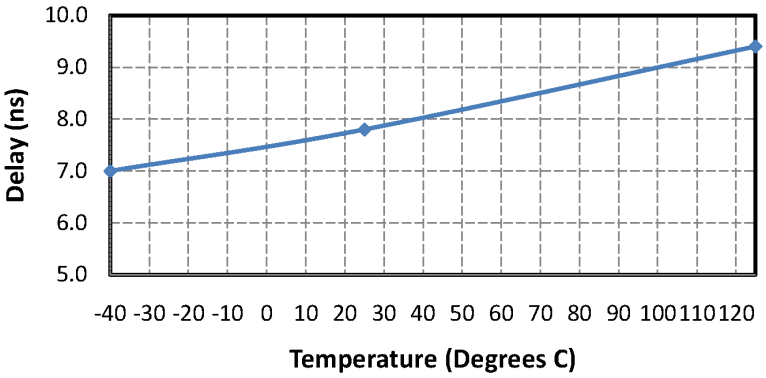


Figure 3.8. Propagation Delay vs. Temperature

4. Electrical Specifications

Table 4.1. Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Junction Operating Temperature	T_J	—	—	150	°C
Ambient Operating Temperature [1]	T_A	–40	25	125	°C
Supply Voltage	V_{DD1}	2.375	—	5.5	V
	V_{DD2}	2.375	—	5.5	V

Note:
1. The maximum ambient temperature is dependent on data frequency, output loading, number of operating channels, and supply voltage.

Table 4.2. Electrical Characteristics

(V_{DD1} = 5 V±10%, V_{DD2} = 5 V±10%, T_A = –40 to 125 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
VDD Undervoltage Threshold	VDDUV+	V_{DD1}, V_{DD2} rising	1.95	2.24	2.375	V
VDD Undervoltage Threshold	VDDUV–	V_{DD1}, V_{DD2} falling	1.88	2.16	2.325	V
VDD Undervoltage Hysteresis	VDD_{HYS}		50	70	95	mV
Positive-Going Input Threshold	VT+	All inputs rising	1.4	1.67	1.9	V
Negative-Going Input Threshold	VT–	All inputs falling	1.0	1.23	1.4	V
Input Hysteresis	V_{HYS}		0.38	0.44	0.50	V
High Level Input Voltage	V_{IH}		2.0	—	—	V
Low Level input voltage	V_{IL}		—	—	0.8	V
High Level Output Voltage	V_{OH}	Ioh = –4 mA	V_{DD1},V_{DD2} – 0.4	4.8	—	V
Low Level Output Voltage	V_{OL}	Iol = 4 mA	—	0.2	0.4	V
Input Leakage Current	I_L		—	—	±10	µA
Output Impedance [1]	Z_O		—	50	—	Ω
Enable Input High Current	I_{ENH}	V_{ENx} = V_{IH}	—	2.0	—	µA
Enable Input Low Current	I_{ENL}	V_{ENx} = V_{IL}	—	2.0	—	µA
DC Supply Current (All Inputs 0 V or at Supply)						
Si8650Bx, Ex, Si8655Bx						

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
V_{DD1}		V_I = 0(Bx), 1(Ex)	—	1.1	1.8	mA
V_{DD2}		V_I = 0(Bx), 1(Ex)	—	3.1	4.7	
V_{DD1}		V_I = 1(Bx), 0(Ex)	—	7.0	9.8	
V_{DD2}		V_I = 1(Bx), 0(Ex)	—	3.3	5.0	
Si8651Bx, Ex						
V_{DD1}		V_I = 0(Bx), 1(Ex)	—	1.5	2.4	mA
V_{DD2}		V_I = 0(Bx), 1(Ex)	—	2.7	4.1	
V_{DD1}		V_I = 1(Bx), 0(Ex)	—	6.6	9.2	
V_{DD2}		V_I = 1(Bx), 0(Ex)	—	4.0	6.0	
Si8652Bx, Ex						
V_{DD1}		V_I = 0(Bx), 1(Ex)	—	2.0	3.0	mA
V_{DD2}		V_I = 0(Bx), 1(Ex)	—	2.4	3.6	
V_{DD1}		V_I = 1(Bx), 0(Ex)	—	5.6	7.8	
V_{DD2}		V_I = 1(Bx), 0(Ex)	—	5.0	7.5	
1 Mbps Supply Current (All Inputs = 500 kHz Square Wave, Cl = 15 pF on All Outputs)						
Si8650Bx, Ex, Si8655Bx						
V_{DD1}			—	4.1	5.7	mA
V_{DD2}			—	3.7	5.2	
Si8651Bx, Ex						
V_{DD1}			—	4.2	5.8	mA
V_{DD2}			—	3.8	5.3	
Si8652Bx, Ex						
V_{DD1}			—	4.0	5.6	mA
V_{DD2}			—	4.0	5.6	
10 Mbps Supply Current (All Inputs = 5 MHz Square Wave, Cl = 15 pF on All Outputs)						
Si8650Bx, Ex, Si8655Bx						
V_{DD1}			—	4.1	5.7	mA
V_{DD2}			—	5.2	7.2	
Si8651Bx, Ex						
V_{DD1}			—	4.4	6.2	mA
V_{DD2}			—	4.9	6.9	
Si8652Bx, Ex						
V_{DD1}			—	4.6	6.4	mA
V_{DD2}			—	4.9	6.8	
100 Mbps Supply Current (All Inputs = 50 MHz Square Wave, Cl = 15 pF on All Outputs)						

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Si8650Bx, Ex, Si8655Bx						
V_{DD1}			—	4.1	5.7	mA
V_{DD2}			—	22.1	28.7	
Si8651Bx, Ex						
V_{DD1}			—	8.0	10.8	mA
V_{DD2}			—	18.4	24	
Si8652Bx, Ex						
V_{DD1}			—	11.7	15.2	mA
V_{DD2}			—	15	19.5	
Timing Characteristics						
Si865xBx, Ex						
Maximum Data Rate			0	—	150	Mbps
Minimum Pulse Width			—	—	5.0	ns
Propagation Delay	t_{PHL}, t_{PLH}	See Figure 4.2 Propagation Delay Timing on page 14	5.0	8.0	13	ns
Pulse Width Distortion $\lvert t_{PLH} - t_{PHL} \rvert$	PWD	See Figure 4.2 Propagation Delay Timing on page 14	—	0.2	4.5	ns
Propagation Delay Skew [2]	$t_{PSK(P-P)}$		—	2.0	4.5	ns
Channel-Channel Skew	t_{PSK}		—	0.4	2.5	ns
All Models						
Output Rise Time	t_r	C_L = 15 pF See Figure 4.2 Propagation Delay Timing on page 14	—	2.5	4.0	ns
Output Fall Time	t_f	C_L = 15 pF See Figure 4.2 Propagation Delay Timing on page 14	—	2.5	4.0	ns
Peak eye diagram jitter	$t_{JIT(PK)}$	See Figure 2.3 Eye Diagram on page 5	—	350	—	ps
Common Mode Transient Immunity	CMTI	$V_I = V_{DD}$ or 0 V V_{CM} = 1500 V (see Figure 4.3 Common Mode Transient Immunity Test Circuit on page 15)	35	50	—	kV/µs
Enable to Data Valid	t_{en1}	See Figure 4.1 ENABLE Timing Diagram on page 14	—	6.0	11	ns
Enable to Data Tri-State	t_{en2}	See Figure 4.1 ENABLE Timing Diagram on page 14	—	8.0	12	ns
Start-up Time [3]	t_{SU}		—	15	40	µs

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit

Notes:

1. The nominal output impedance of an isolator driver channel is approximately 50 Ω, ±40%, which is a combination of the value of the on-chip series termination resistor and channel resistance of the output driver FET. When driving loads where transmission line effects will be a factor, output pins should be appropriately terminated with controlled impedance PCB traces.
2. $t_{PSK(P-P)}$ is the magnitude of the difference in propagation delay times measured between different units operating at the same supply voltages, load, and ambient temperature.
3. Start-up time is the time period from the application of power to valid data at the output.

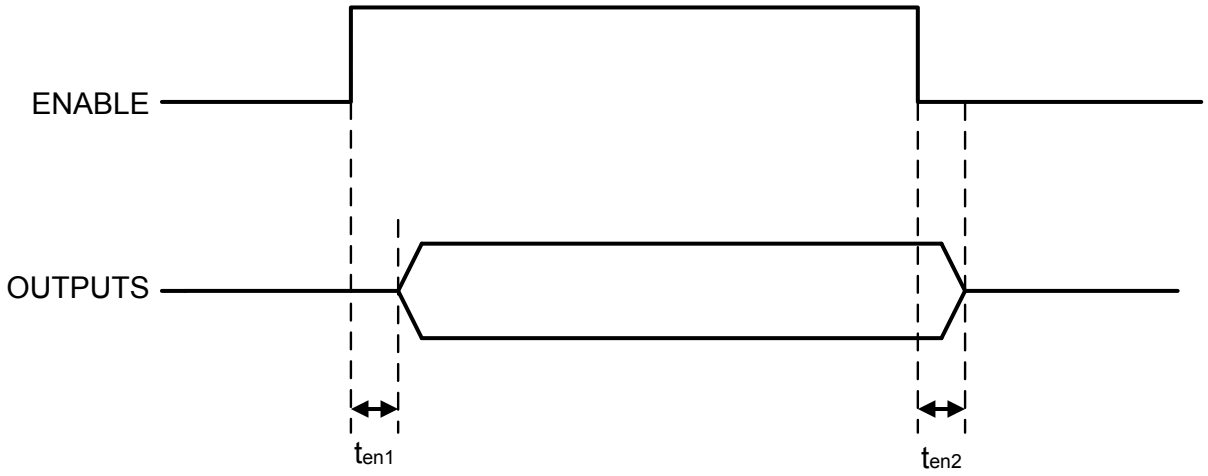


Figure 4.1. ENABLE Timing Diagram

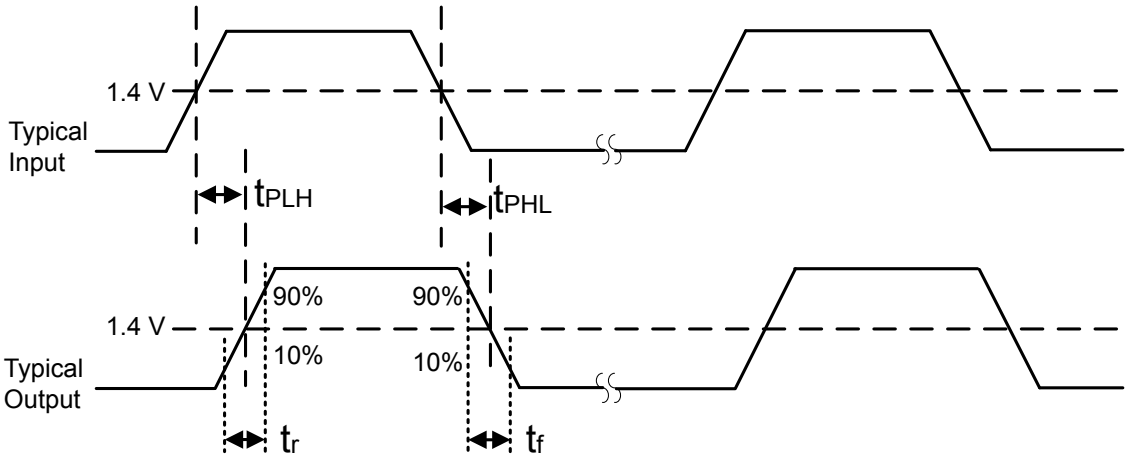


Figure 4.2. Propagation Delay Timing

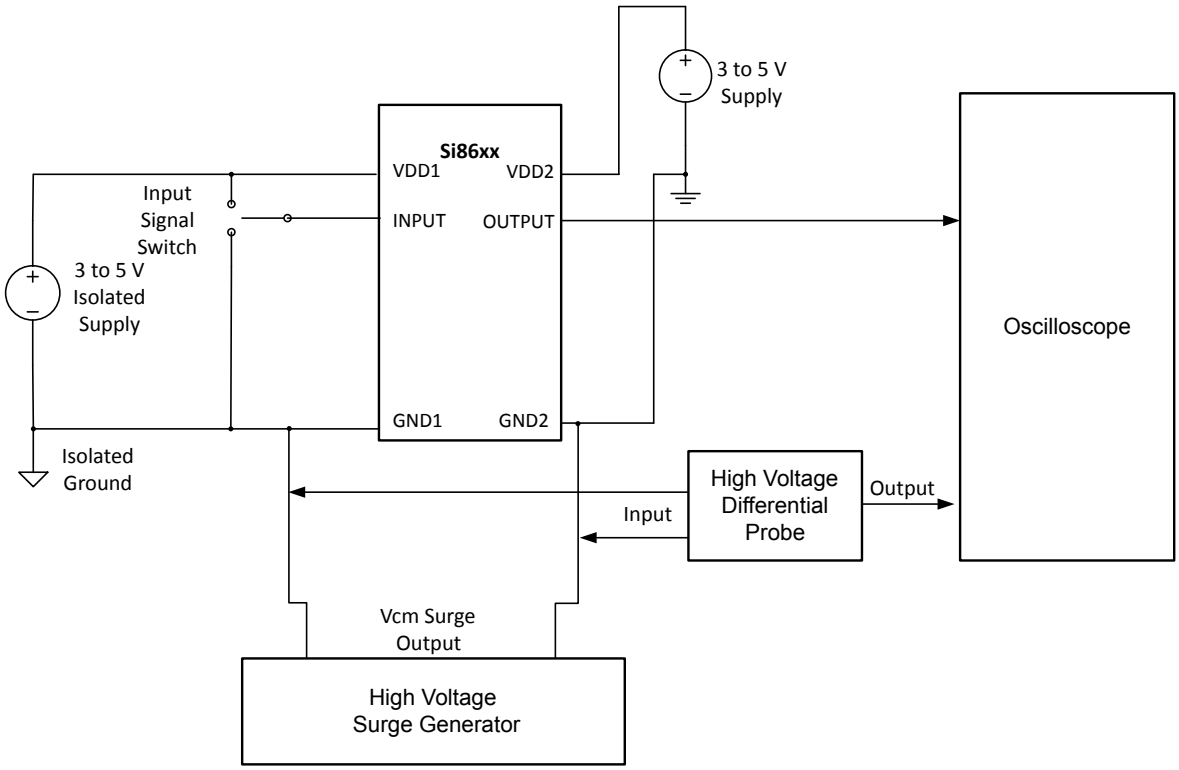


Figure 4.3. Common Mode Transient Immunity Test Circuit

Table 4.3. Electrical Characteristics

(V_{DD1} = 3.3 V±10%, V_{DD2} = 3.3 V±10%, T_A = –40 to 125 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
VDD Undervoltage Threshold	VDDUV+	V_{DD1}, V_{DD2} rising	1.95	2.24	2.375	V
VDD Undervoltage Threshold	VDDUV–	V_{DD1}, V_{DD2} falling	1.88	2.16	2.325	V
VDD Undervoltage Hysteresis	VDD_{HYS}		50	70	95	mV
Positive-Going Input Threshold	VT+	All inputs rising	1.4	1.67	1.9	V
Negative-Going Input Threshold	VT–	All inputs falling	1.0	1.23	1.4	V
Input Hysteresis	V_{HYS}		0.38	0.44	0.50	V
High Level Input Voltage	V_{IH}		2.0	—	—	V
Low Level Input Voltage	V_{IL}		—	—	0.8	V
High Level Output Voltage	V_{OH}	Ioh = –4 mA	V_{DD1},V_{DD2} – 0.4	3.1	—	V
Low Level Output Voltage	V_{OL}	Iol = 4 mA	—	0.2	0.4	V
Input Leakage Current	I_L		—	—	±10	µA
Output Impedance [1]	Z_O		—	50	—	Ω
Enable Input High Current	I_{ENH}	V_{ENx} = V_{IH}	—	2.0	—	µA
Enable Input Low Current	I_{ENL}	V_{ENx} = V_{IL}	—	2.0	—	µA
DC Supply Current (all Inputs 0 V or at Supply)						
Si8650Bx, Ex, Si8655Bx						
V_{DD1}		V_I = 0(Bx), 1(Ex)	—	1.1	1.8	mA
V_{DD2}		V_I = 0(Bx), 1(Ex)	—	3.1	4.7	
V_{DD1}		V_I = 1(Bx), 0(Ex)	—	7.0	9.8	
V_{DD2}		V_I = 1(Bx), 0(Ex)	—	3.3	5.0	
Si8651Bx, Ex						
V_{DD1}		V_I = 0(Bx), 1(Ex)	—	1.5	2.4	mA
V_{DD2}		V_I = 0(Bx), 1(Ex)	—	2.7	4.1	
V_{DD1}		V_I = 1(Bx), 0(Ex)	—	6.6	9.2	
V_{DD2}		V_I = 1(Bx), 0(Ex)	—	4.0	6.0	
Si8652Bx, Ex						
V_{DD1}		V_I = 0(Bx), 1(Ex)	—	2.0	3.0	mA
V_{DD2}		V_I = 0(Bx), 1(Ex)	—	2.4	3.6	
V_{DD1}		V_I = 1(Bx), 0(Ex)	—	5.6	7.8	
V_{DD2}		V_I = 1(Bx), 0(Ex)	—	5.0	7.5	
1 Mbps Supply Current (All Inputs = 500 kHz Square Wave, Cl = 15 pF on All Outputs)						
Si8650Bx, Ex, Si8655Bx						

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
V_{DD1}			—	4.1	5.7	mA
V_{DD2}			—	3.7	5.2	
Si8651Bx, Ex						
V_{DD1}			—	4.2	5.8	mA
V_{DD2}			—	3.8	5.3	
Si8652Bx, Ex						
V_{DD1}			—	4.0	5.6	mA
V_{DD2}			—	4.0	5.6	
10 Mbps Supply Current (All Inputs = 5 MHz Square Wave, Cl = 15 pF on All Outputs)						
Si8650Bx, Ex, Si8655Bx						
V_{DD1}			—	4.1	5.7	mA
V_{DD2}			—	4.4	6.1	
Si8651Bx, Ex						
V_{DD1}			—	4.3	6.0	mA
V_{DD2}			—	4.3	6.0	
Si8652Bx, Ex						
V_{DD1}			—	4.3	6.0	mA
V_{DD2}			—	4.4	6.1	
100 Mbps Supply Current (All Inputs = 50 MHz Square Wave, Cl = 15 pF on All Outputs)						
Si8650Bx, Ex, Si8655Bx						
V_{DD1}			—	4.1	5.7	mA
V_{DD2}			—	15.5	20.1	
Si8651Bx, Ex						
V_{DD1}			—	6.6	8.9	mA
V_{DD2}			—	13.2	17.1	
Si8652Bx, Ex						
V_{DD1}			—	8.9	11.6	mA
V_{DD2}			—	11.1	14.4	
Timing Characteristics						
Si865xBx, Ex						
Maximum Data Rate			0	—	150	Mbps
Minimum Pulse Width			—	—	5.0	ns
Propagation Delay	t_{PHL}, t_{PLH}	See Figure 4.2 Propagation Delay Timing on page 14	5.0	8.0	13	ns
Pulse Width Distortion $\lvert t_{PLH} - t_{PHL} \rvert$	PWD	See Figure 4.2 Propagation Delay Timing on page 14	—	0.2	4.5	ns

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Propagation Delay Skew [2]	$t_{PSK(P-P)}$		—	2.0	4.5	ns
Channel-Channel Skew	t_{PSK}		—	0.4	2.5	ns
All Models						
Output Rise Time	t_r	C_L = 15 pF See Figure 4.2 Propagation Delay Timing on page 14	—	2.5	4.0	ns
Output Fall Time	t_f	C_L = 15 pF (See Figure 4.2 Propagation Delay Timing on page 14)	—	2.5	4.0	ns
Peak eye diagram jitter	$t_{JIT(PK)}$	See Figure 2.3 Eye Diagram on page 5	—	350	—	ps
Common Mode Transient Immunity	CMTI	V_I = V_{DD} or 0 V V_{CM} = 1500 V (See Figure 4.3 Common Mode Transient Immunity Test Circuit on page 15)	35	50	—	kV/µs
Enable to Data Valid	t_{en1}	See Figure 4.1 ENABLE Timing Diagram on page 14	—	6.0	11	ns
Enable to Data Tri-State	t_{en2}	See Figure 4.1 ENABLE Timing Diagram on page 14	—	8.0	12	ns
Start-Up Time [3]	t_{SU}		—	15	40	µs

Notes:
1. The nominal output impedance of an isolator driver channel is approximately 50 Ω, ±40%, which is a combination of the value of the on-chip series termination resistor and channel resistance of the output driver FET. When driving loads where transmission line effects will be a factor, output pins should be appropriately terminated with controlled impedance PCB traces.
2. $t_{PSK(P-P)}$ is the magnitude of the difference in propagation delay times measured between different units operating at the same supply voltages, load, and ambient temperature.
3. Start-up time is the time period from the application of power to valid data at the output.

Table 4.4. Electrical Characteristics

(V_{DD1} = 2.5 V ±5%, V_{DD2} = 2.5 V ±5%, T_A = –40 to 125 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
VDD Undervoltage Threshold	VDDUV+	V_{DD1}, V_{DD2} rising	1.95	2.24	2.375	V
VDD Undervoltage Threshold	VDDUV–	V_{DD1}, V_{DD2} falling	1.88	2.16	2.325	V
VDD Undervoltage Hysteresis	VDD_{HYS}		50	70	95	mV
Positive-Going Input Threshold	VT+	All inputs rising	1.4	1.67	1.9	V
Negative-Going Input Threshold	VT–	All inputs falling	1.0	1.23	1.4	V
Input Hysteresis	V_{HYS}		0.38	0.44	0.50	V
High Level Input Voltage	V_{IH}		2.0	—	—	V
Low Level Input Voltage	V_{IL}		—	—	0.8	V
High Level Output Voltage	V_{OH}	Ioh = –4 mA	V_{DD1},V_{DD2} – 0.4	2.3	—	V

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Low Level Output Voltage	V_{OL}	Iol = 4 mA	—	0.2	0.4	V
Input Leakage Current	I_L		—	—	±10	µA
Output Impedance [1]	Z_O		—	50	—	Ω
Enable Input High Current	I_{ENH}	$V_{ENx} = V_{IH}$	—	2.0	—	µA
Enable Input Low Current	I_{ENL}	$V_{ENx} = V_{IL}$	—	2.0	—	µA
DC Supply Current (All Inputs 0 V or at Supply)						
Si8650Bx, Ex, Si8655Bx						
V_{DD1}		V_I = 0(Bx), 1(Ex)	—	1.1	1.8	mA
V_{DD2}		V_I = 0(Bx), 1(Ex)	—	3.1	4.7	
V_{DD1}		V_I = 1(Bx), 0(Ex)	—	7.0	9.8	
V_{DD2}		V_I = 1(Bx), 0(Ex)	—	3.3	5.0	
Si8651Bx, Ex						
V_{DD1}		V_I = 0(Bx), 1(Ex)	—	1.5	2.4	mA
V_{DD2}		V_I = 0(Bx), 1(Ex)	—	2.7	4.1	
V_{DD1}		V_I = 1(Bx), 0(Ex)	—	6.6	9.2	
V_{DD2}		V_I = 1(Bx), 0(Ex)	—	4.0	6.0	
Si8652Bx, Ex						
V_{DD1}		V_I = 0(Bx), 1(Ex)	—	2.0	3.0	mA
V_{DD2}		V_I = 0(Bx), 1(Ex)	—	2.4	3.6	
V_{DD1}		V_I = 1(Bx), 0(Ex)	—	5.6	7.8	
V_{DD2}		V_I = 1(Bx), 0(Ex)	—	5.0	7.5	
1 Mbps Supply Current (All Inputs = 500 kHz Square Wave, Cl = 15 pF on All Outputs)						
Si8650Bx, Ex, Si8655Bx						
V_{DD1}			—	4.1	5.7	mA
V_{DD2}			—	3.7	5.2	
Si8651Bx, Ex						
V_{DD1}			—	4.2	5.8	mA
V_{DD2}			—	3.8	5.3	
Si8652Bx, Ex						
V_{DD1}			—	4.0	5.6	mA
V_{DD2}			—	4.0	5.6	
10 Mbps Supply Current (All Inputs = 5 MHz Square Wave, Cl = 15 pF on All Outputs)						
Si8650Bx, Ex, Si8655Bx						
V_{DD1}			—	4.1	5.7	mA
V_{DD2}			—	4.0	5.6	

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Si8651Bx, Ex						
V_{DD1}			—	4.2	5.9	mA
V_{DD2}			—	4.0	5.6	
Si8652Bx, Ex						
V_{DD1}			—	4.1	5.8	mA
V_{DD2}			—	4.2	5.9	
100 Mbps Supply Current (All Inputs = 50 MHz Square Wave, Cl = 15 pF on All Outputs)						
Si8650Bx, Ex, Si8655Bx						
V_{DD1}			—	4.1	5.7	mA
V_{DD2}			—	12.5	16.2	
Si8651Bx, Ex						
V_{DD1}			—	6.0	8.1	mA
V_{DD2}			—	10.8	14	
Si8652Bx, Ex						
V_{DD1}			—	7.6	9.9	mA
V_{DD2}			—	9.3	12.0	
Timing Characteristics						
Si865xBx, Ex						
Maximum Data Rate			0	—	150	Mbps
Minimum Pulse Width			—	—	5.0	ns
Propagation Delay	t_{PHL}, t_{PLH}	See Figure 4.2 Propagation Delay Timing on page 14	5.0	8.0	14	ns
Pulse Width Distortion $\lvert t_{PLH} - t_{PHL} \rvert$	PWD	See Figure 4.2 Propagation Delay Timing on page 14	—	0.2	5.0	ns
Propagation Delay Skew [2]	$t_{PSK(P-P)}$		—	2.0	5.0	ns
Channel-Channel Skew	t_{PSK}		—	0.4	2.5	ns
All Models						
Output Rise Time	t_r	C_L = 15 pF See Figure 4.2 Propagation Delay Timing on page 14	—	2.5	4.0	ns
Output Fall Time	t_f	C_L = 15 pF See Figure 4.2 Propagation Delay Timing on page 14	—	2.5	4.0	ns
Peak Eye Diagram Jitter	$t_{JIT(PK)}$	See Figure 2.3 Eye Diagram on page 5	—	350	—	ps

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Common Mode Transient Immunity	CMTI	$V_I = V_{DD}$ or 0 V V_{CM} = 1500 V (See Figure 4.3 Common Mode Transient Immunity Test Circuit on page 15)	35	50	—	kV/µs
Enable to Data Valid	t_{en1}	See Figure 4.1 ENABLE Timing Diagram on page 14	—	6.0	11	ns
Enable to Data Tri-State	t_{en2}	See Figure 4.1 ENABLE Timing Diagram on page 14	—	8.0	12	ns
Startup Time [3]	t_{SU}		—	15	40	µs

Notes:

1. The nominal output impedance of an isolator driver channel is approximately 50 Ω, ±40%, which is a combination of the value of the on-chip series termination resistor and channel resistance of the output driver FET. When driving loads where transmission line effects will be a factor, output pins should be appropriately terminated with controlled impedance PCB traces.
2. $t_{PSK(P-P)}$ is the magnitude of the difference in propagation delay times measured between different units operating at the same supply voltages, load, and ambient temperature.
3. Start-up time is the time period from the application of power to valid data at the output.

Table 4.5. Regulatory Information [1]

CSA
The Si865x is certified under CSA Component Acceptance Notice 5A. For more details, see Master Contract Number 232873.
60950-1, 62368-1: Up to 600 V_{RMS} reinforced insulation working voltage; up to 1000 V_{RMS} basic insulation working voltage.
60601-1: Up to 250 V_{RMS} working voltage and 2 MOPP (Means of Patient Protection).
VDE
The Si865x is certified according to VDE 0884-10. For more details, see certificate 40018443.
0884-10: Up to 1200 V_{peak} for basic insulation working voltage.
60950-1: Up to 600 V_{RMS} reinforced insulation working voltage; up to 1000 V_{RMS} basic insulation working voltage.
UL
The Si865x is certified under UL1577 component recognition program. For more details, see File E257455.
Rated up to 5000 V_{RMS} isolation voltage for basic protection.
CQC
The Si865x is certified under GB4943.1-2011. For more details, see certificates CQC13001096110 and CQC13001096239.
Rated up to 600 V_{RMS} reinforced insulation working voltage; up to 1000 V_{RMS} basic insulation working voltage.

Note:

1. Regulatory Certifications apply to 2.5 kV_{RMS} rated devices which are production tested to 3.0 kV_{RMS} for 1 sec. Regulatory Certifications apply to 3.75 kV_{RMS} rated devices which are production tested to 4.5 kV_{RMS} for 1 sec. Regulatory Certifications apply to 5.0 kV_{RMS} rated devices which are production tested to 6.0 kV_{RMS} for 1 sec.
   For more information, see 1. Ordering Guide.

Table 4.6. Insulation and Safety-Related Specifications

Parameter	Symbol	Test Condition	Value			Unit
			WB SOIC-16	NB SOIC-16	QSOP-16	
Nominal External Air Gap (Clearance)[1]	CLR		8.0	4.9	3.6	mm
Nominal External Tracking (Creepage) [1]	CPG		8.0	4.01	3.6	mm
Minimum Internal Gap (Internal Clearance)	DTI		0.014	0.014	0.014	mm
Tracking Resistance	CTI or PTI	IEC60112	600	600	600	V_{RMS}
Erosion Depth	ED		0.019	0.019	0.031	mm
Resistance (Input-Output)[2]	R_{IO}		10^{12}	10^{12}	10^{12}	Ω
Capacitance (Input-Output)[2]	C_{IO}	f = 1 MHz	2.0	2.0	2.0	pF
Input Capacitance[3]	C_I		4.0	4.0	4.0	pF

Note:

1. The values in this table correspond to the nominal creepage and clearance values. VDE certifies the clearance and creepage limits as 4.7 mm minimum for the NB SOIC-16 package and QSOP-16 packages and 8.5 mm minimum for the WB SOIC-16 package. UL does not impose a clearance and creepage minimum for component-level certifications. CSA certifies the clearance and creepage of the WB SOIC-16 package with designation "IS2" as 8 mm minimum. CSA certifies the clearance and creepage limits as 3.9 mm minimum for the NB SOIC 16, 3.6 mm minimum for the QSOP-16, and 7.6 mm minimum for the WB SOIC-16 package with package designation "IS" as listed in the data sheet.
2. To determine resistance and capacitance, the Si86xx is converted into a 2-terminal device. Pins 1–8 are shorted together to form the first termina and pins 9–16 are shorted together to form the second terminal. The parameters are then measured between these two terminals.
3. Measured from input pin to ground.

Table 4.7. IEC 60664-1 Ratings

Parameter	Test Conditions	Specification		
		WB SOIC-16	NB SOIC-16	QSOP-16
Basic Isolation Group	Material Group	I	I	I
Installation Classification	Rated Mains Voltages ≤ 150 V_{RMS}	I-IV	I-IV	I-IV
	Rated Mains Voltages ≤ 300 V_{RMS}	I-IV	I-III	I-III
	Rated Mains Voltages ≤ 400 V_{RMS}	I-III	I-II	I-II
	Rated Mains Voltages ≤ 600 V_{RMS}	I-III	I-II	I-II

Table 4.8. VDE 0884-10 Insulation Characteristics for Si86xxxx[1]

Parameter	Symbol	Test Condition	Characteristic			Unit
			WB SOIC-16	NB SOIC-16	QSOP-16	
Maximum Working Insulation Voltage	V_{IORM}		1200	630	630	Vpeak
Input to Output Test Voltage	V_{PR}	Method b1 (V_{IORM} x 1.875 = VPR, 100% Production Test, t_m = 1 sec, Partial Discharge < 5 pC)	2250	1182	1182	Vpeak
Transient Overvoltage	V_{IOTM}	t = 60 sec	6000	6000	6000	Vpeak
Surge Voltage	V_{IOSM}	Tested per IEC 60065 with surge voltage of 1.2 µs/50 µs Si865xxB/C/D tested with 4000 V	3077	3077	3077	Vpeak
Pollution Degree (DIN VDE 0110, Table 1)			2	2	2	
Insulation Resistance at T_S, V_{IO} = 500 V	R_S		$>10^9$	$>10^9$	$>10^9$	Ω

Note:
1. Maintenance of the safety data is ensured by protective circuits. The Si86xxxx provides a climate classification of 40/125/21.

Table 4.9. VDE 0884-10 Safety Limiting Values[1]

Parameter	Symbol	Test Condition	Max			Unit
			WB SOIC-16	NB SOIC-16	QSOP-16	
Case Temperature	T_S		150	150	150	°C
Safety Input, Output, or Supply Current	I_S	θ_{JA} = 100 °C/W (WB SOIC-16) 105 °C/W (NB SOIC-16, QSOP-16) V_I = 5.5 V, T_J = 150 °C, T_A = 25 °C	220	215	215	mA
Device Power Dissipation[2]	P_D		415	415	415	mW

Note:
1. Maximum value allowed in the event of a failure; also see the thermal derating curve in Figure 4.4 (WB SOIC-16) Thermal Derating Curve, Dependence of Safety Limiting Values with Case Temperature per VDE 0884-10 on page 24 and Figure 4.5 (NB SOIC-16, QSOP-16) Thermal Derating Curve, Dependence of Safety Limiting Values with Case Temperature per VDE 0884-10 on page 24.
2. The Si86xx is tested with VDD1 = VDD2 = 5.5 V; T_J = 150 ºC; C_L = 15 pF, input a 150 Mbps 50% duty cycle square wave.

Table 4.10. Thermal Characteristics

Parameter	Symbol	WB SOIC-16	NB SOIC-16/QSOP-16	Unit
IC Junction-to-Air Thermal Resistance	θ_{JA}	100	105	°C/W

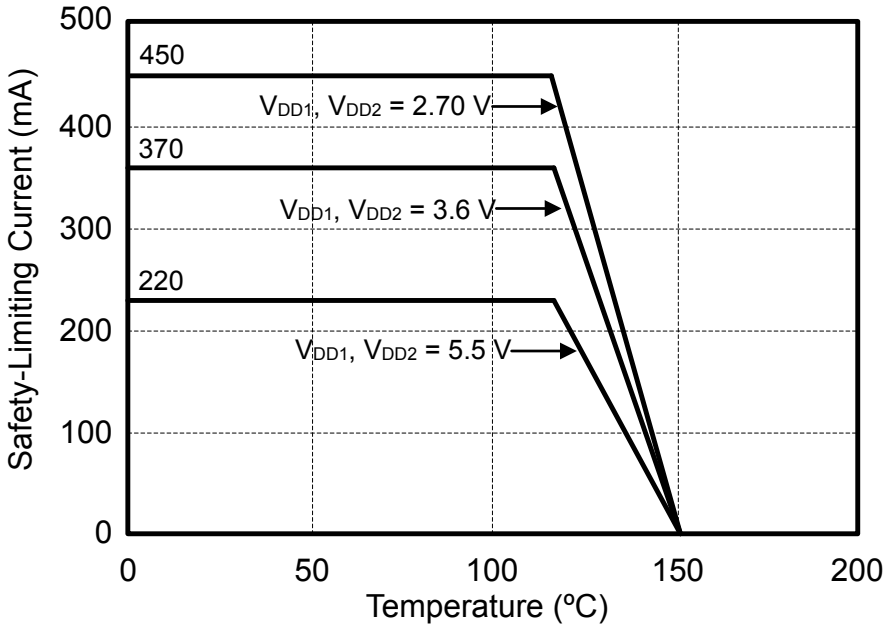


Figure 4.4. (WB SOIC-16) Thermal Derating Curve, Dependence of Safety Limiting Values with Case Temperature per VDE 0884-10

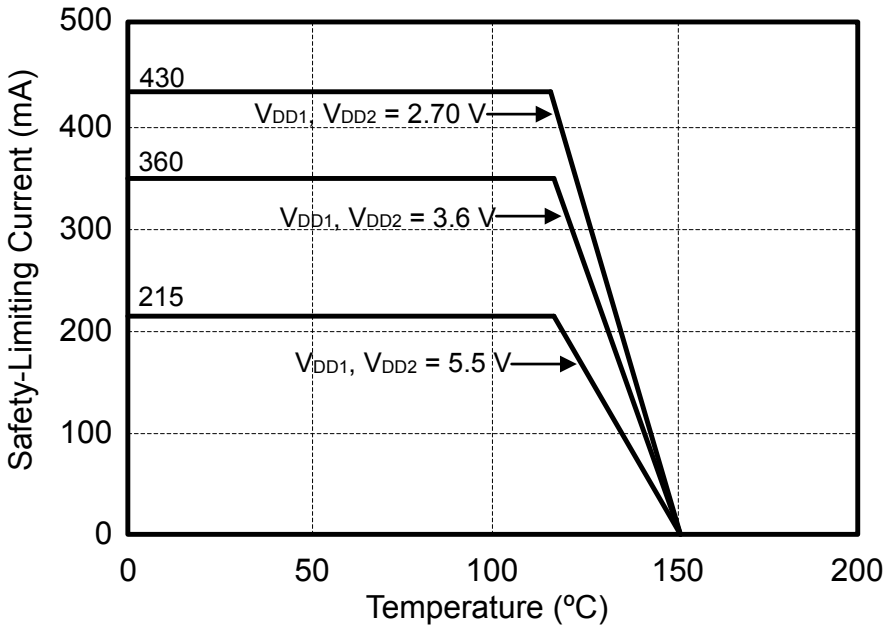


Figure 4.5. (NB SOIC-16, QSOP-16) Thermal Derating Curve, Dependence of Safety Limiting Values with Case Temperature per VDE 0884-10

Table 4.11. Absolute Maximum Ratings [1]

Parameter	Symbol	Min	Max	Unit
Storage Temperature [2]	T_{STG}	–65	150	°C
Ambient Temperature Under Bias	T_A	–40	125	°C
Junction Temperature	T_J	—	150	°C
Supply Voltage	V_{DD1}, V_{DD2}	–0.5	7.0	V
Input Voltage	V_I	–0.5	V_{DD} + 0.5	V
Output Voltage	V_O	–0.5	V_{DD} + 0.5	V
Output Current Drive Channel (All devices unless otherwise stated)	I_O	—	10	mA
Output Current Drive Channel (All Si865xxA-x-xx devices)	I_O	—	22	mA
Latchup Immunity [3]		—	100	V/ns
Lead Solder Temperature (10 s)		—	260	°C
Maximum Isolation (Input to Output) (1 sec) NB SOIC-16, QSOP-16		—	4500	V_{RMS}
Maximum Isolation (Input to Output) (1 sec) WB SOIC-16		—	6500	V_{RMS}

Notes:

1. Permanent device damage may occur if the absolute maximum ratings are exceeded. Functional operation should be restricted to conditions as specified in the operational sections of this data sheet.
2. VDE certifies storage temperature from –40 to 150 °C.
3. Latchup immunity specification is for slew rate applied across GND1 and GND2.

5. Pin Descriptions

5.1 Si8650/51/52 Pin Descriptions

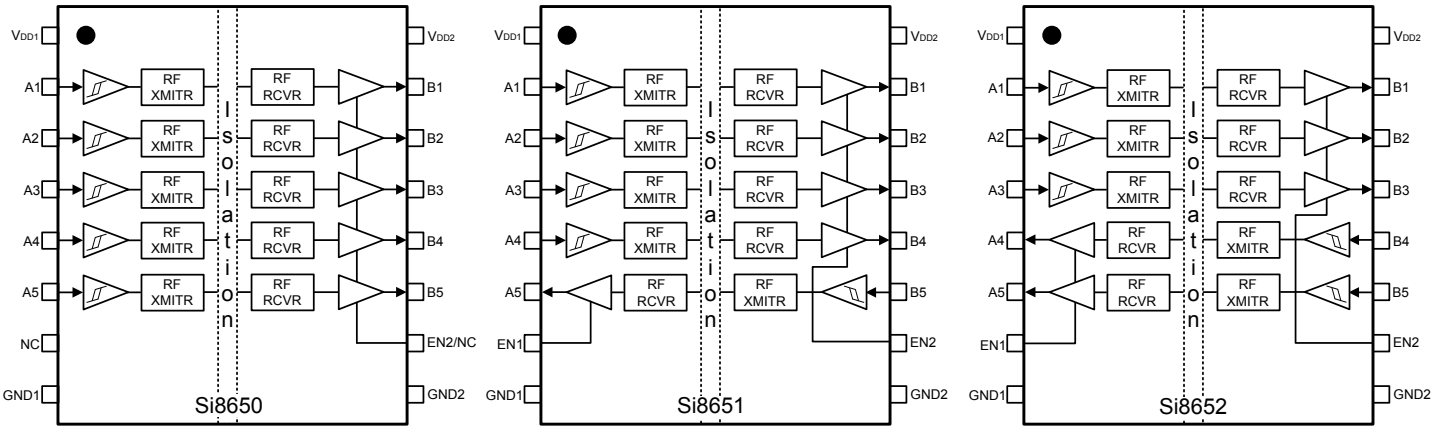


Figure 5.1. Si8650/51/52 Pinout

Table 5.1. Si8650/51/52 Pin Descriptions

Name	SOIC-16 Pin#	Type	Description
V_{DD1}	1	Supply	Side 1 power supply.
A1	2	Digital Input	Side 1 digital input.
A2	3	Digital Input	Side 1 digital input.
A3	4	Digital Input	Side 1 digital input.
A4	5	Digital I/O	Side 1 digital input or output.
A5	6	Digital I/O	Side 1 digital input or output.
EN1/NC[1]	7	Digital Input	Side 1 active high enable. NC on Si8650.
GND1	8	Ground	Side 1 ground.
GND2	9	Ground	Side 2 ground.
EN2	10	Digital Input	Side 2 active high enable.
B5	11	Digital I/O	Side 2 digital input or output.
B4	12	Digital I/O	Side 2 digital input or output.
B3	13	Digital Output	Side 2 digital output.
B2	14	Digital Output	Side 2 digital output.
B1	15	Digital Output	Side 2 digital output.
V_{DD2}	16	Supply	Side 2 power supply.

Note:
1. No Connect. These pins are not internally connected. They can be left floating, tied to V_{DD} or tied to GND.

5.2 Si8655 Pin Descriptions

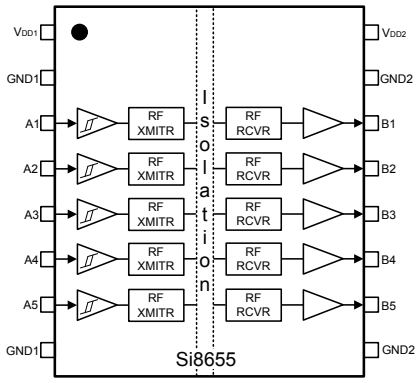


Figure 5.2. Si8655 Pinout

Table 5.2. Si8655 Pin Descriptions

Name	SOIC-16 Pin#	Type	Description
V_{DD1}	1	Supply	Side 1 power supply.
GND1	2[1]	Ground	Side 1 ground.
A1	3	Digital Input	Side 1 digital input.
A2	4	Digital Input	Side 1 digital input.
A3	5	Digital Input	Side 1 digital input.
A4	6	Digital Input	Side 1 digital input.
A5	7	Digital Input	Side 1 digital input.
GND1	8[1]	Ground	Side 1 ground.
GND2	9[1]	Ground	Side 2 ground.
B5	10	Digital Output	Side 2 digital output.
B4	11	Digital Output	Side 2 digital output.
B3	12	Digital Output	Side 2 digital output.
B2	13	Digital Output	Side 2 digital output.
B1	14	Digital Output	Side 2 digital output.
GND2	15[1]	Ground	Side 2 ground.
V_{DD2}	16	Supply	Side 2 power supply.

Note:

1. For narrow-body devices, Pin 2 and Pin 8 GND must be externally connected to respective ground. Pin 9 and Pin 15 must also be connected to external ground.

6. Package Outline (16-Pin Wide Body SOIC)

The figure below illustrates the package details for the Si86xx digital isolator in a 16-pin wide-body SOIC package. The table below lists the values for the dimensions shown in the illustration.

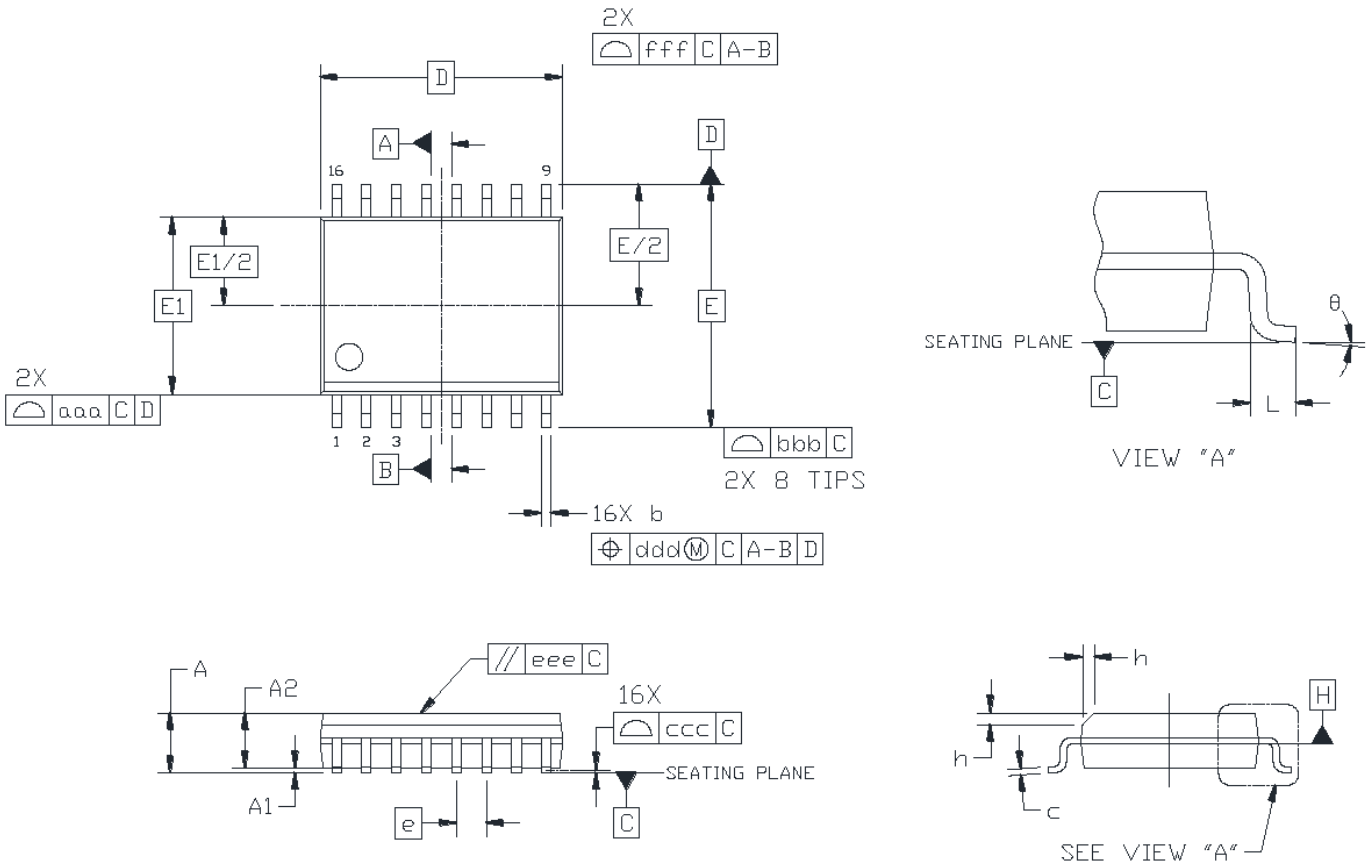


Figure 6.1. 16-Pin Wide Body SOIC

Table 6.1. 16-Pin Wide Body SOIC Package Diagram Dimensions

Dimension	Min	Max
A	—	2.65
A1	0.10	0.30
A2	2.05	—
b	0.31	0.51
c	0.20	0.33
D	10.30 BSC	
E	10.30 BSC	
E1	7.50 BSC	
e	1.27 BSC	
L	0.40	1.27
h	0.25	0.75
θ	0°	8°
aaa	—	0.10
bbb	—	0.33
ccc	—	0.10
ddd	—	0.25
eee	—	0.10
fff	—	0.20

Notes:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to JEDEC Outline MS-013, Variation AA.
4. Recommended reflow profile per JEDEC J-STD-020 specification for small body, lead-free components.

7. Land Pattern (16-Pin Wide-Body SOIC)

The figure below illustrates the recommended land pattern details for the Si86xx in a 16-pin wide-body SOIC package. The table below lists the values for the dimensions shown in the illustration.

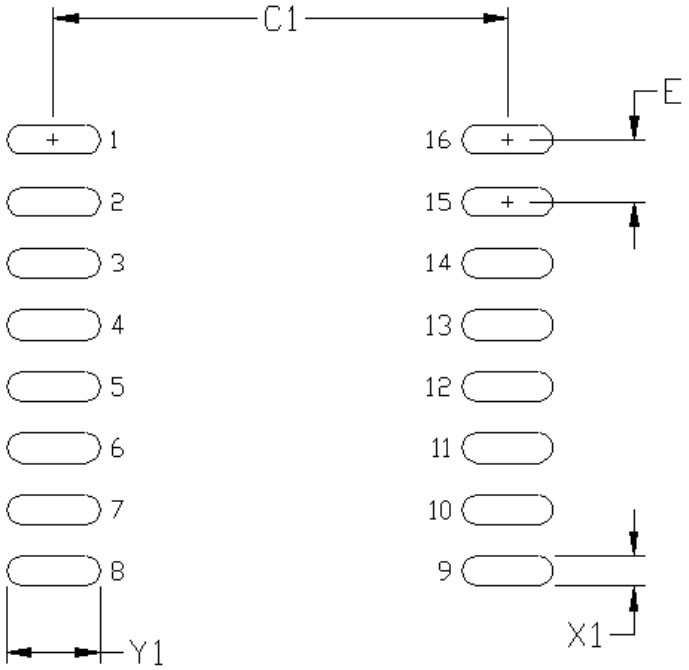


Figure 7.1. 16-Pin Wide Body SOIC PCB Land Pattern

Table 7.1. 16-Pin Wide Body SOIC Land Pattern Dimensions

Dimension	Feature	(mm)
C1	Pad Column Spacing	9.40
E	Pad Row Pitch	1.27
X1	Pad Width	0.60
Y1	Pad Length	1.90

Notes:

1. This Land Pattern Design is based on IPC-7351 pattern SOIC127P1032X265-16AN for Density Level B (Median Land Protrusion).
2. All feature sizes shown are at Maximum Material Condition (MMC) and a card fabrication tolerance of 0.05 mm is assumed.

8. Package Outline (16-Pin Narrow Body SOIC)

The figure below illustrates the package details for the Si86xx in a 16-pin narrow-body SOIC package. The table below lists the values for the dimensions shown in the illustration.

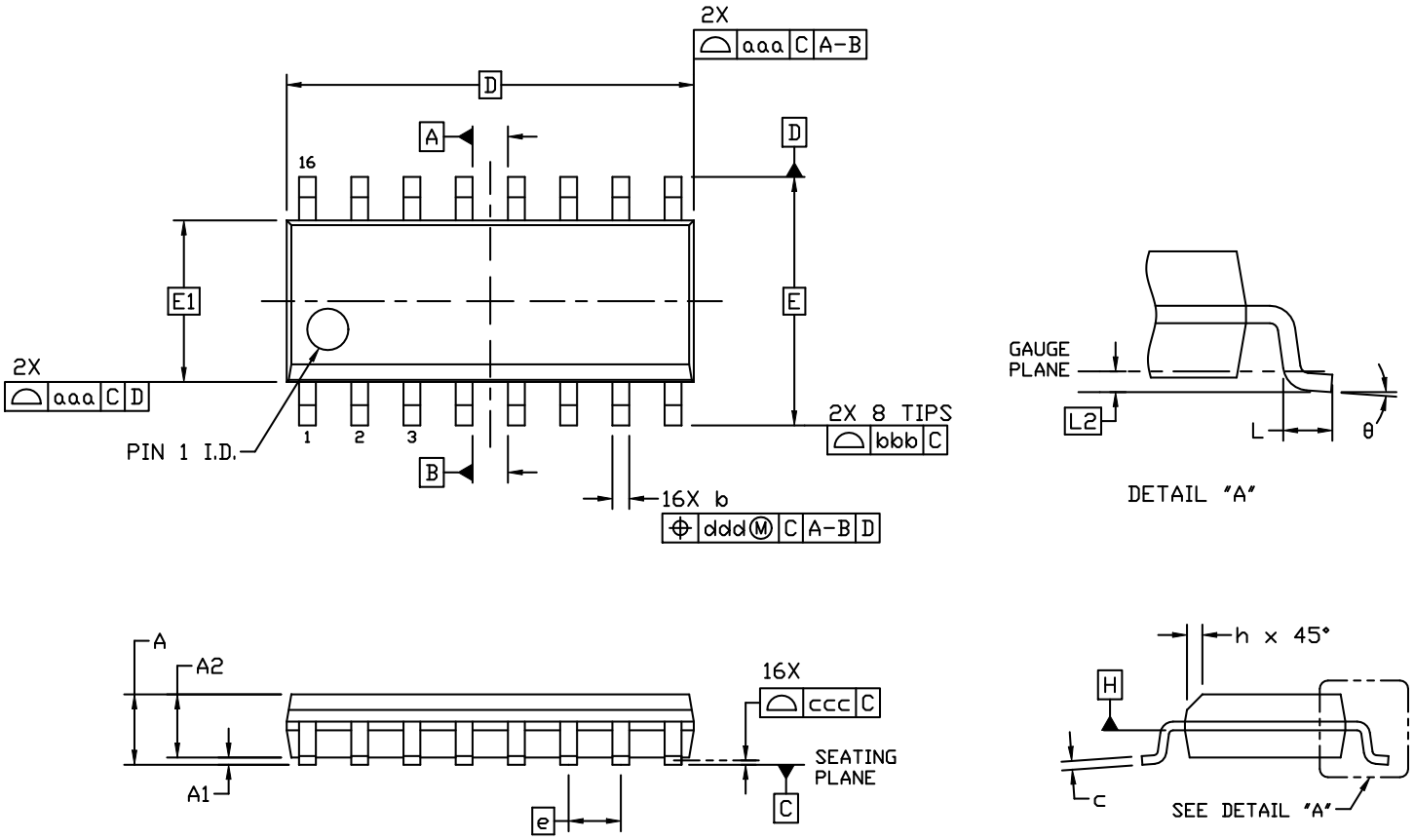


Figure 8.1. 16-Pin Narrow Body SOIC

Table 8.1. 16-Pin Narrow Body SOIC Package Diagram Dimensions

Dimension	Min	Max
A	—	1.75
A1	0.10	0.25
A2	1.25	—
b	0.31	0.51
c	0.17	0.25
D	9.90 BSC	
E	6.00 BSC	
E1	3.90 BSC	
e	1.27 BSC	
L	0.40	1.27
L2	0.25 BSC	
h	0.25	0.50
θ	0°	8°
aaa	0.10	
bbb	0.20	
ccc	0.10	
ddd	0.25	

Notes:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to the JEDEC Solid State Outline MS-012, Variation AC.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

9. Land Pattern (16-Pin Narrow Body SOIC)

The figure below illustrates the recommended land pattern details for the Si86xx in a 16-pin narrow-body SOIC package. The table below lists the values for the dimensions shown in the illustration.

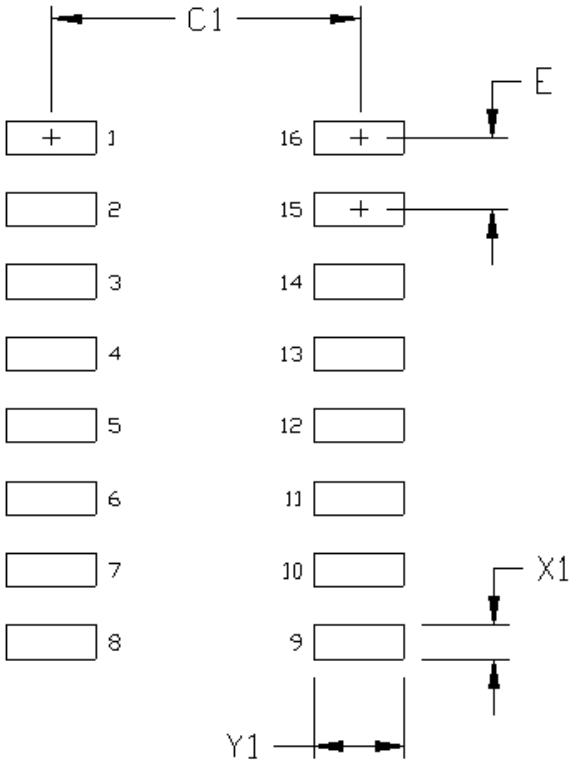


Figure 9.1. 16-Pin Narrow Body SOIC PCB Land Pattern

Table 9.1. 16-Pin Narrow Body SOIC Land Pattern Dimensions

Dimension	Feature	(mm)
C1	Pad Column Spacing	5.40
E	Pad Row Pitch	1.27
X1	Pad Width	0.60
Y1	Pad Length	1.55

Notes:

1. This Land Pattern Design is based on IPC-7351 pattern SOIC127P600X165-16N for Density Level B (Median Land Protrusion).
2. All feature sizes shown are at Maximum Material Condition (MMC) and a card fabrication tolerance of 0.05 mm is assumed.

10. Package Outline (16-Pin QSOP)

The figure below illustrates the package details for the Si86xx in a 16-pin QSOP package. The table below lists the values for the dimensions shown in the illustration.

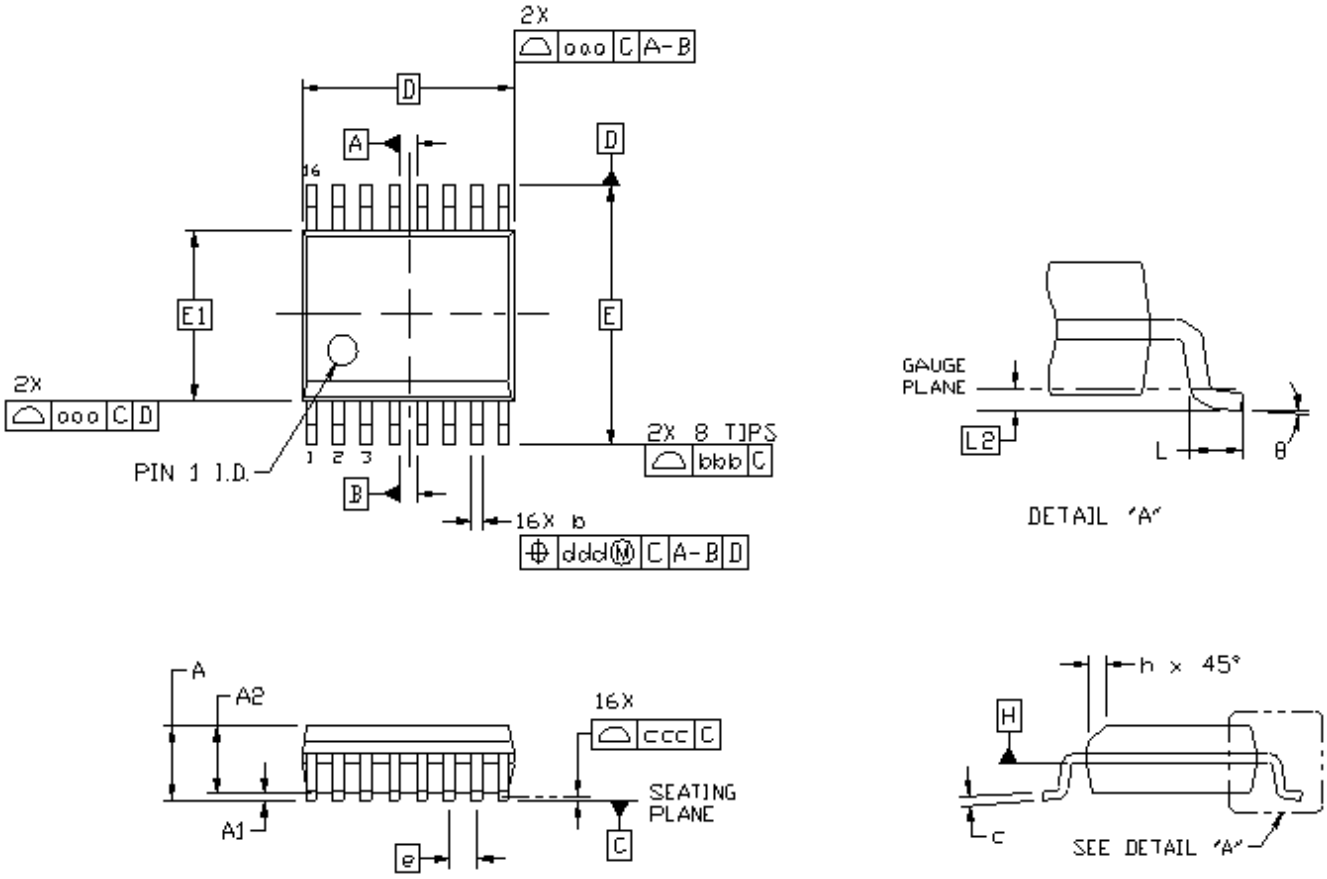


Figure 10.1. 16-Pin QSOP Package

Table 10.1. 16-Pin QSOP Package Diagram Dimensions

Dimension	Min	Max
A	—	1.75
A1	0.10	0.25
A2	1.25	—
b	0.20	0.30
c	0.17	0.25
D	4.89 BSC	
E	6.00 BSC	
E1	3.90 BSC	
e	0.635 BSC	
L	0.40	1.27
L2	0.25 BSC	
h	0.25	0.50
θ	0°	8°
aaa	0.10	
bbb	0.20	
ccc	0.10	
ddd	0.25	

Notes:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to the JEDEC Solid State Outline MO-137, Variation AB.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

11. Land Pattern (16-Pin QSOP)

The figure below illustrates the recommended land pattern details for the Si86xx in a 16-pin QSOP package. The table below lists the values for the dimensions shown in the illustration.

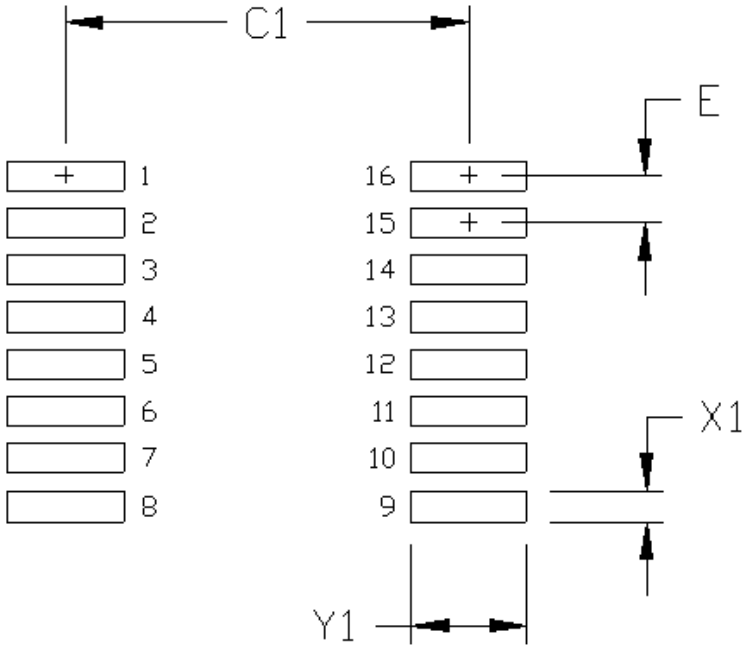


Figure 11.1. 16-Pin QSOP PCB Land Pattern

Table 11.1. 16-Pin QSOP Land Pattern Dimensions

Dimension	Feature	(mm)
C1	Pad Column Spacing	5.40
E	Pad Row Pitch	0.635
X1	Pad Width	0.40
Y1	Pad Length	1.55

Notes:

1. This Land Pattern Design is based on IPC-7351 pattern SOP63P602X173-16N for Density Level B (Median Land Protrusion).
2. All feature sizes shown are at Maximum Material Condition (MMC) and a card fabrication tolerance of 0.05 mm is assumed.

12. Top Marking (16-Pin Wide Body SOIC)

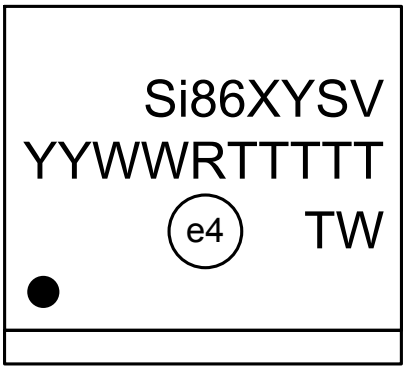


Figure 12.1. 16-Pin Wide Body SOIC Top Marking

Table 12.1. 16-Pin Wide Body SOIC Top Marking Explanation

Line 1 Marking:	Base Part Number Ordering Options (See 1. Ordering Guide for more information).	Si86 = Isolator product series XY = Channel Configuration X = # of data channels (5) Y = # of reverse channels (2, 1, 0) [1] S = Speed Grade (max data rate) and operating mode: A = 1 Mbps (default output = low) B = 150 Mbps (default output = low) D = 1 Mbps (default output = high) E = 150 Mbps (default output = high) V = Insulation rating A = 1 kV; B = 2.5 kV; C = 3.75 kV; D = 5.0 kV
Line 2 Marking:	YY = Year WW = Workweek	Assigned by assembly subcontractor. Corresponds to the year and work week of the mold date.
	RTTTTT = Mfg Code	Manufacturing code from assembly house “R” indicates revision
Line 3 Marking:	Circle = 1.7 mm Diameter (Center-Justified)	“e4” Pb-free symbol
	Country of Origin ISO Code Abbreviation	TW = Taiwan as shown, TH = Thailand
Note: 1. Si8655 has 0 reverse channels.		

1

13. Top Marking (16-Pin Narrow Body SOIC)

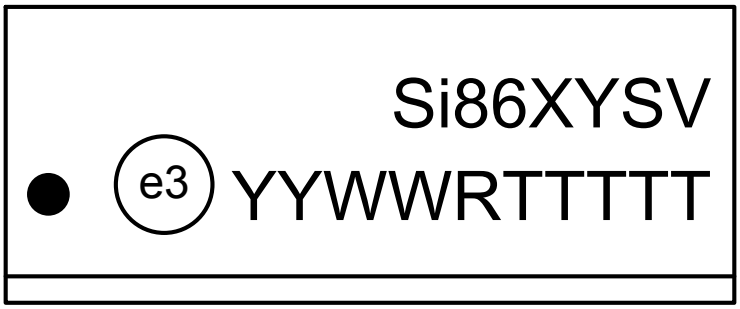


Figure 13.1. 16-Pin Narrow Body SOIC Top Marking

Table 13.1. 16-Pin Narrow Body SOIC Top Marking Explanation

Line 1 Marking:	Base Part Number Ordering Options (See 1. Ordering Guide for more information).	Si86 = Isolator product series XY = Channel Configuration X = # of data channels (5) Y = # of reverse channels (2, 1, 0) [1] S = Speed Grade (max data rate) and operating mode: A = 1 Mbps (default output = low) B = 150 Mbps (default output = low) D = 1 Mbps (default output = high) E = 150 Mbps (default output = high) V = Insulation rating A = 1 kV; B = 2.5 kV; C = 3.75 kV
Line 2 Marking:	Circle = 1.2 mm Diameter	“e3” Pb-Free Symbol
	YY = Year WW = Work Week	Assigned by the assembly subcontractor. Corresponds to the year and work week of the mold date.
	RTTTTT = Mfg Code	Manufacturing code from assembly house. “R” indicates revision.

Note:
1. Si8655 has 0 reverse channels.

14. Top Marking (16-Pin QSOP)

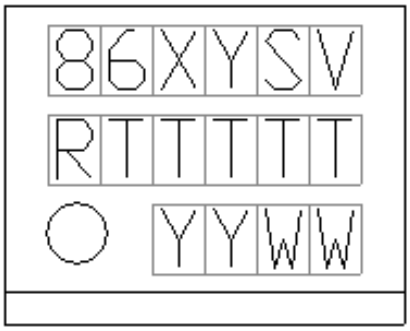


Figure 14.1. 16-Pin QSOP Top Marking

Table 14.1. 16-Pin QSOP Top Marking Explanation

Line 1 Marking:	Base Part Number Ordering Options (See 1. Ordering Guide for more information).	86 = Isolator product series XY = Channel Configuration X = # of data channels (5) Y = # of reverse channels (2, 1, 0) [1] S = Speed Grade (max data rate) and operating mode: A = 1 Mbps (default output = low) B = 150 Mbps (default output = low) D = 1 Mbps (default output = high) E = 150 Mbps (default output = high) V = Insulation rating. A = 1 kV; B = 2.5 kV; C = 3.75 kV
Line 2 Marking:	RTTTTT = Mfg Code	Manufacturing code from assembly house. “R” indicates revision.
Line 3 Marking:	YY = Year WW = Work Week	Assigned by the Assembly House. Corresponds to the year and work week of the mold date.
Note: 1. Si8655 has 0 reverse channels.		

15. Document Change List

Revision 0.1

June 30, 2010
- Initial release.

Revision 0.1 to Revision 0.2

September 15, 2010
- Deleted Sections 4.3.4 and 4.3.5.
- Updated 1. Ordering Guide.
  - Updated Table 1.1 Ordering Guide for Valid OPNs[1, 2, 3] on page 2.
- Added 3.4 Fail-Safe Operating Mode.

Revision 0.2 to Revision 1.0

March 31, 2011
- Added chip graphics on the front page.
- Moved Table 4.1 Recommended Operating Conditions on page 11 and Table 4.11 Absolute Maximum Ratings [1] on page 25.
- Updated 4. Electrical Specifications.
- Moved Table 3.1 Si865x Logic Operation on page 6 and Table 3.2 Enable Input Truth [1] on page 7.
- Moved 3.5 Typical Performance Characteristics.
- Updated 5.1 Si8650/51/52 Pin Descriptions.
- Updated 5.2 Si8655 Pin Descriptions.
- Updated 1. Ordering Guide.

Revision 1.0 to Revision 1.1

July 14, 2011
- Reordered spec tables to conform to new convention.
- Removed "pending" throughout document.

Revision 1.1 to Revision 1.2

September 14, 2011
- Updated High Level Output Voltage VOH to 3.1 V in Table 4.3 Electrical Characteristics on page 16.
- Updated High Level Output Voltage VOH to 2.3 V in Table 4.4 Electrical Characteristics on page 18.

Revision 1.2 to Revision 1.3

November 11, 2011
- Added Output Current Drive Channel specification for Si865xxA-x-xx devices.
- Added Latchup Immunity specification.

Revision 1.3 to Revision 1.4

February 15, 2012
- Updated Table 1.1 Ordering Guide for Valid OPNs[1, 2, 3] on page 2.
  - Updated Note 1 with MSL2A.

Revision 1.4 to Revision 1.5

March 20, 2012
- Updated 1. Ordering Guide to include MSL2A.

Revision 1.5 to Revision 1.6

June 26, 2012

- Added junction temperature spec to Table 4.11 Absolute Maximum Ratings [1] on page 25.
- Updated 3.3.1 Supply Bypass.
- Removed former Section 3.3.2. Pin Connections.
- Updated table notes in 5.1 Si8650/51/52 Pin Descriptions.
- Removed Rev A devices from 1. Ordering Guide.
- Updated 6. Package Outline (16-Pin Wide Body SOIC).
- Added revision description to Top Markings.

Revision 1.6 to Revision 1.7

September 25, 2013

- Added Figure 4.3 Common Mode Transient Immunity Test Circuit on page 15.
- Added references to CQC throughout.
- Added references to 2.5 kV_{RMS} devices throughout.
- Updated 1. Ordering Guide.
- Updated 12. Top Marking (16-Pin Wide Body SOIC).
- Updated 14. Top Marking (16-Pin QSOP).

Revision 1.7 to Revision 1.8

June 18, 2015

- Updated Table 4.5 Regulatory Information [1] on page 21.
  - Added CQC certificate numbers.
- Updated 1. Ordering Guide.
  - Removed references to moisture sensitivity levels.
  - Removed former note 2.

Revision 1.8 to Revision 1.9

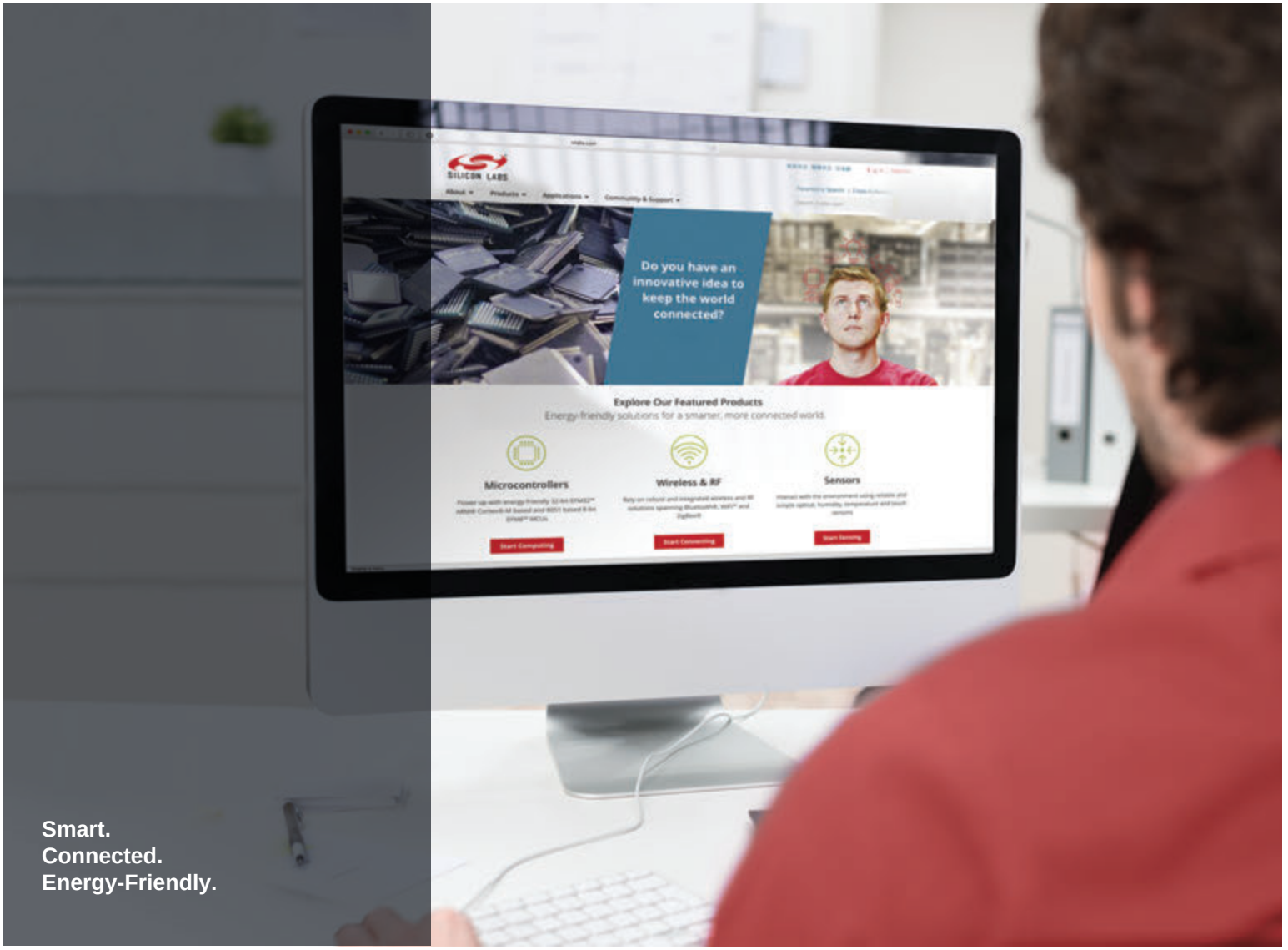
November 30, 2016

- Updated data sheet format.
- Added note to Table 1.1 Ordering Guide for Valid OPNs[1, 2, 3] on page 2 for denoting tape and reel marking.

Revision 1.9 to Revision 2.0

October 18, 2017

- Added new OPNs in Ordering Guide for IU (QSOP) and IS2 (8 mm creepage WB SOIC) package options.
- Added 62368-1 references throughout.
- Removed 61010-1 references throughout.



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