

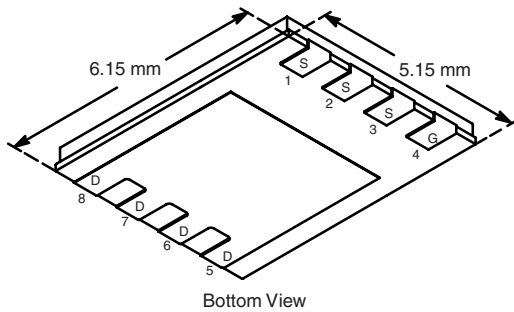


N-Channel 250-V (D-S) MOSFET

PRODUCT SUMMARY

V_{DS} (V)	$R_{DS(on)}$ (Ω)	I_D (A) ^g	Q_g (Typ.)
250	0.118 at $V_{GS} = 10$ V	18.4	32
	0.124 at $V_{GS} = 6$ V	18.0	

PowerPAK SO-8



Ordering Information: Si7190DP-T1-GE3 (Lead (Pb)-free and Halogen-free)

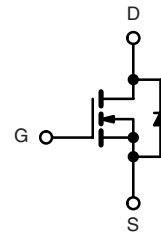
FEATURES

- Halogen-free According to IEC 61249-2-21 Definition
- TrenchFET[®] Power MOSFET
- Low Thermal Resistance PowerPAK[®] Package
- 100 % R_g Tested
- 100 % UIS Tested
- Compliant to RoHS Directive 2002/95/EC


RoHS
 COMPLIANT
 HALOGEN
FREE

APPLICATIONS

- Primary Side Switch
- Industrial
- POL



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS $T_A = 25$ °C, unless otherwise noted

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	250	V
Gate-Source Voltage	V_{GS}	± 20	
Continuous Drain Current ($T_J = 150$ °C)	I_D	$T_C = 25$ °C	18.4
		$T_C = 70$ °C	14.7
		$T_A = 25$ °C	4.4 ^{b, c}
		$T_A = 70$ °C	3.5 ^{b, c}
Pulsed Drain Current	I_{DM}	30	A
Continuous Source-Drain Diode Current	I_S	$T_C = 25$ °C	
		$T_A = 25$ °C	4.5 ^{b, c}
Avalanche Current	I_{AS}	7	mJ
Single-Pulse Avalanche Energy	E_{AS}	2.4	
Maximum Power Dissipation	P_D	$T_C = 25$ °C	96
		$T_C = 70$ °C	61.5
		$T_A = 25$ °C	5.4 ^{b, c}
		$T_A = 70$ °C	3.5 ^{b, c}
Operating Junction and Storage Temperature Range	T_J, T_{stg}	- 55 to 150	°C
Soldering Recommendations (Peak Temperature) ^{d, e}		260	

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient ^{b, f}	R_{thJA}	18	23	°C/W
Maximum Junction-to-Case (Drain)	R_{thJC}	1.0	1.3	

Notes:

a. Package limited.

b. Surface Mounted on 1" x 1" FR4 board.

c. $t = 10$ s.
 d. See Solder Profile (www.vishay.com/ppg?73461). The PowerPAK SO-8 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.

e. Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.

f. Maximum under Steady State conditions is 65 °C/W.

g. Based on $T_C = 25$ °C.

SPECIFICATIONS $T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted						
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0\text{ V}, I_D = 1\text{ mA}$	250			V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	$I_D = 250\text{ }\mu\text{A}$		258		mV/ $^\circ\text{C}$
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$			-9.8		
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	2		4	V
Gate-Source Leakage	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 250\text{ V}, V_{GS} = 0\text{ V}$			1	μA
		$V_{DS} = 250\text{ V}, V_{GS} = 0\text{ V}, T_J = 55\text{ }^\circ\text{C}$			10	
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} \geq 5\text{ V}, V_{GS} = 10\text{ V}$	20			A
Drain-Source On-State Resistance ^a	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 4.4\text{ A}$		0.098	0.118	Ω
		$V_{GS} = 6\text{ V}, I_D = 4.3\text{ A}$		0.103	0.124	
Forward Transconductance ^a	g_{fs}	$V_{DS} = 15\text{ V}, I_D = 4.4\text{ A}$		19		S
Dynamic^b						
Input Capacitance	C_{iss}	$V_{DS} = 125\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$		2214		pF
Output Capacitance	C_{oss}			96		
Reverse Transfer Capacitance	C_{rss}			50		
Total Gate Charge	Q_g	$V_{DS} = 125\text{ V}, V_{GS} = 10\text{ V}, I_D = 4.4\text{ A}$		48	72	nC
				32	48	
Gate-Source Charge	Q_{gs}	$V_{DS} = 125\text{ V}, V_{GS} = 6\text{ V}, I_D = 4.4\text{ A}$		12		
Gate-Drain Charge	Q_{gd}			15		
Gate Resistance	R_g	$f = 1\text{ MHz}$	0.2	0.9	1.8	Ω
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 125\text{ V}, R_L = 35.7\text{ }\Omega$ $I_D \cong 3.5\text{ A}, V_{GEN} = 6\text{ V}, R_g = 1\text{ }\Omega$		21	32	ns
Rise Time	t_r			14	21	
Turn-Off Delay Time	$t_{d(off)}$			24	36	
Fall Time	t_f			10	20	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 125\text{ V}, R_L = 35.7\text{ }\Omega$ $I_D \cong 3.5\text{ A}, V_{GEN} = 10\text{ V}, R_g = 1\text{ }\Omega$		13	20	
Rise Time	t_r			12	18	
Turn-Off Delay Time	$t_{d(off)}$			28	42	
Fall Time	t_f			9	18	
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I_S	$T_C = 25\text{ }^\circ\text{C}$			30	A
Pulse Diode Forward Current ^a	I_{SM}				30	
Body Diode Voltage	V_{SD}	$I_S = 3.5\text{ A}$		0.8	1.2	V
Body Diode Reverse Recovery Time	t_{rr}	$I_F = 3.5\text{ A}, dI/dt = 100\text{ A}/\mu\text{s}, T_J = 25\text{ }^\circ\text{C}$		87	131	ns
Body Diode Reverse Recovery Charge	Q_{rr}			300	450	nC
Reverse Recovery Fall Time	t_a			62		ns
Reverse Recovery Rise Time	t_b			25		

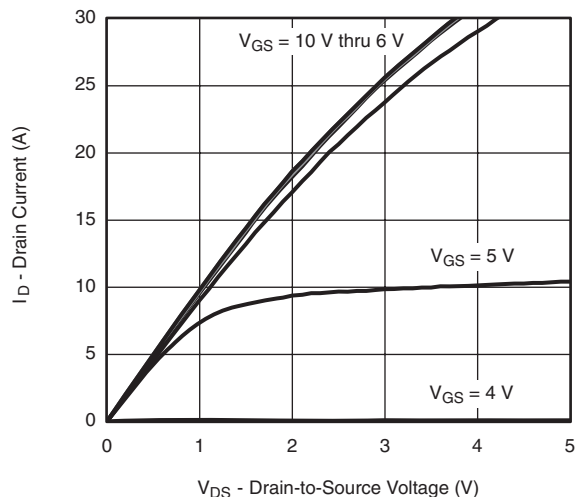
Notes:

- a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.
b. Guaranteed by design, not subject to production testing.

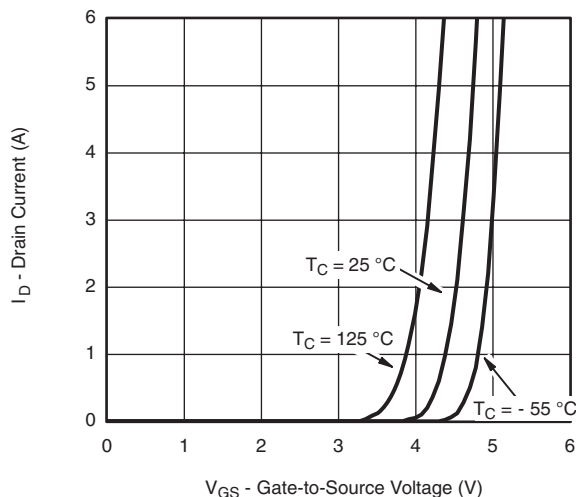
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



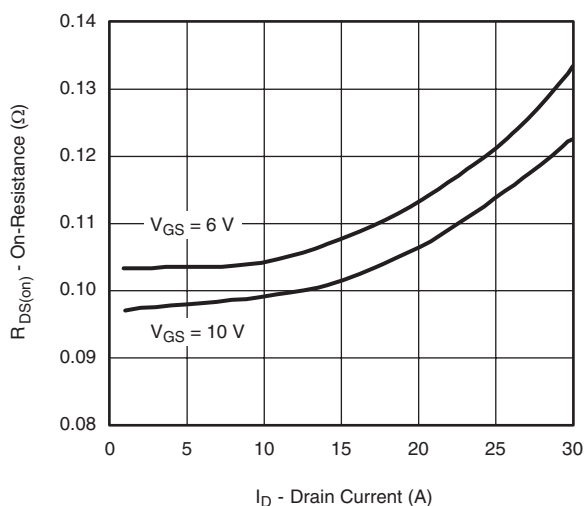
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



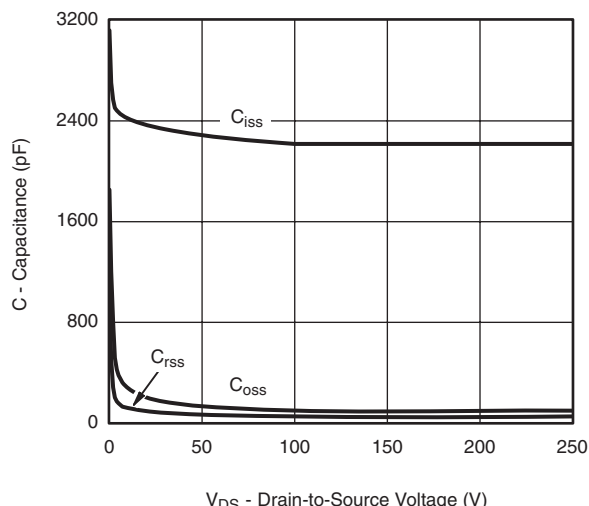
Output Characteristics



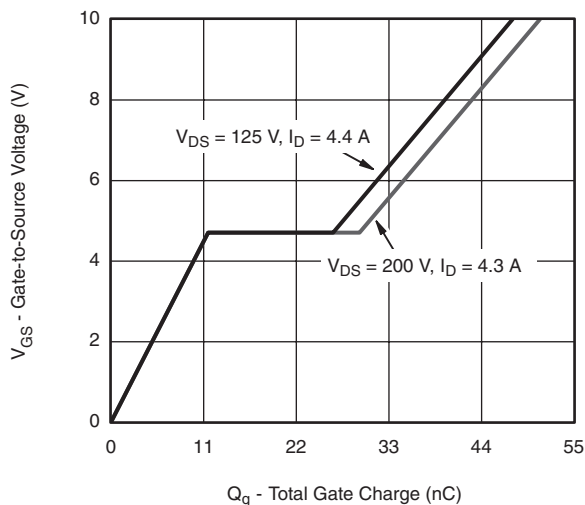
Transfer Characteristics



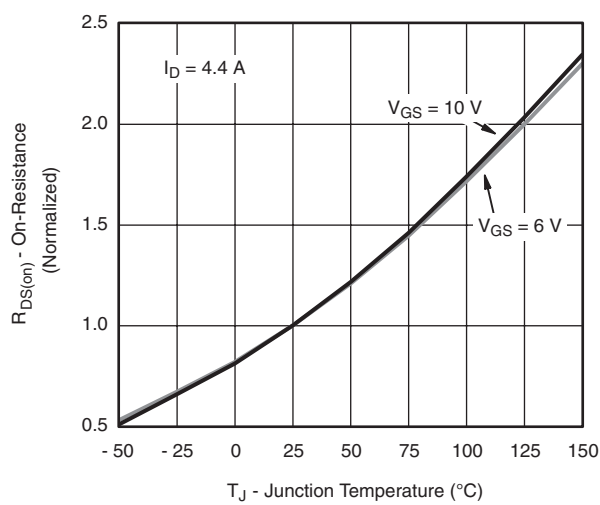
On-Resistance vs. Drain Current and Gate Voltage



Capacitance



Gate Charge



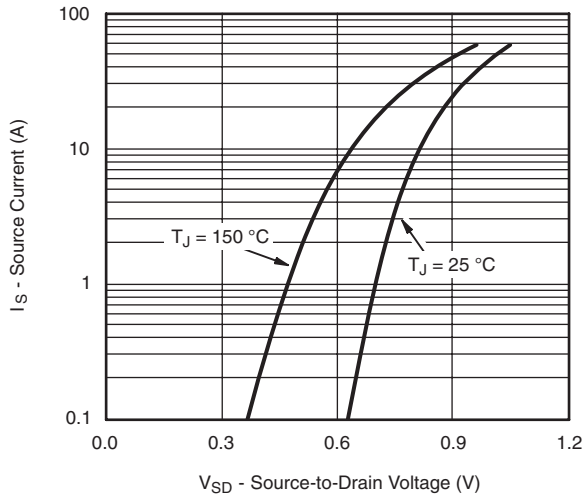
On-Resistance vs. Junction Temperature

Si7190DP

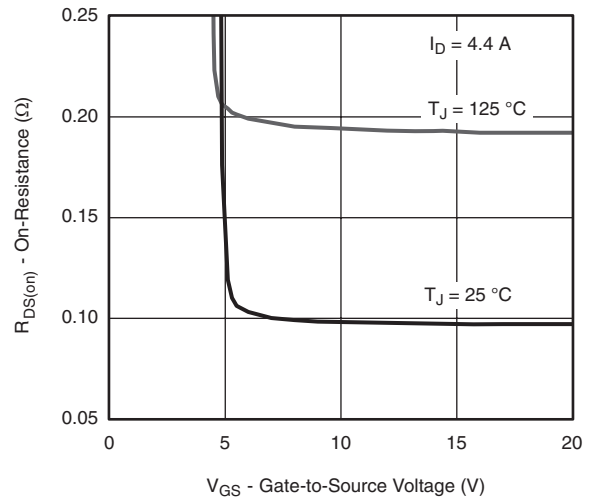
Vishay Siliconix



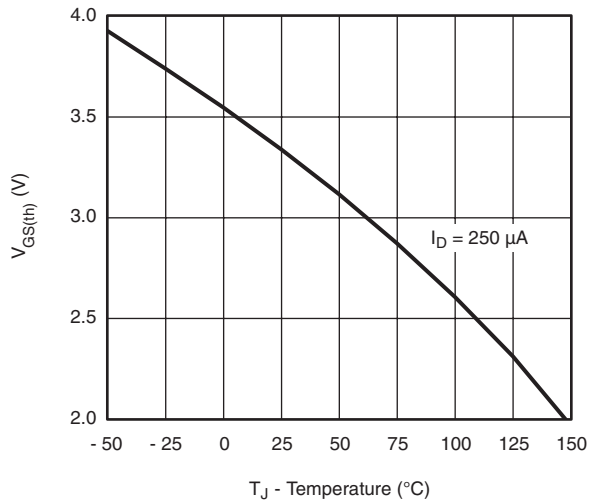
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



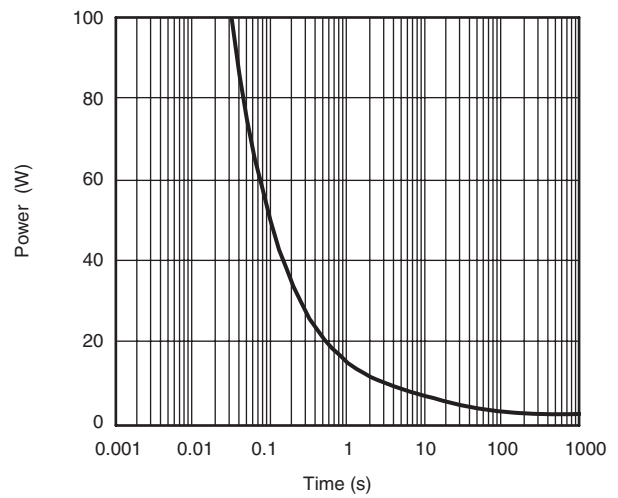
Source-Drain Diode Forward Voltage



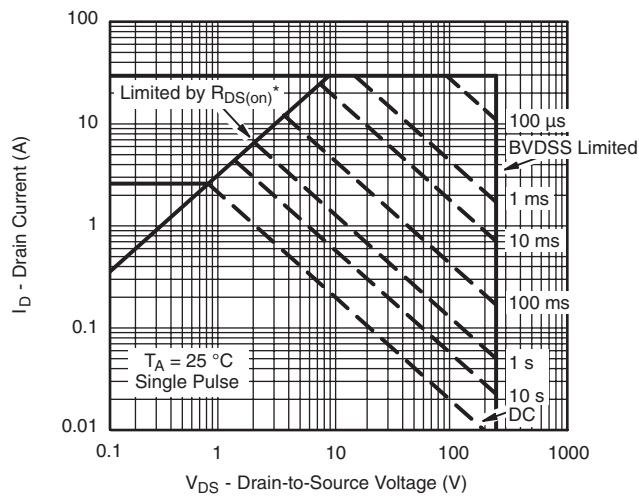
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



Single Pulse Power, Junction-to-Ambient

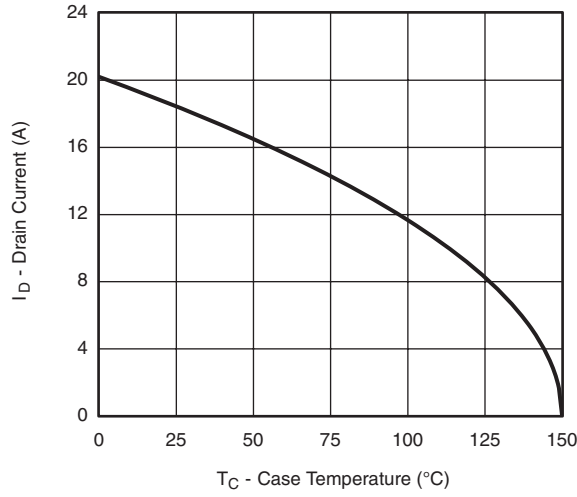


* $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified

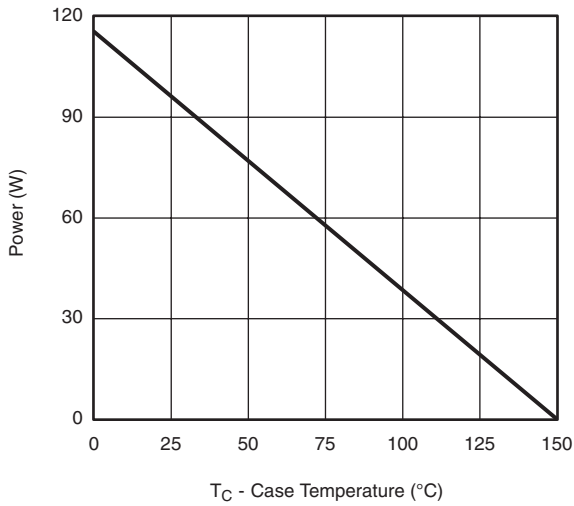
Safe Operating Area, Junction-to-Ambient



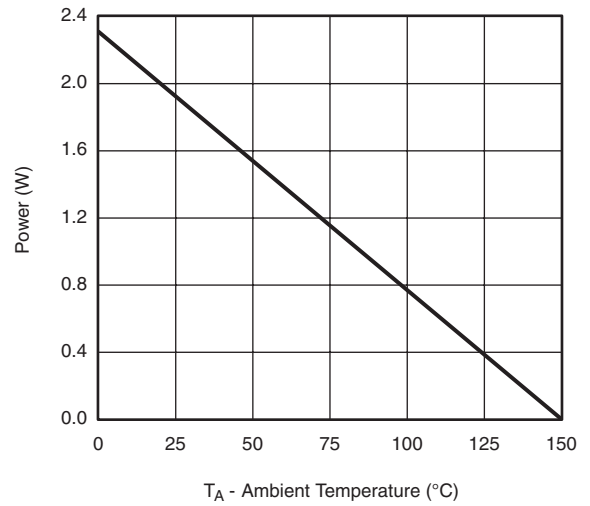
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



Current Derating*



Power, Junction-to-Case



Power, Junction-to-Ambient

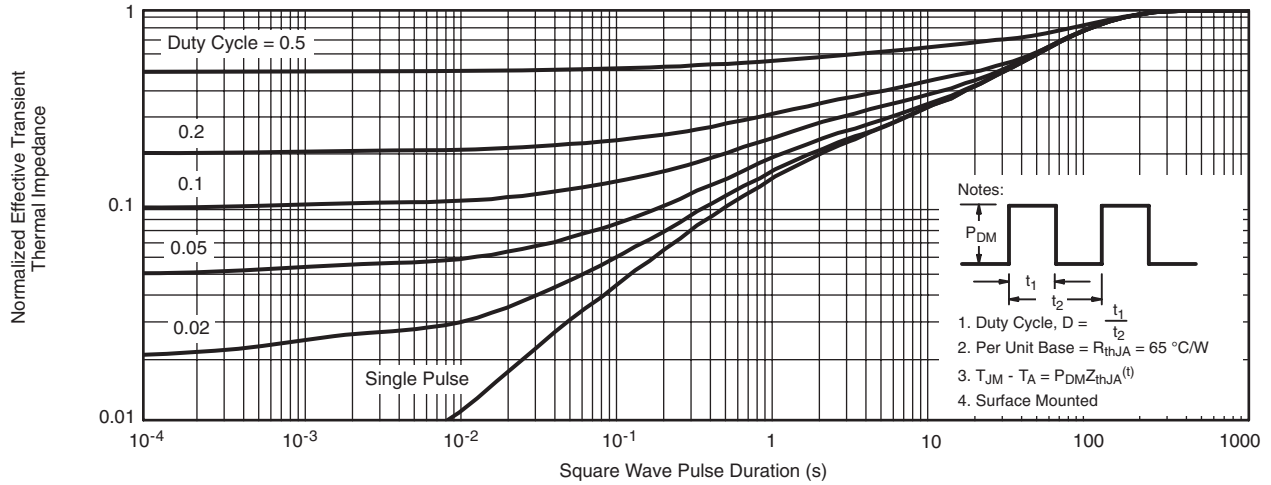
* The power dissipation P_D is based on $T_{J(max)} = 150$ °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

Si7190DP

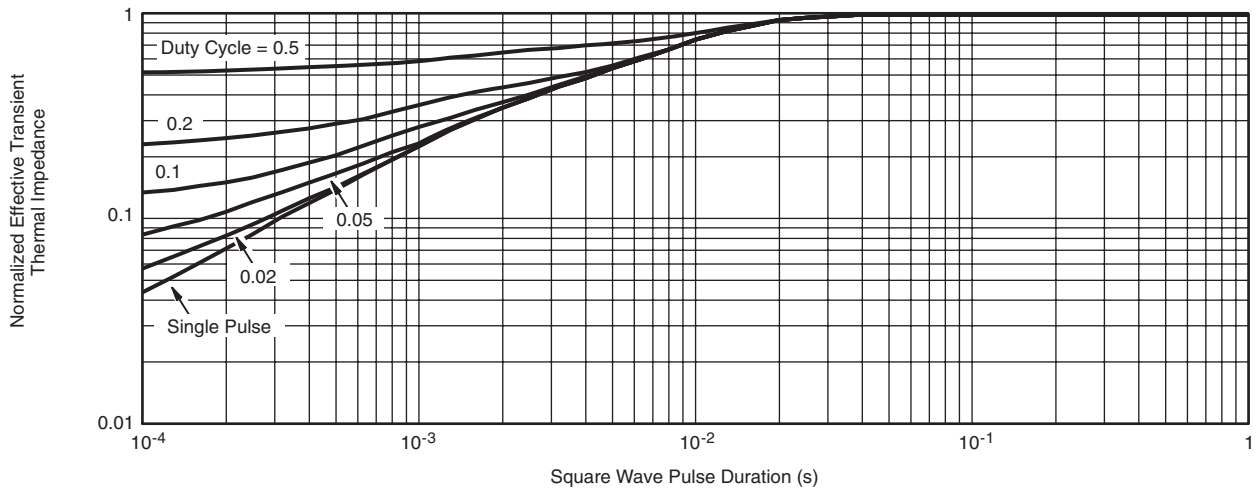
Vishay Siliconix



TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case

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