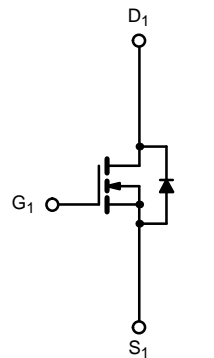
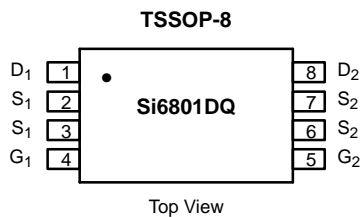




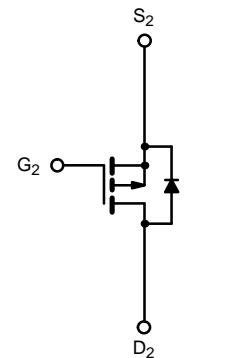
N- and P-Channel, Reduced Q_g , Fast Switching MOSFET

**High-Efficiency
PWM Optimized**

PRODUCT SUMMARY			
	V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
N-Channel	20	0.160 @ $V_{GS} = 4.5$ V	± 1.9
		0.260 @ $V_{GS} = 3.0$ V	± 1.5
P-Channel	-20	0.190 @ $V_{GS} = -4.5$ V	± 1.7
		0.280 @ $V_{GS} = -3.0$ V	± 1.3



N-Channel MOSFET



P-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)				
Parameter	Symbol	N-Channel	P-Channel	Unit
Drain-Source Voltage	V_{DS}	20	-20	V
Gate-Source Voltage	V_{GS}	± 12		
Continuous Drain Current ($T_J = 150^\circ\text{C}$) ^a	I_D	$T_A = 25^\circ\text{C}$	± 1.9	± 1.7
		$T_A = 70^\circ\text{C}$	± 1.5	± 1.3
Pulsed Drain Current	I_{DM}	± 8		A
Continuous Source Current (Diode Conduction) ^a	I_S	1.0	-1.0	
Maximum Power Dissipation ^a	P_D	$T_A = 25^\circ\text{C}$	1.0	
		$T_A = 70^\circ\text{C}$	0.64	
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 to 150		$^\circ\text{C}$

THERMAL RESISTANCE RATINGS			
Parameter	Symbol	N- or P-Channel	Unit
Maximum Junction-to-Ambient ^a	R_{thJA}	125	$^\circ\text{C/W}$

Notes

a. Surface Mounted on FR4 Board, $t \leq 10$ sec.



SPECIFICATIONS (T _J = 25 °C UNLESS OTHERWISE NOTED)							
Parameter	Symbol	Test Condition	Min	Typ	Max	Unit	
Static							
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	N-Ch	0.6			V
		V _{DS} = V _{GS} , I _D = -250 μA	P-Ch	-0.6			
Gate-Body Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ±12 V	N-Ch		±100	nA	
			P-Ch		±100		
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 20 V, V _{GS} = 0 V	N-Ch		1	μA	
		V _{DS} = -20 V, V _{GS} = 0 V	P-Ch		-1		
		V _{DS} = 20 V, V _{GS} = 0 V, T _J = 70 °C	N-Ch		25		
		V _{DS} = -20 V, V _{GS} = 0 V, T _J = 70 °C	P-Ch		-25		
On-State Drain Current ^a	I _{D(on)}	V _{DS} = 5 V, V _{GS} = 4.5 V	N-Ch	6		A	
		V _{DS} = -5 V, V _{GS} = -4.5 V	P-Ch	-6			
Drain-Source On-State Resistance ^a	r _{DS(on)}	V _{GS} = 4.5 V, I _D = 1.9 A	N-Ch		0.120	0.160	Ω
		V _{GS} = -4.5 V, I _D = -1.7 A	P-Ch		0.155	0.190	
		V _{GS} = 3.0 V, I _D = 1.5 A	N-Ch		0.160	0.260	
		V _{GS} = -3.0 V, I _D = -1.3 A	P-Ch		0.210	0.280	
Forward Transconductance ^a	g _{fs}	V _{DS} = 15 V, I _D = 1.9 A	N-Ch		5.4	S	
		V _{DS} = -15 V, I _D = -1.7 A	P-Ch		4.0		
Diode Forward Voltage ^a	V _{SD}	I _S = 1.0 A, V _{GS} = 0 V	N-Ch		0.77	1.2	V
		I _S = -1.0 A, V _{GS} = 0 V	P-Ch		-0.77	-1.2	
Dynamic^b							
Total Gate Charge	Q _g	N-Channel V _{DS} = 3.5 V, V _{GS} = 4.5 V, I _D = 0.3 A P-Channel V _{DS} = -3.5 V, V _{GS} = -4.5 V I _D = -0.3 A	N-Ch		1.7	3.5	nC
Gate-Source Charge	Q _{gs}		N-Ch		0.26		
Gate-Drain Charge	Q _{gd}		N-Ch		0.41		
Turn-On Delay Time	t _{d(on)}	N-Channel V _{DD} = 3.5 V, R _L = 11.5 Ω I _D ≅ 0.3 A, V _{GEN} = 4.5 V, R _G = 6 Ω P-Channel V _{DD} = -3.5 V, R _L = 11.5 Ω I _D ≅ -0.3 A, V _{GEN} = -4.5 V, R _G = 6 Ω	N-Ch		7.3	15	ns
Rise Time	t _r		P-Ch		6.0	15	
Turn-Off Delay Time	t _{d(off)}		N-Ch		10.0	20.0	
			P-Ch		10.0	20.0	
Fall Time	t _f		N-Ch		11.0	20.0	
			P-Ch		10.0	20.0	
Source-Drain Reverse Recovery Time	t _{rr}		N-Channel—I _F = 1.0 A, di/dt = 100 A/μs	N-Ch		31	
		P-Channel—I _F = -1.0 A, di/dt = 100 A/μs	P-Ch		35	60	

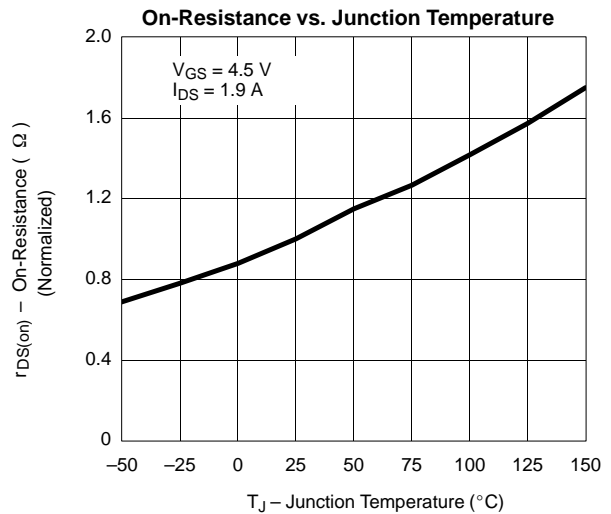
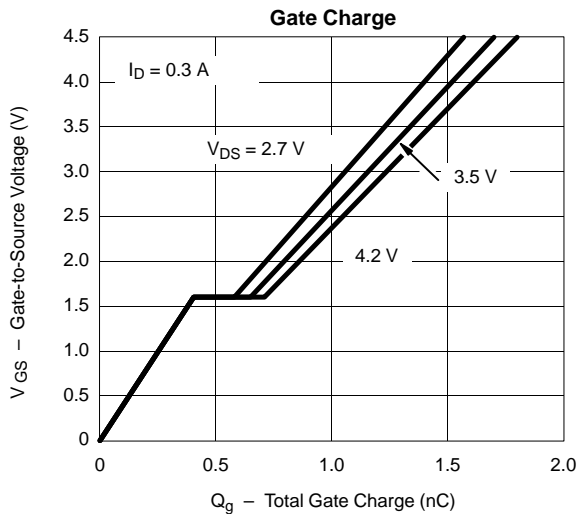
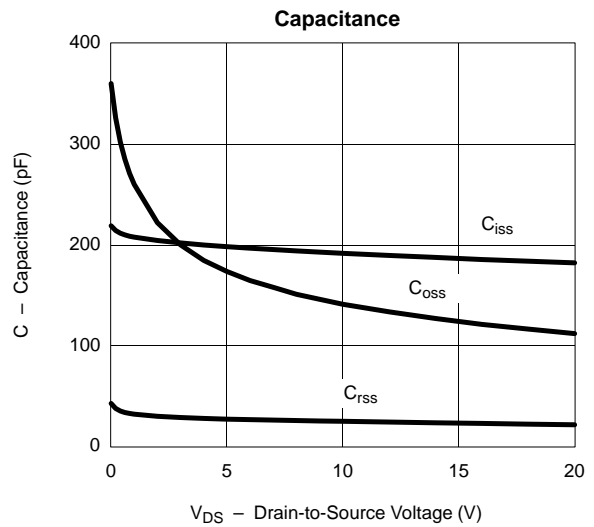
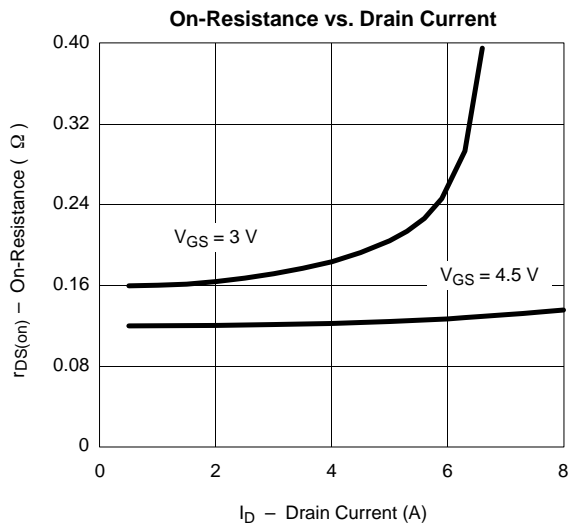
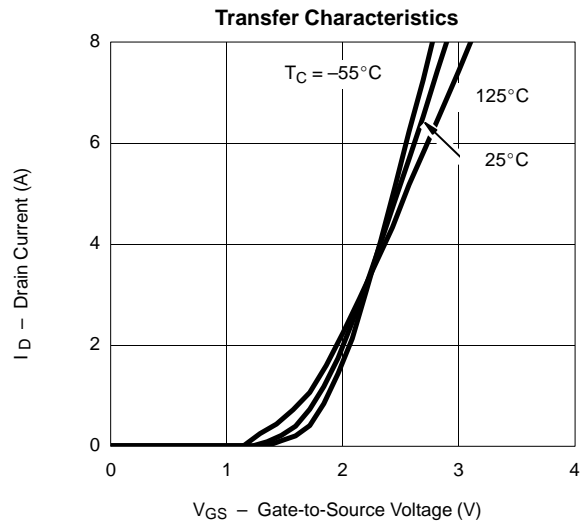
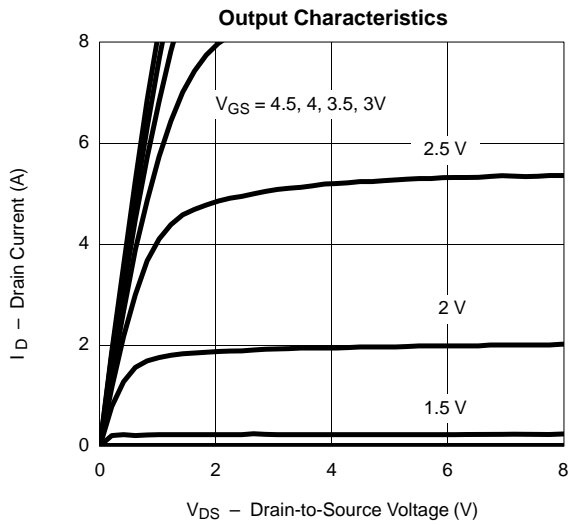
Notes

- a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.
- b. Guaranteed by design, not subject to production testing.

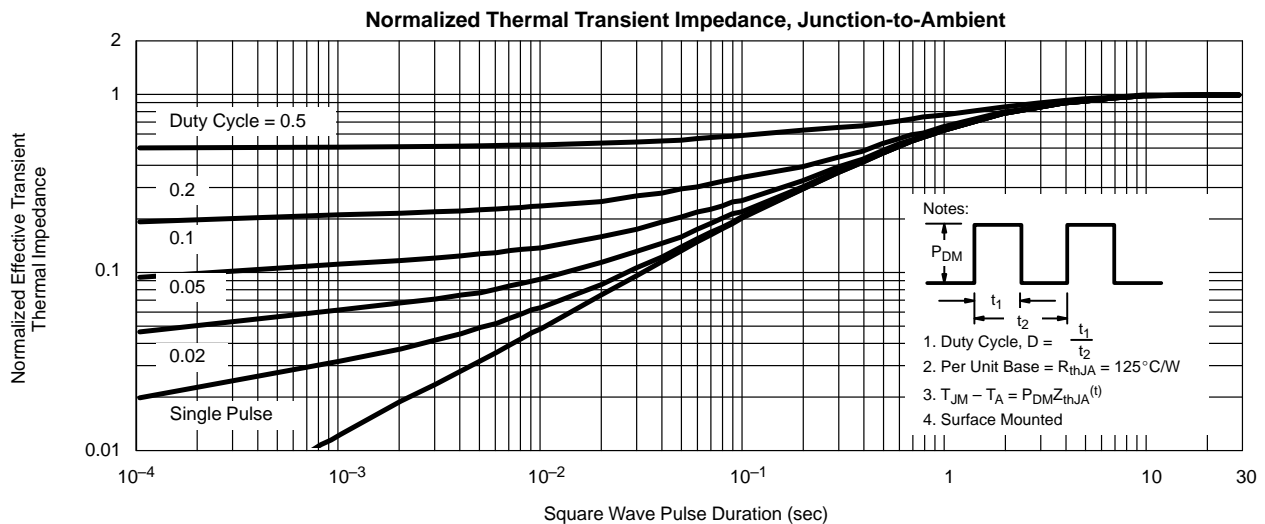
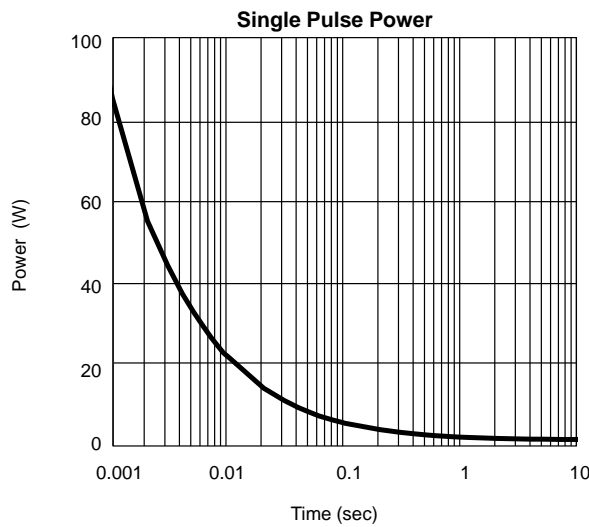
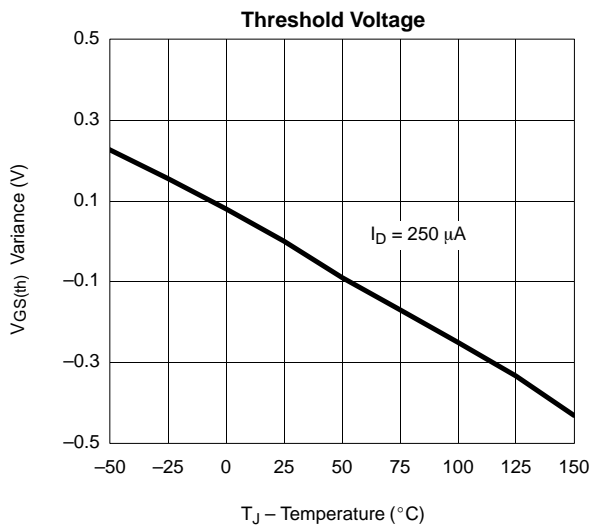
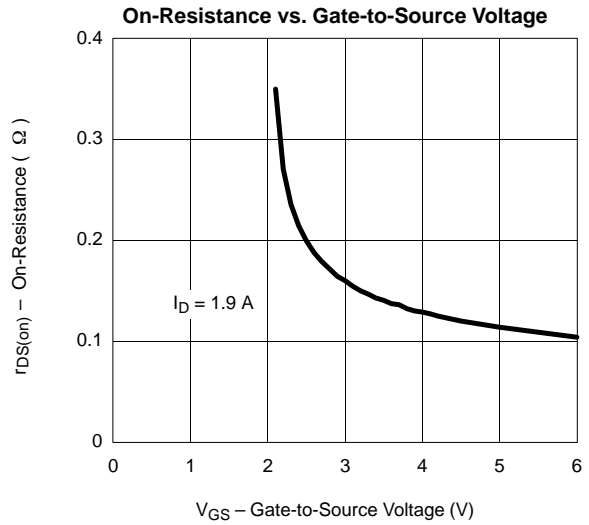
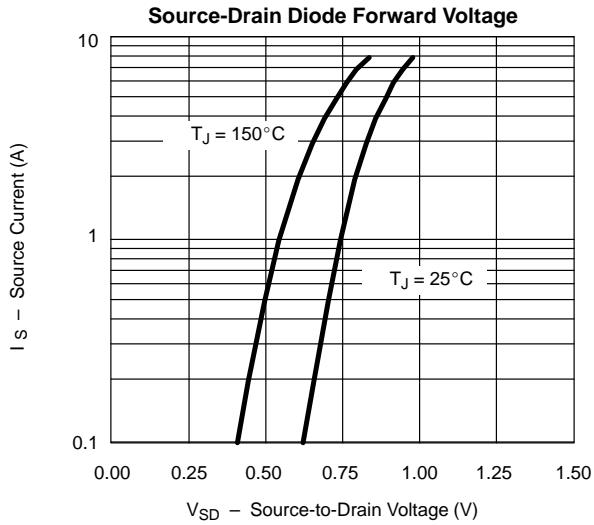


TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

N-CHANNEL



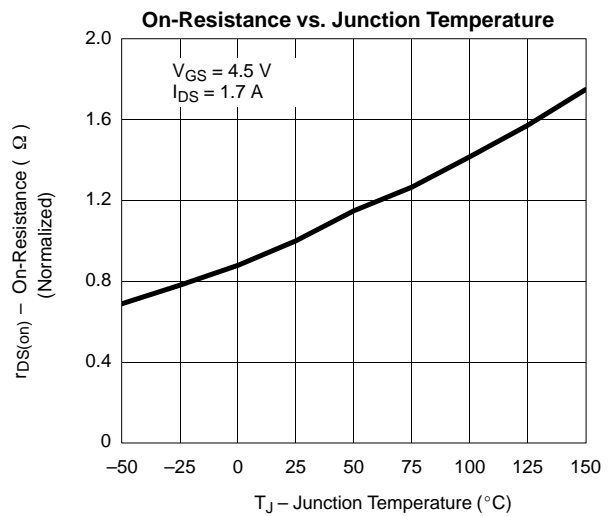
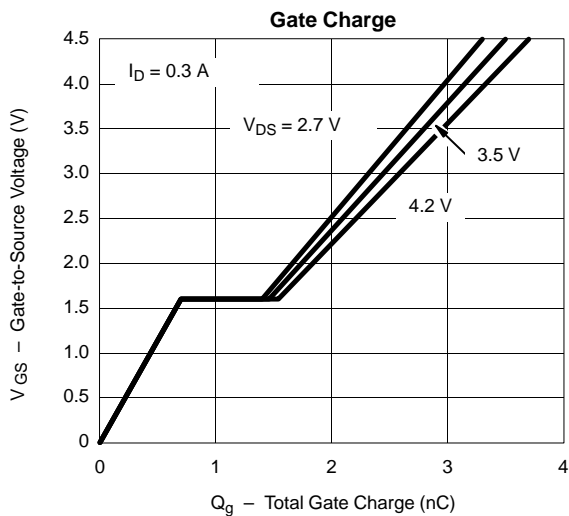
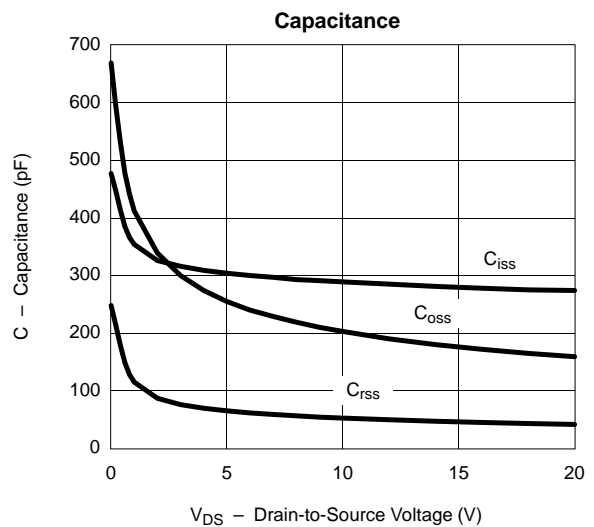
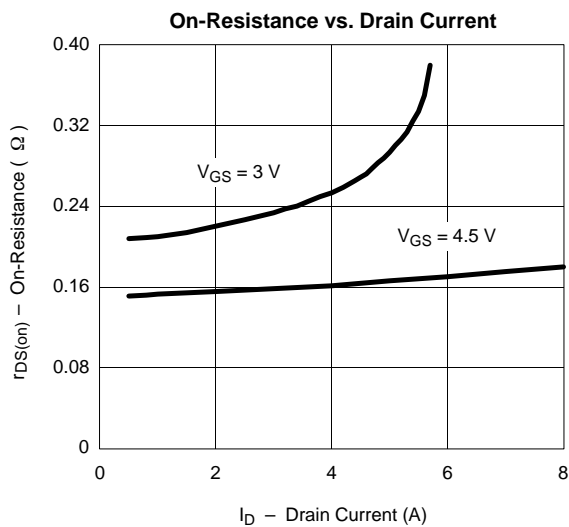
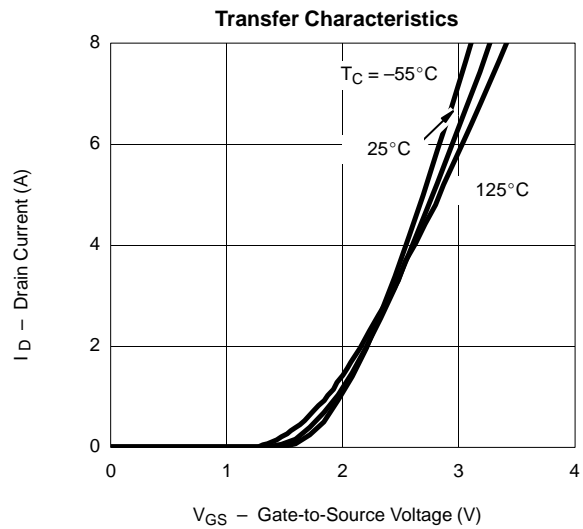
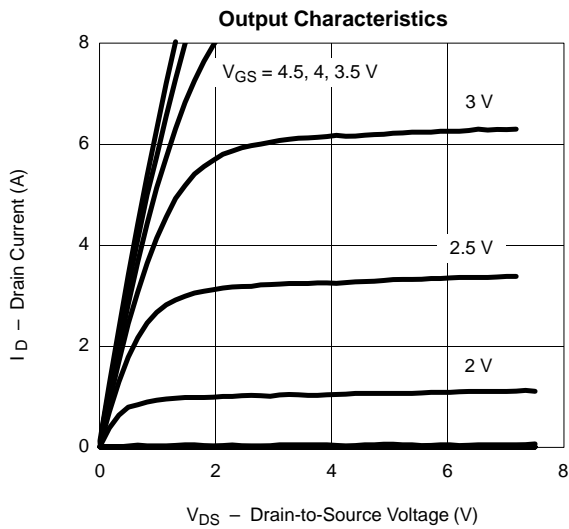
TYPICAL CHARACTERISTICS (25°C UNLESS NOTED) N-CHANNEL



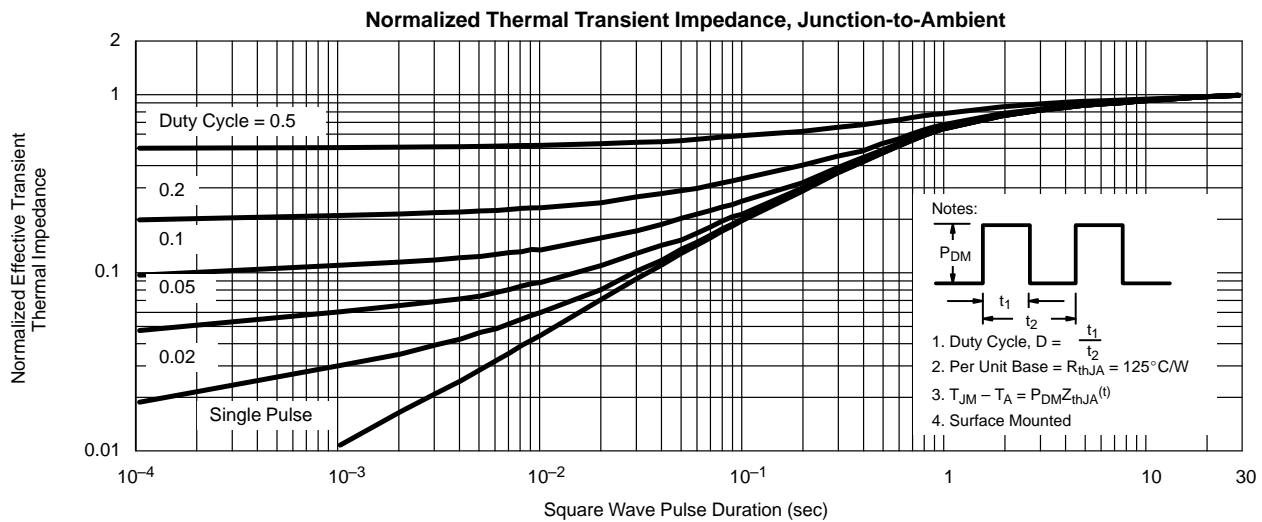
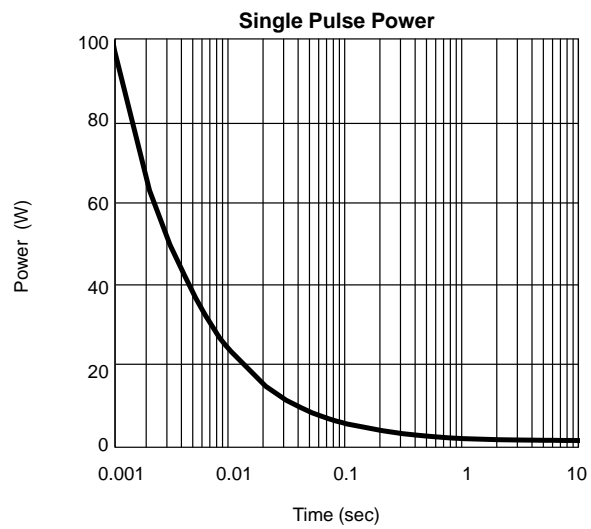
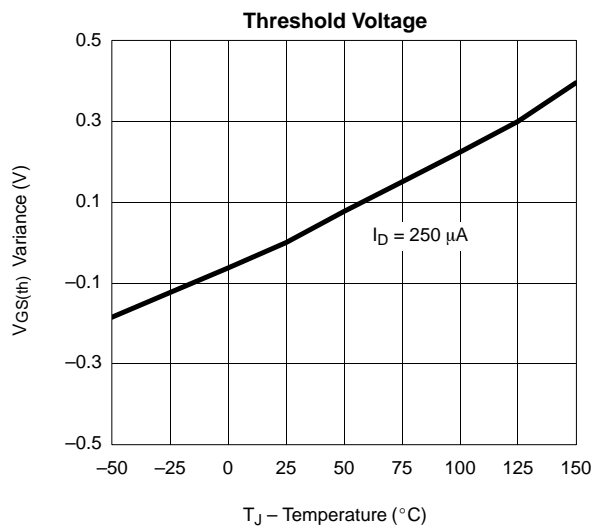
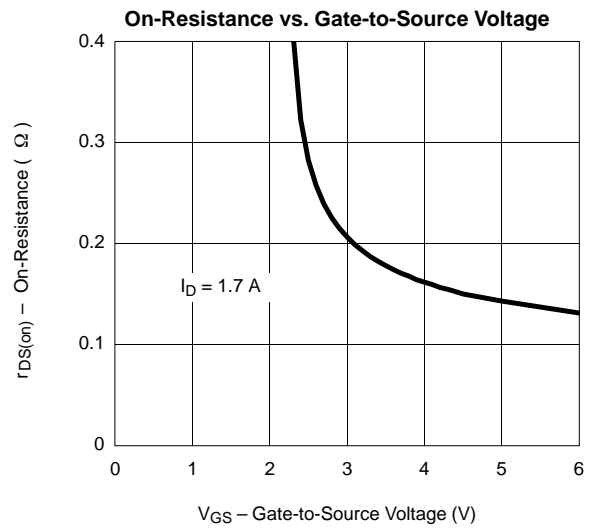
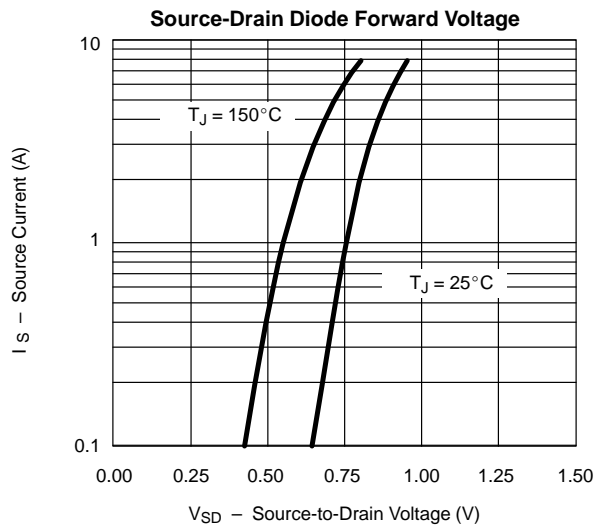


TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

P-CHANNEL



TYPICAL CHARACTERISTICS (25 °C UNLESS NOTED) P-CHANNEL





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