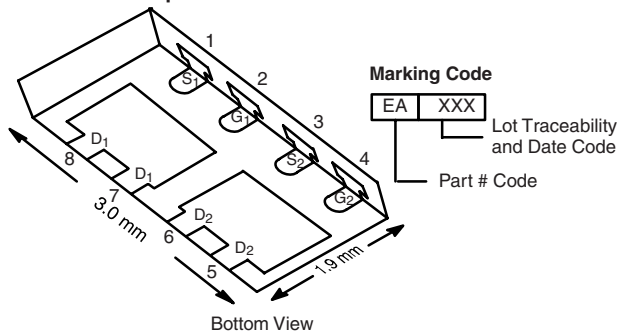


N- and P-Channel 20-V (D-S) MOSFET

PRODUCT SUMMARY				
	V _{DS}	R _{DS(on)} (Ω)	I _D (A) ^a	Q _g
N-Channel	20	0.039 at V _{GS} = 4.5 V	6	6 nc
		0.045 at V _{GS} = 2.5 V	6	
		0.055 at V _{GS} = 1.8 V	6	
P-Channel	- 20	0.072 at V _{GS} = - 4.5 V	- 6	5.5 nc
		0.100 at V _{GS} = - 2.5 V	- 6	
		0.131 at V _{GS} = - 18 V	- 6	

PowerPAK ChipFET Dual



Ordering Information: Si5517DU-T1-GE3 (Lead (Pb)-free and Halogen-free)

FEATURES

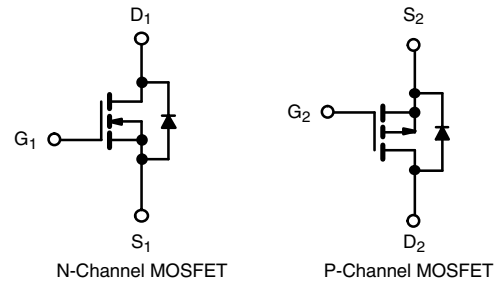
- Halogen-free
- TrenchFET[®] Power MOSFETs
- New Thermally Enhanced PowerPAK[®] ChipFET[®] Package
 - Small Footprint Area
 - Low On-Resistance
 - Thin 0.8 mm Profile



RoHS
COMPLIANT

APPLICATIONS

- Complementary MOSFET for Portable Devices
- Ideal for Buck-Boost Circuits



ABSOLUTE MAXIMUM RATINGS T _A = 25 °C, unless otherwise noted					
Parameter	Symbol	N-Channel	P-Channel	Unit	
Drain-Source Voltage	V _{DS}	20	- 20	V	
Gate-Source Voltage	V _{GS}	± 8			
Continuous Drain Current (T _J = 150 °C)	I _D	T _C = 25 °C	6 ^a	- 6 ^a	A
		T _C = 70 °C	6 ^a	- 6 ^a	
		T _A = 25 °C	7.2 ^{b, c}	- 4.6 ^{b, c}	
		T _A = 70 °C	5.8 ^{b, c}	- 3.7 ^{b, c}	
Pulsed Drain Current	I _{DM}	20	- 15		
Source-Drain Current Diode Current	I _S	T _C = 25 °C	6.9	- 6.9	
		T _A = 25 °C	1.9 ^{b, c}	- 1.9 ^{b, c}	
Maximum Power Dissipation	P _D	T _C = 25 °C	8.3	8.3	W
		T _C = 70 °C	5.3	5.3	
		T _A = 25 °C	2.3 ^{b, c}	2.3 ^{b, c}	
		T _A = 70 °C	1.5 ^{b, c}	1.5 ^{b, c}	
Operating Junction and Storage Temperature Range	T _J , T _{stg}	- 55 to 150		°C	
Soldering Recommendations (Peak Temperature) ^{d, e}		260			

THERMAL RESISTANCE RATINGS						
Parameter	Symbol	N-Channel		P-Channel		Unit
		Typ.	Max.	Typ.	Max.	
Maximum Junction-to-Ambient ^{b, f}	R _{thJA}	45	55	45	55	°C/W
Maximum Junction-to-Case (Drain)	R _{thJC}	12	15	12	15	

Notes:

- Based on T_C = 25 °C.
- Surface Mounted on 1" x 1" FR4 board.
- t = 5 s.
- See Solder Profile (<http://www.vishay.com/ppg?73257>). The PowerPAK ChipFET is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.
- Maximum under Steady State conditions is 105 °C/W for both channels.

SPECIFICATIONS $T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted							
Parameter	Symbol	Test Conditions	Min.	Typ. ^a	Max.	Unit	
Static							
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0\text{ V}, I_D = 1\text{ mA}$	N-Ch	20		V	
		$V_{GS} = 0\text{ V}, I_D = -1\text{ mA}$	P-Ch	-20			
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	$I_D = 250\text{ }\mu\text{A}$	N-Ch		17	mV/ $^\circ\text{C}$	
		$I_D = -250\text{ }\mu\text{A}$	P-Ch		-20		
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$	$I_D = 250\text{ }\mu\text{A}$	N-Ch		-2.6		
		$I_D = -250\text{ }\mu\text{A}$	P-Ch		2.4		
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	N-Ch	0.4	1	V	
		$V_{DS} = V_{GS}, I_D = -250\text{ }\mu\text{A}$	P-Ch	-0.4	-1		
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 8\text{ V}$	N-Ch		100	nA	
			P-Ch		-100		
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 20\text{ V}, V_{GS} = 0\text{ V}$	N-Ch		1	μA	
		$V_{DS} = -20\text{ V}, V_{GS} = 0\text{ V}$	P-Ch		-1		
		$V_{DS} = 20\text{ V}, V_{GS} = 0\text{ V}, T_J = 55\text{ }^\circ\text{C}$	N-Ch		10		
		$V_{DS} = -20\text{ V}, V_{GS} = 0\text{ V}, T_J = 55\text{ }^\circ\text{C}$	P-Ch		-10		
On-State Drain Current ^b	$I_{D(on)}$	$V_{DS} \leq 5\text{ V}, V_{GS} = 4.5\text{ V}$	N-Ch	20		A	
		$V_{DS} \leq -5\text{ V}, V_{GS} = -4.5\text{ V}$	P-Ch	-15			
Drain-Source On-State Resistance ^b	$R_{DS(on)}$	$V_{GS} = 4.5\text{ V}, I_D = 4.4\text{ A}$	N-Ch		0.032	0.039	Ω
		$V_{GS} = -4.5\text{ V}, I_D = -3.3\text{ A}$	P-Ch		0.060	0.072	
		$V_{GS} = 2.5\text{ V}, I_D = 4.1\text{ A}$	N-Ch		0.037	0.045	
		$V_{GS} = -2.5\text{ V}, I_D = -2.8\text{ A}$	P-Ch		0.083	0.100	
		$V_{GS} = 1.8\text{ V}, I_D = 1.8\text{ A}$	N-Ch		0.0455	0.055	
		$V_{GS} = -1.8\text{ V}, I_D = -0.76\text{ A}$	P-Ch		0.108	0.131	
Forward Transconductance ^b	g_{fs}	$V_{DS} = 10\text{ V}, I_D = 4.4\text{ A}$	N-Ch		22	S	
		$V_{DS} = -10\text{ V}, I_D = -3.3\text{ A}$	P-Ch		9		
Dynamic^a							
Input Capacitance	C_{iss}	N-Channel $V_{DS} = 10\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$	N-Ch		520	pF	
			P-Ch		455		
Output Capacitance	C_{oss}	P-Channel $V_{DS} = -10\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$	N-Ch		100		
			P-Ch		105		
Reverse Transfer Capacitance	C_{rss}	N-Channel $V_{DS} = -10\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$	N-Ch		60		
			P-Ch		65		
Total Gate Charge	Q_g	$V_{DS} = 10\text{ V}, V_{GS} = 8\text{ V}, I_D = 4.4\text{ A}$	N-Ch		10.5	16	nC
		$V_{DS} = -10\text{ V}, V_{GS} = -8\text{ V}, I_D = -4.6\text{ A}$	P-Ch		9.1	14	
		N-Channel $V_{DS} = 10\text{ V}, V_{GS} = 4.5\text{ V}, I_D = 4.4\text{ A}$	N-Ch		6	9	
			P-Ch		5.5	8.5	
Gate-Source Charge	Q_{gs}	P-Channel $V_{DS} = -10\text{ V}, V_{GS} = -4.5\text{ V}, I_D = -1.8\text{ A}$	N-Ch		0.91		
			P-Ch		0.75		
Gate-Drain Charge	Q_{gd}	N-Channel $V_{DS} = -10\text{ V}, V_{GS} = -4.5\text{ V}, I_D = -1.8\text{ A}$	N-Ch		0.7		
			P-Ch		1.5		
Gate Resistance	R_g	$f = 1\text{ MHz}$	N-Ch		1.9	Ω	
			P-Ch		8		



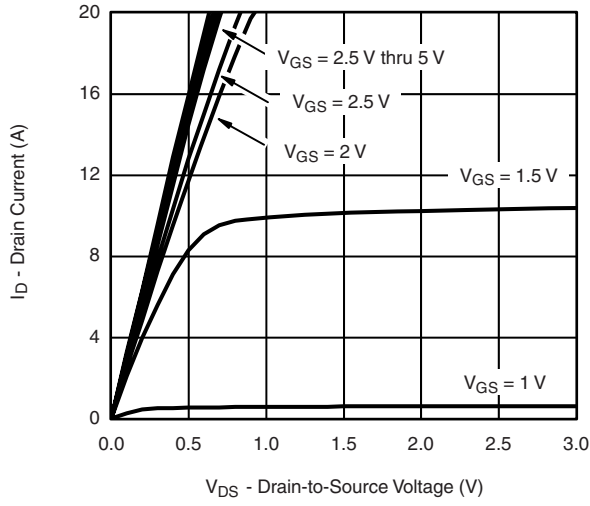
SPECIFICATIONS $T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted							
Parameter	Symbol	Test Conditions		Min.	Typ. ^a	Max.	Unit
Dynamic^a							
Turn-On Delay Time	$t_{d(on)}$	N-Channel $V_{DD} = 10\text{ V}, R_L = 2.8\ \Omega$ $I_D \cong 3.6\text{ A}, V_{GEN} = 4.5\text{ V}, R_g = 1\ \Omega$	N-Ch		20	30	ns
			P-Ch		8	15	
Rise Time	t_r		N-Ch		65	100	
			P-Ch		35	55	
Turn-Off Delay Time	$t_{d(off)}$	P-Channel $V_{DD} = -10\text{ V}, R_L = 2.7\ \Omega$ $I_D \cong -3.7\text{ A}, V_{GEN} = -4.5\text{ V}, R_g = 1\ \Omega$	N-Ch		40	60	
			P-Ch		40	60	
Fall Time	t_f		N-Ch		10	15	
			P-Ch		55	85	
Turn-On Delay Time	$t_{d(on)}$	N-Channel $V_{DD} = 10\text{ V}, R_L = 2.8\ \Omega$ $I_D \cong 3.6\text{ A}, V_{GEN} = 8\text{ V}, R_g = 1\ \Omega$	N-Ch		5	10	
			P-Ch		5	10	
Rise Time	t_r		N-Ch		12	20	
			P-Ch		15	25	
Turn-Off Delay Time	$t_{d(off)}$	P-Channel $V_{DD} = -10\text{ V}, R_L = 2.7\ \Omega$ $I_D \cong -3.7\text{ A}, V_{GEN} = -8\text{ V}, R_g = 1\ \Omega$	N-Ch		26	40	
			P-Ch		30	45	
Fall Time	t_f		N-Ch		8	15	
			P-Ch		45	70	
Drain-Source Body Diode Characteristics							
Continuous Source-Drain Diode Current	I_S	$T_C = 25\text{ }^\circ\text{C}$	N-Ch			6.9	A
			P-Ch			-6.9	
Pulse Diode Forward Current ^a	I_{SM}		N-Ch			20	A
			P-Ch			-15	
Body Diode Voltage	V_{SD}	$I_S = 1.2\text{ A}, V_{GS} = 0\text{ V}$	N-Ch		0.8	1.2	V
		$I_S = -1.0\text{ A}, V_{GS} = 0\text{ V}$	P-Ch		-0.8	-1.2	
Body Diode Reverse Recovery Time	t_{rr}	N-Channel $I_F = 1.2\text{ A}, di/dt = 100\text{ A}/\mu\text{s}, T_J = 25\text{ }^\circ\text{C}$	N-Ch		45	70	ns
			P-Ch		30	60	
Body Diode Reverse Recovery Charge	Q_{rr}	N-Channel $I_F = 1.2\text{ A}, di/dt = 100\text{ A}/\mu\text{s}, T_J = 25\text{ }^\circ\text{C}$	N-Ch		21	32	nC
			P-Ch		15	30	
Reverse Recovery Fall Time	t_a	P-Channel $I_F = -1\text{ A}, di/dt = 100\text{ A}/\mu\text{s}, T_J = 25\text{ }^\circ\text{C}$	N-Ch		29		ns
			P-Ch		11		
Reverse Recovery Rise Time	t_b		N-Ch		16		
			P-Ch		19		

Notes:

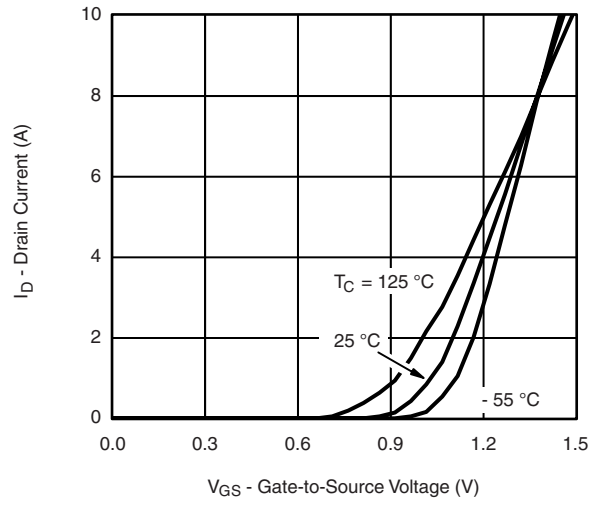
- a. Guaranteed by design, not subject to production testing.
- b. Pulse test; pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

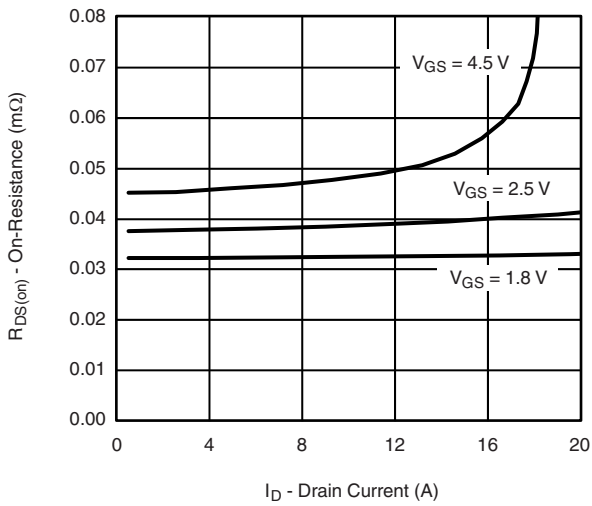
N-CHANNEL TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



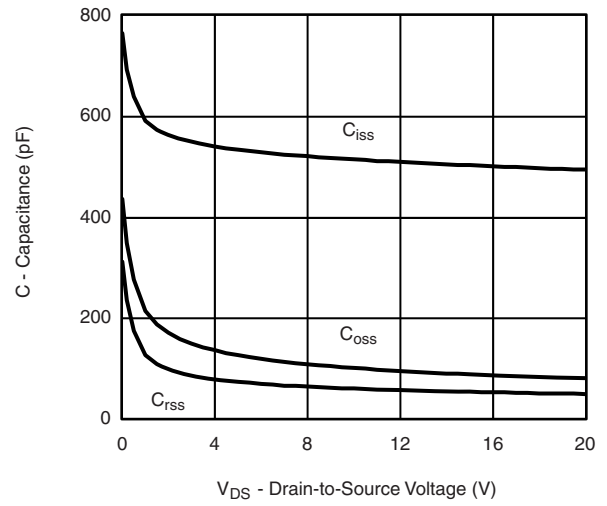
Output Characteristics



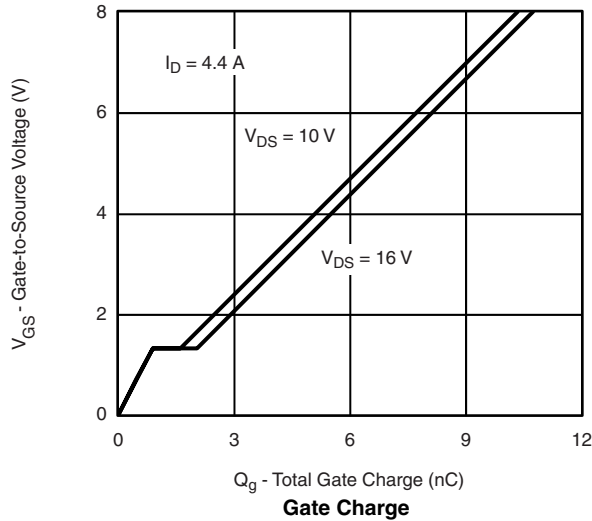
Transfer Characteristics



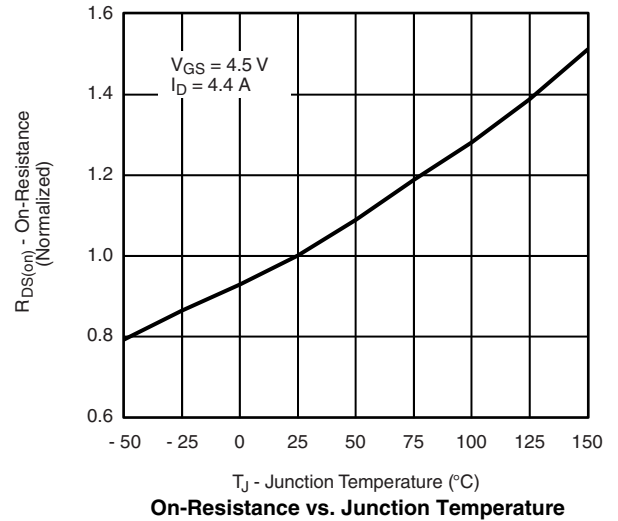
On-Resistance vs. Drain Current and Gate Voltage



Capacitance

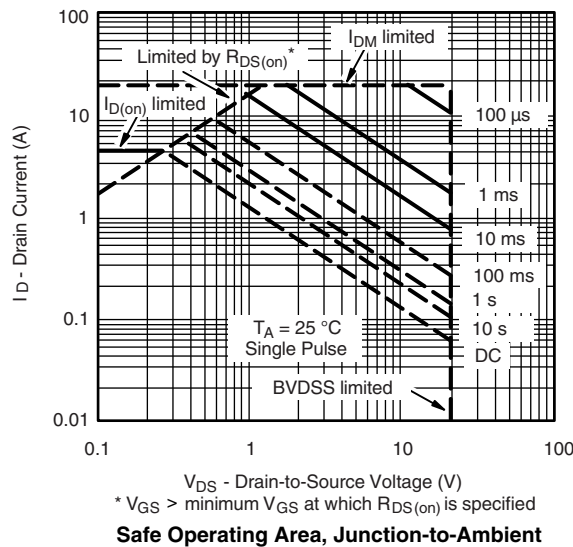
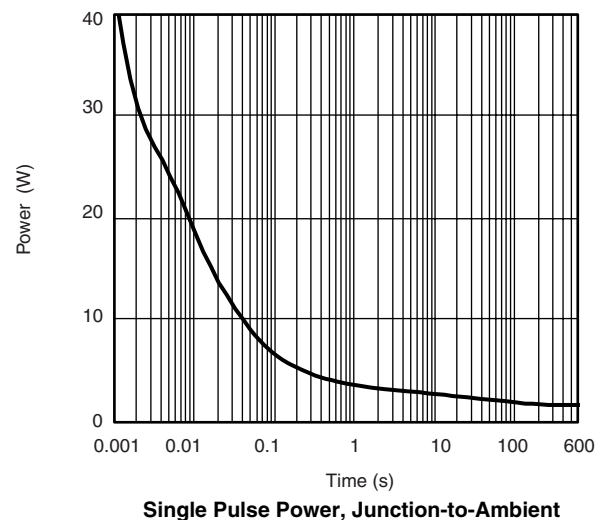
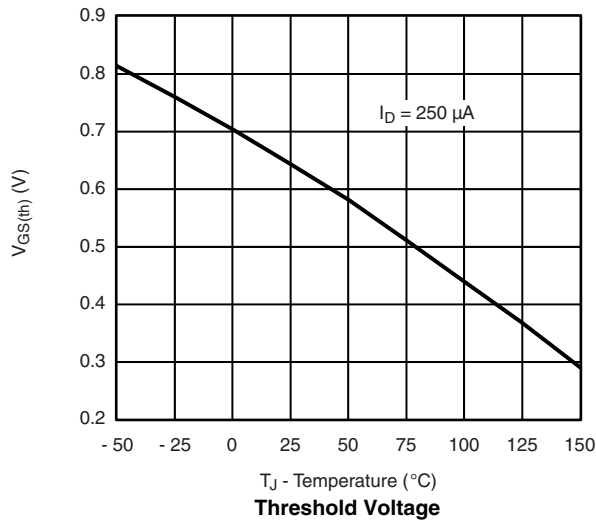
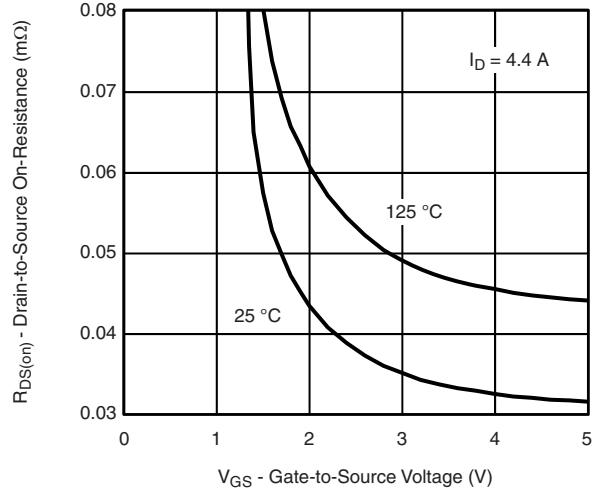
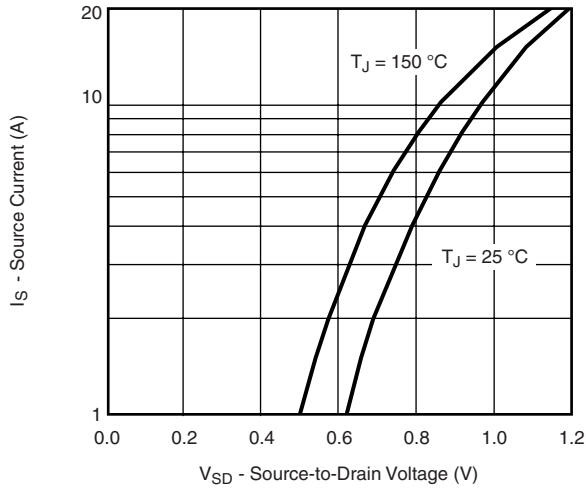


Gate Charge

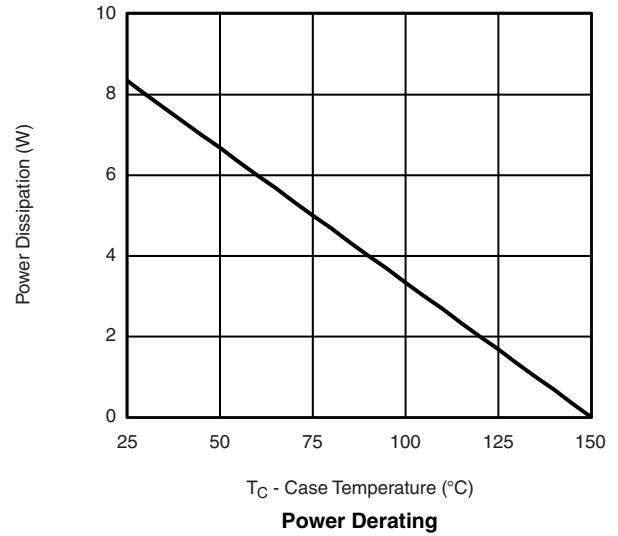
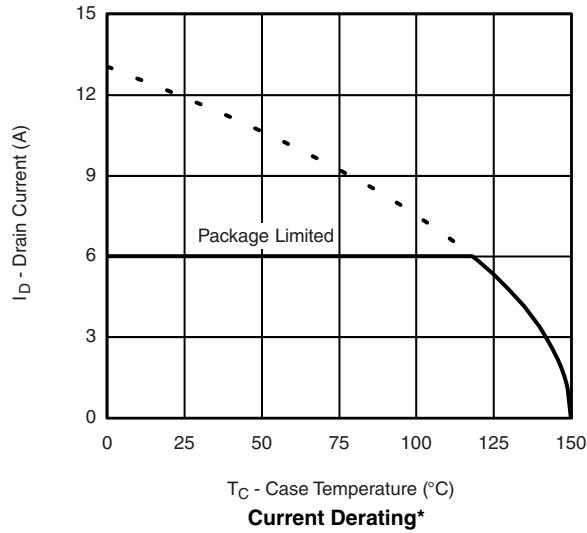


On-Resistance vs. Junction Temperature

N-CHANNEL TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

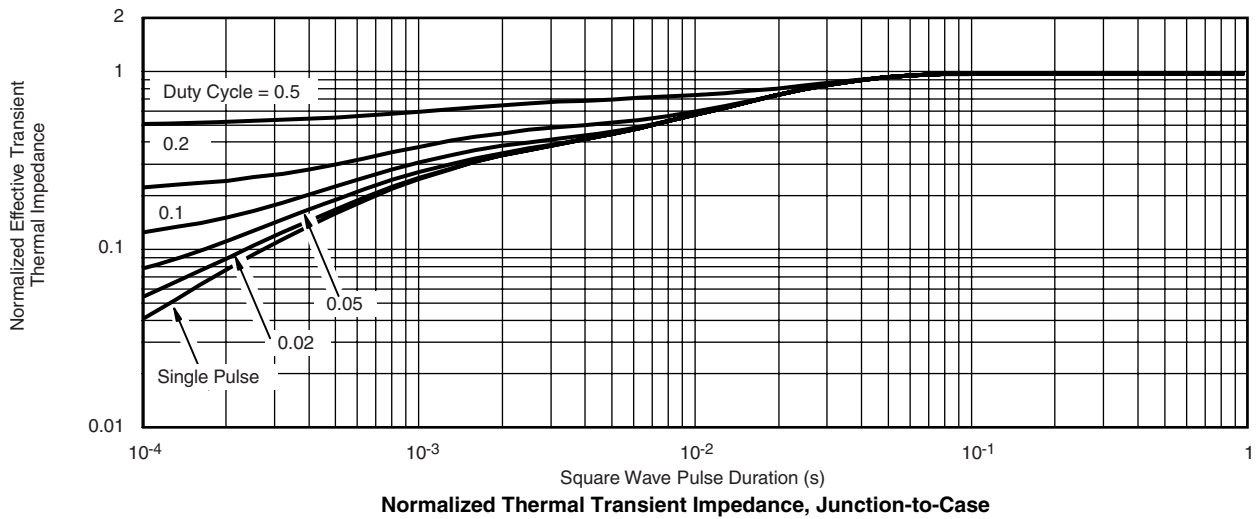
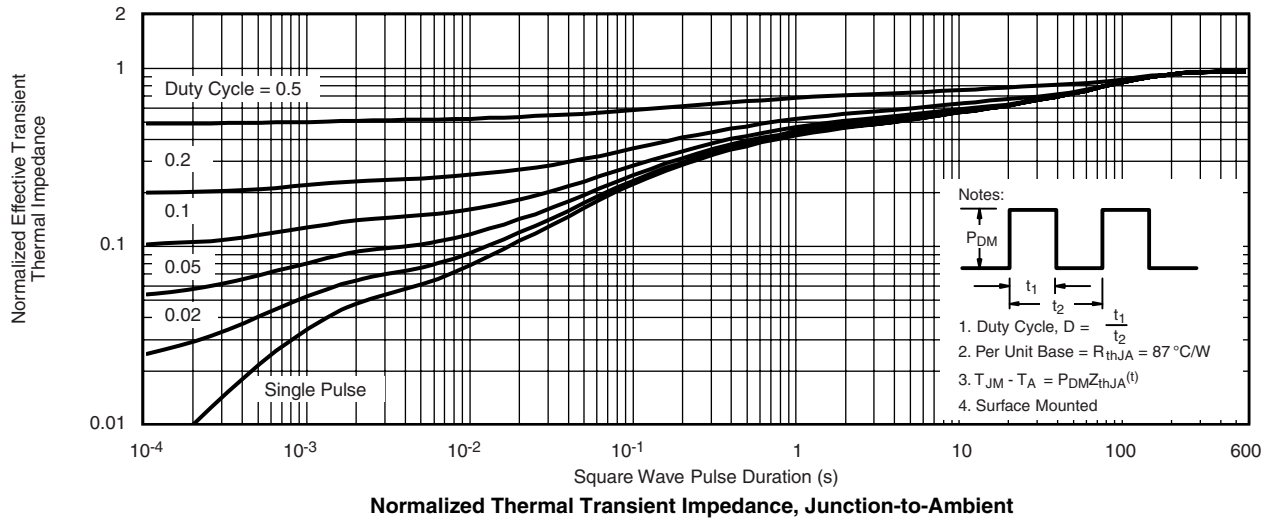


N-CHANNEL TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

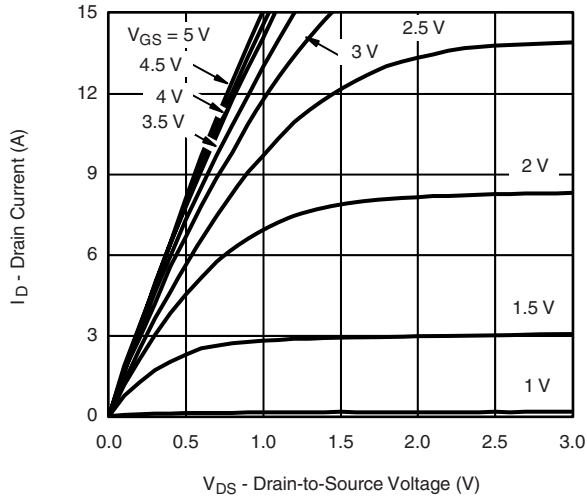


* The power dissipation P_D is based on $T_{J(max)} = 150$ °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

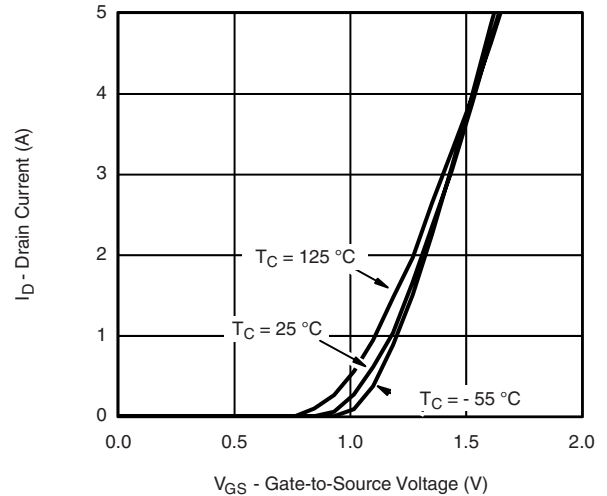
N-CHANNEL TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



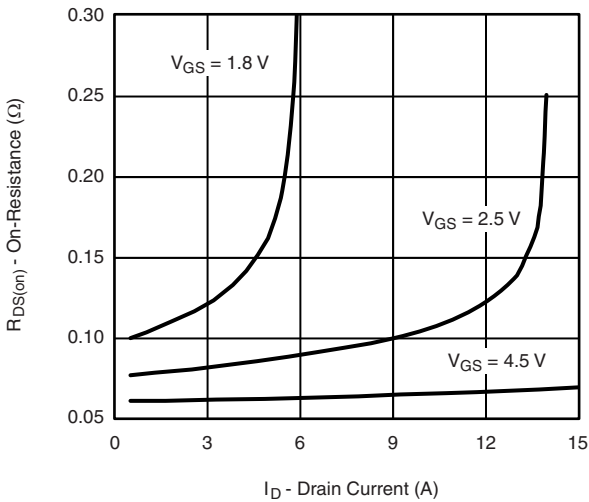
P-CHANNEL TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



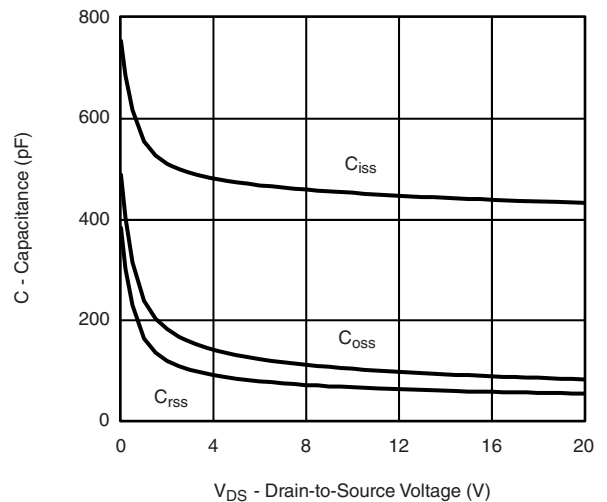
Output Characteristics



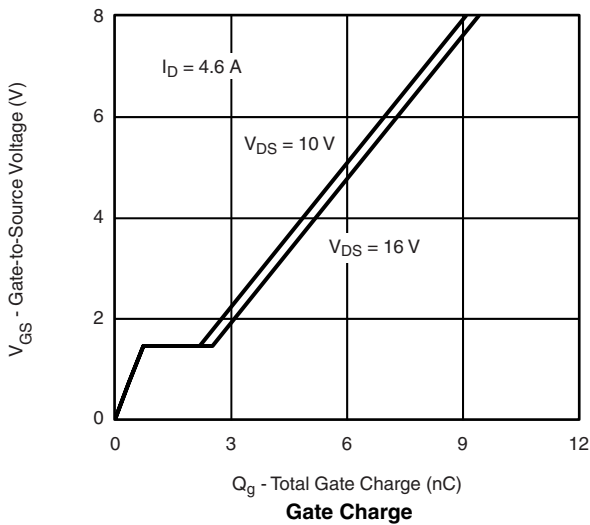
Transfer Characteristics



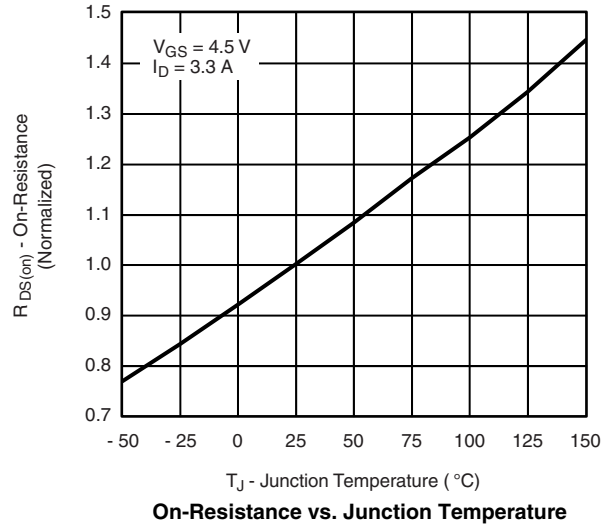
On-Resistance vs. Drain Current and Gate Voltage



Capacitance

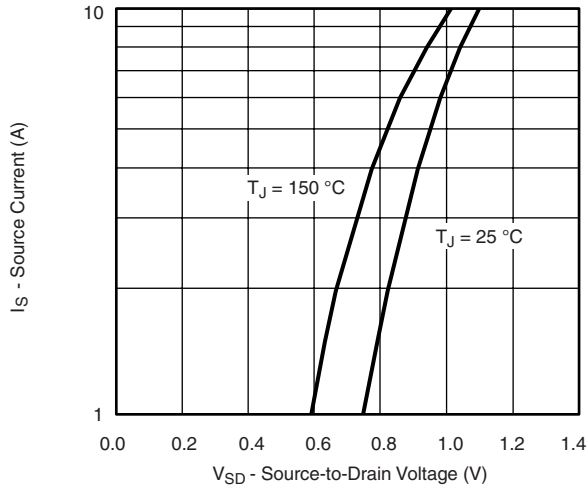


Gate Charge

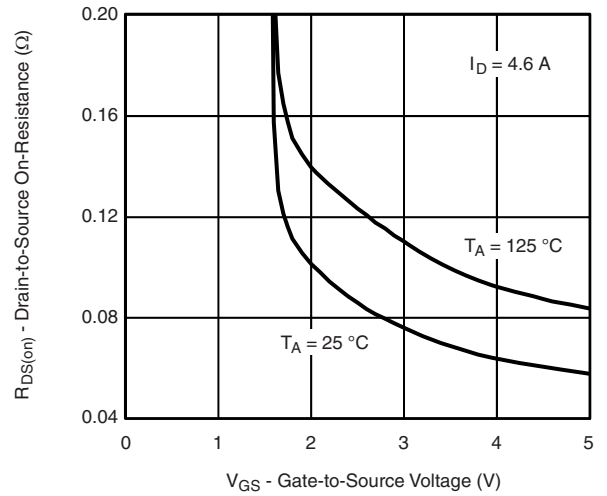


On-Resistance vs. Junction Temperature

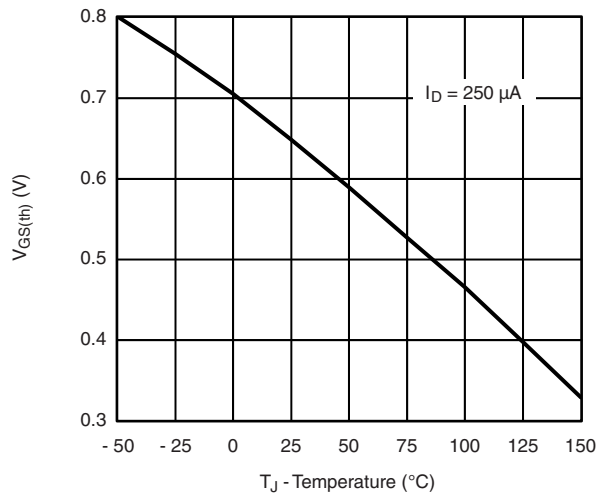
P-CHANNEL TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



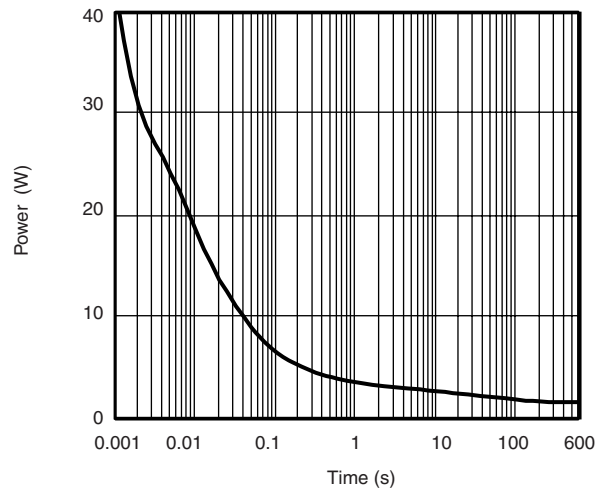
Source-Drain Diode Forward Voltage



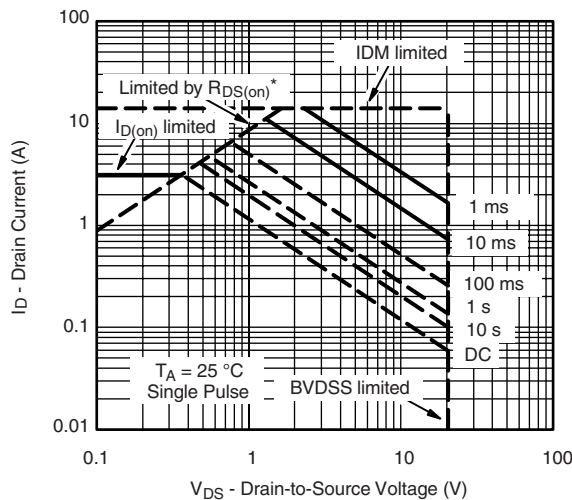
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



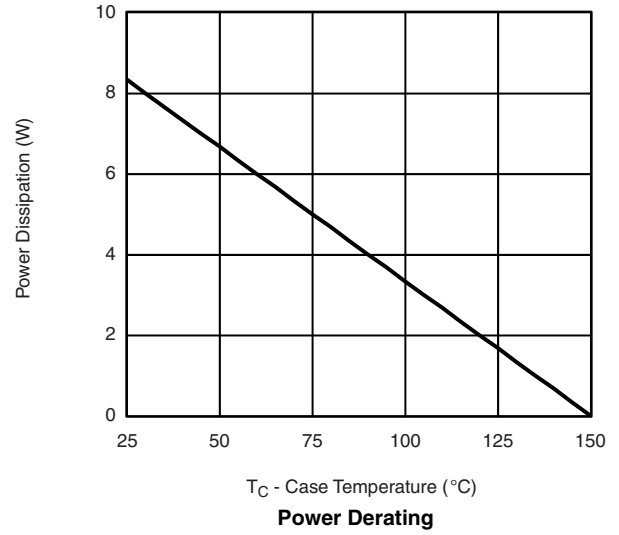
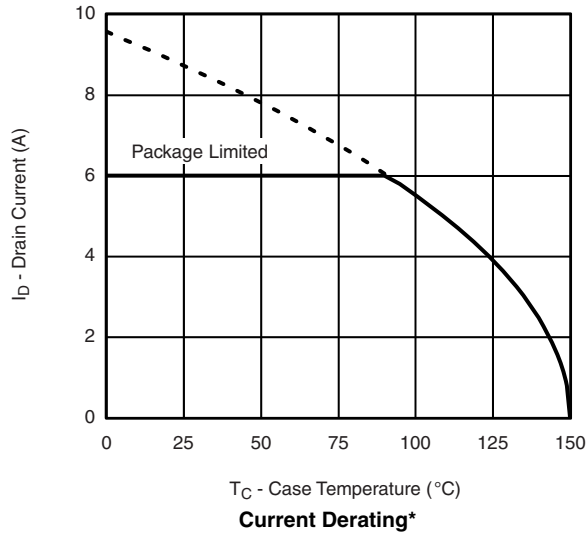
Single Pulse Power, Junction-to-Ambient



* $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified

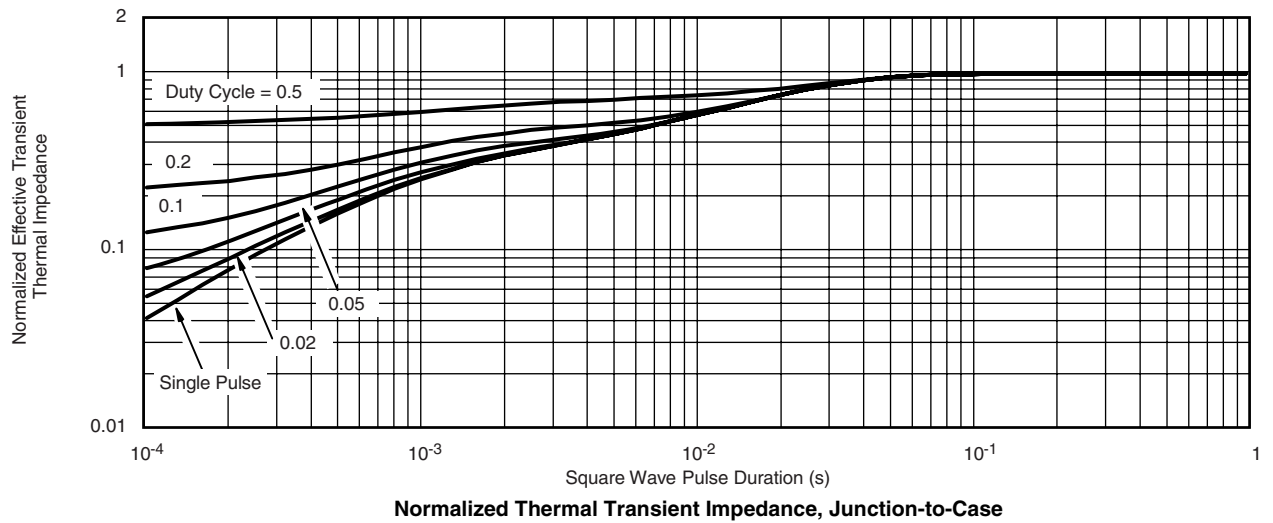
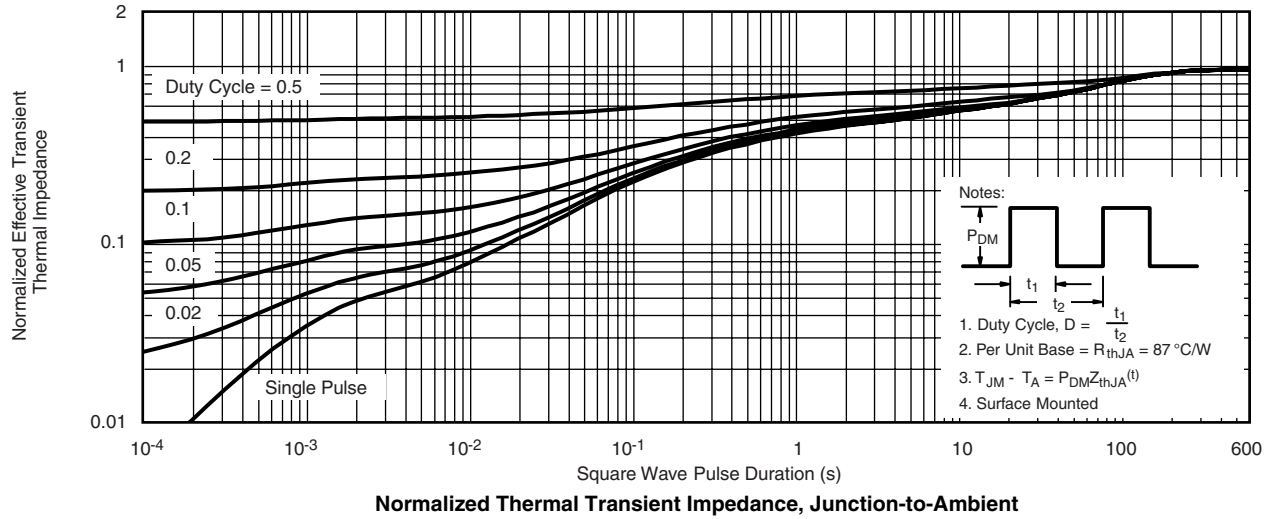
Safe Operating Area, Junction-to-Case

P-CHANNEL TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



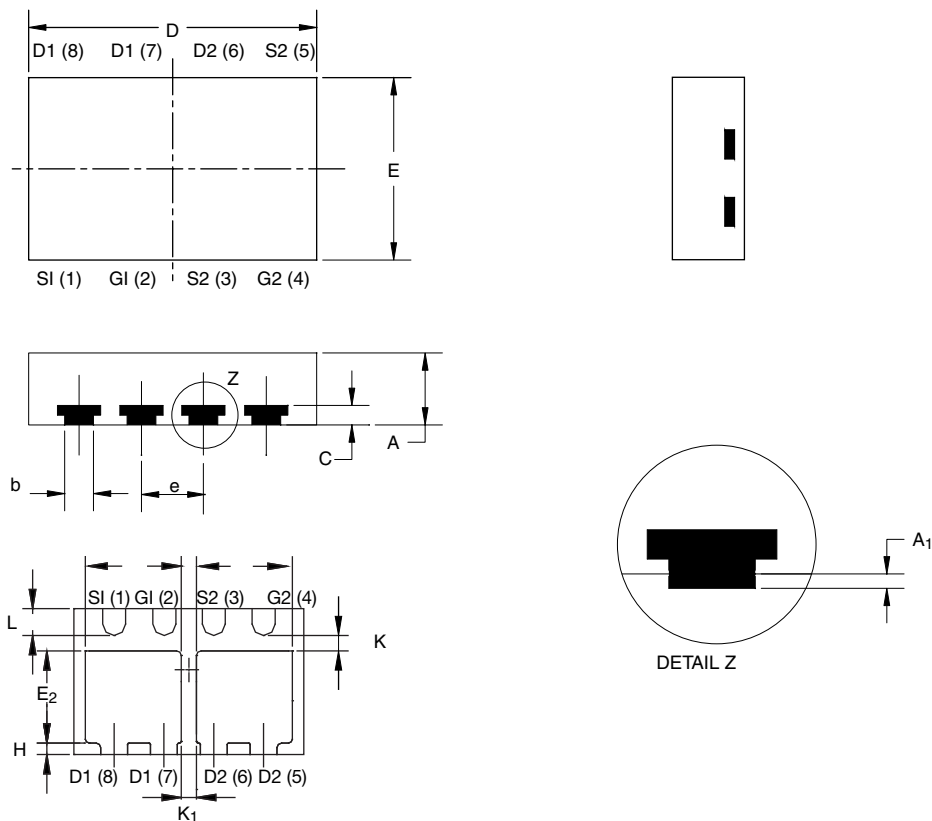
* The power dissipation P_D is based on $T_{J(max)} = 150$ °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

P-CHANNEL TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see <http://www.vishay.com/ppg?73529>.

PowerPAK® ChipFET® DUAL PAD



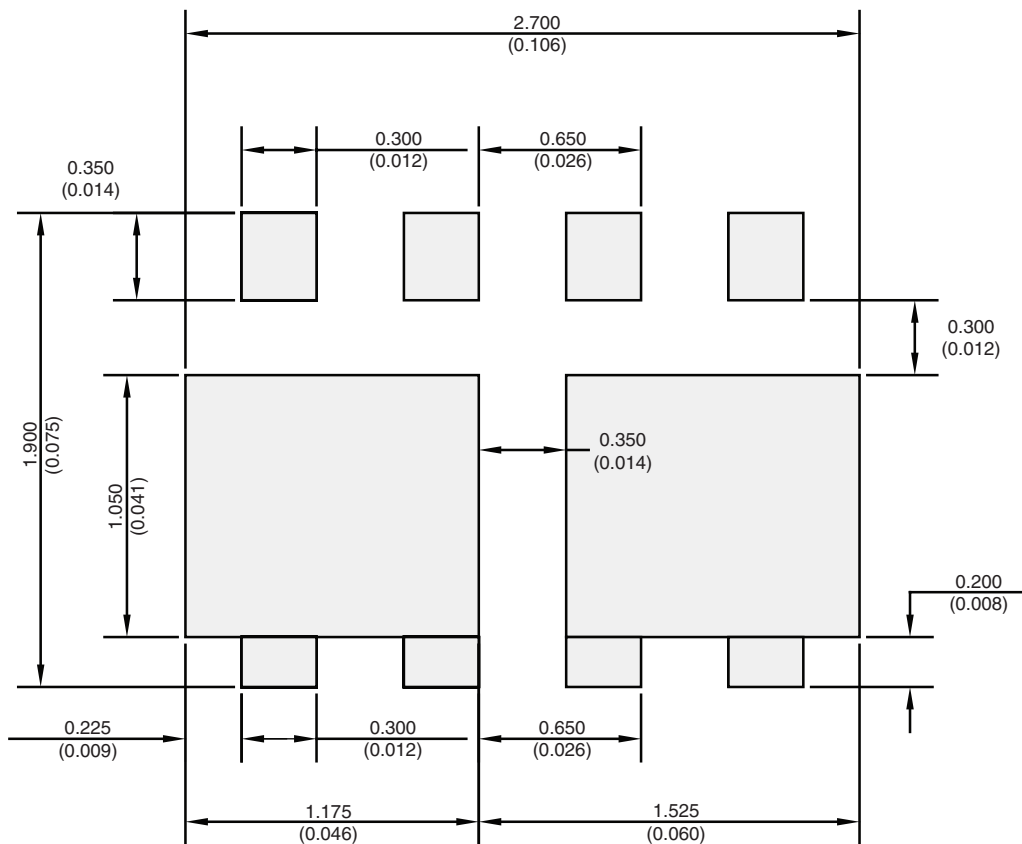
Backside view of dual pad

DIM.	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.85	0.028	0.030	0.033
A ₁	0	-	0.05	0	-	0.002
b	0.25	0.30	0.35	0.010	0.012	0.014
C	0.15	0.20	0.25	0.006	0.008	0.010
D	2.92	3.00	3.08	0.115	0.118	0.121
D ₂	1.07	1.20	1.32	0.042	0.047	0.052
E	1.82	1.90	1.98	0.072	0.075	0.078
E ₂	0.92	1.05	1.17	0.036	0.041	0.046
e	0.65 BSC			0.026 BSC		
H	0.15	0.20	0.25	0.006	0.008	0.010
K	0.20	-	-	0.008	-	-
K ₁	0.20	-	-	0.008	-	-
L	0.30	0.35	0.40	0.012	0.014	0.016

ECN: C10-0618-Rev. C, 19-Jul-09

DWG: 5940

RECOMMENDED MINIMUM PADS FOR PowerPAK® ChipFET® Dual



Recommended Minimum Pads
Dimensions in mm/(Inches)

Note: This is Flipped Mirror Image
Pin #1 Location is Top Left Corner



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