超低相位噪声，12输出JESD204B 时钟发生器 Si5380 数据表

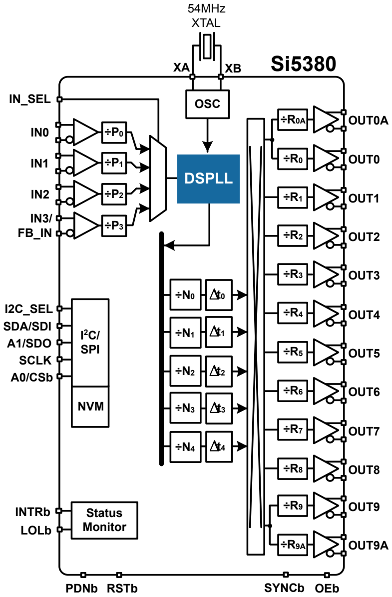
Si5380 是一款基于整数 (M/N) 的高性能时钟发生器，适用于要求最高级别集成度和相位噪声性能的小型基站应用。 Si5380 采用 Silicon Laboratories 的第四代 DSPLL 技术，将频率合成与抖动衰减完美地融入至一个高度集成的数字解决方案中，无需配置外部 VCXO 和环路滤波器元件。 低成本的固定频率晶体能够在自由运行和保持模式下提供频率稳定性。 这种全数字解决方案提供出色的性能，具有极强的抗外部电路板干扰（比如电源噪声）的能力。

应用

- JESD204B 时钟生成
- 远端射频单元 (RRU)、远端存取网路 (RAN)、微微蜂窝基站、小型基站
- 无线基站（3G、GSM、W-CDMA、4G/LTE、LTE-A）
- 远端射频头 (RRH)、无线中继器、无线回程
- 数据转换采样时钟（ADC、DAC、DDC、DUC）

主要特点

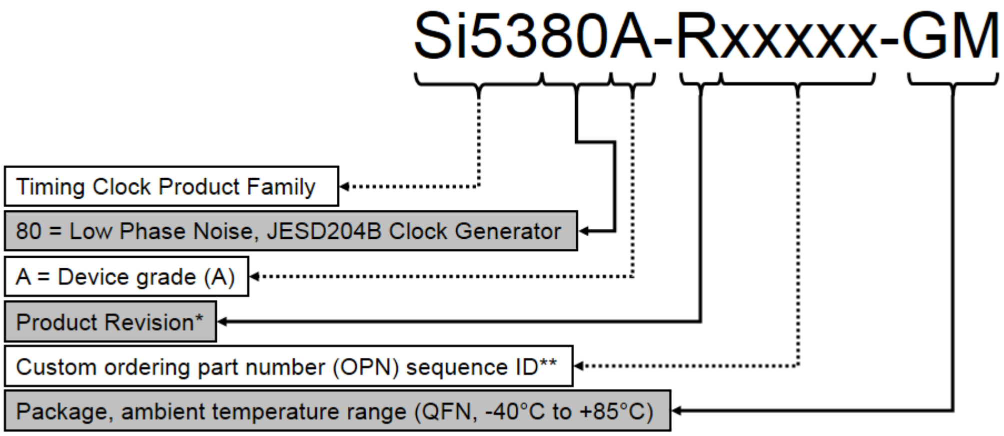
- 借助于数字频率合成，无需配置外部 VCXO 和模拟环路滤波器元件
- 支持 JESD204B 时钟： DCLK 和 SYSREF
- 输入频率范围：
  - 差分： 10 MHz – 750 MHz
  - LVCMOS： 10 MHz – 250 MHz
- 输出频率范围：
  - 差分： 480 kHz – 1.47456 GHz
  - LVCMOS： 480 kHz – 250 MHz



1. 功能

- 借助于数字频率合成，无需配置外部 VCXO 和模拟环路滤波器元件
- 支持 JESD204B 时钟： DCLK 和 SYSREF
- 输入频率范围：
  - 差分： 10 MHz – 750 MHz
  - LVCMOS： 10 MHz – 250 MHz
- 输出频率范围：
  - 差分：高达 1.47456 GHz
  - LVCMOS：高达 250 MHz
- 出色的抖动性能：
  - 70 fs 典型值 (12 kHz – 20 MHz)
- 相位本底噪声： –159 dBc/Hz
- 杂散性能： –103 dBc 最大值（相对于 122.88 MHz 载波）
- 可配置的输出：
  - 信号摆动： 200 至 3200 mVpp
  - 与 LVDS 和 LVPECL 兼容
  - 3.3、2.5 或 1.8 V LVCMOS
- 输出至输出偏移： 20 ps（典型值，与 N 进制分频器相同）
- 可调节的输出至输出延迟： 68 ps/阶进，±128 阶进
- 可选的零延迟模式
- 独立的输出时钟电源引脚： 3.3、2.5 或 1.8 V
- 内核电压：
  - VDD = 1.8 V ±5%
  - VDDA = 3.3 V ±5%
- 自动化自由运行、锁定和保持模式
- 可选的数字化回路带宽 0.1 Hz 至 4 kHz
- 输入时钟无缝切换
- 状态监控（LOS、OOF、LOL）
- 串行接口： I2C 或 SPI，在线可编程，具有非易失性 OTP 存储器
- ClockBuilder^{TM} Pro 软件工具能够简化设备配置
- 4 种输入、12 种输出、64 QFN
- 温度范围： –40 至 +85 ° C
- 无铅、符合 RoHS-6

2. Ordering Guide



*See Ordering Guide table for current product revision
** 5 digits; assigned by ClockBuilder Pro

Table 2.1. Ordering Guide

Ordering Part Number	Number of Outputs	Output Clock Frequency Range	Package	RoHS-6, Pb-Free	Temperature Range
Si5380A-B-GM	12	480 kHz—1.47456 GHz	64-Lead 9x9 mm QFN	Yes	–40 to +85 °C
Si5380-EVB			Evaluation Board		

Note:

1. Add an “R” at the end of the device to denote tape and reel options.
2. Custom, factory pre-programmed devices are available. Ordering part numbers are assigned by ClockBuilder Pro. Part number format is: Si5380A-Bxxxxx-GM, where “xxxxx” is a unique numerical sequence representing the pre-programmed configuration.

3. Functional Description

The Si5380 is a high performance clock generator that is capable of synthesizing up to 10 unique integer related frequencies at any of the device's 12 outputs. The output clocks can be generated in free-run mode or synchronized to any one of the four external inputs. Clock generation is provided by Silicon Laboratories' 4th generation DSPLL technology which combines frequency synthesis and jitter attenuation in a highly integrated digital solution that eliminates the need for external VCXO and loop filter components. The Si5380 device is fully configurable using the I2C or SPI serial interface and has in-circuit programmable non-volatile memory.

3.1 Frequency Configuration

The DSPLL provides the synthesis for generating the output clock frequencies which are synchronous to the selected input clock frequency or free-running XTAL. It consists of a phase detector, a programmable digital loop filter, a high-performance ultra-low phase noise analog 15 GHz VCO, and a user configurable feedback divider. An internal oscillator (OSC) provides the DSPLL with a stable low-noise clock source for frequency synthesis and for maintaining frequency accuracy in the free-run or holdover modes. The oscillator simply requires an external, low cost 54 MHz fundamental mode crystal to operate. No other external components are required for frequency generation. A key feature of this DSPLL is that it provides immunity to external noise coupling from power supplies and other uncontrolled noise sources that normally exist on printed circuit boards.

3.1.1 Si5380 LTE Frequency Configuration

The device's frequency configuration is fully programmable through the serial interface and can also be stored in non-volatile memory. The combination of flexible integer dividers and a high frequency VCO allows the device to generate multiple output clock frequencies for applications that require ultra-low phase noise and spurious performance. At the core of the device are the N dividers which determine the number of unique frequencies that can be generated from the device. The table below shows a list of possible output frequencies for LTE applications. The Si5380's DSPLL core can generate up to five unique frequencies. These frequencies are distributed to the output dividers using a configurable crosspoint mux. The R dividers allow further division for up to 10 unique integer-ratio related frequencies on the Si5380. The ClockBuilder Pro software utility provides a simple means of automatically calculating the optimum divider values (P, M, N and R) for the frequencies listed in the table below.

Table 3.1. Example of Possible LTE Clock Frequencies

Fin (MHz)[1]	LTE Device Clock Frequencies Fout (MHz)[2]
15.36	15.36
19.20	19.20
30.72	30.72
38.40	38.40
61.44	61.44
76.80	76.80
122.88	122.88
153.60	153.60
184.32	184.32
245.76	245.76
307.20	307.20
368.64	368.64
491.52	491.52
614.40	614.40
737.28	737.28
—	983.04
—	1228.80
—	1474.56

Fin (MHz)[1]	LTE Device Clock Frequencies Fout (MHz)[2]

Note:

1. The Si5380 locks to any one of the frequencies listed in the Fin column and generates LTE device clock frequencies.
2. R output dividers allow other frequencies to be generated. These are useful for applications like JESD204B SYSREF clocks.

3.1.2 Si5380 Configuration for JESD204B Clock Generation

The Si5380 can be used as a high performance, fully integrated JEDEC JESD204B jitter cleaner while eliminating the need for discrete VCXO and loop filter components. The Si5380 supports JESD204B subclass 0 and subclass 1 clocking by providing both device clocks (DCLK) and system reference clocks (SYSREF). The 12 clock outputs can be independently configured as device clocks or SYSREF clocks to drive JESD204B converters, FPGAs, or other logic devices. The Si5380 will clock up to four JESD204B targets using four or more DCLKs and four SYSREF clocks with adjustable delay.Each DCLK is grouped with a SYSREF clock in this configuration.If SYSREF clocking is implemented in external logic, then the Si5380 will clock up to 12 JESD204B targets.Not limited to JESD204B applications, each of the 12 outputs is individually configurable as a high performance output for traditional clocking applications. An example of a JESD204B frequency configuration is shown in the figure below. In this case, the N dividers determine the device clock frequency and the R dividers provide the divided SYSREF clock which is used as the lower frequency frame clock. The N divider path also includes a configurable delay path (Δt) for controlling deterministic latency. The example shows a configuration where all the device clocks are controlled by a single delay path (Δt0) while the SYSREF clocks each have their own independent delay paths (Δt1 – Δt4), though other combinations are also possible. Delay is programmable in steps of 68 ps in the range of ±128 steps (±8.6 ns). See the 3.5.15 Output Skew Control (Δt_0 - Δt_4) section for details on skew control. The SYSREF clock is always periodic and can be controlled (on/off) without glitches by enabling or disabling its output through register writes.

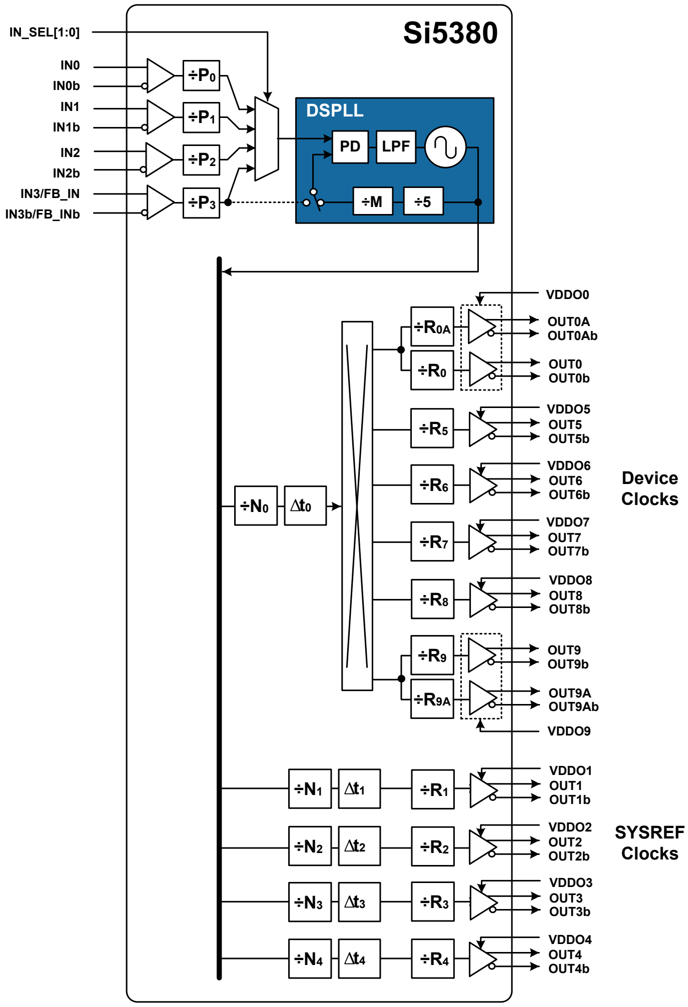


Figure 3.1. Example Divider Configuration for Generating JESD204B Subclass 1 Clocks

3.1.3 DSPLL Loop Bandwidth

The DSPLL loop bandwidth determines the amount of input clock jitter attenuation. Register configurable DSPLL loop bandwidth settings in the range of 0.1 Hz to 100 Hz are available for selection. The DSPLL will always remain stable with less than 0.1 dB of peaking regardless of the DSPLL loop bandwidth selection.

3.1.4 Fastlock Feature

Selecting a low DSPLL loop bandwidth (e.g., 1 Hz) will generally lengthen the lock acquisition time. The fastlock feature allows setting a temporary fastlock loop bandwidth that is used during the lock acquisition process. Higher fastlock loop bandwidth settings will enable the DSPLL to lock faster. Once lock acquisition has completed, the DSPLL's loop bandwidth will automatically revert to the DSPLL Loop Bandwidth setting. Fastlock loop bandwidth settings in the range of 100 Hz to 4 kHz are available for selection. The fastlock feature can be enabled or disabled by register configuration.

3.1.5 Modes of Operation

Once initialization is complete, the Si5380 operates in one of four modes: Free-run Mode, Lock Acquisition Mode, Locked Mode, or Holdover Mode. A state diagram showing the modes of operation is shown in the figure below. The following sections describe each of these modes in greater detail.

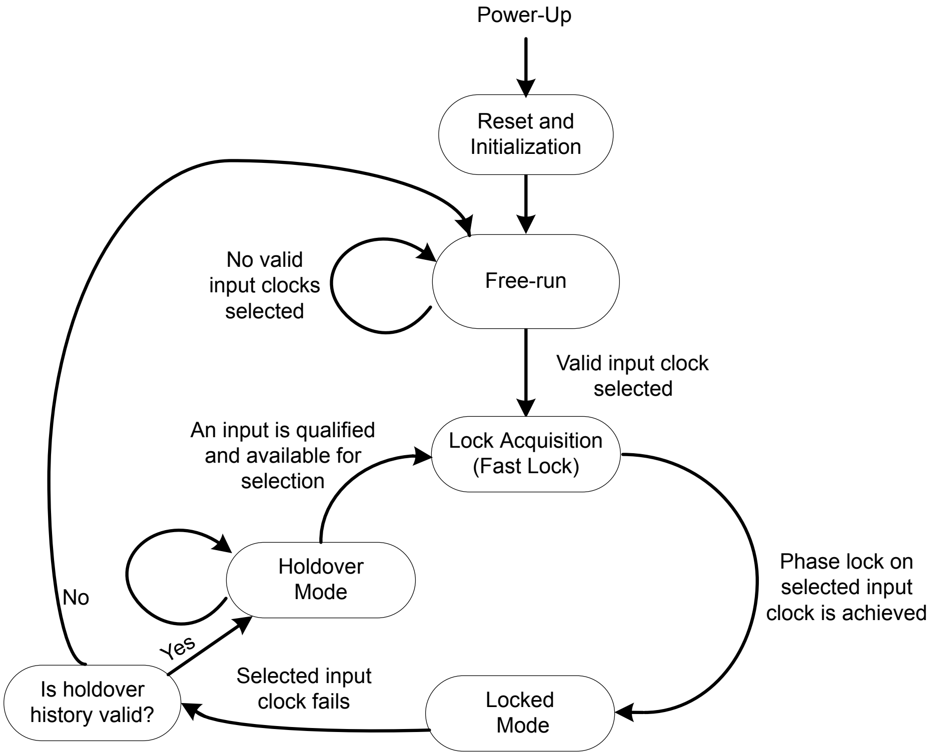


Figure 3.2. Modes of Operation

3.1.6 Initialization and Reset

When power is applied, the device begins an initialization period where it downloads default register values and configuration data from NVM and performs other initialization tasks. Communicating with the device through the serial interface is possible once this initialization period is complete. No clocks will be generated until the initialization is complete. There are two types of resets available. A hard reset is functionally similar to a device power-up. All registers will be restored to the values stored in NVM and all circuits, including the serial interface, will be restored to their initial state. A hard reset is initiated using the RSTb pin or by asserting the hard reset bit. A soft reset bypasses the NVM download. It is simply used to initiate register configuration changes.

3.1.7 Freerun Mode

Once power is applied to the Si5380 and initialization is complete, the device will automatically enter freerun mode. Output clocks will be generated on the outputs with their configured frequencies. The frequency accuracy of the generated output clocks in freerun mode is dependent on the frequency accuracy of the external crystal or reference clock on the XA/XB pins. For example, if the crystal frequency is ±100 ppm, then all the output clocks will be generated at their configured frequency ±100 ppm in freerun mode. Any change or drift of the crystal frequency or external reference on the XA/XB pins will be tracked at the output clock frequencies.

3.1.8 Lock Acquisition

If a valid input clock is selected for synchronization, the DSPLL will automatically start the lock acquisition process. If the fast lock feature is enabled, the DSPLL will acquire lock using the Fastlock Loop Bandwidth setting and then transition to the DSPLL Loop Bandwidth setting when lock acquisition is complete. During lock acquisition the outputs will generate a clock that follows the VCO frequency change as it pulls-in to the input clock frequency.

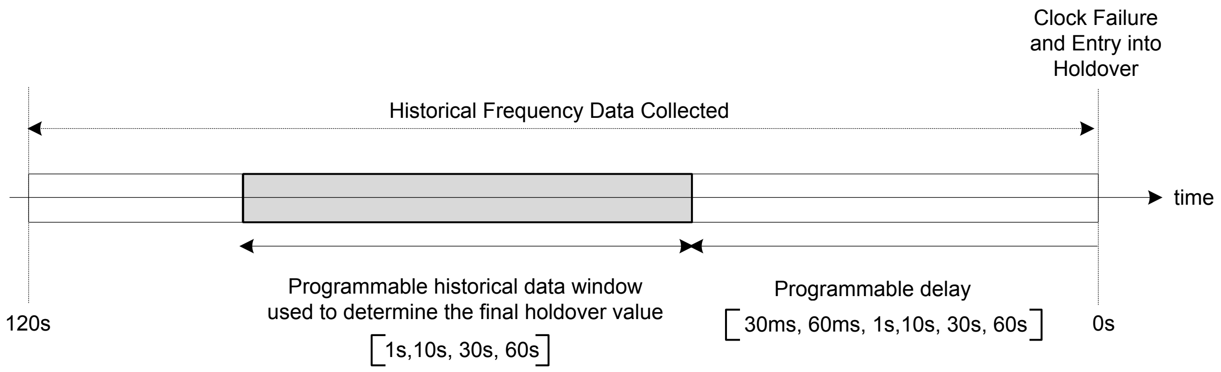
3.1.9 Locked Mode

Once lock is achieved, the Si5380 will generate output clocks that are both frequency and phase locked to the input clock. The DSPLL will provide jitter attenuation of the input clock using the selected DSPLL loop bandwidth. At this point, any XTAL frequency drift outside of the loop bandwidth will not affect the output frequencies. When lock is achieved, the LOLb pin will output a logic high level. The LOL status bit and LOLb status pin will also indicate that the DSPLL is locked. See the 3.4.6 LOL Detection section for more details on LOLb detection time.

3.1.10 Holdover Mode

The DSPLL will automatically enter holdover mode when the selected input clock becomes invalid and no other valid input clocks are available for selection. The DSPLL uses an averaged input clock frequency as its final holdover frequency to minimize the disturbance of the output clock phase and frequency when an input clock suddenly fails. The holdover circuit stores up to 120 seconds of historical frequency data while the DSPLL is locked to a valid clock input. The final averaged holdover frequency value is calculated from a programmable window within the stored historical frequency data. Both the window size and the delay are programmable as shown in the figure below. The window size determines the amount of holdover frequency averaging. The delay value allows ignoring frequency data that may be corrupt just before the input clock failure.

Figure 3.3. Programmable Holdover Window

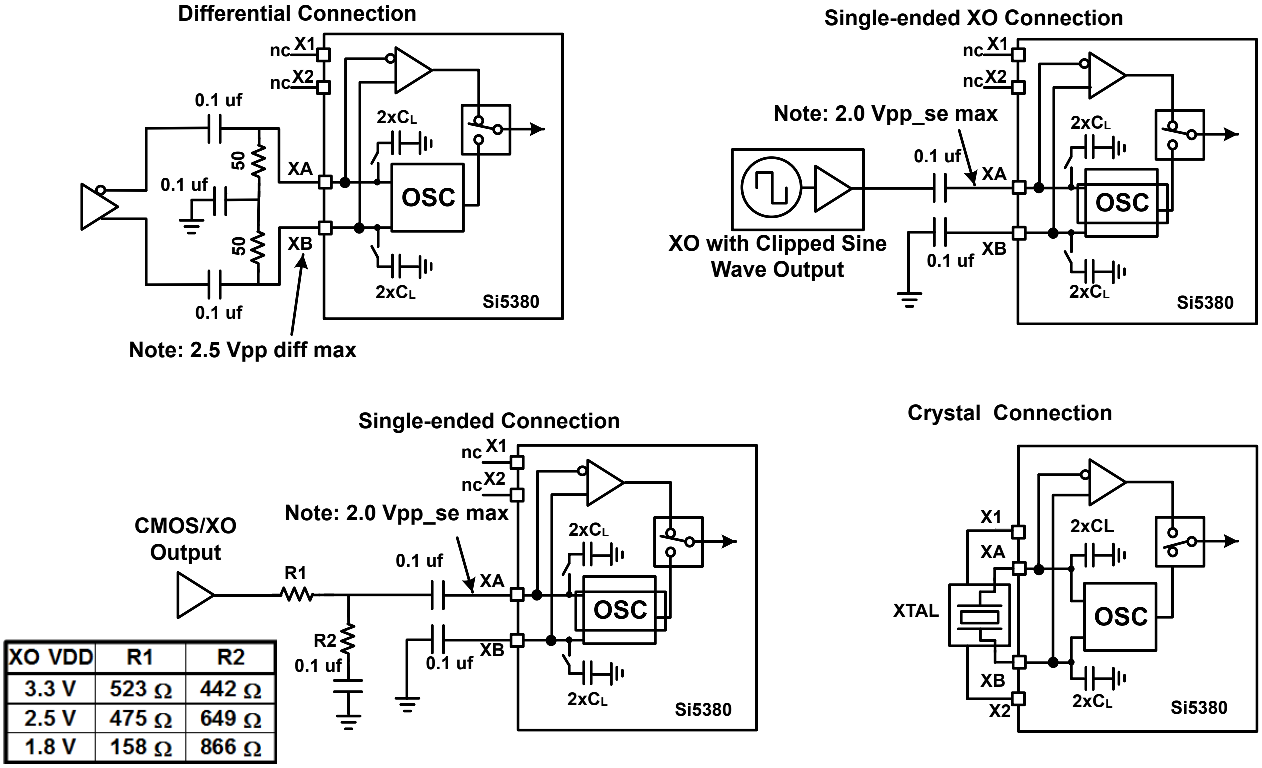


When entering holdover, the DSPLL will pull the output clock frequencies referred to the calculated averaged holdover frequency. While in holdover, the output frequency drift is entirely dependent on the external crystal or external reference clock connected to the XA/XB pins. If a new clock input becomes valid, the DSPLL will automatically exit the holdover mode and re-acquire lock to the new input clock. This process involves pulling the output clock frequencies to achieve frequency and phase lock with the new input clock. This pull-in process is glitchless and its rate is controlled by the DSPLL bandwidth and the Fastlock bandwidth. These options are register programmable.

3.2 External Reference (XA/XB)

An external crystal (XTAL) is used in combination with the internal oscillator (OSC) to produce an ultra-low phase noise reference clock for the DSPLL and for providing a stable reference for the free-run and holdover modes. A simplified diagram is shown in the figure below. The Si5380 includes internal XTAL loading capacitors which eliminates the need for external capacitors and also has the benefit of reduced noise coupling from external sources. Refer to the Table 5.12 Crystal Specifications on page 32 for crystal specifications. A crystal frequency of 54 MHz is required, with a total accuracy of ±100 ppm* recommended for best performance. The Si5380 includes built-in XTAL load capacitors (C_L) of 8 pF, which are switched out of the circuit when using an external XO. The Si5380 Reference Manual provides additional information on PCB layout recommendations for the crystal to ensure optimum jitter performance. The Si5380 can also accommodate an external reference clock (REFCLK) instead of a crystal. Selection between the external XTAL or REFCLK is controlled by register configuration. The internal crystal loading capacitors (CL) are disabled in this mode. It is important to note that when using the REFCLK option the close-in phase noise of the outputs is directly affected by the phase noise of the external XO reference. Refer to the Table 5.3 Input Clock Specifications on page 23 for REFCLK requirements when using this mode.

Note: Including initial frequency tolerance and frequency variation over the full operating temperature range, voltage range, load conditions, and aging.



XO VDD	R1	R2
3.3 V	523 Ω	442 Ω
2.5 V	475 Ω	649 Ω
1.8 V	158 Ω	866 Ω

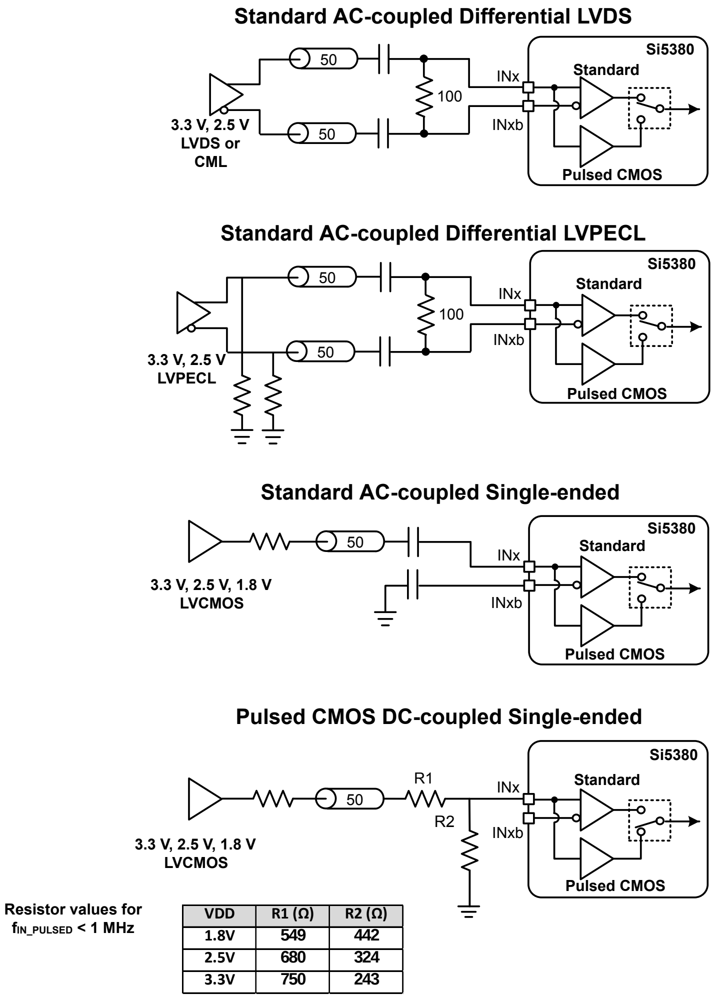
Figure 3.4. XAXB Crystal Resonator and External Reference Clock Connection Options

3.3 Inputs (IN0, IN1, IN2, IN3/FB_IN)

Four clock inputs are available to synchronize the DSPLL. The inputs are compatible with both single-ended and differential signals. Input selection can be manual (pin or register controlled) or automatic with definable priorities.

3.3.1 Input Configuration and Terminations

Each of the inputs can be configured as differential or single-ended LVCMOS. The recommended input termination schemes are shown in the figure below. Standard 50% duty cycle signals must be ac-coupled, while low duty cycle Pulsed CMOS signals can be DC-coupled. Unused inputs can be disabled and left unconnected when not in use.


Standard AC-coupled Differential LVDS

Standard AC-coupled Differential LVPECL

Standard AC-coupled Single-ended

Pulsed CMOS DC-coupled Single-ended

Resistor values for f_{IN_PULSED} < 1 MHz

VDD	R1 (Ω)	R2 (Ω)
1.8V	549	442
2.5V	680	324
3.3V	750	243

Figure 3.5. Termination of Differential and LVCMOS Input Signals

3.3.2 Manual Input Selection (IN0, IN1, IN2, IN3/FB_IN)

Input clock selection can be made manually using the IN_SEL[1:0] pins or through a register. A register bit determines input selection as pin selectable or register selectable. The IN_SEL pins are selected by default. If there is no clock signal on the selected input, the device will automatically enter free-run or holdover mode. When the zero delay mode is enabled, IN3 becomes the feedback input (FB_IN) and is not available for selection as a clock input.

Table 3.2. Manual Input Selection Using IN_SEL[1:0] Pins

IN_SEL[1:0]		Selected Input	
		Zero Delay Mode Disabled	Zero Delay Mode Enabled
0	0	IN0	IN0
0	1	IN1	IN1
1	0	IN2	IN2
1	1	IN3	Reserved

3.3.3 Automatic Input Switching (IN0, IN1, IN2, IN3/FB_IN)

An automatic input selection state machine is available in addition to the manual switching option. In automatic mode, the selection criteria is based on reference qualification, input priority, and the revertive option. Only references which are valid can be selected by the automatic state machine. If there are no valid references available, the DSPLL will enter the holdover mode. With revertive switching enabled, the highest priority input with a valid reference is always selected. If an input with a higher priority becomes valid, then an automatic switchover to that input will be initiated. With non-revertive switching, the active input will always remain selected while it is valid. If it becomes invalid, an automatic switchover to a valid input with the highest priority will be initiated.

3.3.4 Hitless Input Switching

Hitless switching is a feature that prevents a phase transient from propagating to the output when switching between two frequency locked clock inputs that have a fixed phase difference between them. A hitless switch can only occur when the two input frequencies are frequency locked meaning that they have to be exactly at the same frequency, or have an integer frequency relationship to each other. When this feature is enabled, the DSPLL simply absorbs the phase difference between the two input clocks during an input switch. When disabled (normal switching), the phase difference between the two inputs is propagated to the output at a rate determined by the DSPLL loop bandwidth.

3.3.5 Glitchless Input Switching

The DSPLL has the ability of switching between two input clocks that are up to 200 ppm apart in frequency. The DSPLL will pull-in to the new frequency using the DSPLL loop bandwidth or using the Fastlock loop bandwidth if it is enabled. The loss of lock (LOL) indicator will be asserted while the DSPLL is pulling-in to the new clock frequency. There will be no output runt pulses generated at the output. Glitchless input switching is available regardless of whether the hitless switching feature is enabled or disabled.

3.3.6 Zero Delay Mode

A zero delay mode is available for applications that require fixed and consistent minimum delay between the selected input and outputs. The zero delay mode is configured by opening the internal feedback loop through software configuration and closing the loop externally as shown in the figure below. This helps to cancel out the internal delay introduced by the dividers, the crosspoint, the input, and the output drivers. Any one of the outputs can be fed back to the IN3/FB_IN pins, although using the output driver that achieves the shortest trace length will help to minimize the input-to-output delay. The OUT9A and IN3/FB_IN pins are recommended for the external feedback connection. The FB_IN input pins must be terminated and ac-coupled when zero delay mode is used. A differential external feedback path connection is necessary for best performance. The order of the OUT9A and FB_IN polarities is such that they may be routed on the device side of the PCB without requiring vias or needing to cross each other.

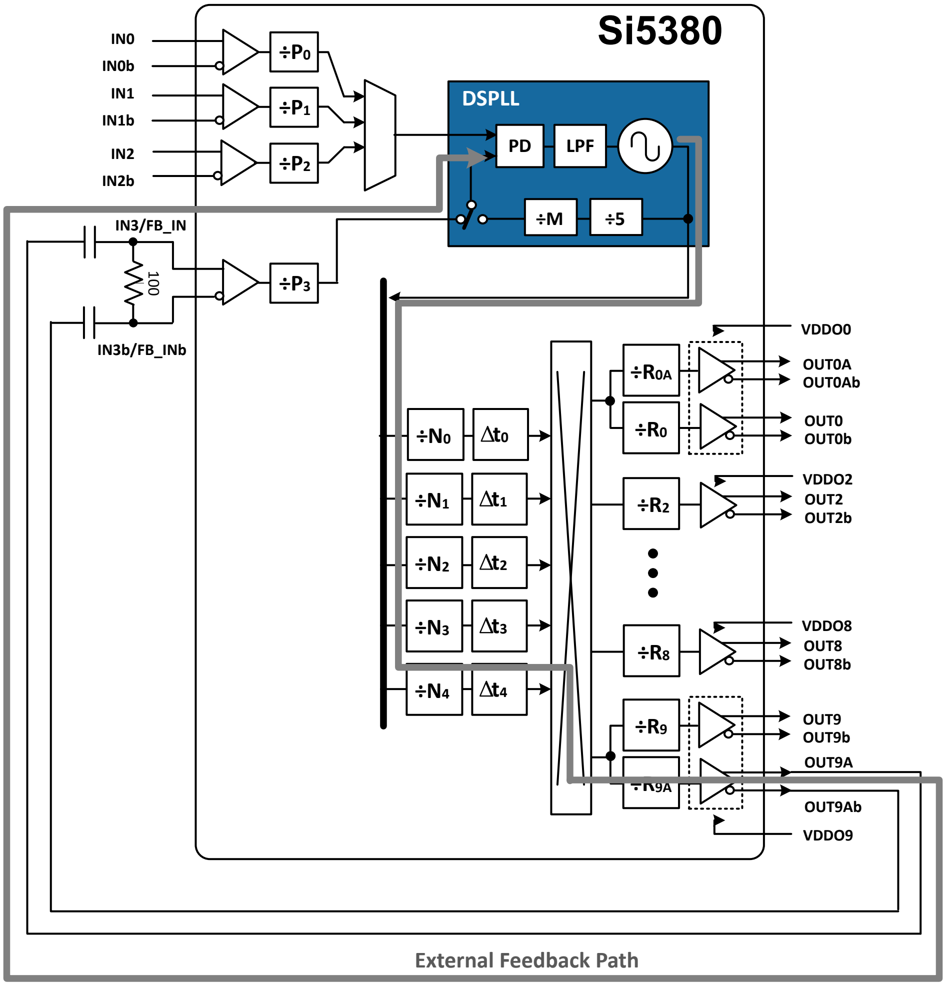


Figure 3.6. Si5380 Zero Delay Mode Set-up

3.4 Fault Monitoring

All four input clocks (IN0, IN1, IN2, IN3/FB_IN) are monitored for loss of signal (LOS) and out-of-frequency (OOF) as shown in the figure below. The reference at the XA/XB pins is also monitored for LOS since it provides a critical reference clock for the DSPLL. The DSPLL also has a Loss Of Lock (LOL) indicator, which is asserted when the DSPLL has lost synchronization with the selected input clock.

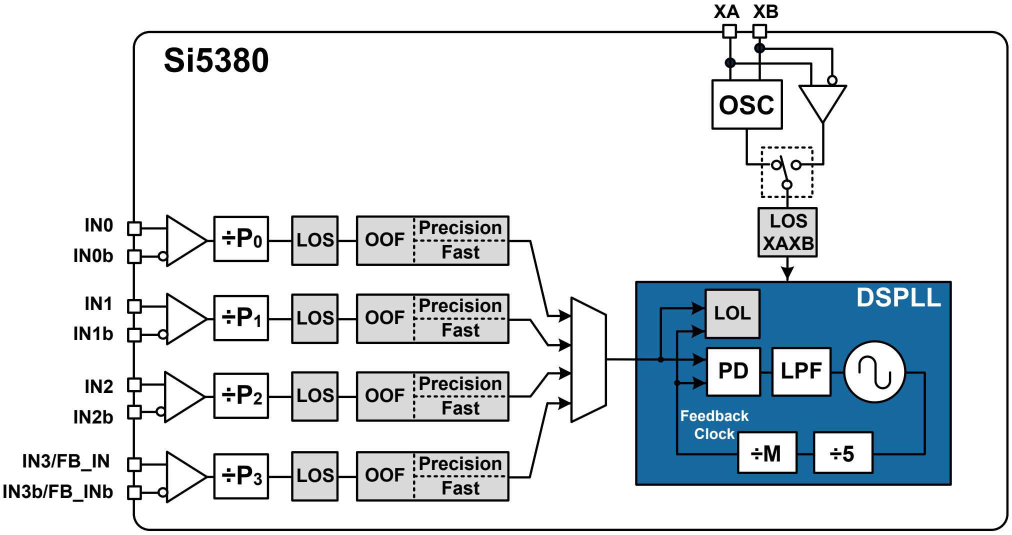


Figure 3.7. Si5380 Fault Monitors

3.4.1 Input LOS Detection

The loss of signal monitor measures the period of each input clock cycle to detect phase irregularities or missing clock edges. Each of the input LOS circuits have their own programmable sensitivity which allows ignoring missing edges or intermittent errors. Loss of signal sensitivity is configurable using the ClockBuilder Pro utility. The LOS status for each of the monitors is accessible by reading a status register. The live LOS register always displays the current LOS state and a sticky register always stays asserted until cleared. An option to disable any of the LOS monitors is also available.

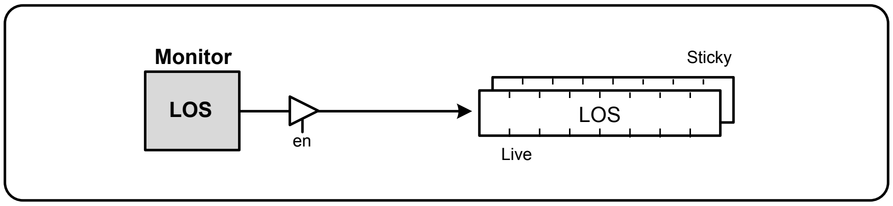


Figure 3.8. LOS Status Indicators

3.4.2 XA/XB LOS Detection

An LOS monitor is available to ensure that the external crystal or reference clock is valid. By default, the output clocks are disabled when XAXB LOS is detected. This feature can be disabled such that the device will continue to produce output clocks when XAXB LOS is detected. See the 3.5.15 Output Skew Control (Δt_0 - Δt_4) section for details.

3.4.3 OOF Detection

Each input clock is monitored for frequency accuracy with respect to a OOF reference which it considers as its “0_ppm” reference. This OOF reference can be selected as either: XAXB, IN0, IN1, IN2 or IN3. IN3 is only available as the OOF reference when not in ZDM. The final OOF status is determined by the combination of both a precise OOF monitor and a fast OOF monitor as shown in the figure below. An option to disable either monitor is also available. The live OOF register always displays the current OOF state, and its sticky register bit stays asserted until cleared.

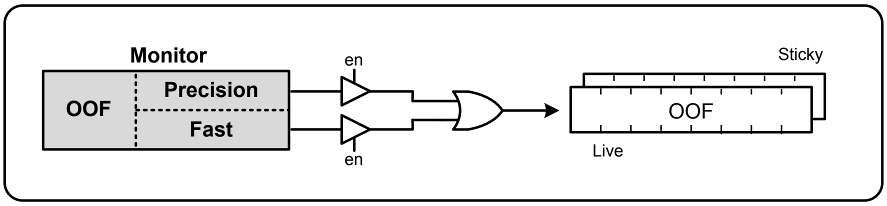


Figure 3.9. OOF Status Indicator

3.4.4 Precision OOF Monitor

The Precision OOF monitor circuit measures the frequency of all input clocks to within ±1 ppm accuracy with respect to the frequency at the XA/XB pins. The OOF monitor considers the frequency at the XA/XB pins as its 0 ppm OOF reference. A valid input frequency is one that remains within the OOF frequency range which is register configurable from ±2 ppm to ±500 ppm in steps of 2 ppm. A configurable amount of hysteresis is also available to prevent the OOF status from toggling at the failure boundary. An example is shown in the figure below. In this case the OOF monitor is configured with a valid frequency range of ±6 ppm and with 2 ppm of hysteresis. An option to use one of the input pins (IN0–IN3) as the 0 ppm OOF reference instead of the XA/XB pins is available. This option is register configurable.

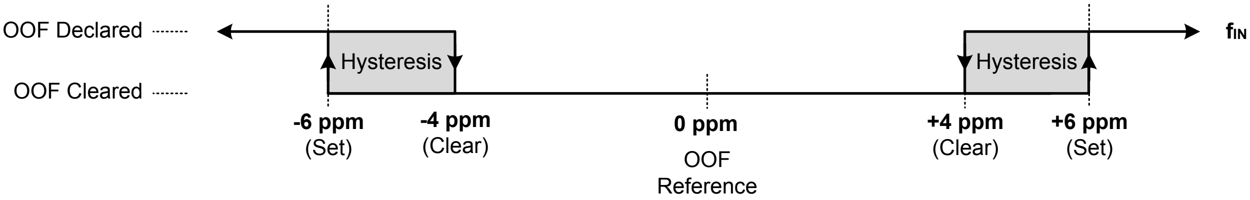


Figure 3.10. Example of Precise OOF Monitor Assertion and De-assertion Triggers

3.4.5 Fast OOF Monitor

Because the precision OOF monitor needs to provide 1 ppm of frequency measurement accuracy, it must measure the monitored input clock frequencies over a relatively long period of time. This may be too slow to detect an input clock that is quickly ramping in frequency. An additional level of OOF monitoring called the Fast OOF monitor runs in parallel with the precision OOF monitors to quickly detect a ramping input frequency. The Fast OOF monitor asserts OOF on an input clock frequency that has changed by 1,000 to 16,000 ppm.

3.4.6 LOL Detection

A loss of lock (LOL) monitor asserts the LOL bit when the DSPLL has lost synchronization with the selected input clock. There is also a dedicated active-low LOLb pin which reflects the loss of lock condition. The LOL monitor measures the frequency difference between the input and feedback clocks at the phase detector. There are two LOL frequency monitors, one that sets the LOL indicator (LOL Set) and another that clears the indicator (LOL Clear). A block diagram of the LOL monitor is shown in the figure below. The live LOL register always displays the current LOL state and a sticky register always stays asserted until cleared. The LOLb pin reflects the current state of the LOL monitor.

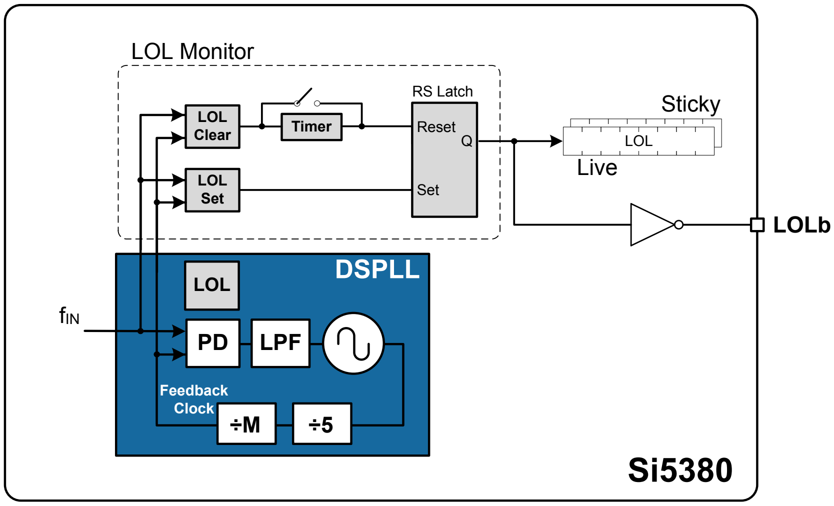


Figure 3.11. LOL Status Indicators

Each of the frequency monitors have adjustable sensitivity which is register configurable from 0.1 ppm to 10000 ppm. Having two separate frequency monitors allows for hysteresis to help prevent chattering of LOL status. An example configuration where LOCK is indicated when there is less than 0.2 ppm frequency difference at the inputs of the phase detector and LOL is indicated when there is more than 2 ppm frequency difference is shown in the figure below.

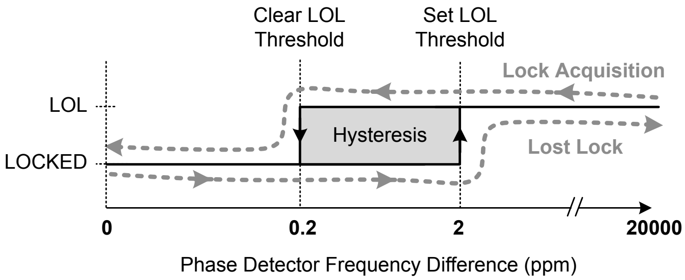


Figure 3.12. LOL Set and Clear Thresholds

An optional timer is available to delay clearing of the LOL indicator to allow additional time for the DSPLL to completely phase lock to the input clock. The timer is also useful to prevent the LOL indicator from toggling or chattering as the DSPLL completes lock acquisition. The configurable delay value depends on frequency configuration and loop bandwidth of the DSPLL and is automatically calculated using the ClockBuilder Pro utility.

3.4.7 Interrupt Pin INTRb

An interrupt pin INTRb indicates a change in state of the status indicators shown in the figure below. Any of the status indicators are maskable to prevent assertion of the interrupt pin. The state of the INTRb pin is reset by clearing the status register that caused the interrupt. The sticky version of the fault monitors is used for this function to ensure that the fault condition is still available when responding to the interrupt.

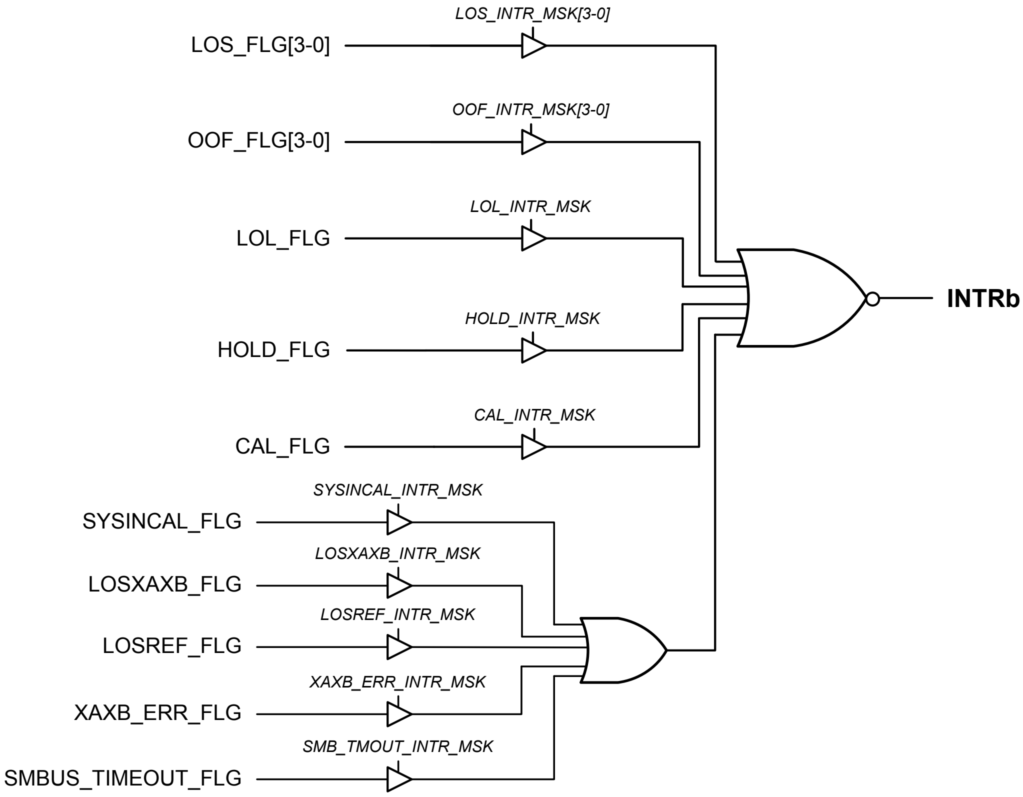


Figure 3.13. Interrupt Triggers and Masks

3.5 Outputs

The Si5380 supports 12 differential output drivers which can be independently configured as differential or LVCMOS.

3.5.1 Output Crosspoint

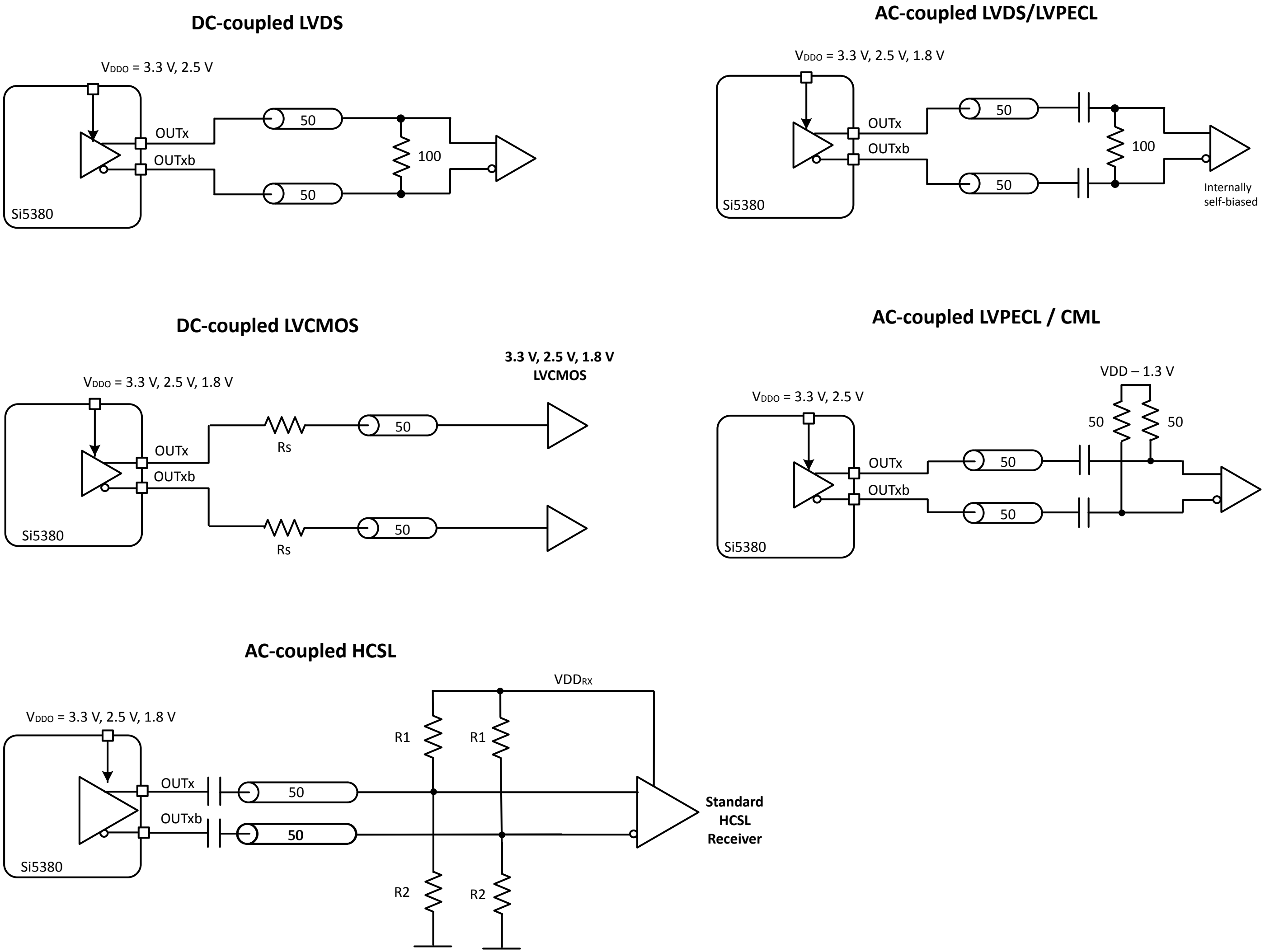
The output crosspoint allows any of the N dividers to connect to any of the clock outputs.

3.5.2 Output Signal Format

The differential output amplitude and common mode voltage are both fully programmable covering a wide variety of signal formats including LVPECL, LVDS, HCSL, and CML. In addition to supporting differential signals, any of the outputs can be configured as LVCMOS (3.3 V, 2.5 V, or 1.8 V) drivers providing up to 24 single-ended outputs, or any combination of differential and single-ended outputs.

3.5.3 Output Terminations

The output drivers support both ac-coupled and dc-coupled terminations as shown in the following figure.



For V_{CM} = 0.35 V

VDD_{RX}	R1	R2
3.3 V	442 Ω	56.2 Ω
2.5 V	332 Ω	59 Ω
1.8 V	243 Ω	63.4 Ω

Figure 3.14. Supported Output Terminations

3.5.4 Differential Output Modes

There are two selectable differential output modes: Normal and Low Power. Each output can support a unique mode.

- **Differential Normal Mode**: When an output driver is configured in normal amplitude mode, its output amplitude is selectable as one of 8 settings ranging from 130 mVpp_se to 920 mVpp_se in increments of 100 mV. The output impedance in the normal mode is 100 Ω differential. Any of the ac-coupled terminations shown in Figure 3.14 Supported Output Terminations on page 15 are supported in this mode.
- **Differential Low Power Mode**: When an output driver is configured in low power mode, its output amplitude is configurable as one of 8 settings ranging from 200 mVpp_se to 1600 mVpp_se in increments of 200 mV. The output driver is in high impedance mode and supports standard 50 Ω PCB traces. Any of the ac-coupling terminations shown in Figure 3.14 Supported Output Terminations on page 15 are supported in this mode.

3.5.5 Programmable Common Mode Voltage for Differential Outputs

The common mode voltage (VCM) for the differential normal and low power modes is programmable in 100 mV increments from 0.7 V to 2.3 V depending on the voltage available at the output's VDDO pin. Setting the common mode voltage is useful when dc-coupling the output drivers.

3.5.6 LVCMOS Output Terminations

LVCMOS outputs are dc-coupled with source-side series termination as shown in the figure below.

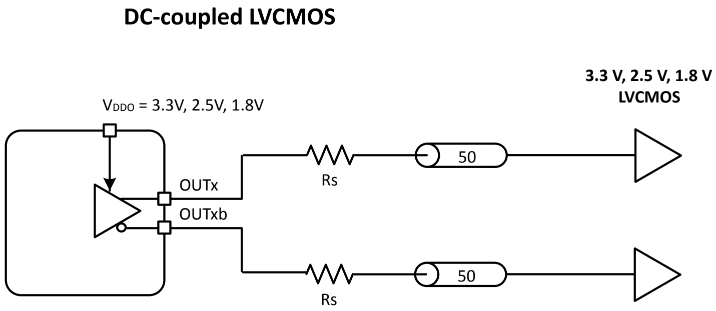


Figure 3.15. LVCMOS Output Terminations

3.5.7 LVCMOS Output Impedance and Drive Strength Selection

Each LVCMOS driver has a configurable output impedance to accommodate different trace impedances and drive strengths. A source termination resistor is recommended to help match the selected output impedance to the trace impedance. There are three programmable output impedance selections for each VDDO options as shown in the table below.

Table 3.3. LVCMOS Output Impedance and Drive Strength Selections

VDDO	OUTx_CMOS_DRV	Source Impedance (Zs)	Drive Strength (Iol/Ioh)
3.3 V	0x01	38 Ω	10 mA
	0x02	30 Ω	12 mA
	0x03*	22 Ω	17 mA
2.5 V	0x01	43 Ω	6 mA
	0x02	35 Ω	8 mA
	0x03*	24 Ω	11 mA
1.8 V	0x03*	31 Ω	5 mA
Note: Use of the lowest impedance setting is recommended for all supply voltages for best edge rates.			

3.5.8 LVCMOS Output Signal Swing

The signal swing (VOL/VOH) of the LVCMOS output drivers is set by the voltage on the VDDO pins. Each output driver has its own VDDO pin allowing a unique output voltage swing for each of the LVCMOS drivers. OUT0 and OUT0A share the same VDDO pin. OUT9 and OUT9A also share the VDDO pin. All other outputs have their own individual VDDO pins. Each output driver automatically detects the voltage on the VDDO pin to properly determine the correct output voltage.

3.5.9 LVCMOS Output Polarity

When a driver is configured as an LVCMOS output it generates a clock signal on both pins (OUTx and OUTxb). By default the clock on the OUTxb pin is generated with the same polarity (in phase) with the clock on the OUTx pin. The polarity of these clocks is configurable enabling complimentary clock generation and/or inverted polarity with respect to other output drivers.

3.5.10 Output Enable/Disable

The OEb pin provides a convenient method of disabling or enabling all of the output drivers at the same time. When the OEb pin is held high all outputs will be disabled. When held low, the outputs will all be enabled. Outputs in the enabled state can still be individually disabled through register control.

3.5.11 Output Disable During LOL

By default, a DSPLL that is out of lock will generate either free-running clocks or generate clocks in holdover mode. There is an option to disable the outputs when a DSPLL is LOL. This option can be useful to force a downstream PLL into holdover.

3.5.12 Output Disable During XAXB_LOS

The internal oscillator circuit (OSC) in combination with the external crystal (XTAL) provides a critical function for the operation of the DSPLLs. In the event of a crystal failure, the device will assert an XAXB_LOS alarm. By default, all outputs will be disabled during assertion of the XAXB_LOS alarm. There is an option to leave the outputs enabled during an XAXB_LOS alarm, but the frequency accuracy and stability will be indeterminate during this fault condition.The internal oscillator circuit (OSC) in combination with the external crystal (XTAL) provides a critical function for the operation of the DSPLLs. In the event of a crystal failure, the device will assert an XAXB_LOS alarm. By default, all outputs will be disabled during assertion of the XAXB_LOS alarm. There is an option to leave the outputs enabled during an XAXB_LOS alarm, but the frequency accuracy and stability will be indeterminate during this fault condition.

3.5.13 Output Driver State When Disabled

The disabled state of an output driver is configurable as either disable low or disable high.

3.5.14 Synchronous Enable/Disable Feature

The output drivers provide a selectable synchronous enable/disable feature. Output drivers with this feature active will wait until a clock period has completed before the driver is disabled or enabled. This prevents unwanted runt pulses from occurring when enabling or disabling an output. When this feature is turned off, the output clock will disable immediately without waiting for the period to complete.

3.5.15 Output Skew Control (Δt_0 - Δt_4)

The Si5380 uses independent dividers (N0 - N4) to generate up to 5 unique frequencies to its 12 outputs through a crosspoint switch. A delay path (Dt0 - Dt4) associated with each of these dividers is available for applications that need a specific output skew configuration. This is useful for compensating PCB trace delay differences or for applications that require quadrature clock generation. The resolution of the phase adjustment is approximately 68 ps per step up to 128 steps of added phase delay (+8.6 ns late), or 128 steps of negative delay (–8.6 ns early). Phase adjustments are register configurable. An example of generating two frequencies with unique configurable path delays is shown in the following figure.

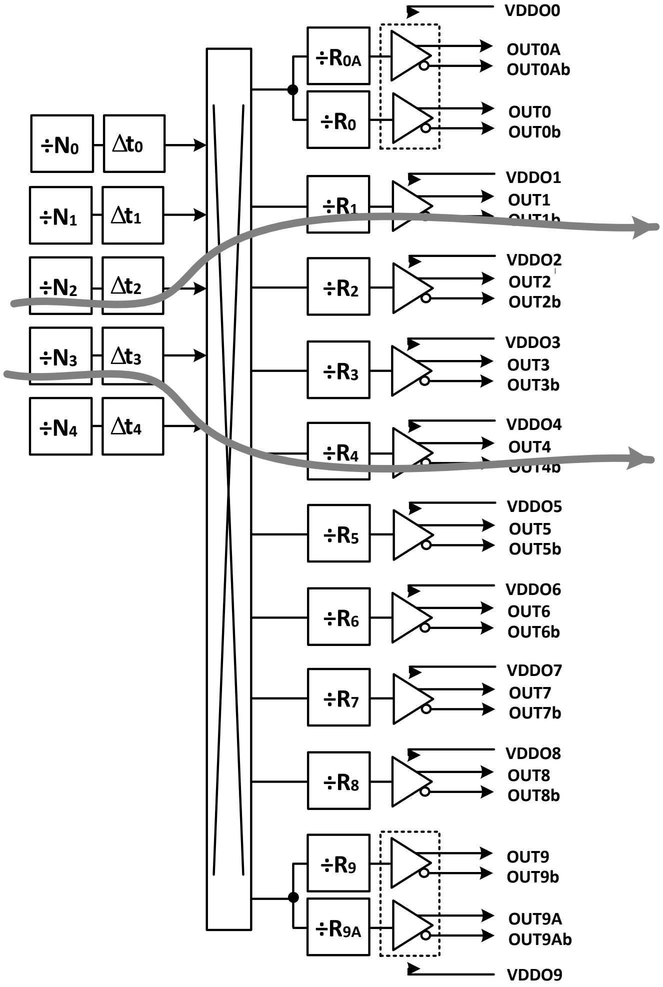


Figure 3.16. Example of Independently Configurable Path Delays

All phase delay values are restored to their default values after power-up, power-on reset, or hardware reset using the RSTb pin. Phase delay default values can be written to NVM allowing a custom phase offset configuration at power-up or after power-on reset, or after a hardware reset using the RSTb pin.

3.5.16 Output Divider (R) Synchronization

All the output R dividers are reset to a known state during the power-up initialization period. This ensures consistent and repeatable phase alignment across all output drivers. Resetting the device using the RSTb pin or asserting the reset bit will have the same result. Asserting the sync register bit provides another method of realigning the R dividers without resetting the device.

3.6 Power Management

Unused inputs and output drivers can be powered down when unused. Consult the Si5380 Reference Manual and ClockBuilder Pro configuration utility for details.

3.6.1 Power Down Pin (PDNb)

A power down pin is provided to force the device in a low power mode. The device's configuration will be maintained but no output clocks will be generated. Most of the internal blocks will be shut down but device communication via the serial interface will still be available. When the PDNb pin is pulled low the outputs will shut down without glitching (the clock's complete period will be generated before shutting down). When PDNb is released the device will start generating clocks without glitches. The device will generate free-running clocks until the DSPLL has acquired lock to the selected input clock source.

3.7 In-Circuit Programming

The Si5380 is fully configurable using the serial interface (I2C or SPI). At power-up, the device downloads its default register values from internal non-volatile memory (NVM). Application specific default configurations can be written into NVM allowing the device to generate specific clock frequencies at power-up. Writing default values to NVM is in-circuit programmable with normal operating power supply voltages applied to its VDD and VDDA pins. The NVM is writable two times. Once a new configuration has been written to NVM, the old configuration is no longer accessible. Refer to the Si5380 Reference Manual for a detailed procedure for writing registers to NVM.

3.8 Serial Interface

Configuration and operation of the Si5380 is controlled by reading and writing registers using the I2C or SPI interface. The I2C_SEL pin selects I2C or SPI operation. The Si5380 supports communication with a 3.3 V or 1.8 V host by setting the IO_VDD_SEL configuration bit. The SPI mode supports 4-wire or 3-wire by setting the SPI_3WIRE configuration bit. See the Si5380 Reference Manual for details.

3.9 Custom Factory Preprogrammed Devices

For applications where a serial interface is not available for programming the device, custom pre-programmed parts can be ordered with a specific configuration written into NVM. A factory pre-programmed device will generate clocks at power-up. Custom, factory-pre-programmed devices are available. Use the ClockBuilder Pro custom part number wizard (www.silabs.com/clockbuilderpro) to quickly and easily request and generate a custom part number for your configuration.

In less than three minutes, you will be able to generate a custom part number with a detailed data sheet addendum matching your design's configuration. Once you receive the confirmation email with the data sheet addendum, simply place an order with your local Silicon Labs sales representative. Samples of your pre-programmed device will ship to you typically within two weeks.

3.10 How to Enable Features and/or Configuration Settings Not Available in ClockBuilder Pro for Factory Pre-programmed Devices

As with essentially all software utilities, ClockBuilder Pro is continuously updated and enhanced. By registering at www.silabs.com and opting in for updates to software, you will be notified whenever changes are made and what the impact of those changes are. This update process will ultimately enable ClockBuilder Pro users to access all features and register setting values documented in this data sheet and the Si5380 Reference Manual .

However, if you must enable or access a feature or register setting value so that the device starts up with this feature or a register setting, but the feature or register setting is NOT yet available in CBPro, you must contact a Silicon Labs applications engineer for assistance. Examples of this type of feature or custom setting are the customizable output amplitude and common voltages for the clock outputs. After careful review of your project file and custom requirements, all Silicon Labs applications engineer will email back your CBPro project file with your specific features and register settings enabled, using what is referred to as the manual "settings override" feature of CBPro. "Override" settings to match your request(s) will be listed in your design report file. Examples of setting "overrides" in a CBPro design report are shown below:

Table 3.4. Setting Overrides

Location	Customer Name	Engineering Name	Type	Target	Dec Value	Hex Value
0x0435[0]	FORCE_HOLD_PLLA	OLA_HO_FORCE	No NVM	N/A	1	0x1
0x0B48[0:4]	OOF_DIV_CLK_DIS	OOF_DIV_CLK_DIS	User	OPN and EVB	0	0x00

Once you receive the updated design file, simply open it in CBPro. After you create a custom OPN, the device will begin operation after startup with the values in the NVM file, including the Silicon Labs-supplied override settings.

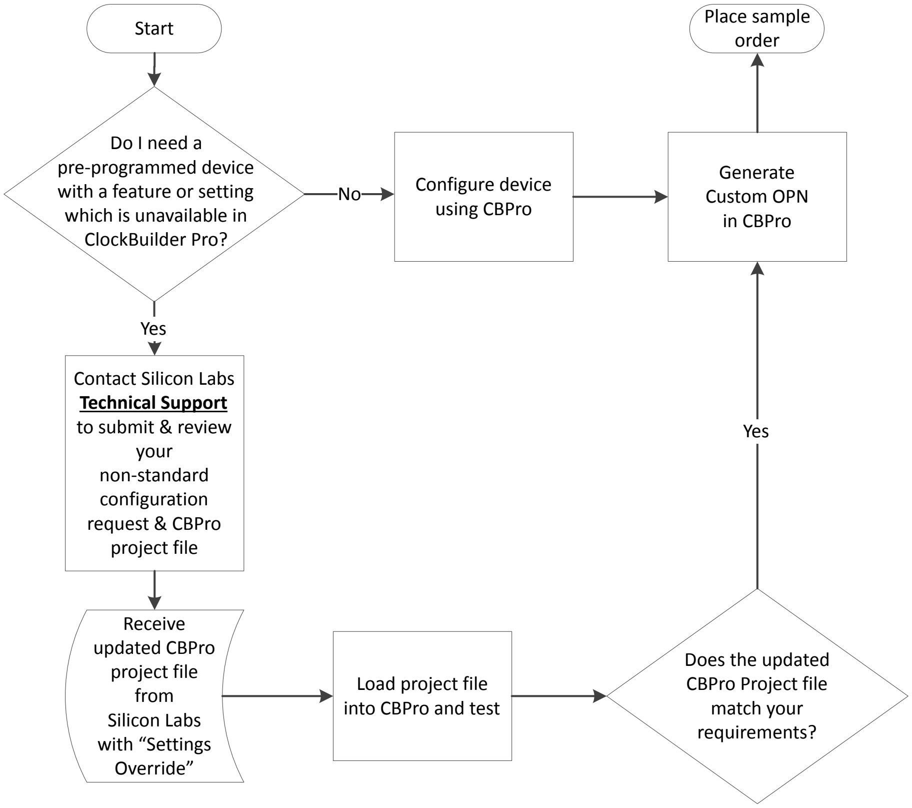


Figure 3.17. Flowchart to Order Custom Parts with Features not Available in CBPro

4. Register Map

This document provides a brief list of available registers. For a complete list of registers and settings, please refer to the Si5380 Reference Manual .

5. Electrical Specifications

Table 5.1. Recommended Operating Conditions[1]

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Ambient Temperature	T_A		–40	25	85	°C
Maximum Junction Temperature	T_{JMAX}		—	—	125	°C
Core Supply Voltage	V_{DD}		1.71	1.80	1.89	V
	V_{DDA}		3.14	3.30	3.47	V
Output Driver Supply Voltage	V_{DDO}		3.14	3.30	3.47	V
			2.38	2.50	2.62	V
			1.71	1.80	1.89	V

Note:

1. All minimum and maximum specifications are guaranteed and apply across the recommended operating conditions. Typical values apply at nominal supply voltages and an operating temperature of 25 °C unless otherwise noted.

Table 5.2. DC Characteristics

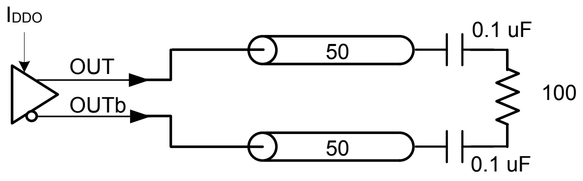
Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Core Supply Current[1, 5]	I_{DD}	See Note [1]	—	170	265	mA
	I_{DDA}		—	125	135	mA
Output Buffer Supply Current[2, 5]	I_{DDO}	LVPECL Output[3] @ 1474.56 MHz	—	28	34	mA
		LVPECL Output[3] @ 153.6 MHz	—	21	25	mA
		LVDS Output[3] @ 1474.56 MHz	—	17	23	mA
		LVDS Output[3] @ 153.6 MHz	—	15	17	mA
		3.3 V LVCMOS Output [4] @ 153.6 MHz	—	21	25	mA
		2.5 V LVCMOS Output [4] @ 153.6 MHz	—	16	18	mA
		1.8 V LVCMOS Output [4] @ 153.6 MHz	—	12	13	mA
Total Power Dissipation[1,2]	P_d	Typical Outputs[1]	—	1250	1450	mW

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit

Note:

1. Si5380 test configuration 1: 4 x 3.3 V LVPECL outputs enabled @122.88 MHz, 2 x 3.3 V LVDS outputs enabled @122.88 MHz, one input enabled, locked to 30.72 MHz. Excludes power in termination resistors.
2. Detailed power consumption for any configuration can be estimated using ClockBuilder Pro when an evaluation board (EVB) is not available. All EVBs support detailed current measurements for any configuration.
3. Differential outputs terminated into an ac-coupled 100 Ω load.
4. LVCMOS outputs measured into a 6-inch 50 Ω PCB trace with 5 pF load. The LVCMOS outputs were set to OUTx_CMOS_DRV=3, which is the strongest driver setting. Refer to the Si5380 Reference Manual for more details on register settings.
5. V_{DDO0} supplies power to both OUT0 and OUT0A buffers. Similarly, VDDO9 supplies power to both OUT9 and OUT9A buffers.

Differential Output Test Configuration



LVCMOS Output Test Configuration

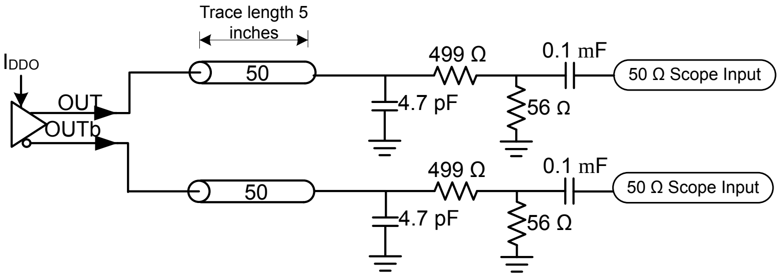


Table 5.3. Input Clock Specifications

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Standard Differential or Single-Ended/LVCMOS—AC-coupled (IN0/IN0, IN1/IN1, IN2/IN2, IN3/IN3, FB_IN/FB_IN)						
Input Frequency Range	f_{IN_DIFF}	Differential	10	—	750	MHz
	f_{IN_SE}	Single-ended/LVCMOS	10	—	250	MHz
Input Voltage Amplitude	V_{IN}	F_{IN} < 400 MHz	100	—	3600	mVpp_se, mVpp_dif
		400 MHz < F_{IN} < 750 MHz	225	—	3600	mVpp_se, mVpp_dif
Slew Rate[1, 2]	SR		400	—	—	V/µs
Duty Cycle	DC		40	—	60	%
Capacitance	C_{IN}		—	2	—	pF
Pulsed CMOS—DC-coupled (IN0, IN1, IN2, IN3/FB_IN)[3]						
Input Frequency	f_{IN_CMOS}		10	—	250	MHz
Input Voltage Thresholds	V_{IL}		–0.2	—	0.33	V
	V_{IH}		0.49	—	—	V
Slew Rate[1, 2]	SR		400	—	—	V/µs
Duty Cycle	DC	Clock Input	40	—	60	%
Minimum Pulse Width	PW	Pulse Input	1.6	—	—	ns
Input Resistance	R_{IN}		—	8	—	kΩ
REFCLK (applied to XA/XB)						

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
REFCLK[4]	f_{IN_REF}	LTE	—	54	—	MHz
Total Frequency Tolerance[5]	f_{range}		–100	—	+100	ppm
Input Voltage Swing	V_{IN_SE}		365	—	2000	mVpp_se
	V_{IN_DIFF}		365	—	2500	mVpp_diff
Slew Rate[1, 2]	SR	Imposed for phase noise performance	400	—	—	V/µs
Input Duty Cycle	DC		40	—	60	%

Note:

1. Imposed for phase noise performance.
2. Rise and fall times can be estimated using the following simplified equation: $tr/tf_{80\text{-}20} = ((0.8 – 0.2) * V_{IN\_Vpp\_se}) / SR$.
3. This mode is intended primarily for single-ended LVCMOS input clocks < 1 MHz, which must be dc-coupled, having a duty cycle significantly less than 50%. A typical application example is a low frequency video frame sync pulse. Since the input thresholds (VIL, VIH) of the input buffer are non-standard, refer to the input attenuator circuit for dc-coupled Pulsed LVCMOS in the in the Si5380 Reference Manual . Otherwise, for standard LVCMOS input clocks, use the "AC-coupled Single-Ended" mode as shown in Figure 6.14.
4. The REFCLK frequency for the Si5380 is fixed at 54 MHz. Contact the applications group for more information.
5. Includes initial tolerance, drift after reflow, change over temperature (–40 °C to +85 °C), V_{DD} variation, load pulling, and aging.

Table 5.4. Control Input Pin Specifications[1]

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Si5380 Control Input Pins (I2C_SEL, IN_SEL[1:0], RSTb, OEb, SYNCb, PDNb, A1/SDO, SDA/SDIO, SCLK, A0/CSb)						
Input Voltage Thresholds	V_{IL}		—	—	$0.3xV_{DDIO}$*	V
	V_{IH}		0.7 x V_{DDIO}*	—	—	V
Input Capacitance	C_{IN}		—	2	—	pF
Input Resistance	I_L		—	20	—	kΩ
Minimum Pulse Width	PW	RSTb, SYNCb, PDNb	100	—	—	ns

Note:

1. V_{DDIO} is determined by the IO_VDD_SEL bit. It is selectable as V_{DDA} or V_{DD}. See the Si5380 Reference Manual for more details on the register settings.

Table 5.5. Differential Clock Output Specifications

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output Frequency	f_{OUT}		0.48	—	1474.56	MHz
Duty Cycle	DC	f < 400 MHz	48	—	52	%
		400 MHz < f < 800 MHz	45	—	55	%
		f >800 MHz	40	—	60	%

Parameter	Symbol	Test Condition		Min	Typ	Max	Unit
Output-Output Skew	T_{SK}	Differential Outputs Same N-divider		—	20	50	ps
		Differential Outputs Different N-dividers		—	20	100	ps
OUT-OUTb Skew	T_{SK_OUT}	Measured from the positive to negative output pins		—	0	100	ps
Output Voltage Amplitude[1]	**Normal Mode**						
	V_{OUT}	V_{DDO} = 3.3 V or 2.5 V or 1.8 V	LVDS	340	470	550	mVpp_se
			LVPECL	530	810	950	
	Low Power Mode						
	V_{OUT}	V_{DDO} = 3.3 V or 2.5 V or 1.8 V	LVDS	300	420	530	mVpp_se
		V_{DDO} = 3.3 V or 2.5 V	LVPECL	530	820	1060	
Common Mode Voltage[1, 2]	**Normal or Low Power Modes**						
	V_{CM}	V_{DDO} = 3.3 V	LVDS	1.10	1.25	1.30	V
			LVPECL	1.90	2.05	2.10	
		V_{DDO} = 2.5 V	LVPECL	1.15	1.25	1.30	
			LVDS				
		V_{DDO} = 1.8 V	LVDS	0.87	0.93	0.98	
Rise and Fall Times (20% to 80%)	t_R/t_F	Normal Mode		—	170	240	ps
		Low Power Mode		—	300	430	
Differential Output Impedance[3]	Z_O	Normal Power Mode		—	100	—	Ω
		Low Power Mode		—	Hi-Z	—	

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Power Supply Noise Rejection[4]	PSRR	**Normal Mode**				
		10 kHz sinusoidal noise	—	-93	—	dBc
		100 kHz sinusoidal noise	—	-93	—	
		500 kHz sinusoidal noise	—	-84	—	
		1 MHz sinusoidal noise	—	-79	—	
		Low Power Mode				
		10 kHz sinusoidal noise	—	-98	—	dB
		100 kHz sinusoidal noise	—	-95	—	
		500 kHz sinusoidal noise	—	-84	—	
		1 MHz sinusoidal noise	—	-76	—	
Output-Output Cross-talk	XTALK	Measured spur from adjacent output	—	-75	—	dB

Note:

1. Normal mode and low power mode amplitude and common mode voltage are programmable through register settings and can be stored in NVM. Each output driver can be programmed independently. The typical normal mode (or low power mode) LVDS maximum is 100 mV (or 80 mV) higher than the TIA/EIA-644 maximum. Refer to the Si5380 Reference Manual for more details on register settings.
2. Not all combinations of voltage amplitude and common mode voltages settings are possible. See the Si5380 Reference Manual for more information.
3. Driver output impedance depends on selected output mode (Normal, Low Power).
4. Measured for 122.88 MHz carrier frequency. Sinewave noise added to VDDO (1.8 V = 50 mVpp, 2.5 V/3.3 V = 100 mVpp) and noise spur amplitude measured.
5. Measured across two adjacent outputs, both in LVDS mode, with the victim running at 76.8 MHz and the aggressor at 92.08 MHz. Refer to application note, "AN862: Optimizing Si534x Jitter Performance in Next Generation Internet Infrastructure Systems", for guidance on crosstalk optimization. Note that all active outputs must be terminated when measuring crosstalk

Table 5.6. LVCMOS Clock Output Specifications

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output Frequency			0.48	—	250	MHz
Duty Cycle	DC	f_{OUT} < 100 MHz	47	—	53	%
		100 MHz < f_{OUT} < 250 MHz	44	—	55	
Output-to-Output Skew	T_{SK}		—	—	100	ps

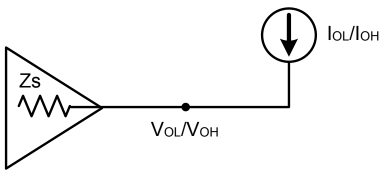
Parameter	Symbol	Test Condition		Min	Typ	Max	Unit
Output Voltage High[1, 2, 3]	V_{OH}	V_{DDO} = 3.3 V					
		OUTx_CMOS_DRV=1	I_{OH} = –10 mA	V_{DDO} x 0.75	—	—	V
		OUTx_CMOS_DRV=2	I_{OH} = –12 mA		—	—	
		OUTx_CMOS_DRV=3	I_{OH} = –17 mA		—	—	
		V_{DDO} = 2.5 V					
		OUTx_CMOS_DRV=1	I_{OH} = –6 mA	V_{DDO} x 0.75	—	—	V
		OUTx_CMOS_DRV=2	I_{OH} = –8 mA		—	—	
		OUTx_CMOS_DRV=3	I_{OH} = –11 mA		—	—	
		V_{DDO} = 1.8 V					
		OUTx_CMOS_DRV=2	I_{OH} = –4 mA	V_{DDO} x 0.75	—	—	V
		OUTx_CMOS_DRV=3	I_{OH} = –5 mA		—	—	
Output Voltage Low[1, 2, 3]	V_{OL}	V_{DDO} = 3.3 V					
		OUTx_CMOS_DRV=1	I_{OL} = 10 mA	—	—	V_{DDO} x 0.15	V
		OUTx_CMOS_DRV=2	I_{OL} = 12 mA	—	—		
		OUTx_CMOS_DRV=3	I_{OL} = 17 mA	—	—		
		V_{DDO} = 2.5 V					
		OUTx_CMOS_DRV=1	I_{OL} = 6 mA	—	—	V_{DDO} x 0.15	V
		OUTx_CMOS_DRV=2	I_{OL} = 8 mA	—	—		
		OUTx_CMOS_DRV=3	I_{OL} = 11 mA	—	—		
		V_{DDO} = 1.8 V					
		OUTx_CMOS_DRV=2	I_{OL} = 4 mA	—	—	V_{DDO} x 0.15	V
		OUTx_CMOS_DRV=3	I_{OL} = 5 mA	—	—		
LVCMOS Rise and Fall Times[2] (20% to 80%)	tr/tf	V_{DDO} = 3.3 V		—	420	550	ps
		V_{DDO} = 2.5 V		—	475	625	ps
		V_{DDO} = 1.8 V		—	525	705	ps

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit

Note:

1. Driver strength is a register programmable setting and stored in NVM. Options are OUTx_CMOS_DRV = 1, 2, 3. Refer to the Si5380 Reference Manual for more details on register settings.
2. I_{OL}/I_{OH} is measured at V_{OL}/V_{OH} as shown in the DC test configuration
3. A 5 pF capacitive load is assumed. The LVCMOS outputs were set to OUTx_CMOS_DRV = 3.

DC Test Configuration



AC Output Test Configuration

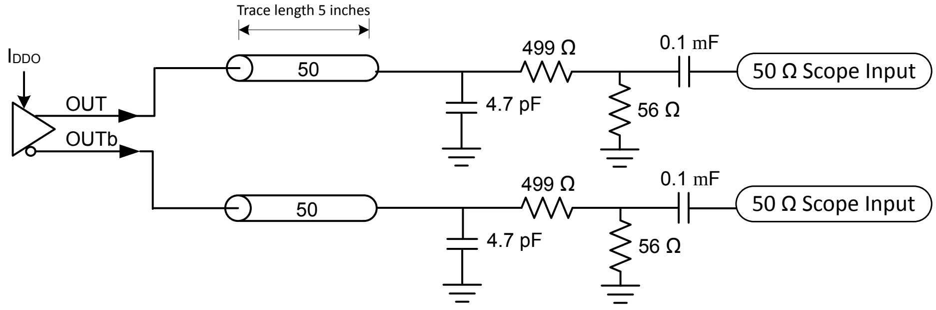


Table 5.7. Output Status Pin Specifications

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Si5380 Status Output Pins (LOLb, INTRb)						
Output Voltage	V_{OH}	$I_{OH} = -2$ mA	V_{DDIO}[1] x 0.75	—	—	V
	V_{OL}	$I_{OL} = 2$ mA	—	—	V_{DDIO}[1] x 0.15	V

Note:

1. V_{DDIO} is determined by the IO_VDD_SEL bit. It is selectable as V_{DDA} or V_{DD}. See the Si5380 Reference Manual for more details on the register settings.

Table 5.8. Performance Characteristics

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
PLL Loop Bandwidth Programming Range[3]	f_{BW}	Loop bandwidth is register programmable	0.1	40	100	Hz
Initial Start-Up Time	t_{START}	Time from power-up or de-assertion of PDNb to when the device generates free-running clocks.	—	30	45	ms
PLL Lock Time	t_{ACQ}	Fastlock enabled[4]	—	500	600	ms
Output Delay Adjustment	t_{DELAY}[2]	$t_{DELAY} = 1/f_{VCO}$	—	67.8	—	ps
	t_{RANGE}[2]	$+/-128 / f_{VCO}$	—	±8.6	—	ns
POR to Serial Interface Ready[1]	t_{RDY}		—	—	15	ms
Jitter Peaking	J_{PK}	When locked, any loop bandwidth	—	—	0.1	dB

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Maximum Phase Transient	t_{SWITCH}	Automatic Hitless Switch	—	—	2.8	ns
Pull-in Range	Ω_P		—	500	—	ppm
Input-to-Output Delay Variation	$t_{IODELAY}$	In Regular Mode	1	2	—	ns
	t_{ZDELAY}	In Zero Delay Mode[2]	—	110	—	ps
RMS Jitter Generation[5]	J_{GEN}	LVPECL Output @ 1474.56 MHz	—	0.070	0.080	ps RMS
		LVPECL Output @ 122.88 MHz	—	0.080	0.125	ps RMS
Phase Noise Performance[5] (122.88 MHz Carrier Frequency)	PN	10Hz	—	–71	—	dBc/Hz
		100 Hz	—	–98	—	dBc/Hz
		1 kHz	—	–123	—	dBc/Hz
		10 kHz	—	–136	—	dBc/Hz
		100 kHz	—	–144	—	dBc/Hz
		1 MHz	—	–154	—	dBc/Hz
		10 MHz	—	–165	—	dBc/Hz
Spur Performance [5](122.88 MHz Carrier Frequency)	SPUR	Up to 1 MHz offset	—	–103	—	dBc
		From 1 MHz to 30 MHz offset	—	–95	—	dBc

Note:

1. Measured as time from valid V_{DD}/V_{DDA} rails (both >90% of settled voltage) to when the serial interface is ready to respond to commands.
2. Measured from the INx input to the feedback input, with both clocks running at 15.36 MHz and having the same slew rate. The rise time of the reference input should not exceed 200 ps in order to guarantee this specification.
3. Actual loop bandwidth might be lower; refer to ClockBuilder Pro for actual value on your frequency plan.
4. Lock Time can vary significantly depending on several parameters, such as bandwidths, LOL thresholds, etc. For this case, lock time was measured with nominal and fastlock bandwidths both set to 100 Hz, LOL set/clear thresholds of 3/0.3 ppm respectively, using IN0 as clock reference by removing the reference and enabling it again, then measuring the delta time between the first rising edge of the clock reference and the LOL indicator de-assertion.
5. Jitter generation test conditions: f_{IN} = 30.72 MHz, f_{OUT} = 122.88 MHz LVPECL, DSPLL LBW = 100 Hz. Does not include jitter from PLL input reference.

Table 5.9. I2C Timing Specifications (SCL,SDA)

Parameter	Symbol	Test Condition	Min	Max	Min	Max	Unit
			Standard Mode **100 kbps**		**Fast Mode** **400 kbps**		
SCL Clock Frequency	f_{SCL}		0	100	0	400	kHz
SMBus Timeout	—	When Timeout is Enabled	25	35	25	35	ms
Hold Time (Repeated) START Condition	$t_{HD:STA}$		4.0	—	0.6	—	µs
Low Period of the SCL Clock	t_{LOW}		4.7	—	1.3	—	µs

Parameter	Symbol	Test Condition	Min	Max	Min	Max	Unit
HIGH Period of the SCL Clock	t_{HIGH}		4.0	—	0.6	—	µs
Set-up Time for a Repeated START Condition	$t_{SU:STA}$		4.7	—	0.6	—	µs
Data Hold Time	$t_{HD:DAT}$		100	—	100	—	ns
Data Set-up Time	$t_{SU:DAT}$		250	—	100	—	ns
Rise Time of Both SDA and SCL Signals	t_r		—	1000	20	300	ns
Fall Time of Both SDA and SCL Signals	t_f		—	300	—	300	ns
Set-up Time for STOP Condition	$t_{SU:STO}$		4.0	—	0.6	—	µs
Bus Free Time between a STOP and START Condition	t_{BUF}		4.7	—	1.3	—	µs
Data Valid Time	$t_{VD:DAT}$		—	3.45	—	0.9	µs
Data Valid Acknowledge Time	$t_{VD:ACK}$		—	3.45	—	0.9	µs

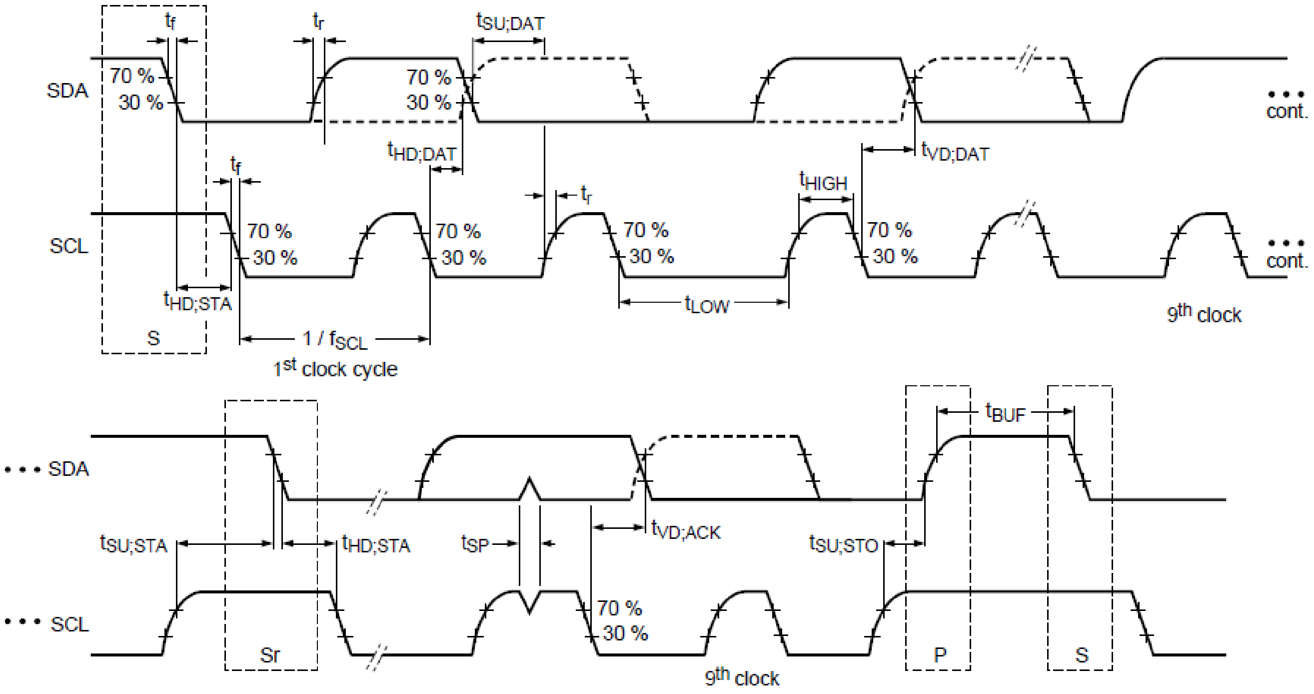


Figure 5.1. I²C Serial Prot Timing Standard and Fast Modes

Table 5.10. SPI Timing Specifications (4-Wire)

Parameter	Symbol	Min	Typ	Max	Unit
SCLK Frequency	f_{SPI}	—	—	20	MHz
SCLK Duty Cycle	T_{DC}	40	—	60	%

Parameter	Symbol	Min	Typ	Max	Unit
SCLK Rise and Fall Time	Tr/Tf	—	—	10	ns
SCLK Period	T_C	50	—	—	ns
Delay Time, SCLK Fall to SDO Active	T_{D1}	—	—	12.5	ns
Delay Time, SCLK Fall to SDO	T_{D2}	—	—	12.5	ns
Delay Time, CSb Rise to SDO Tri-State	T_{D3}	—	—	12.5	ns
Setup Time, CSb to SCLK	T_{SU1}	25	—	—	ns
Hold Time, SCLK Fall to CSb	T_{H1}	25	—	—	ns
Setup Time, SDI to SCLK Rise	T_{SU2}	12.5	—	—	ns
Hold Time, SDI to SCLK Rise	T_{H2}	12.5	—	—	ns
Delay Time Between Chip Selects (CSb)	T_{CS}	1.9	—	—	T_c

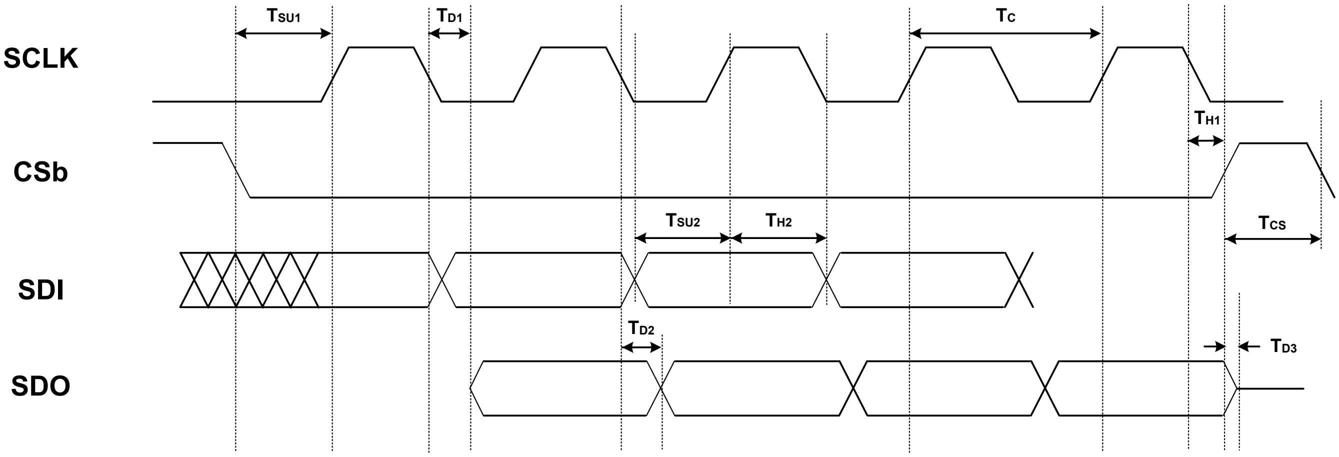


Figure 5.2. 4-Wire SPI Serial Interface Timing

Table 5.11. SPI Timing Specifications (3-Wire)

Parameter	Symbol	Min	Typ	Max	Unit
SCLK Frequency	f_{SPI}	—	—	20	MHz
SCLK Duty Cycle	T_{DC}	40	—	60	%
SCLK Rise and Fall Time	Tr/Tf	—	—	10	ns
SCLK Period	T_C	50	—	—	ns
Delay Time, SCLK Fall to SDIO Turn-on	T_{D1}	—	—	12.5	ns
Delay Time, SCLK Fall to SDIO Next-bit	T_{D2}	—	—	12.5	ns
Delay Time, CSb Rise to SDIO Tri-State	T_{D3}	—	—	12.5	ns
Setup Time, CSb to SCLK	T_{SU1}	25	—	—	ns
Hold Time, SCLK Fall to CSb	T_{H1}	25	—	—	ns

Parameter	Symbol	Min	Typ	Max	Unit
Setup Time, SDI to SCLK Rise	T_{SU2}	12.5	—	—	ns
Hold Time, SDI to SCLK Rise	T_{H2}	12.5	—	—	ns
Delay Time Between Chip Selects (CSb)	T_{CS}	1.9	—	—	T_c

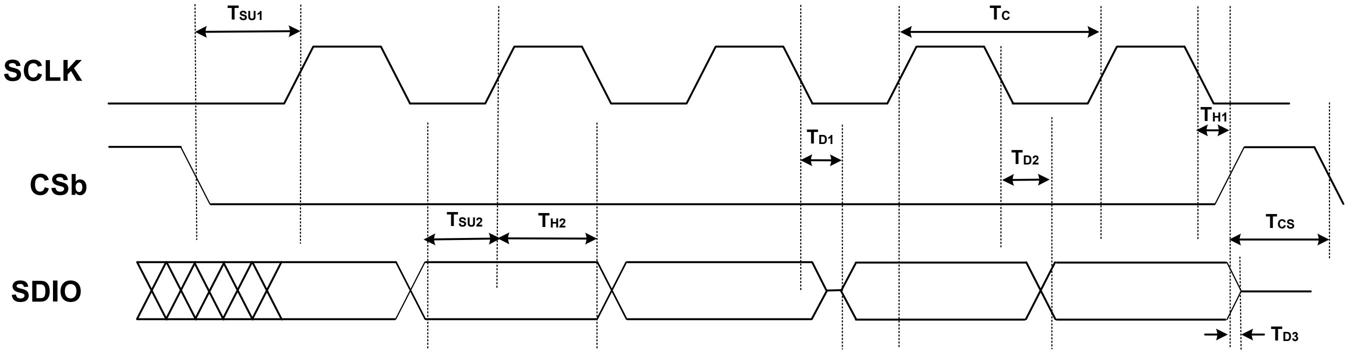


Figure 5.3. 3-Wire SPI Serial Interface Timing

Table 5.12. Crystal Specifications

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Crystal Frequency[1]	f_{XTAL}		—	54	—	MHz
Total Frequency Tolerance[2]	f_{RANGE}		–100	—	+100	ppm
Load Capacitance	C_L		—	8	—	pF
Crystal Output Capacitance	C_O		—	—	2	pF
Equivalent Series Resistance	r_{ESR}		—	—	23	Ω
Crystal Drive Level	d_L	The crystal resonator must be able to tolerate 200 μW of drive level	—	—	200	μW

Note:

1. Refer to the Si5380 Reference Manual for qualified crystals. The Si5380 is designed to operate with crystals that meet the specifications in the Table 5.14 Absolute Maximum Ratings[1,2,3, 4] on page 33. See the Si5380 Reference Manual for a list of qualified 54 MHz crystals.
2. Includes initial tolerance, drift after reflow, change over temperature (–40 °C to +85 °C), V_{DD} variation, load pulling, and aging.

Table 5.13. Thermal Characteristics[1]

Parameter	Symbol	Test Condition	Value	Unit
Si5380—64QFN				

Parameter	Symbol	Test Condition	Value	Unit
Thermal Resistance Junction to Ambient	Θ_{JA}	Still Air	22	°C/W
		Air Flow 1 m/s	19.4	
		Air Flow 2 m/s	18.3	
Thermal Resistance Junction to Case	Θ_{JC}		9.5	
Thermal Resistance Junction to Board	Θ_{JB}		9.4	
Thermal Resistance Junction to Board	Ψ_{JB}		9.3	
Thermal Resistance Junction to Top Center	Ψ_{JT}		0.2	

Note:

1. Based on PCB Dimension: 3x4.5”, PCB Thickness: 1.6 mm, PCB Land/Via: 36, Number of Cu Layers: 4.

Table 5.14. Absolute Maximum Ratings[1,2,3, 4]

Parameter	Symbol	Test Condition	Value	Unit
DC Supply Voltage	V_{DD}		–0.5 to 3.8	V
	V_{DDA}		–0.5 to 3.8	V
	V_{DDO}		–0.5 to 3.8	V
Input Voltage Range	V_{I1}	IN0-IN3/FB_IN	–0.85 to 3.8	V
	V_{I2}	IN_SEL[1:0], RSTb, PDNb,OEb, SYNCb, I2C_SEL, SCLK, A0/CSb, A1/SDO, SDA/SDIO	–0.5 to 3.8	
	V_{I3}	XA/XB	–0.5 to 2.7	V
Latch-up Tolerance	LU		JESD78 Compliant	
ESD Tolerance	HBM	100 pF, 1.5 kΩ	2.0	kV
Storage Temperature Range	T_{STG}		–55 to 150	°C
Junction Temperature	T_{JCT}		–55 to 150	°C
Soldering Temperature (Pb-free profile)[4]	T_{PEAK}		260	°C
Soldering Temperature Time at T_{PEAK} (Pb-free profile)[4]	T_P		20 to 40	sec

Parameter	Symbol	Test Condition	Value	Unit

Note:

1. Permanent device damage may occur if the absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as specified in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. 64-QFN is RoHS-6 compliant.
3. For MSL rating and additional packaging information, go to http://www.silabs.com/support/quality/pages/RoHSInformation.aspx.
4. The device is compliant with JEDEC J-STD-020.

6. Typical Application Diagrams

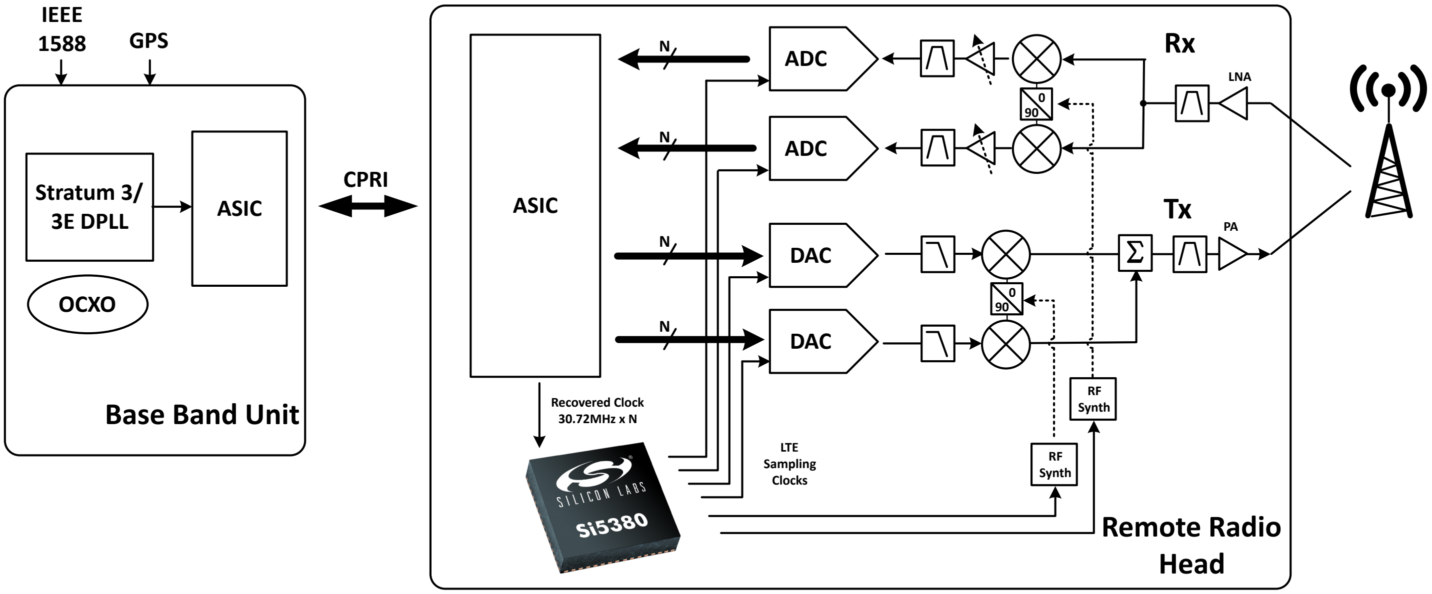


Figure 6.1. LTE Base Station Remote Radio Head

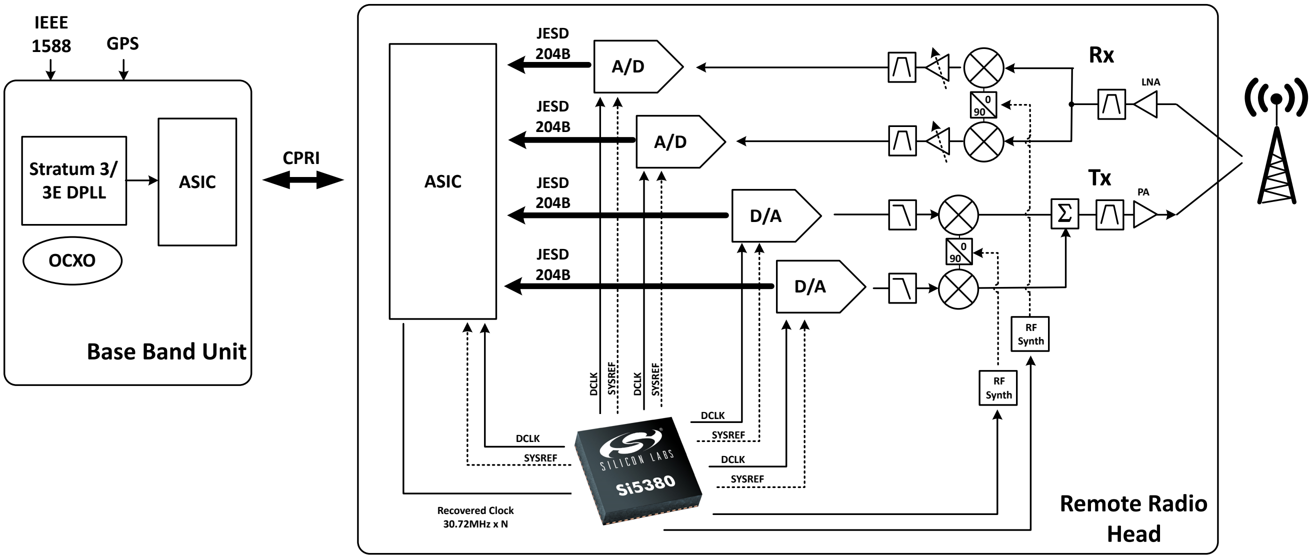


Figure 6.2. LTE Base Station Using JESD204B Data Converters

7. Detailed Block Diagram

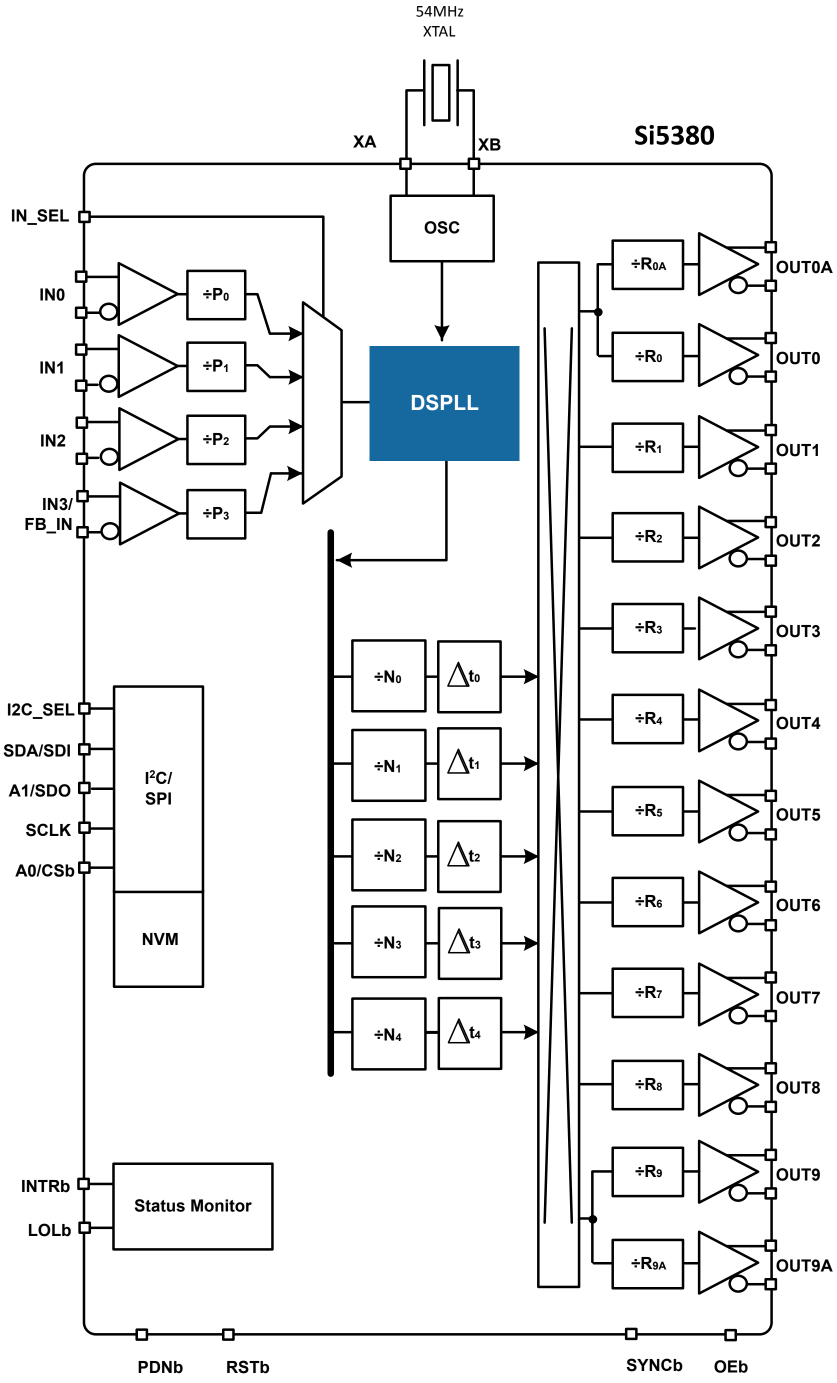
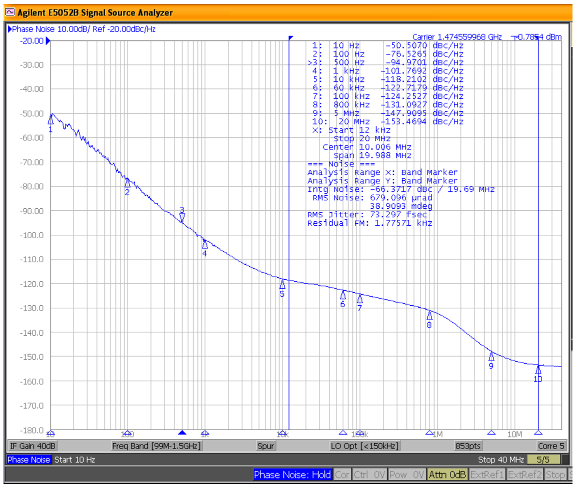


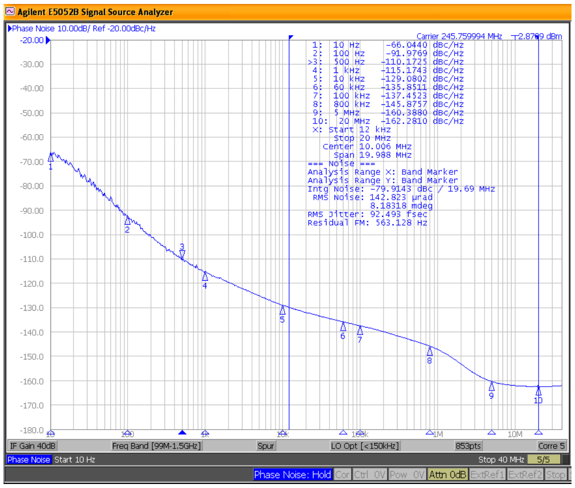
Figure 7.1. Si5380 Block Diagram

8. Typical Operating Characteristics (Phase Noise & Jitter)



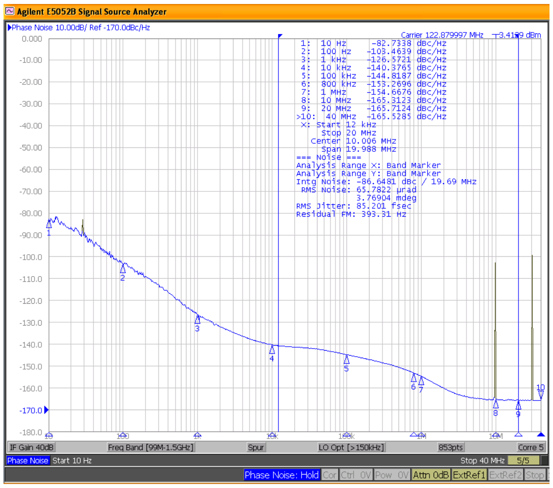
```
Carrier 1.474559968 GHz   -0.7854 dBm
 1:  10 Hz     -50.5070 dBc/Hz
 2:  100 Hz    -76.5265 dBc/Hz
>3:  500 Hz    -94.9701 dBc/Hz
 4:  1 kHz    -101.7692 dBc/Hz
 5:  10 kHz   -118.2102 dBc/Hz
 6:  60 kHz   -122.7179 dBc/Hz
 7:  100 kHz  -124.2527 dBc/Hz
 8:  800 kHz  -131.0927 dBc/Hz
 9:  5 MHz    -147.9095 dBc/Hz
10:   20 MHz  -153.4694 dBc/Hz
 X: Start 12 kHz
     Stop 20 MHz
   Center 10.006 MHz
     Span 19.988 MHz
=== Noise ===
Analysis Range X: Band Marker
Analysis Range Y: Band Marker
Intg Noise: -66.3717 dBc / 19.69 MHz
 RMS Noise: 679.096 µrad
            38.9093 mdeg
RMS Jitter: 73.297 fsec
Residual FM: 1.77571 kHz
```

Figure 8.1. Typical Phase Noise and Jitter—1,474.56 MHz



```
Carrier 245.759994 MHz   2.8789 dBm
 1:  10 Hz     -66.0440 dBc/Hz
 2:  100 Hz    -91.9769 dBc/Hz
>3:  500 Hz   -110.1725 dBc/Hz
 4:  1 kHz    -115.1743 dBc/Hz
 5:  10 kHz   -129.0802 dBc/Hz
 6:  60 kHz   -135.8511 dBc/Hz
 7:  100 kHz  -137.4523 dBc/Hz
 8:  800 kHz  -145.8757 dBc/Hz
 9:  5 MHz    -160.3880 dBc/Hz
10:   20 MHz  -162.2810 dBc/Hz
 X: Start 12 kHz
     Stop 20 MHz
   Center 10.006 MHz
     Span 19.988 MHz
=== Noise ===
Analysis Range X: Band Marker
Analysis Range Y: Band Marker
Intg Noise: -79.9143 dBc / 19.69 MHz
 RMS Noise: 142.823 µrad
            8.18318 mdeg
RMS Jitter: 92.493 fsec
Residual FM: 563.128 Hz
```

Figure 8.2. Typical Phase Noise and Jitter—245.76 MHz



```
Carrier 122.879997 MHz   3.4139 dBm
 1:  10 Hz     -82.7338 dBc/Hz
 2:  100 Hz   -103.4639 dBc/Hz
 3:  1 kHz    -126.5721 dBc/Hz
 4:  10 kHz   -140.3765 dBc/Hz
 5:  100 kHz  -144.8187 dBc/Hz
 6:  800 kHz  -153.2696 dBc/Hz
 7:  1 MHz    -154.6676 dBc/Hz
 8:  10 MHz   -165.3123 dBc/Hz
 9:  20 MHz   -165.7124 dBc/Hz
>10:  40 MHz  -165.5285 dBc/Hz
 X: Start 12 kHz
     Stop 20 MHz
   Center 10.006 MHz
     Span 19.988 MHz
=== Noise ===
Analysis Range X: Band Marker
Analysis Range Y: Band Marker
Intg Noise: -86.6481 dBc / 19.69 MHz
 RMS Noise: 65.7822 µrad
            3.76904 mdeg
RMS Jitter: 85.201 fsec
Residual FM: 393.31 Hz
```

Figure 8.3. Typical Phase Noise and Jitter—122.88 MHz

9. Pin Description

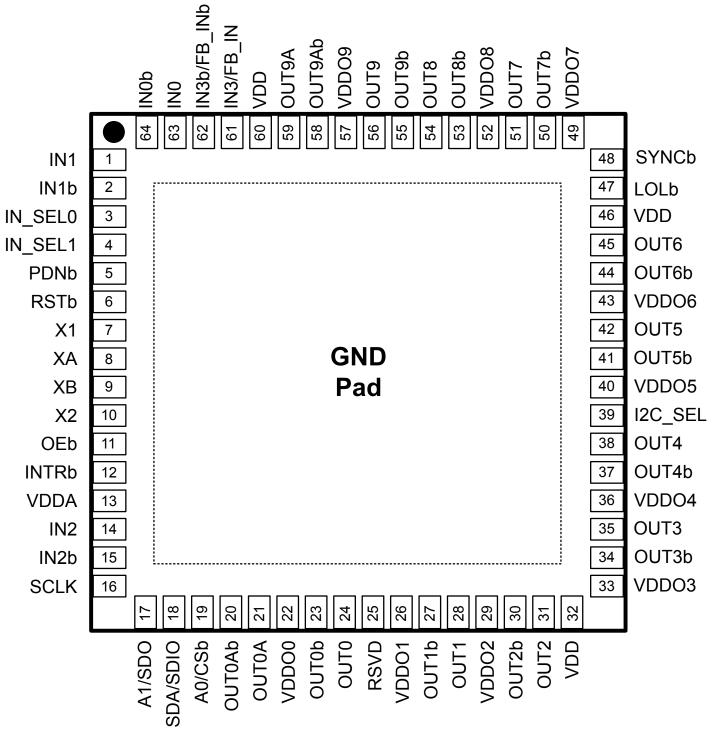


Figure 9.1. Si5380 64-QFN Top View

Table 9.1. Pin Descriptions

Pin Name	Pin Number	Pin Type[1]	Function
XA	8	I	**Crystal Input.** Input pin for external crystal (XTAL). Alternatively these pins can be driven with an external reference clock (REFCLK). An internal register bit selects XTAL or REFCLK mode. Default is XTAL mode. Single-ended inputs must be connected to the XA pin, with the XB pin appropriately terminated.
XB	9	I	
X1	7	I	**XTAL Shield.** Connect these pins directly to the crystal ground pins. Both the X1/X2 pins and Crystal ground pins should be separated from the PCB ground plane. Refer to the Reference Manual for layout guidelines.
X2	10	I	
IN0	63	I	**Clock Inputs.** These pins accept an input clock for synchronizing the device. They support both differential and single-ended clock signals. Refer to section 3.3.1 Input Configuration and Terminations for input termination options. These pins are high-impedance and must be terminated externally, when being used. The negative side of the differential input must be ac-grounded when accepting a single-ended clock. Unused inputs may be left unconnected.
IN0b	64	I	
IN1	1	I	
IN1b	2	I	
IN2	14	I	
IN2b	15	I	

Pin Name	Pin Number	Pin Type[1]	Function
IN3/FB_IN	61	I	**Clock Input 3/External Feedback Input.** By default, these pins are used as the 4th clock input (IN3/IN3b). They can also be used as the external feedback input (FB_IN/FB_INb) for the optional zero delay mode. See section 5.3.6 for details on the optional zero delay mode.
IN3b/FB_INb	62	I	
Outputs			
OUT0A	21	O	**Output Clocks.** These output clocks support programmable signal amplitude and common mode voltage. Desired output signal format is configurable using register control. Termination recommendations are provided in the sections, 3.5.4 Differential Output Modes and 3.5.6 LVCMOS Output Terminations. Unused outputs should be left unconnected.
OUT0Ab	20	O	
OUT0	24	O	
OUT0b	23	O	
OUT1	28	O	
OUT1b	27	O	
OUT2	31	O	
OUT2b	30	O	
OUT3	35	O	
OUT3b	34	O	
OUT4	38	O	
OUT4b	37	O	
OUT5	42	O	
OUT5b	41	O	
OUT6	45	O	
OUT6b	44	O	
OUT7	51	O	
OUT7b	50	O	
OUT8	54	O	
OUT8b	53	O	
OUT9	56	O	
OUT9b	55	O	
OUT9A	59	O	
OUT9Ab	58	O	
Serial Interface			
I2C_SEL	39	I	**I2C Select.** This pin selects the serial interface mode as I^2C (I2C_SEL = 1) or SPI (I2C_SEL = 0). This pin is internally pulled high.

Pin Name	Pin Number	Pin Type[1]	Function
SDA/SDIO	18	I/O	**Serial Data Interface.** This is the bidirectional data pin (SDA) for the I^2C mode, the bidirectional data pin (SDIO) in the 3-wire SPI mode, or the input data pin (SDI) in 4-wire SPI mode. When in I^2C mode or unused, this pin must be pulled-up using an external resistor of at least 1 kΩ. No pull-up resistor is needed when in SPI mode. This pin is 3.3 V tolerant.
A1/SDO	17	I/O	**Address Select 1/Serial Data Output.** In I^2C mode this pin functions as the A1 address input pin. In 4-wire SPI mode, this is the serial data output (SDO) pin. This pin is 3.3 V tolerant. This pin must be pulled-up externally when unused.
SCLK	16	I	**Serial Clock Input.** This pin functions as the serial clock input for both I^2C and SPI modes. When in I^2C mode or unused, this pin must be pulled-up using an external resistor of at least 1 kΩ. No pull-up resistor is needed when in SPI mode. This pin is 3.3 V tolerant.
A0/CSb	19	I	**Address Select 0/Chip Select.** This pin functions as the hardware controlled address A0 in I^2C mode. In SPI mode, this pin functions as the chip select input (active low). This pin is internally pulled-up. This pin is 3.3 V tolerant.
Control/Status			
INTRb	12	O	**Interrupt.** [2] This pin is asserted low when a change in device status has occurred. This pin must be pulled-up externally using a resistor of at least 1 kΩ. It should be left unconnected when not in use.
PDNb	5	I	**Power Down.** [2] The device enters into a low power mode when this pin is pulled low. This pin is internally pulled-up. This pin is 3.3 V tolerant. It can be left unconnected when not in use.
RSTb	6	I	**Device Reset.** [2] Active low input that performs power-on reset (POR) of the device. Resets all internal logic to a known state and forces the device registers to their default values. Clock outputs are disabled during reset. This pin is internally pulled-up. This pin is 3.3 V tolerant.
OEb	11	I	**Output Enable.** [2] This pin disables all outputs when held high. This pin is internally pulled low and can be left unconnected when not in use. This pin is 3.3 V tolerant.
LOLb	47	O	**Loss Of Lock.** [2] This output pin indicates when the DSPLL is locked (high) or out-of-lock (low). When in use, this pin must be pulled-up using an external resistor of at least 1 kΩ. It can be left unconnected when not in use.
SYNCb	48	I	**Output Clock Synchronization.** [2] An active low signal on this pin resets the output dividers for the purpose of re-aligning the output clocks. This pin is internally pulled-up and can be left unconnected when not in use.

Pin Name	Pin Number	Pin Type[1]	Function
IN_SEL0	3	I	**Input Reference Select.** [2] The IN_SEL[1:0] pins are used in manual pin controlled mode to select the active clock input as shown in Table 3.2 Table 6.2 on page 8. These pins are internally pulled-down and may be left unconnected when unused.
IN_SEL1	4	I	
RSVD	25		**Reserved.** Leave disconnected.
Power			
VDD	32	P	**Core Supply Voltage.** The device operates from a 1.8 V supply. A 1 uF bypass capacitor should be placed very close to each pin.
VDD	46	P	
VDD	60	P	
VDDA	13	P	**Core Supply Voltage 3.3 V**. This core supply pin requires a 3.3 V power source. A 1 uF bypass capacitor should be placed very close to this pin.
VDDO0	22	P	**Output Clock Supply Voltage. Supply voltage (3.3 V, 2.5 V, 1.8 V) for OUTx, OUTxb Outputs**. Note that VDDO0 supplies power to OUT0 and OUT0A; VDDO9 supplies power to OUT9 and OUT9A. Leave VDDO pins of unused output drivers unconnected. An alternative option is to connect the VDDO pin to a power supply and disable the output driver to minimize current consumption. A 1 μF bypass capacitor should be placed very close to each connected VDDO pin.
VDDO1	26	P	
VDDO2	29	P	
VDDO3	33	P	
VDDO4	36	P	
VDDO5	40	P	
VDDO6	43	P	
VDDO7	49	P	
VDDO8	52	P	
VDDO9	57	P	
GND PAD		P	**Ground Pad**. This pad provides connection to ground and must be connected for proper operation.

Note:

1. I = Input, O = Output, P = Power
2. The IO_VDD_SEL control bit (0x0943 bit 0) selects 3.3 V or 1.8 V operation.

10. Package Outline

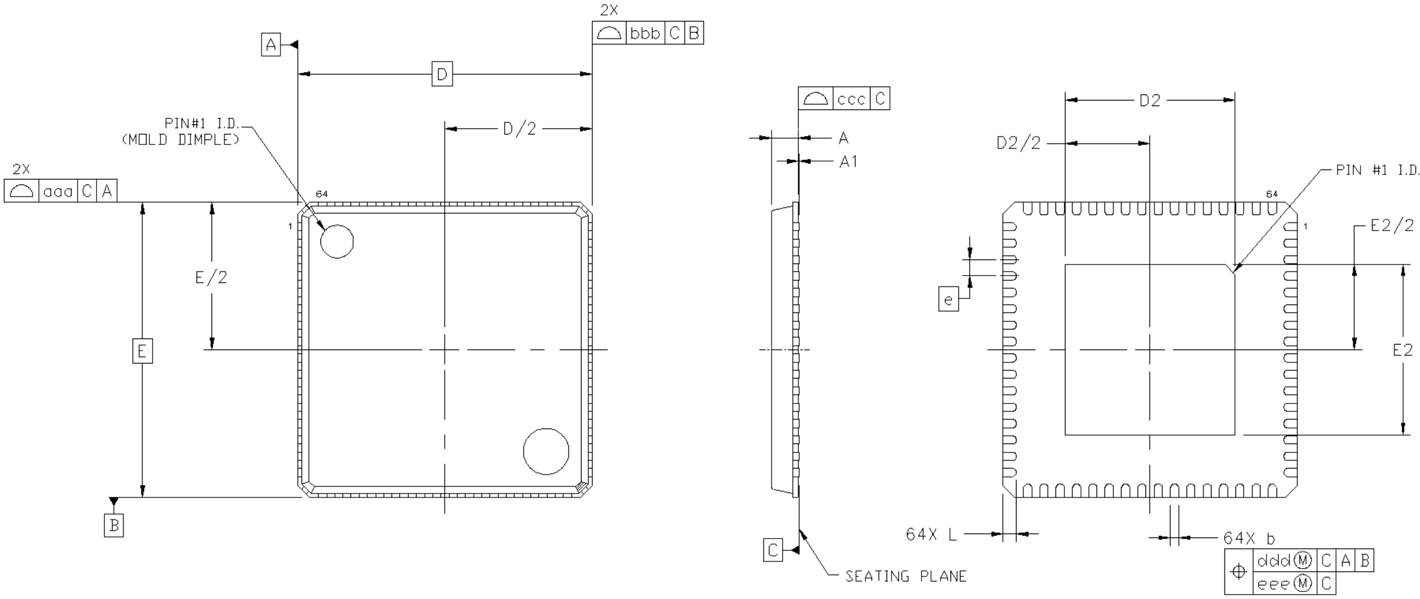


Figure 10.1. Si5380 9x9 mm 64-QFN Package Diagram

Table 10.1. Package Diagram Dimensions

Dimension	MIN	NOM	MAX
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
b	0.18	0.25	0.30
D	9.00 BSC		
D2	5.10	5.20	5.30
e	0.50 BSC		
E	9.00 BSC		
E2	5.10	5.20	5.30
L	0.30	0.40	0.50
aaa	—	—	0.10
bbb	—	—	0.10
ccc	—	—	0.08
ddd	—	—	0.10

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to the JEDEC Solid State Outline MO-220.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

11. PCB Land Pattern

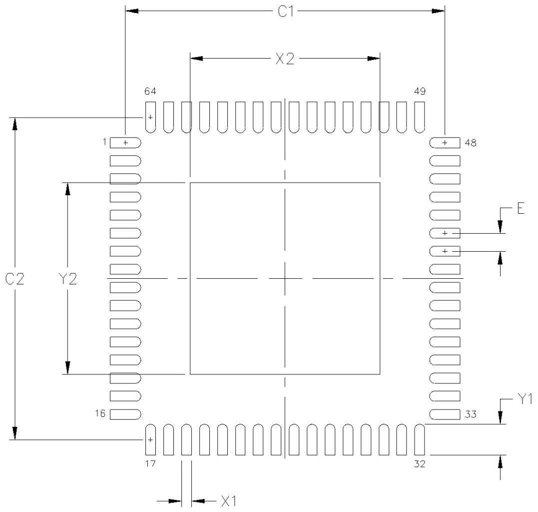


Figure 11.1. 9x9 mm 64-QFN Land Pattern

Table 11.1. PCB Land Pattern Dimensions

Dimension	Max
C1	8.90
C2	8.90
E	0.50
X1	0.30
Y1	0.85
X2	5.30
Y2	5.30

Dimension	Max
General Note: 1. All dimensions shown are in millimeters (mm) unless otherwise noted. 2. This Land Pattern Design is based on the IPC-7351 guidelines. 3. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition is calculated based on a fabrication Allowance of 0.05 mm. **Solder Mask Design** 1. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad. **Stencil Design** 1. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release. 2. The stencil thickness should be 0.125 mm (5 mils). 3. The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pads. 4. A 3x3 array of 1.25 mm square openings on 1.80 mm pitch should be used for the center ground pad. **Card Assembly** 1. A No-Clean, Type-3 solder paste is recommended. 2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.	

12. Top Marking

64-QFN

Figure 12.1. Si5380 Top Marking

Table 12.1. Top Marking Explanation

Line	Characters	Description
Line 1	Si5380A-	Base part number for Ultra Low Phase Noise, 12-output JESD204B Clock Generator: Si5380A: 12-output clock generator in 64-QFN package. – = Dash character.
Line 2	Rxxxxx-GM	R = Product revision. (See Ordering Guide for current ordering revision). xxxxx = Customer specific NVM sequence number. Optional NVM code assigned for custom, factory pre-programmed devices. Characters are not included for standard, factory default configured devices. See Ordering Guide for more information. -GM = Package (QFN) type and temperature range (–40 to +85 °C).
Line 3	YYWWTTTTTT	YYWW = Characters correspond to the year (YY) and work week (WW) of package assembly. TTTTTT = Manufacturing trace code.
Line 4	Circle w/ 1.6 mm diameter	Pin 1 indicator; left-justified
	e4 TW	Pb-free symbol; Center-Justified TW = Taiwan; Country of Origin (ISO Abbreviation)

13. Device Errata

Please log in or register at www.silabs.com to access the device errata document.

ClockBuilder Pro

One-click access to Timing tools, documentation, software, source code libraries & more. Available for Windows and iOS (CBGo only).

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