Si5118 SmartClock™ Synthesizer

AEC-Q100 Qualified SmartClock™ Synthesizer

The Si5118 is a SmartClock Synthesizer intended for automotive electronics applications where health monitoring and fault detection functions of a reference clock are needed in between the frequency source and the intended endpoint. FPGAs, SoCs, and ASICs often include on-chip PLLs for frequency synthesis, which can supply output clocks to other endpoints within a system design. Si5118 monitors the health of those clocks, can output fault detection flags, and migrate to a redundant backup reference source if a fault is detected on the primary source. In the event of both primary input reference and backup redundant crystal reference frequencies fail, Si5118 enters into AlwaysOn mode to allow the output clocks to continue operating within +/-5% of the output frequency, enabling the system to continue sourcing reference clocks while entering a safe state.

Applications:

- ADAS ECUs
- Automotive Networking/Gateways
- Digital Cockpit/IVI
- Lidar/Radar Sensors
- Automated Driving ECUs
- Camera/Vision Systems

KEY FEATURES

- Input reference clock health monitoring
- Fault detection output flags
- Local backup reference source
- Up to 7 reference clock outputs
- Frequency range: 16 - 50MHz
- AlwaysOn mode
- Automotive grade 2: -40 to +105C
- 40-pin QFN
- AEC-Q100 qualified
- AEC-Q006 qualified

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1. Features List

- SmartClock health monitoring and fault detection capability of input sources
- Primary and redundant input reference sources
- AlwaysON sources clock outputs if primary/secondary sources fault
- Up to 7 reference clock outputs
- Frequency range: 16-50 MHz
- User-configurable clock output signal format per output: LVDS, LVPECL, HCSL, LVCMOS
- 1.8 V, 2.5 V, 3.3 V core VDD
- Independent output supply pins for each bank of outputs:
  - 1.8 V, 2.5 V, or 3.3 V differential
  - 1.5 V, 1.8 V, 2.5 V, 3.3 V LVCMOS
- Integrated power supply filtering
- AEC-Q100 qualified
- AEC-Q006 qualified
- Automotive grade 2 temperature range: –40 to +105 °C
- RoHS-6 compliant

2. Ordering Guide

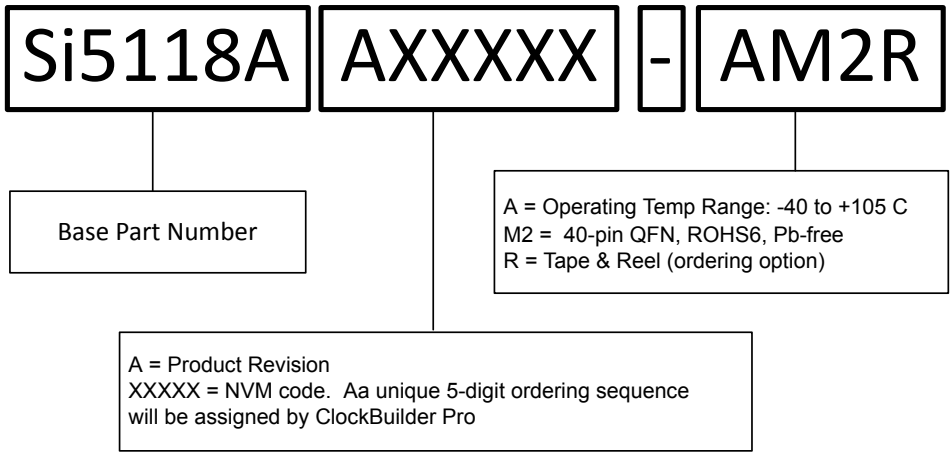


Figure 2.1. Orderable Part Number Guide

3. Functional Description

The Si5118 is a SmartClock synthesizer, intended for automotive electronics applications where health monitoring and fault detection functions of a reference clock are needed between a frequency source and the intended endpoint. FPGAs, SoCs, and ASICs often include on-chip PLLs for frequency synthesis, and can often be supplied to other endpoints within a system design. Si5118 monitors the health of those clocks, can output fault detection flags, and migrate to a redundant backup reference source if a fault is detected on the primary source. In the event of both primary input reference and backup redundant crystal reference frequencies fail, Si5118 enters into AlwaysOn mode to allow the output clocks to continue operating within +/-5% of the output frequency, enabling the system to continue sourcing reference clocks while entering a safe state.

The Si5118 is capable of taking three input reference sources: a primary clock generated by an external source (such as a crystal oscillator, FPGA, SoC), a backup crystal reference source, and a feedback reference source from one of the SI5118 outputs. All three input sources must be the same frequency. The device actively monitors the health of the primary reference input source using the SmartClock out of frequency (FOOF) monitors, and provides up to 7 reference clock outputs of the same frequency that can be supplied to various endpoints within the system design.

If a FOOF fault is detected on the primary input reference clock, the device communicates an output signal flag to an external microcontroller or system safety manager.. To ensure the Si5118 output clocks continue to run uninterrupted, the microcontroller or system safety manager can instruct the Si5118 to change the input reference source from the primary clock source to the backup crystal source using the CLK_SEL pins. Should the backup crystal reference source also fault, the device will again communicate the failure to the external microcontroller or system safety manager, and then will enter AlwaysOn mode. AlwaysOn mode allows the output clocks to continue operating within +/-5% of the output frequency, enabling the system to continue sourcing reference clocks even though the primary and backup sources have faulted.

3.1 Functional Block Diagram

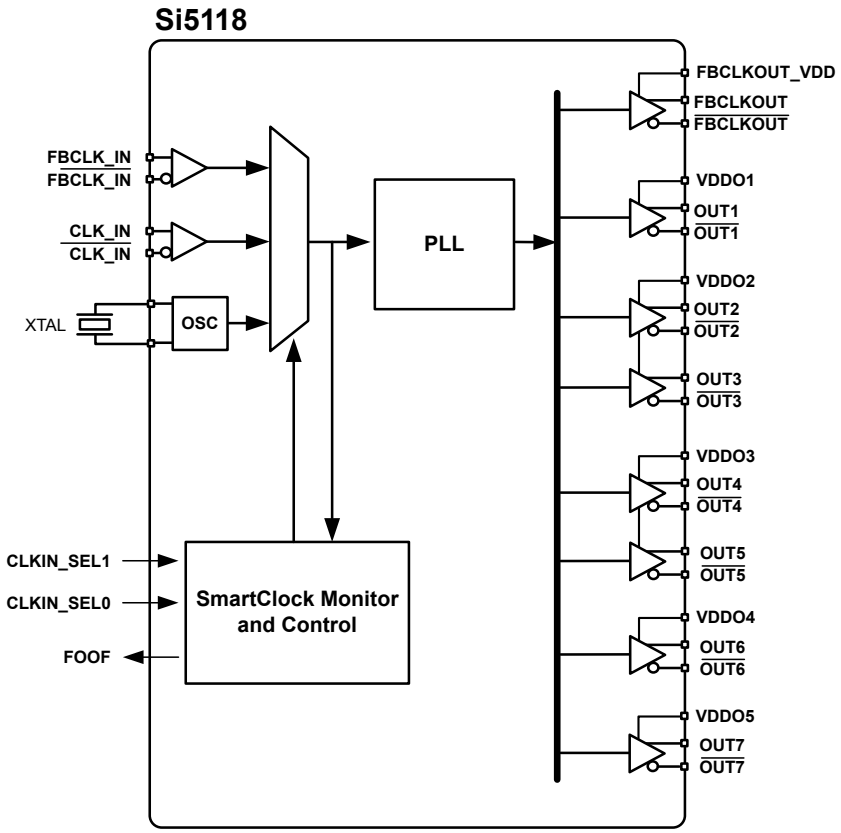


Figure 3.1. Si5118 Block Diagram

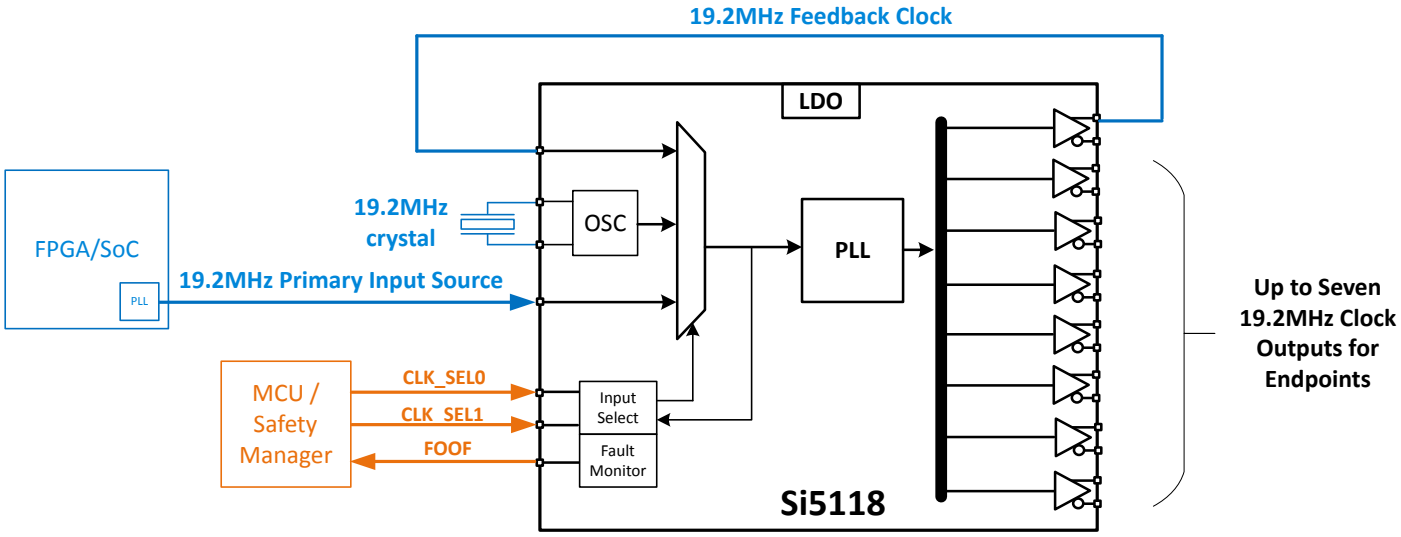


Figure 3.2. Si5118 System Level Block Diagram

Note: The Si5118 supports input frequencies of 16-50 MHz. All three input sources must be the same frequency.

3.2 Modes of Operation

The primary functions of the Si5118 are to:

1. Monitor the health of an input reference clock and detect if a fault has occurred,
2. Communicate a fault condition to an external microcontroller or safety manager IC, and
3. Transition output clocks to a redundant backup reference source in the event of a fault on the primary reference input.

The Fault Monitor continuously monitors the status of the input clock reference to the PLL. If a fault condition is detected, a signal is provided to the external microcontroller or system safety manager IC, which can then direct the Si5118 to switch the reference source from the primary to the backup input source. The Fault Monitor block includes 3 signals, 2 input and 1 output, as follows:

- FOOF (Fast Out of Frequency) output: This output asserts when the difference between the PLL input reference frequency and PLL feedback frequency falls outside of a set band. FOOF assertion is an indication the PLL has either fallen out of lock or other PLL fault condition has occurred and the PLL may either be unlocked or otherwise not operational. The band limits are automatically set by ClockBuilder Pro based on the reference input frequency.
- CLKIN_SEL[1:0]: Two logic inputs used to select one of 4 possible input clock sources for PLL reference.

CLK_SEL1	CLK_SEL0	Input Source to PLL
0	0	Disabled
0	1	Crystal reference source (backup)
1	0	External clock input (primary)
1	1	Feedback clock input

The FOOF signal output indicates that a fault condition has occurred. No action is automatically taken by the Si5118 as a result of this fault indication. Si5118 is intended to be used with an external device, such as an ASIL-rated microcontroller or other system safety manager IC, which must monitor the FOOF output from the Si5118. In the event that Si5118 detects a fault, the FOOF output signal is asserted and the external microcontroller is informed. The microcontroller can subsequently make a system level decision on the course of action to take in order to maintain acceptable levels of system safety. For example, microcontroller can then instruct the Si5118 to migrate the PLL input reference to the redundant backup crystal source by using the CLKIN_SEL[1:0] inputs, ensuring the Si5118 outputs continue sourcing reference clocks to the endpoints, or take action at the system level based on the severity of the detected fault.

When running system power-up or other diagnostics, the microcontroller software can test the functionality of FOOF by selecting the input “Disabled” setting and then confirming assertion FOOF as a result. Similarly, the microcontroller software can also confirm proper operation of any alternate clock input sources by selecting the alternate source(s) and confirming the FOOF is not asserted.

In the event of faults detected on both the primary input clock source, as well as the backup crystal source, the Si5118 enters into AlwaysOn mode. In this mode, the output clocks will continue to run; however, they will experience degraded frequency stability (within +/-5%).

3.2.1 Initialization

When power is applied, the device begins an initialization period where it downloads default register values and configuration data from NVM and performs other initialization tasks. The clock outputs will be squelched until the device initialization is done. Controlling the device through the CLK_SEL pins is possible once this initialization period is complete.

3.3 Inputs

The Si5118 supports input frequencies of 16-50MHz. All three input sources must be the same frequency.

3.3.1 Crystal Reference

A 16-50MHz crystal reference serves as the backup reference source, and must be equal to the same frequency as the primary input clock source. Total stability of the crystal source should not exceed the stability level of the input clock reference.

The external crystal should be connected to the Si5118's XIN/XOUT inputs as shown below. For purposes of calculating external crystal loading capacitor values, the internal stray loading capacitance is approximately 2.5 pf.

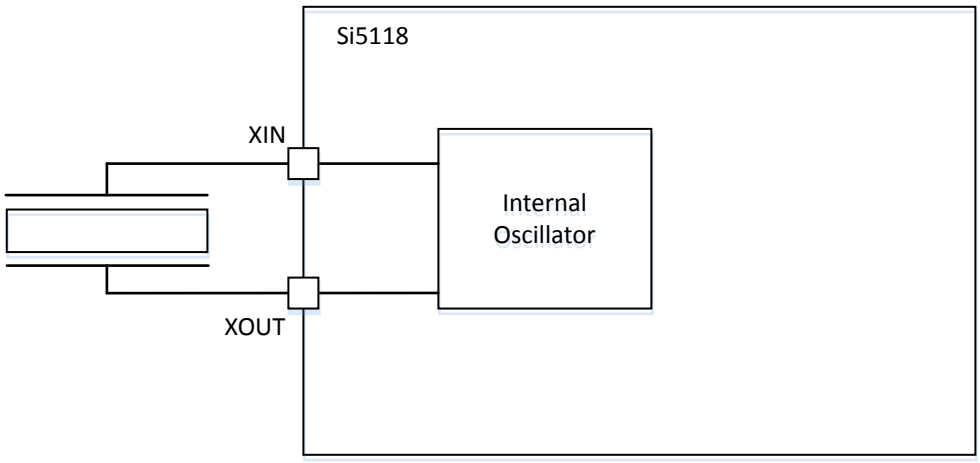


Figure 3.3. External Crystal Connection

A list of recommended AEC-Q200 qualified crystals for the Si5118 can be found in AN1239: Recommended Automotive AEC-Q200 Crystals for Si5332 and Si5225x Clock Generators.

3.3.2 Primary Reference Input Clock

When supplying differential input clocks into the CLKIN_x/CLKIN_x# inputs, AC or DC coupling can be used. The figures below show the AC and DC coupled differential input clock connection to the Si5118 clock inputs. (There are some restrictions to observe when using DC coupled input clocks as described further below.) The input clock Format Termination shown in below figures is dependent on the driver's termination requirements. The Si5118 clock inputs are high impedance inputs and the clock driven into the Si5118 must meet the Clock Input Specifications electrical requirements specified in Table 4.3 on page 19. When using differential input clocks, the respective Si5118 input must be configured as a differential input using CBPro.

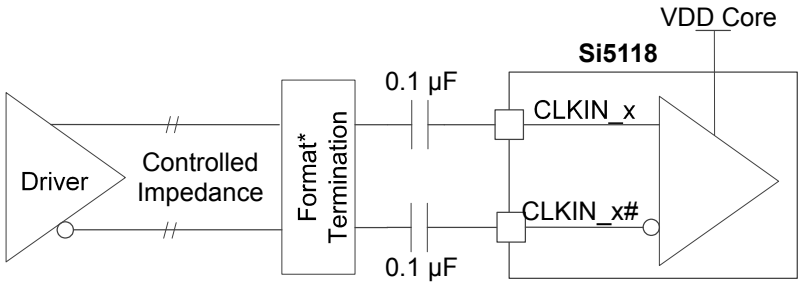


Figure 3.4. AC-Coupled Differential Input Clock (LVDS, LVPECL, HCSL, CML, etc.)

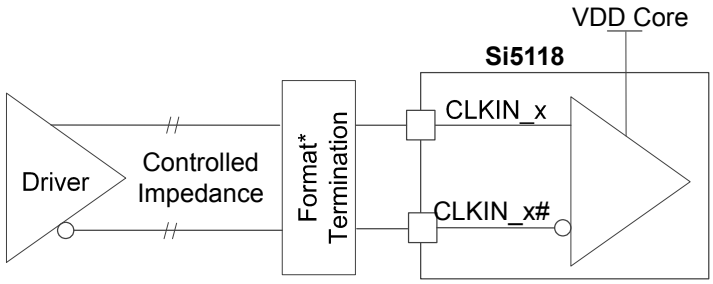


Figure 3.5. DC-Coupled Differential Input Clock

To determine if a specific DC-coupled differential input clock arrangement is supported, refer to the table below.

Table 3.1. Si5118 Input Clock Coupling Restrictions (AC or DC)

Format	VDD_Core		
	3.3 V	2.5 V	1.8 V
LVDS 3.3 V/2.5 V	AC or DC	AC only	AC only
LVDS 1.8 V	AC or DC	AC only	AC only
LVPECL 3.3 V/2.5 V	AC or DC	AC only	AC only
HCSL	AC or DC	AC or DC	AC only
CML	AC only	AC only	AC only
LVCMOS	AC only	AC only	AC only

Note:
1. For DC-coupled, input clock peak voltage must not exceed VDD_Core and minimum voltage must not be below GND.
2. For AC-coupled, peak swing must not exceed VDD_Core.

The figure below shows how to connect single-ended input clocks, such as LVCMOS. The single-ended clock must be connected to the positive CLKIN input as shown below.

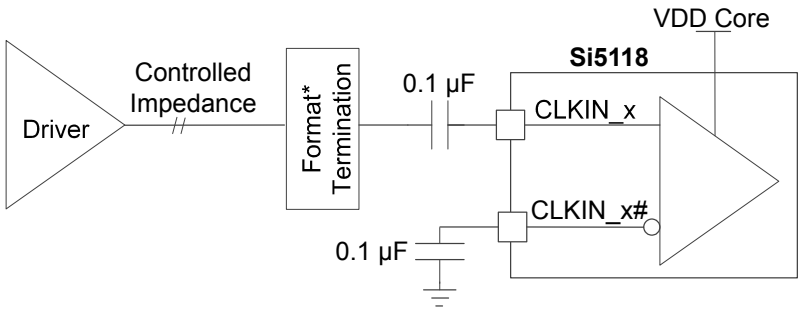


Figure 3.6. AC-Coupled Single-Ended Input Clock (LVCMOS)

For AC-coupled single-ended input clocks (such as LVCMOS) the Vswing of the clock must be limited to the maximum VDD_Core voltage. (VDD_Core is defined as the following group of VDD supply pins: VDD_DIG, VDDA, and VDD_XTAL.) The Input clock format termination is dependent on the driver format used and is usually specified by the driving device and/or industry standard clock format specification.

For example, in the case of using a LVCMOS input clock, the driving device may recommend a series termination resistor. When using LVCMOS input clocks the Si5118 input must be configured in LVCMOS mode in CBPro. The single-ended CLKIN input of Si5118 is a high impedance input.

3.3.3 Input Selection

The active clock input is selected by defining two universal input pins as CLKIN_SEL[1:0] in ClockBuilder Pro. If there is no clock signal on the selected input at power-up, the device will not generate output clocks.

The CLK_SEL[1:0] hardware input pins control the input reference source to the PLL. Upon switching the input clock source, the output will not be glitch free. It is intended for the user to set this pin to a known state before the system is powered up or have the receiver address any unintended output signals when switching to a different input source clock.

The SmartClock health monitoring and fault detection features utilize the CLK_SEL pins. If a fault is detected on the primary input source, the external MCU can toggle the CLK_SEL pins to migrate the PLL reference source from the faulted primary input source to the backup crystal input source to ensure Si5118 clock outputs continue to operate.

When running system power-up or other diagnostics, the MCU software can test the functionality of FOOF SmartClock function by selecting the Input Disabled setting and then confirming assertion of FOOF as a result. Similarly, the MCU software can also confirm proper operation of any alternate input sources by selecting the alternate source(s) and confirming FOOF is not asserted.

Table 3.2. CLKIN_SEL[1:0] Input Clock Selects: Input Clock Selection and Validation

CLKIN_SEL1	CLKIN_SEL0	Clock Selected	Note
0	0	Input disabled	To test input clock fault condition
0	1	Crystal Oscillator Input	
1	0	External Reference Clock Input	
1	1	Feedback Clock Input	

3.4 Outputs

The Si5118 supports up to 8 differential output drivers, one of which must be used as the feedback input reference source. Each output can be independently configured as a differential pair or as dual LVCMOS outputs when developing a configuration file in ClockBuilder Pro.

3.4.1 Output Signal Format

The differential output swing and common mode voltage are compatible with a wide variety of signal formats including HCSL, LVDS and LVPECL. In addition to supporting differential signals, any of the outputs can be configured as LVCMOS drivers, enabling the device to support both differential and single-ended clock outputs. Output formats can be defined in ClockBuilder Pro. Each output driver in Si5118 can be defined to its own signal format level during ClockBuilder Pro configuration file development.

3.4.2 Differential Output Terminations

LVDS Driver Termination

For a general LVDS interface, the recommended value for the differential termination impedance (Z_T) is between 90 Ω and 132 Ω. The actual value should be selected to match the differential impedance (Z0) of the transmission line. A typical point-to-point LVDS design uses a 100 Ω parallel resistor at the receiver and a 100 Ω differential transmission-line environment. To avoid any transmission-line reflection issues, surface mount the components and place them as close to the receiver as possible. The standard LVDS termination schematic as shown in Figure 3.7 Standard LVDS Termination on page 11 can be used with either type of output structure. Figure 3.8 Optional LVDS Termination on page 11, which can also be used with both output types, is an optional termination with center tap capacitance to help filter common mode noise. The capacitor value should be approximately 0.01 to 0.1 µF. If using a non-standard termination, please contact Silicon Labs to confirm if the output structure is current source or voltage source type. In addition, since these outputs are LVDS compatible, the input receiver's amplitude and common-mode input range should be verified for compatibility with the output.

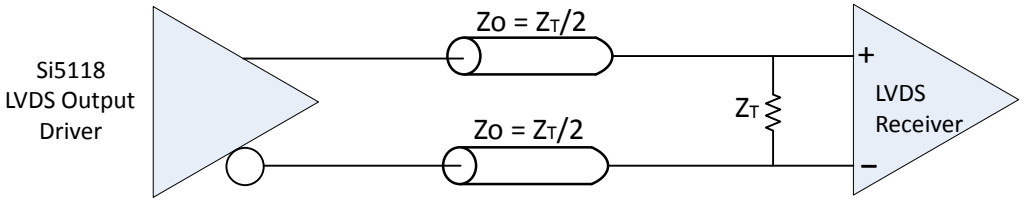


Figure 3.7. Standard LVDS Termination

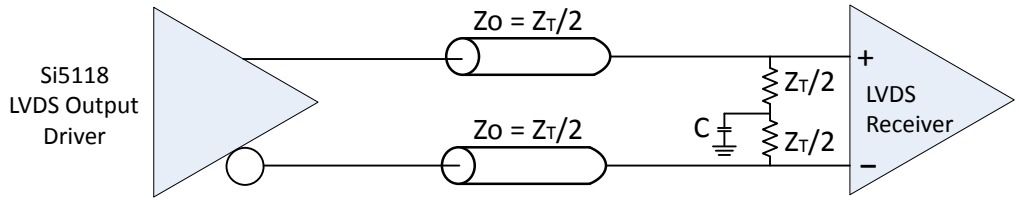


Figure 3.8. Optional LVDS Termination

Termination for 3.3 V LVPECL Outputs

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines. The differential outputs generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50 Ω transmission lines. Use matched impedance techniques to maximize operating frequency and minimize signal distortion. Figure 3.9 3.3 V LVPECL Output Termination, Option 1 on page 12 and Figure 3.10 3.3 V LVPECL Output Termination, Option 2 on page 12 show two different layouts. Other suitable clock layouts may exist, but it is recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

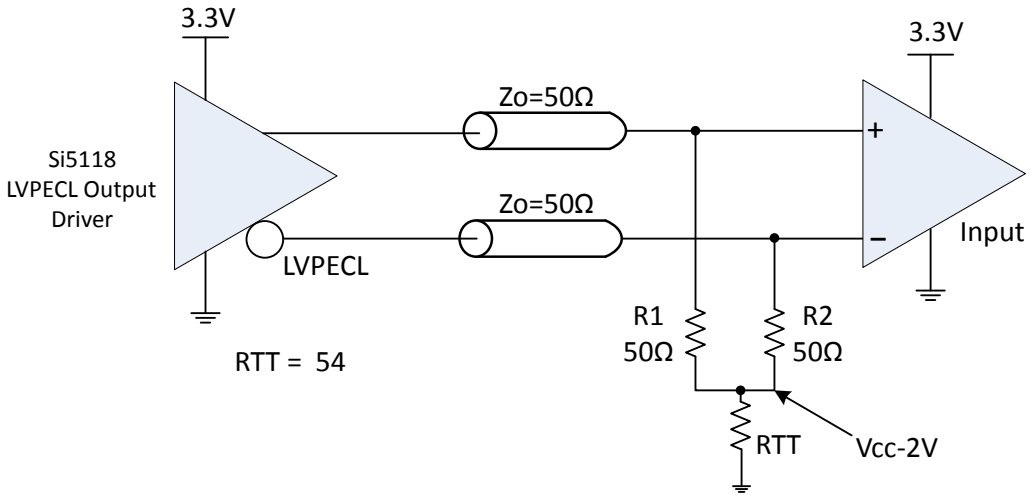


Figure 3.9. 3.3 V LVPECL Output Termination, Option 1

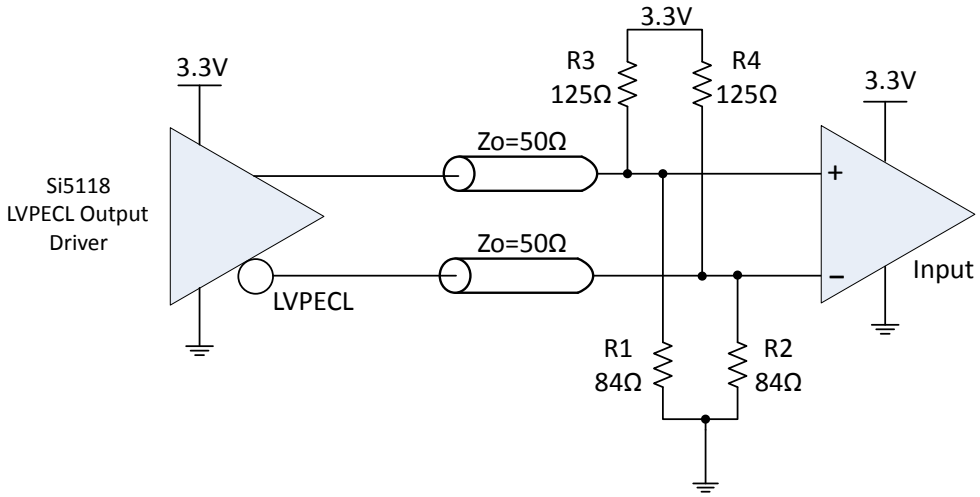


Figure 3.10. 3.3 V LVPECL Output Termination, Option 2

Termination for 2.5 V LVPECL Outputs

Figure 3.11 2.5 V LVPECL Termination Example, Option 1 on page 13 and Figure 3.12 2.5 V LVPECL Termination Example, Option 2 on page 13 show examples of termination for the 2.5 V LVPECL driver option. These terminations are equivalent to terminating 50 Ω to VDDO – 2 V. For VDDO = 2.5 V, the VDDO – 2 V is very close to ground level. The R3 in Figure 3.12 2.5 V LVPECL Termination Example, Option 2 on page 13 can be optionally eliminated using the termination shown in Figure 3.11 2.5 V LVPECL Termination Example, Option 1 on page 13.

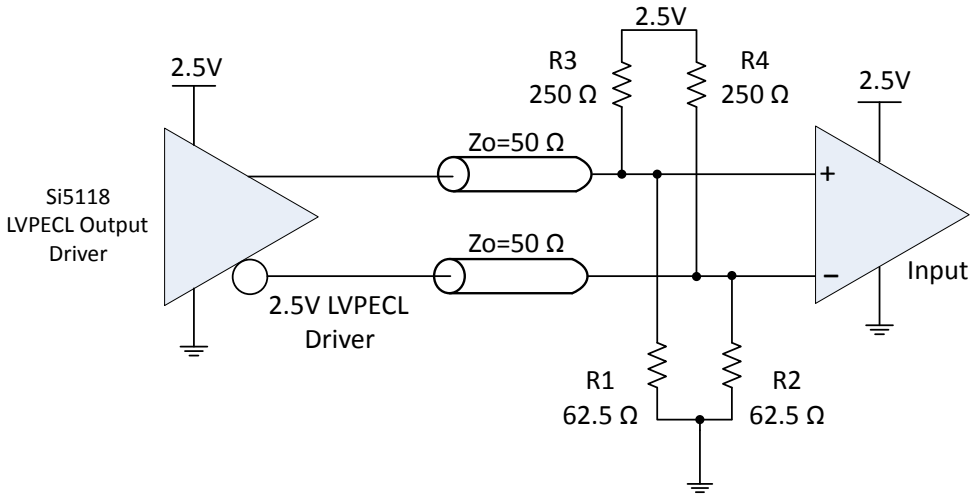


Figure 3.11. 2.5 V LVPECL Termination Example, Option 1

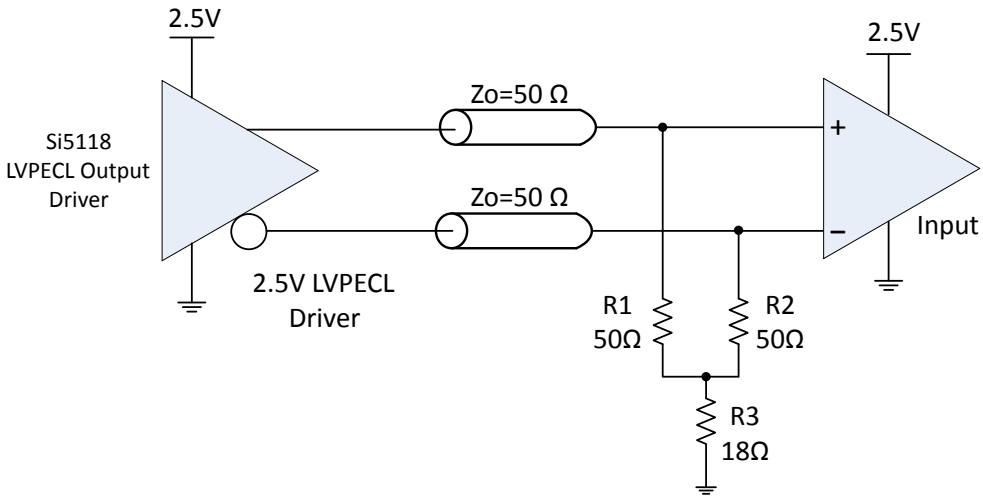


Figure 3.12. 2.5 V LVPECL Termination Example, Option 2

Termination for HCSL Outputs

The Si5118 HCSL driver option integrates termination resistors to simplify interfacing to an HCSL receiver. The HCSL driver supports both 100 Ω and 85 Ω transmission line options. This configuration option may be specified using ClockBuilder Pro.

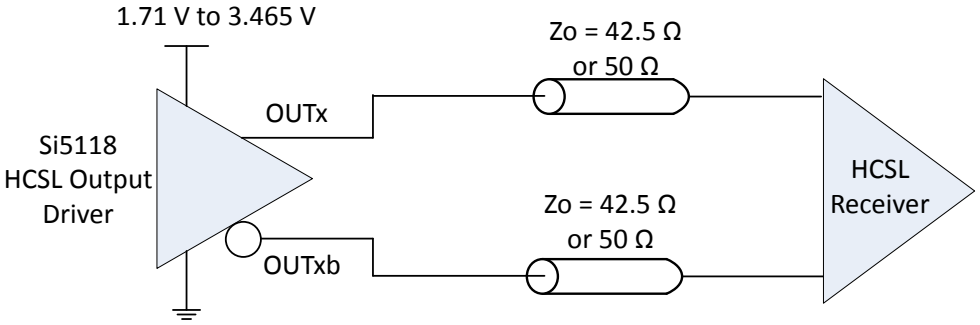


Figure 3.13. HCSL Internal Termination Mode

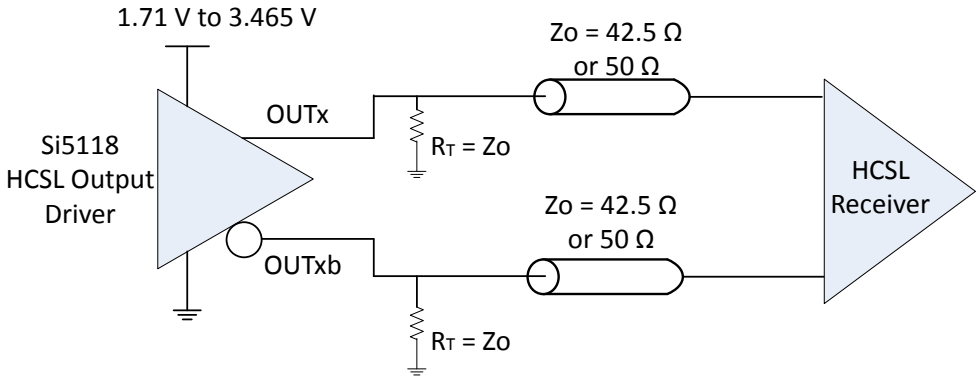


Figure 3.14. HCSL External Termination Mode

3.4.3 LVCMOS Output Terminations

LVCMOS outputs can be dc-coupled, as shown in the figure below.

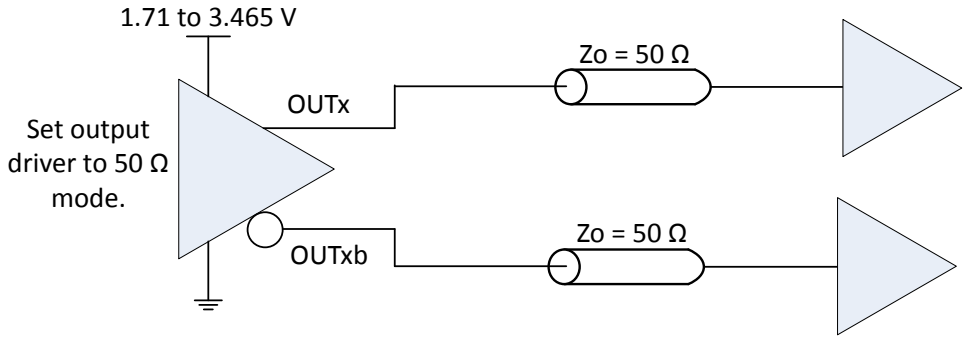


Figure 3.15. LVCMOS Output Termination Example, Option 1

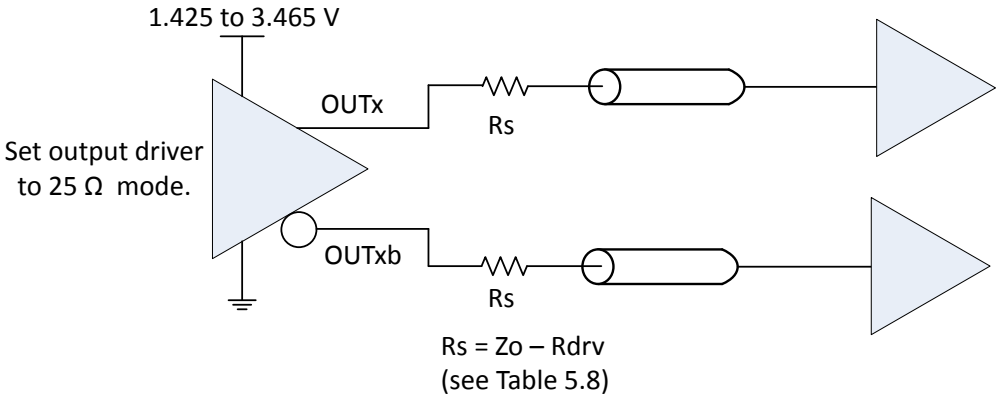


Figure 3.16. LVCMOS Output Termination Example, Option 2

The Si5118 features complementary LVCMOS driver options on all outputs. Silicon Labs recommends the use of complementary LVCMOS output drivers for all single-ended clock outputs in order to minimize unwanted emissions. Further details about using complementary LVCMOS output drivers, and the positive effects in CISPR25 Class4 and Class5 testing results, can be found in "AN1237: Si5332 Design Guidelines for Minimizing EMI".

3.4.4 LVCMOS Output Signal Swing

The signal swing (V_{OL}/V_{OH}) of the LVCMOS output drivers is set by the voltage on the VDDO pin for the respective bank.

3.4.5 LVCMOS Output Polarity

When a driver is configured as an LVCMOS output it generates a clock signal on both pins (OUTx and OUTxb). The LVCMOS outputs, OUTx and OUTxb, can be configured in CBPro to be either in-phase or complementary (180 degrees out of phase).

3.5 SmartClock Fault Detection Feature

FOOF (Fast Out of Frequency) Output

FOOF is a SmartClock feature that indicates the PLL can no longer track the input reference clock. This can be the result of input reference clock failure or other PLL fault. The FOOF output can be connected to a system safety manager IC or ASIL-B/D MCU to alert the system of a reference clock fault. If a fault is detected and the FOOF is asserted, the system safety manager IC or ASIL-B/D MCU can subsequently switch from the primary input source (that has faulted) to a secondary, back-up source so that the Si5332-AM continues sourcing output clocks. The FOOF output is active low, open drain, and requires an external pull-up resistor of 1 kΩ to 10 kΩ. For further detailed information on how to implement this function, please refer to "AN1292: Si5332-AM Fault Detection and Monitoring."

3.6 Configuring Si5118

A configuration file must be created for Si5118 using the ClockBuilder Pro software utility, and a corresponding orderable part number will be assigned specific to each individual configuration.

In less than three minutes, you will be able to generate a custom part number with a detailed data sheet addendum matching your design's configuration. Once you receive the confirmation email with the data sheet addendum, simply place an order with your local Silicon Labs sales representative. Samples of your pre-programmed device will ship within two weeks.

3.7 Minimizing Power Consumption

All power consumption of the device must be limited to the maximum specifications noted in Table 4.2 DC Characteristics on page 18.

ClockBuilder Pro provides power consumption and T_J estimates to help with power estimation and budgeting as a configuration file is being developed. If the maximum power consumption limit is exceeded, ClockBuilder Pro will provide a warning to the user. Silicon Labs recommends the following guidelines:

To minimize power consumption:

- Use 1.8 V VDD and/or VDDO instead of 2.5 V or 3.3 V whenever possible.
- For differential clock outputs, use LVDS output drivers instead of LVPECL or HCSL.
- For HCSL clock outputs:
  - Select 100 Ω impedance driver instead of 85 Ω
  - Select external termination instead of internal termination
- For single-ended clock outputs
  - Use the lowest frequency option available for your design. Lower frequencies consumes lower output driver current.
  - Use the lowest capacitive loading available for your design. Lower capacitive loading consumes lower output driver current.
  - When two outputs of the same frequency are needed, select a dual-complementary CMOS output driver instead of two independent single-CMOS output drivers.

4. Electrical Specifications

Table 4.1. Recommended Operating Conditions

(V_{DD_Core} = 1.8 V to 3.3 V +5%/-5%, V_{DDO} = 1.8 V ±5%, 2.5 V ±5%, or 3.3 V ±5%, T_A = –40 to 105 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Ambient Temperature	T_A		–40	25	105	°C
Junction Temperature	TJ_{MAX}		—	—	125	°C
Core Supply Voltage	V_{DDA}, V_{DD_DIG}, V_{DD_xtal}		1.71	—	3.46	V
Output Driver Supply Voltage	V_{DDO}		1.42[3]	—	3.46	V

Note:

1. All minimum and maximum specifications are guaranteed and apply across the recommended operating conditions. Typical values apply at nominal supply voltages and an operating temperature of 25 °C unless otherwise noted.
2. VDD_Core must be connected to the same voltage.
3. LVCMOS outputs only.

Table 4.2. DC Characteristics

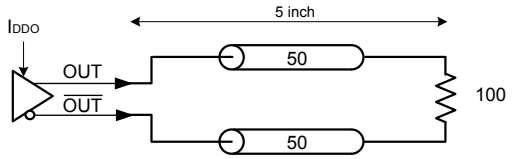
(V_{DD_Core} = 1.8 V to 3.3 V +5%/-5%, V_{DDO} = 1.8 V ±5%, 2.5 V ±5%, or 3.3 V ±5%, T_A = –40 to 105 °C)

Parameter	Symbol	Test Condition		Min	Typ	Max	Units
Core Supply Current	I_{DD}			—	45	70	mA
Output Buffer Supply Current	I_{DDOx}	LVPECL Output[1]		—	33	35	mA
		HCSL Output[1]		—	20	22	mA
		LVDS Output[1]		—	11	13	mA
		3.3 V VDDO LVCMOS[2] output		—	16	19	mA
		2.5 V VDDO LVCMOS[2] output		—	9	11	mA
		1.8 VDDO LVCMOS[2] output		—	7.5	8.5	mA
Total Power Dissipation	P_d	40-pin	Notes 3, 4	—	320	875	mW

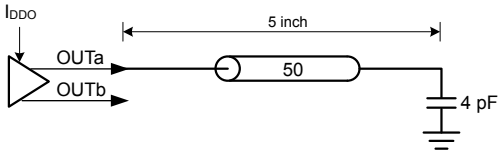
Note:

1. Differential outputs terminated into a 100 Ω load.
2. LVCMOS outputs measured into a 5 inch 50 Ω PCB trace with 4 pF load.

Differential Output Test Configuration



LVCMOS Output Test Configuration



3. ClockBuilderPro includes a power consumption indicator. Users should always enter the desired configuration into ClockBuilder-Pro to ensure the maximum power dissipation limits are not exceeded.
4. If configurations exceed the Max Total Power Dissipation specifications, the maximum ambient temperature limit of 105 °C and maximum junction temperature limits of 125 °C are void.

Table 4.3. Clock Input Specifications

(V_{DD_Core} = 1.8 V to 3.3 V +5%/-5%, V_{DDO} = 1.8 V ±5%, 2.5 V ±5%, or 3.3 V ±5%, T_A = –40 to 105 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Input Clock (AC-Coupled Differential Input Clock on CLK_IN/CLK_IN# or FBCLK_IN/FBCLK_IN#)						
Frequency	F_{IN}		16	—	50	MHz
Voltage Swing	V_{PP_DIFF}[3]	Differential AC-coupled	0.5	—	1.8	V_{PP_diff}
Slew Rate[1,2]	SR/SF	20-80%	0.75	—	—	V/ns
Duty Cycle	DC		40	—	60	%
Input Impedance	R_{IN}		10	—	—	kΩ
Input Capacitance	C_{IN}		2	3.5	6	pF
Input Clock (AC-Coupled LVCMOS Input Clock on CLK_IN or FBCLK_IN)						
Frequency	F_{IN}		16	—	50	MHz
Input High Voltage	V_{IH}		0.8 × V_{DD}	—	—	V
Input Low Voltage	V_{IL}		—	—	0.2 × V_{DD}	V
Slew Rate[1,2]	SR/SF	20-80%	0.75	—	—	V/ns
Duty Cycle	DC		40	—	60	%
Input Capacitance	C_{IN}		2	3.5	6	pF

Notes:

1. Imposed for jitter performance.
2. Rise and fall times can be estimated using the following simplified equation: $tr/tf_{80\text{-}20} = ((0.8 - 0.2) * V_{IN\_Vpp\_se}) / SR$.
3. $V_{PP\_DIFF} = 2 \times V_{PP\_SINGLE\text{-}ENDED}$

Table 4.4. External Crystal Input Specification

(V_{DD_Core} = 1.8 V to 3.3 V +5%/-5%, V_{DDO} = 1.8 V ±5%, 2.5 V ±5%, or 3.3 V ±5%, T_A = –40 to 105 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Crystal Frequency	F_{xtal}			16-50		MHz
Load Capacitance	C_L	16 - 30 MHz	6	12	20	pF
		31 - 50 MHz	—	—	10	pF
Shunt Capacitance	C_O	16 - 30 MHz	—	—	7	pF
		31 - 50 MHz	—	—	2	pF
ESR		16 - 30 MHz	—	—	50	Ω
		31 - 50 MHz	—	—	50	Ω
Max Crystal Drive Level	d_L		—	—	250	µW
Input Capacitance [1]	C_{IN}	Internal stray loading capacitance	—	2.5	—	pF
Input Voltage	V_{XIN}		-0.3	—	1.3	V

Notes:
1. Refer to Section 3.3.1 Crystal Reference for more detailed information.

Table 4.5. Control Pins

(V_{DD_Core} = 1.8 V to 3.3 V ±5%, T_A = –40 to 105 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
CLK_SEL[1:0] Pins (Inputs)						
Input Voltage	V_{IL}		-0.1	—	0.3 × V_{DD}[1]	V
	V_{IH}		0.7 × VDD[1]	—	1.1 × V_{DD}[1]	V
Input Capacitance	C_{IN}		—	—	4	pF
Pull-up/down Resistance	R_{IN}		—	50	—	kΩ
FOOF Pin (Output)						
Output Voltage	V_{OL}	Pull up = 1 kΩ	—	—	0.4	V
Pull-up Resistance	R_{PU}	1	—	10		kΩ
FOOF Assertion Time		—	170	—		µs
FOOF De-assertion Time		—	850	—		µs

Note:
1. V_{DD} indicates V_{DD_Core}.

Table 4.6. Differential Clock Output Specifications

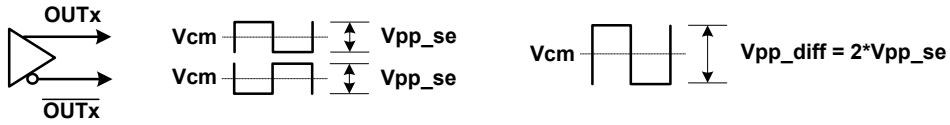
(V_{DD_Core} = 1.8 V to 3.3 V +5%/-5%, V_{DDO} = 1.8 V ±5%, 2.5 V ±5%, or 3.3 V ±5%, T_A = –40 to 105 °C)

Parameter	Symbol	Test Condition		Min	Typ	Max	Units
Output Frequency	f_{OUT}			16	—	50	MHz
Duty Cycle	DC			48	—	52	%
Output-Output Skew	T_{SK}	Within the same bank		—	—	30	ps
		Across banks		—	—	80	ps
Output Voltage Swing	V_{SEPP}	LVPECL		0.6	0.75	0.85	V_{PP}
		LVDS[11]	1.8/2.5/3.3 V	0.3	0.375	0.45	V_{PP}
		HCSL		0.7	0.8	0.9	V_{PP}
Common Mode Voltage	V_{CM}	LVPECL		—	VDDO-1.4	—	V
		LVDS	2.5/3.3 V	1.125	1.2	1.275	V
		LVDS	1.8 V	0.75	0.8	0.85	V
		HCSL		0.35	0.4	0.45	V
HCSL Edge Rate	Edgr	Notes 2, 4, 6		1	—	4.5	V/ns
HCSL Delta Tr	D_{tr}	Notes 4, 5, 10		—	—	155	ps
HCSL Delta Tf	D_{tf}	Notes 4, 5, 10		—	—	155	ps
HCSL Vcross Abs	V_{xa}	Notes 1, 3, 4, 5		250	—	550	mV
HCSL Delta Vcross	D_{vcrs}	Notes 4, 5, 9		—	—	140	mV
HCSL Vovs	V_{ovs}	Notes 4, 5, 7		—	—	V_{HIGH}+300	mV
HCSL Vuds	V_{uds}	Notes 4, 5, 8		—	—	V_{LOW}-300	mV
HCSL Vrng	V_{rng}	Notes 4, 5		V_{HIGH}-200	—	V_{LOW}+200	mV
Rise and Fall Times (20% to 80%)	t_R/t_F	LVDS (fast mode)	3.3 V or 2.5 V	150	200	350	ps
		LVDS (slow mode)	3.3 V or 2.5 V	350	530	620	ps
			1.8 V	150	225	350	ps
Rise and Fall Times (20% to 80%)	t_R/t_F	LVPECL		150	—	320	ps
		HCSL		—	—	420	ps

Parameter	Symbol	Test Condition	Min	Typ	Max	Units

Notes:

1. Measured at crossing point where the instantaneous voltage value of the rising edge of CLK equals the falling edge of CLK#.
2. Measure taken from differential waveform on a component test board. The edge (slew) rate is measured from -150 mV to +150 mV on the differential waveform . Scope is set to average because the scope sample clock is making most of the dynamic wiggles along the clock edge. Only valid for Rising clock and Falling Clock#. Signal must be monotonic through the Vol to Voh region for Trise and Tfall.
3. This measurement refers to the total variation from the lowest crossing point to the highest, regardless of which edge is crossing.
4. Applies to a 2 pf load with both internal or external 50 Ω or 42.5 Ω Rp.
5. Measurement taken from Single Ended waveform.
6. Measurement taken from differential waveform.
7. Overshoot is defined as the absolute value of the maximum voltage.
8. Undershoot is defined as the absolute value of the minimum voltage.
9. ΔVcross is defined as the total variation of all crossing voltages of Rising CLOCK and Falling CLOCK#. This is the maximum allowed variance in Vcross for any particular system.
10. Measured with oscilloscope, averaging off, using min max statistics. Variation is the delta between min and max.



11. LVDS swing levels for 50 Ω transmission lines.

Table 4.7. LVCMOS Clock Output Specifications

(V_{DD_Core} = 1.8 V to 3.3 V +5%/-5%, V_{DDO} = 1.5 V ±5%, 1.8 V ±5%, 2.5 V ±5%, or 3.3 V ±5%, T_A = –40 to 105 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Frequency	fout	1.5-3.3 V CMOS	16	—	50	MHz
Rise/Fall Time, 3.3 V (20-80%)	t_R/t_F	50 Ω impedance, 5” trace, CL = 4 pf	—	0.5	0.8	ns
Rise/Fall Time, 2.5 V (20-80%)	t_R/t_F	50 Ω impedance, 5” trace CL = 4 pf	—	0.6	0.95	ns
Rise/Fall Time, 1.8 V (20-80%)	t_R/t_F	50 Ω impedance, 5” trace CL = 4 pf	—	0.75	1.3	ns
Rise/Fall Time, 1.5 V (20-80%)	t_R/t_F	50 Ω impedance, 5” trace CL = 4 pf	—	0.9	1.3	ns
CMOS Output Resistance (Single Strength. Corresponds to CBPro LVCMOS 50 Ω mode.)		3.3 V	—	46	—	Ω
		2.5 V	—	48	—	Ω
		1.8 V	—	53	—	Ω
		1.5 V	—	58	—	Ω
CMOS Output Resistance (Double Strength. Corresponds to CBPro LVCMOS 25 Ω mode.)		3.3 V	—	23	—	Ω
		2.5 V	—	24	—	Ω
		1.8 V	—	27	—	Ω
		1.5 V	—	29	—	Ω
CMOS Output Voltage	V_{OH}	–4 mA load	VDDO-0.3	—	—	V
	V_{OL}	4 mA load	—	—	0.3	V
Duty Cycle	DC	XO and PLL mode	45	—	55	%

Table 4.8. Performance Characteristics

(V_{DD_Core} = 1.8 V to 3.3 V +5%/-5%, V_{DDO} = 1.8 V ±5%, 2.5 V ±5%, or 3.3 V ±5%, T_A = –40 to 105 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Power Ramp	t_{VDD}	0 V to V_{DDmin}	0.1	—	10	ms
Clock Stabilization from Power-up	t_{STABLE}	Time for clock outputs to appear after POR and selected input clock active	—	15	25	ms

Table 4.9. Jitter Performance Specifications

(V_{DD_Core} = 1.8 V to 3.3 V +5%/-5%, V_{DDO} = 1.8 V ±5%, 2.5 V ±5%, or 3.3 V ±5%, T_A = –40 to 105 °C)

Parameter	Symbol	Test Condition	Typ	Max	Units
Jitter Generation, Locked to External Clock Input Source (Primary)	J_{GEN}	12 kHz – 20 MHz[1]	290		fs RMS
	J_{PER}	Derived from integrated phase noise at a BER of 1e-12	5.8		ps Pk-Pk
	J_{CC}		4.5		ps Pk
Jitter Generation, Locked to External Crystal Input Source (Backup)	J_{GEN}	12 kHz – 20 MHz [1]	260		fs RMS
	J_{PER}	Derived from integrated phase noise at a BER of 1e-12	4.5		ps Pk-Pk
	J_{CC}		3.7		ps Pk

Notes:

1. All jitter data in this table is based upon all output formats being differential, at 50 MHz. When LVCMOS outputs are used, there is the potential that the output jitter may increase due to the nature of LVCMOS outputs. If your configuration implements any LVCMOS output and any output is required to have jitter less than 3 ps RMS, contact Silicon Labs for support to validate your configuration and ensure the best jitter performance.

Table 4.10. Thermal Characteristics

Parameter	Symbol	Test Condition	Value	Units
Si5118 — 40 QFN				
Thermal Resistance, Junction to Ambient	θ_{JA}	Still Air	23.1	°C/W
		Air Flow 1 m/s	17.5	
		Air Flow 2 m/s	16.5	
Thermal Resistance, Junction to Case	θ_{JC}	Still Air	13.4	
Thermal Resistance, Junction to Board	θ_{JB}	Still Air	8.7	
	Ψ_{JB}	Still Air	8.4	
Thermal Resistance, Junction to Top Center	Ψ_{JT}	Still Air	0.3	

Table 4.11. Absolute Maximum Ratings[1,2,3]

Parameter	Symbol	Test Condition	Value	Units
Storage Temperature Range	T_{STG}		–55 to +150	°C
DC Supply Voltage	V_{DD_Core}		–0.5 to 3.8	V
	V_{DDO}		–0.5 to 3.8	V
Input Voltage Range	V_I	XIN/XOUT	–0.3 to 1.3	V
Latch-up Tolerance	LU		JESD78 Compliant	
ESD Tolerance	HBM		2.0	kV
	CDM		500	V
Junction Temperature	T_{JCT}		–55 to 125	°C
Soldering Temperature	T_{PEAK}		260	°C
Soldering Temperature Time at T_{PEAK}	T_P		20 to 40	sec

Notes:

1. Permanent device damage may occur if the absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as specified in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. For more packaging information, go to www.silabs.com/support/quality/pages/RoHSInformation.aspx.
3. The device is compliant with JEDEC J-STD-020.

5. Pin Descriptions

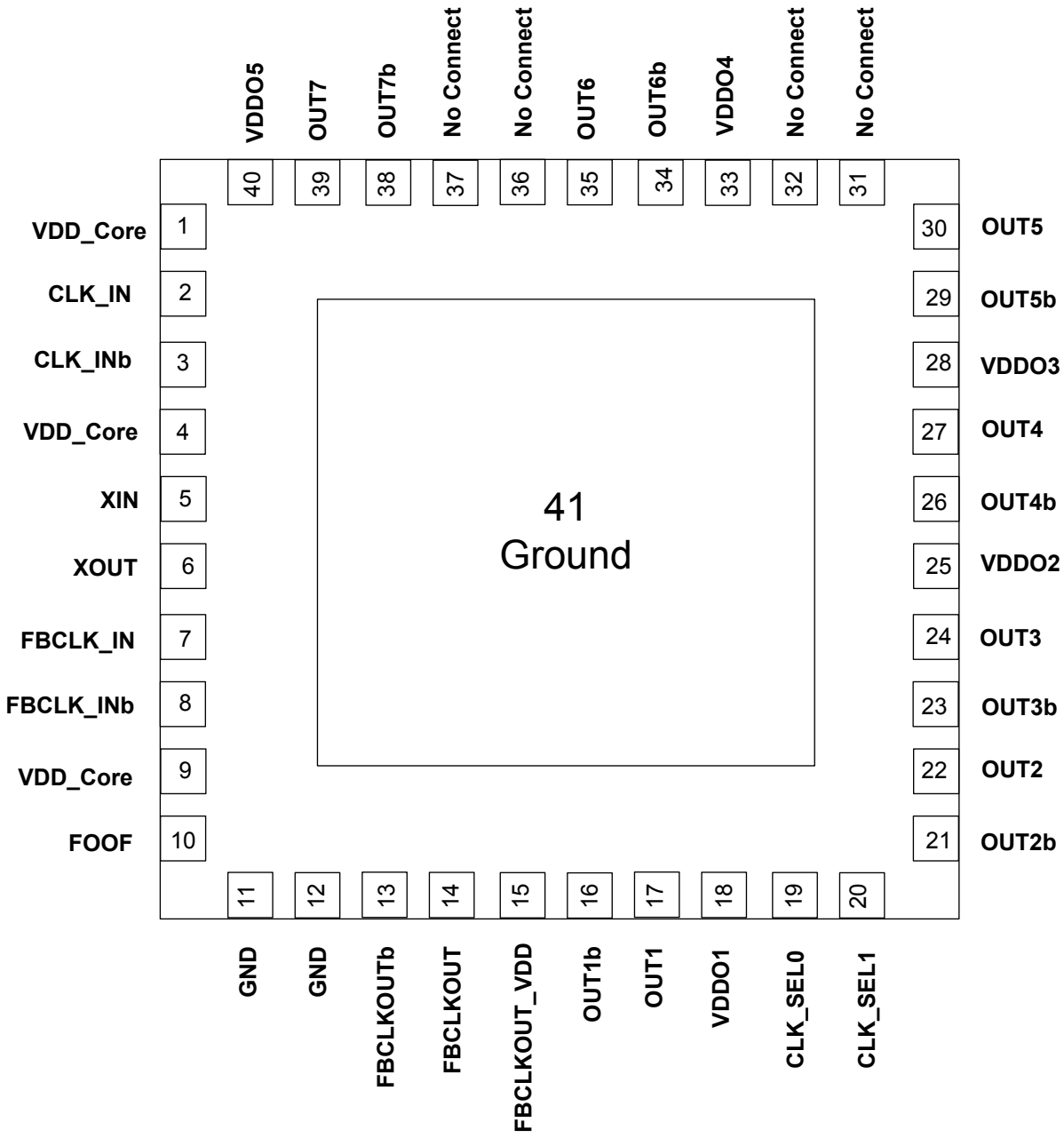


Figure 5.1. 40-QFN

Table 5.1. Pin Descriptions (40-QFN)

Pin Number	Pin Name	Pin Type	Function
1	VDD_Core	P	Voltage supply. Connect to 1.8–3.3 V. Part of internal core VDD voltage. Must be connected to same voltage as Pin 4 and Pin 9.
2	CLK_IN	I	Primary input clock reference. These pins accept both differential and single-ended clock signals. Refer to Section 3.3.2 Primary Reference Input Clock for input termination options. These pins are high-impedance and must be terminated externally.
3	CLK_INb	I	
4	VDD_Core	P	Voltage supply. Connect to 1.8–3.3 V. Part of internal core VDD voltage. Must be connected to same voltage as Pin 1 and Pin 9.
5	XIN	I	Backup input reference crystal source. Frequency must match CLK_IN frequency on Pin 2 and Pin 3. Refer to Section 4. Electrical Specifications for recommended crystal specifications.
6	XOUT	O	
7	FBCLK_IN	I	Feedback clock input, must be connected to Pin 13 and Pin 14. These pins are high impedance and must be terminated externally.
8	FBCLK_INb	I	
9	VDD_Core	P	Core Supply Voltage. Connect to 1.8–3.3 V. Must be connected to same voltage as Pin 1 and Pin 4.
10	FOOF	OD	FOOF hardware output pin. Open-drain, active low output requiring a 1 kΩ to 10 kΩ external pull-up on the PCB.
11	GND	GND	Connect to ground.
12	GND	GND	Connect to ground.
13	FBCLKOUTb	O	Feedback clock output. Must be connected to Pin 7 and Pin 8. Termination recommendations are provided in 3.4.2 Differential Output Terminations and 3.4.3 LVCMOS Output Terminations. Unused outputs should be left unconnected.
14	FBCLKOUT	O	
15	FBCLKOUT_VDD	P	**Supply Voltage (1.8–3.3 V, or 1.5 V for CMOS only) for FBCLKOUT**
16	OUT1b	O	**Output Clock** These output clocks support a programmable signal swing and common mode voltage. Desired output signal format is configurable in ClockBuilder Pro during configuration file development. Termination recommendations are provided in 3.4.2 Differential Output Terminations and 3.4.3 LVCMOS Output Terminations. Unused outputs should be left unconnected.
17	OUT1	O	
18	VDDO1	P	**Supply Voltage (1.8–3.3 V, or 1.5 V for CMOS only) for OUT1** Leave VDDOx pins of unused output drivers unconnected. An alternate option is to connect the VDDOx pin to a power supply and disable the output driver to minimize current consumption.
19	CLK_SEL0	I	Input reference HW pin.
20	CLK_SEL1	I	Input reference HW pin.
21	OUT2b	O	**Output Clock** These output clocks support a programmable signal swing and common mode voltage. Desired output signal format is configurable in ClockBuilder Pro during configuration file development. Termination recommendations are provided in 3.4.2 Differential Output Terminations and 3.4.3 LVCMOS Output Terminations. Unused outputs should be left unconnected.
22	OUT2	O	

Pin Number	Pin Name	Pin Type	Function
23	OUT3b	O	**Output Clock** These output clocks support a programmable signal swing and common mode voltage. Desired output signal format is configurable in ClockBuilder Pro during configuration file development. Termination recommendations are provided in 3.4.2 Differential Output Terminations and 3.4.3 LVCMOS Output Terminations. Unused outputs should be left unconnected.
24	OUT3	O	
25	VDDO2	P	**Supply Voltage (1.8–3.3 V, or 1.5 V for CMOS only) for OUT2 and OUT3** Leave VDDOx pins of unused output drivers unconnected. An alternate option is to connect the VDDOx pin to a power supply and disable the output driver to minimize current consumption.
26	OUT4b	O	**Output Clock** These output clocks support a programmable signal swing and common mode voltage. Desired output signal format is configurable in ClockBuilder Pro during configuration file development. Termination recommendations are provided in 3.4.2 Differential Output Terminations and 3.4.3 LVCMOS Output Terminations. Unused outputs should be left unconnected.
27	OUT4	O	
28	VDDO3	P	**Supply Voltage (1.8–3.3 V, or 1.5 V for CMOS only) for OUT4 and OUT5** Leave VDDOx pins of unused output drivers unconnected. An alternate option is to connect the VDDOx pin to a power supply and disable the output driver to minimize current consumption.
29	OUT5b	O	**Output Clock** These output clocks support a programmable signal swing and common mode voltage. Desired output signal format is configurable in ClockBuilder Pro during configuration file development. Termination recommendations are provided in 3.4.2 Differential Output Terminations and 3.4.3 LVCMOS Output Terminations. Unused outputs should be left unconnected.
30	OUT5	O	
31	No Connect	NC	Do not connect this pin to anything.
32	No Connect	NC	Do not connect this pin to anything.
33	VDDO4	P	**Supply Voltage (1.8–3.3 V, or 1.5 V for CMOS only) for OUT6** Leave VDDOx pins of unused output drivers unconnected. An alternate option is to connect the VDDOx pin to a power supply and disable the output driver to minimize current consumption.
34	OUT6b	O	**Output Clock** These output clocks support a programmable signal swing and common mode voltage. Desired output signal format is configurable in ClockBuilder Pro during configuration file development. Termination recommendations are provided in 3.4.2 Differential Output Terminations and 3.4.3 LVCMOS Output Terminations. Unused outputs should be left unconnected.
35	OUT6	O	
36	No Connect	NC	Do not connect this pin to anything.
37	No Connect	NC	Do not connect this pin to anything.
38	OUT7b	O	**Output Clock** These output clocks support a programmable signal swing and common mode voltage. Desired output signal format is configurable in ClockBuilder Pro during configuration file development. Termination recommendations are provided in 3.4.2 Differential Output Terminations and 3.4.3 LVCMOS Output Terminations. Unused outputs should be left unconnected.
39	OUT7	O	

Pin Number	Pin Name	Pin Type	Function
40	VDDO5	P	**Supply Voltage (1.8–3.3 V, or 1.5 V for CMOS only) for OUT7** Leave VDDOx pins of unused output drivers unconnected. An alternate option is to connect the VDDOx pin to a power supply and disable the output driver to minimize current consumption.
41	GND PAD	P	**Ground Pad** This pad provides electrical and thermal connection to ground and must be connected for proper operation.

6. Package Outline

6.1 6x6mm 40-QFN Package Diagram

The figure below illustrates the package details for the 40-QFN. The table below lists the values for the dimensions shown in the illustration.

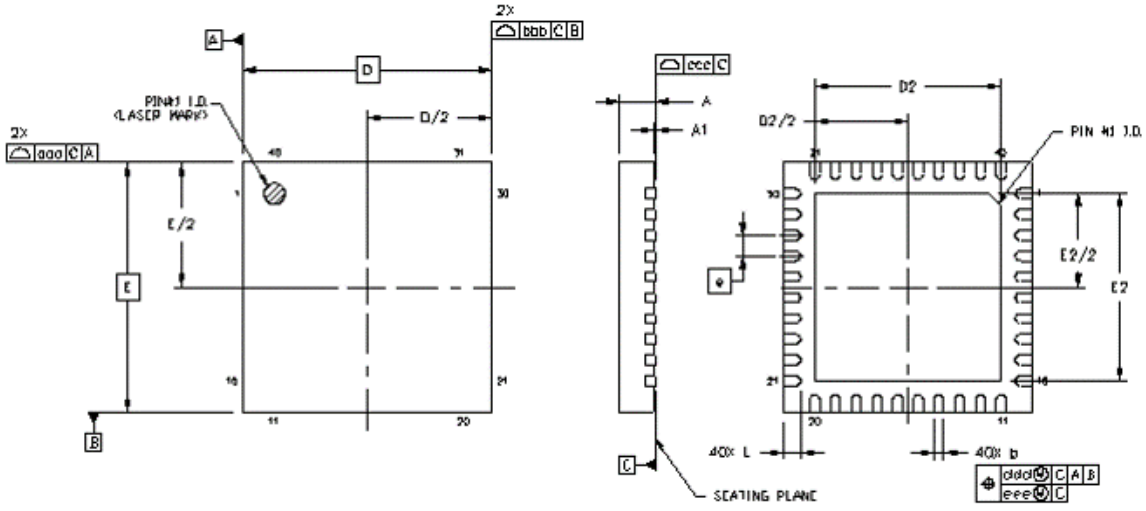


Figure 6.1. 40-Pin Quad Flat No-Lead (QFN)

Table 6.1. Package Dimensions

Dimension	Min	Nom	Max
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
b	0.18	0.25	0.30
D		6.00 BSC	
D2	4.35	4.50	4.65
e		0.50 BSC	
E		6.00 BSC	
E2	4.35	4.50	4.65
L	0.30	0.40	0.50
aaa	—	—	0.15
bbb	—	—	0.15
ccc	—	—	0.08
ddd	—	—	0.10
eee			0.05

Dimension	Min	Nom	Max

Notes:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to the JEDEC Solid State Outline MO-220.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

7. PCB Land Pattern

7.1 6x6mm 40-QFN Land Pattern

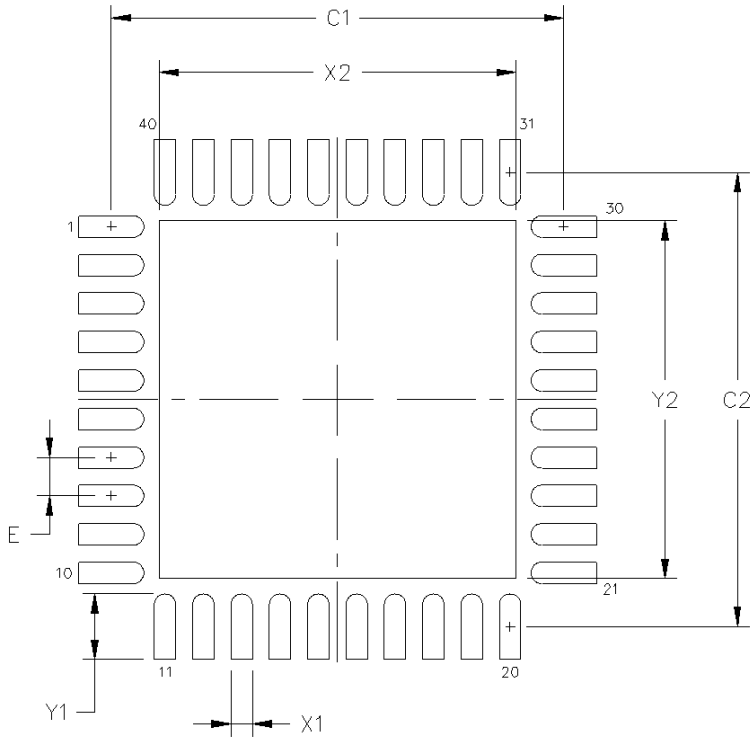


Figure 7.1. 40-QFN Land Pattern

Table 7.1. PCB Land Pattern Dimensions

Dimension	mm
C1	5.90
C2	5.90
e	0.50 BSC
X1	0.30
Y1	0.85
X2	4.65
Y2	4.65

Dimension	mm

Notes:
General

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. This Land Pattern Design is based on the IPC-7351 guidelines.

Solder Mask Design

1. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.

Stencil Design

1. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
2. The stencil thickness should be 0.125 mm (5 mils).
3. The ratio of stencil aperture to land pad size can be 1:1 for all perimeter pads.
4. The stencil aperture to land pad size recommendation is 70% paste coverage.

Card Assembly

1. A No-Clean, Type-3 solder paste is recommended.
2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

8. Top Marking

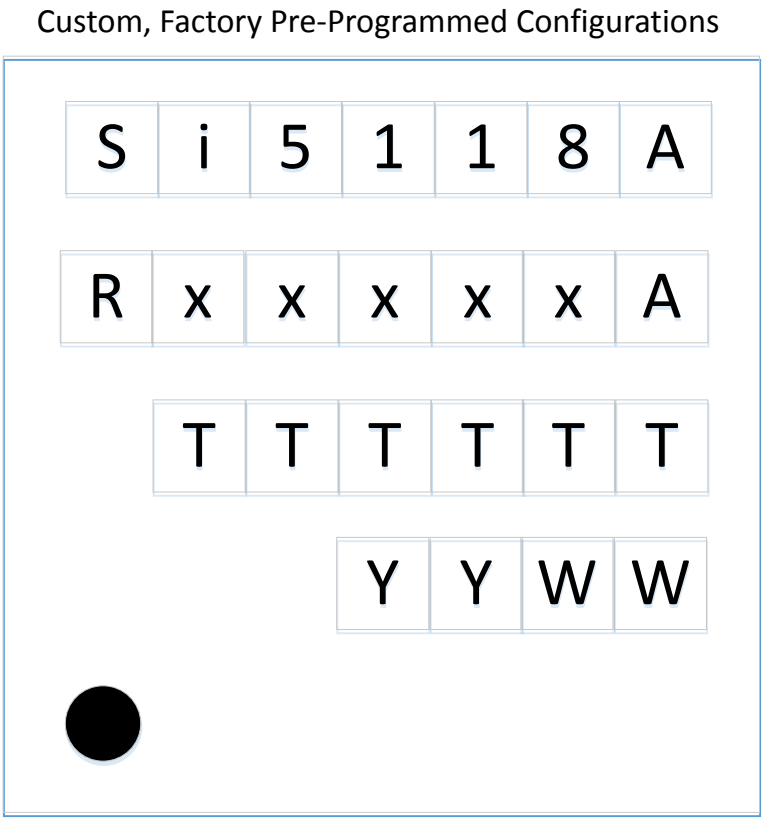


Figure 8.1. Top Marking

Table 8.1. Top Marking Explanation

Line	Characters	Description
1	Si5118A	Base part number
2	RxxxxxA	R = product revision
		xxxxx = Customer specific NVM sequence number. NVM code assigned for custom, factory pre-programmed devices using ClockBuilder Pro. A = automotive grade, 40-QFN package See Ordering Guide for more information.
3	TTTTTT	Manufacturing trace code
4	YYWW	Year (YY) and work week (WW) of package assembly

9. Revision History

Revision 0.7

January, 2021

- Initial release.

ClockBuilder Pro

One-click access to Timing tools, documentation, software, source code libraries & more. Available for Windows and iOS (CBGo only).

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