



Si52254/Si52258 数据表

4/8 输出 PCIe Gen1/2/3/4/5 时钟发生器

Si52258/54 是业界性能高、功耗低的汽车级 PCI Express 时钟发生器，适用于 PCIe Gen 1/2/3/4/5 公共时钟和/或 SRIS 应用。Si52258 和 Si52254 分别提供 8 路和 4 路 100 MHz PCIe 差分时钟输出。所有时钟输出均符合 PCIe Gen 1/2/3/4/5 公共时钟和单独参考时钟体系结构规格。

硬件控制引脚可用于启用和禁用输出，以及扩频使能/禁用（以降低 EMI）。

要详细了解 PCI Express、Silicon Labs 的完整 PCIe 产品组合、应用说明和设计工具，包括符合 PCI Express 标准的 Silicon Labs PCIe 时钟抖动工具，请访问 Silicon Labs PCIe Express 学习中心。

应用：

- 信息娱乐
- ADAS ECU
- 雷达传感器
- LiDar 传感器

主要特点

- 8/4 输出，带内部终端
- 符合 PCIe Gen 1/2/3/4/5 标准
- 汽车级 2：-40 至 +105 °C
- 内部 100 Ω 或 85 Ω 线匹配
- 出色的抖动性能
 - 0.05 ps RMS (Gen3/4)
 - 0.025 ps RMS (Gen5)
- 三角扩频，用于降低 EMI，向下扩频 0.25% 或 0.5%
- 独立硬件控制引脚，用于输出使能、使能扩频
- 使能和频率选择
- 25 MHz 晶体输入或时钟输入
- 1.8 - 3.3 V 电源
- 无铅、符合 RoHS-6

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1. 功能列表

- 8/4-100 MHz HCSL 输出，带内部终端
- 符合 PCIe Gen1/2/3/4/5 标准
- 汽车级 2: -40 至 +105 °C
- 内部 100 Ω 或 85 Ω 线匹配
- 出色的抖动性能
 - 0.05 ps RMS (Gen3/4)
 - 0.025 ps RMS (Gen5)
- 三角扩频，用于降低 EMI，向下扩频 0.25% 或 0.5%
- 独立硬件控制引脚，用于阻抗选择、输出使能、使能扩频
- 信号丢失 (LOS) 输出引脚
- 25 MHz 晶体输入或时钟输入
- 1.8 - 3.3 V 电源
- 无铅、符合 RoHS-6

2. Ordering Guide

Number of Outputs	Part Number	Package Type	Temperature
8	Si52258A-D01AM	40-QFN	Automotive, -40 to 105 °C
	Si52258A-D01AMR	40-QFN – Tape and Reel	Automotive, -40 to 105 °C
4	Si52254A-D01AM	32-QFN	Automotive, -40 to 105 °C
	Si52254A-D01AMR	32-QFN – Tape and Reel	Automotive, -40 to 105 °C

3. Functional Description

3.1 Functional Block Diagram

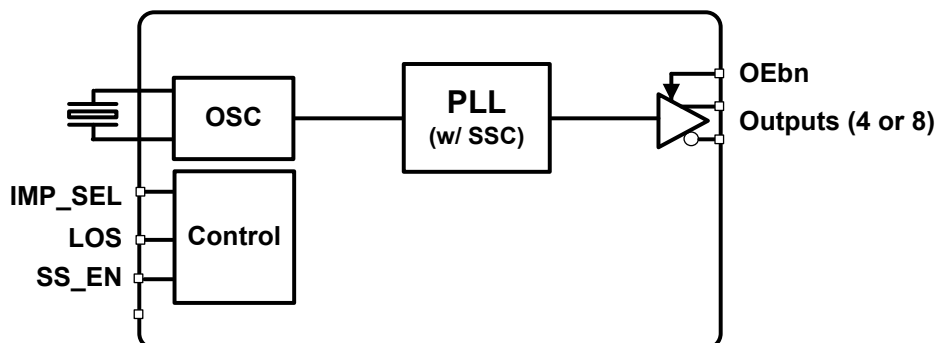


Figure 3.1. Si5225x Block Diagram

3.2 Crystal Recommendations

The Si52258/4 operates from a parallel resonance 25 MHz crystal. Crystal operation requires external loading capacitors to match crystal capacitive loading requirements. Si52258/4 XA/XB inputs present 2.5 pF of stray capacitance.

3.3 HCSL Differential Output Terminations

Termination for HCSL Outputs

The Si52254/8 HCSL drivers feature integrated termination resistors to simplify interfacing to an HCSL receiver. The HCSL driver supports both 100 Ω and 85 Ω transmission line options, and can be selected using the IMP_SEL hardware input pin.

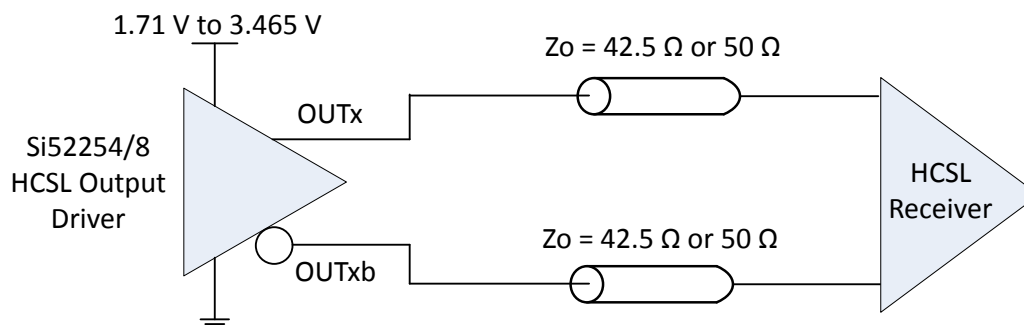


Figure 3.2. HCSL Internal Termination Mode

3.4 Output Enable/Disable

An output enable pin provides a convenient method of disabling or enabling the output drivers. When the output enable pin is held high, all designated outputs will be disabled. When held low, the designated outputs will be enabled.

3.5 Spread Spectrum

To help reduce electromagnetic interference (EMI), the Si52254/8 supports spread spectrum modulation. Spread spectrum can be enabled by the hardware input pin.

3.6 Loss of Signal (LOS)

The LOS indicator is used to check for the presence of an input reference source (crystal). LOS will assert when the reference source frequency drops below approximately 10 MHz.

In the event that a reference source is not present, the associated LOS pin will assume a logic low (LOS = 0) state. When a reference source is present, the LOS pin will assume a logic high (LOS = 1) state.

The LOS output is active low, open drain, and requires an external pull-up resistor of 1 k Ω or greater.

4. Power Supply Filtering Recommendations

The Si52258/4 features internal LDOs on each power supply pin, providing excellent power supply noise rejection. As a guideline, each power supply pin should use a parallel combination of a 1 μf and a 0.1 μF bypass capacitor placed as close to the supply pin as possible.

5. Electrical Specifications

Table 5.1. Recommended Operating Conditions
 $(V_{DD} = V_{DDA} = V_{DD_DIG} = V_{DD_XTAL} = 1.8\text{ V to }3.3\text{ V }+5\%/-5\%, V_{DDO} = 1.8\text{ V } \pm 5\%, 2.5\text{ V } \pm 5\%, \text{ or } 3.3\text{ V } \pm 5\%, T_A = -40\text{ to }105\text{ }^\circ\text{C})$

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Ambient Temperature	T_A		-40	25	105	$^\circ\text{C}$
Junction Temperature	T_{JMAX}		—	—	125	$^\circ\text{C}$
Core Supply Voltage ^{1, 2}	$V_{DDA}, V_{DD_DIG}, V_{DD_xtal}$		1.71	—	3.46	V
Output Driver Supply Voltage	V_{DDO}		1.71	—	3.46	V

Note:

- All minimum and maximum specifications are guaranteed and apply across the recommended operating conditions. Typical values apply at nominal supply voltages and an operating temperature of 25 $^\circ\text{C}$ unless otherwise noted.
- All core voltages (V_{DD_DIG} , V_{DDA} , V_{DD_XTAL}) must be connected to the same voltage.

Table 5.2. DC Characteristics
 $(V_{DD} = V_{DDA} = V_{DD_DIG} = V_{DD_XTAL} = 1.8\text{ V to }3.3\text{ V }+5\%/-5\%, V_{DDO} = 1.8\text{ V } \pm 5\%, 2.5\text{ V } \pm 5\%, \text{ or } 3.3\text{ V } \pm 5\%, T_A = -40\text{ to }105\text{ }^\circ\text{C})$

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Core Supply Current	I_{DD}		—	26	40	mA
Output Buffer Supply Current	I_{DDOx}	HCSL Output ¹ @ 100 MHz	—	20	22	mA
Total Power Dissipation ²	P_d	40-pin		550	750	mW
		32-pin	—	300	445	mW

Notes:

- Differential outputs terminated into a 100 Ω load at 3.3 V.
- Total power dissipation calculated with all 100 MHz HCSL running at 3.3 V.

Table 5.3. External Crystal Input Specification
 $(V_{DD} = V_{DDA} = V_{DD_DIG} = V_{DD_XTAL} = 1.8\text{ V to }3.3\text{ V }+5\%/-5\%, V_{DDO} = 1.8\text{ V } \pm 5\%, 2.5\text{ V } \pm 5\%, \text{ or } 3.3\text{ V } \pm 5\%, T_A = -40\text{ to }105\text{ }^\circ\text{C})$

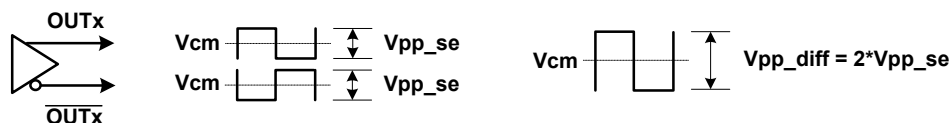
Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Crystal Frequency	F_{xtal}			25		MHz
Crystal Drive Level	d_L		—	—	250	μW
Input Capacitance	C_{IN}		—	2.5	—	pF
Input Voltage	V_{XIN}		-0.3	—	1.3	V

Table 5.4. Differential Clock Output Specifications(V_{DD} = V_{DDA} = V_{DD_DIG} = V_{DD_XTAL} = 1.8 V to 3.3 V +5%/-5%, V_{DDO} = 1.8 V ±5%, 2.5 V ±5%, or 3.3 V ±5%, T_A = -40 to 105 °C)

Parameter	Symbol	Test Condition		Min	Typ	Max	Units
Output Frequency	f _{OUT}			100			MHz
Duty Cycle	DC			48	—	52	%
Output-Output Skew	T _{SK}			—	—	80	ps
Output Voltage Swing	V _{SEPP}	HCSL		0.7	0.8	0.9	V _{PP}
Common Mode Voltage	V _{CM}	HCSL		0.35	0.4	0.45	V
HCSL Edge Rate	Edgr	Notes 1, 2, 3		1	—	4.5	V/ns
HCSL Delta Tr	D _{tr}	Notes 2, 4, 5		—	—	155	ps
HCSL Delta Tf	D _{tf}	Notes 2, 4, 5		—	—	155	ps
HCSL Vcross Abs	V _{xa}	Notes 6, 7, 2, 4		250	—	550	mV
HCSL Delta Vcross	D _{vcrs}	Notes 2, 4, 8		—	—	140	mV
HCSL Vovs	V _{ovs}	Notes 2, 4, 9		—	—	V _{HIGH} +300	mV
HCSL Vuds	V _{uds}	Notes 2, 4, 10		—	—	V _{LOW} -300	mV
HCSL Vrng	V _{rng}	Notes 2, 4		V _{HIGH} -200	—	V _{LOW} +200	mV
Rise and Fall Times (20% to 80%)	t _R /t _F	HCSL		—	—	420	ps

Notes:

1. Measure taken from differential waveform on a component test board. The edge (slew) rate is measured from -150 mV to +150 mV on the differential waveform. Scope is set to average because the scope sample clock is making most of the dynamic wiggles along the clock edge. Only valid for Rising clock and Falling Clock#. Signal must be monotonic through the Vol to Voh region for Trise and Tfall.
2. Applies to a 2 pF load with both internal or external 50 Ω or 42.5 Ω R_p.
3. Measurement taken from differential waveform.
4. Measurement taken from Single Ended waveform.
5. Measured with oscilloscope, averaging off, using min max statistics. Variation is the delta between min and max.



6. Measured at crossing point where the instantaneous voltage value of the rising edge of CLK equals the falling edge of CLK#.
7. This measurement refers to the total variation from the lowest crossing point to the highest, regardless of which edge is crossing.
8. ΔV_{cross} is defined as the total variation of all crossing voltages of Rising CLOCK and Falling CLOCK#. This is the maximum allowed variance in V_{cross} for any particular system.
9. Overshoot is defined as the absolute value of the maximum voltage.
10. Undershoot is defined as the absolute value of the minimum voltage.

Table 5.5. Performance Characteristics $(V_{DD} = V_{DDA} = V_{DD_DIG} = V_{DD_XTAL} = 1.8\text{ V to }3.3\text{ V }+5\%/-5\%, V_{DDO} = 1.8\text{ V } \pm 5\%, 2.5\text{ V } \pm 5\%, \text{ or } 3.3\text{ V } \pm 5\%, T_A = -40\text{ to }105\text{ }^\circ\text{C})$

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Power Ramp	t_{VDD}	0 V to V_{DDmin}	0.1	—	10	ms
Clock Stabilization from Power-up	t_{STABLE}	Time for clock outputs to appear after POR	—	15	25	ms
0.5% Down Spread Frequency Deviation	SSDEV		0.4	0.45	0.5	%
Spread Spectrum Modulation Rate	SSDEV		30	31.5	33	kHz
Notes: 1. Default value is ~31.5 kHz.						

Table 5.6. PCI-Express Clock Outputs (100 MHz HCSSL)(V_{DD} = V_{DDA} = V_{DD_DIG} = V_{DD_XTAL} = 1.8 V to 3.3 V +5%/-5%, V_{DDO} = 1.8 V ±5%, 2.5 V ±5%, or 3.3 V ±5%, T_A = -40 to 105 °C)

Parameter	Test Condition	SSC On/Off	Typ	Max	Units
PCIe Gen 1.1	Includes PLL BW 1.5–22 MHz, Peaking = 3 dB, Td = 10 ns, Ftrk = 1.5 MHz with BER = 1E-12 ¹	Off	11	19	ps RMS
		On	22	30	ps RMS
PCIe Gen 2.1	Includes PLL BW 5MHz and 8–16 MHz, Jitter Peaking = 0.01–1 dB and 3 dB, Td = 12 ns, Low Band, F < 1.5 MHz ¹	Off	0.02	0.026	ps RMS
		On	0.12	0.21	ps RMS
	Includes PLL BW 5 MHz and 8–16 MHz, Jitter Peaking = 0.01–1 dB and 3 dB, Td = 12 ns, High Band, 1.5 MHz < F < Nyquist ¹	Off	0.2	0.31	ps RMS
		On	0.8	1.35	ps RMS
PCIe Gen 3.0 Common Clock	Includes PLL BW 2–4 MHz and 5 MHz, Peaking = 0.01–2 dB and 1 dB, Td = 12 ns, CDR = 10 MHz ^{1,2}	Off	0.06	0.1	ps RMS
		On	0.26	0.38	ps RMS
PCIe Gen3.0 SRIS	Includes PLL BW 4 MHz Peaking = 2 dB and 1dB, Td = 12 ns CDR = 10 MHz ^{1,2}	On	0.35	0.37	ps RMS
PCIe Gen 4.0 Common Clock	Includes PLL BW 2–4 MHz and 5 MHz, Peaking = 0.01–2 dB and 1dB, Td = 12 ns, CDR = 10 MHz ^{1,2}	Off	0.05	0.1	ps RMS
		On	0.26	0.38	ps RMS
PCIe Gen4.0 SRIS	Includes PLL BW 4 MHz Peaking = 2 dB and 1 dB, Td = 12 ns CDR = 10 MHz ^{1,2}	On	0.31	0.38	ps RMS
PCIe Gen5.0 Common Clock		Off	0.025	0.04	ps RMS
		On	0.1	0.15	ps RMS
PCIe Gen5.0 SRIS		On	0.08	0.1	ps RMS

Note:

1. All output clocks 100 MHz HCSSL format. Jitter data taken from Clock Jitter Tool v.1.3.
2. Excludes oscilloscope sampling noise.

Table 5.7. Thermal Characteristics

Parameter	Symbol	Test Condition ¹	Value	Units
Si52258 — 40 QFN				
Thermal Resistance, Junction to Ambient	θ_{JA}	Still Air	23.1	°C/W
		Air Flow 1 m/s	17.5	
		Air Flow 2 m/s	16.5	
Thermal Resistance, Junction to Case	θ_{JC}		13.4	
Thermal Resistance, Junction to Board	θ_{JB}		8.7	
	Ψ_{JB}	Still Air	8.4	
Si52254 — 32 QFN				
Thermal Resistance, Junction to Ambient	θ_{JA}	Still Air	28.4	°C/W
		Air Flow 1 m/s	24	
		Air Flow 2 m/s	23	
Thermal Resistance, Junction to Case	θ_{JC}		15.9	
Thermal Resistance, Junction to Board	θ_{JB}		11.5	
	Ψ_{JB}	Still Air	11.2	
Note:				
1. Based on JEDEC standard 4-layer PCB.				

Table 5.8. Absolute Maximum Ratings^{1,2,3}

Parameter	Symbol	Test Condition	Value	Units
Storage Temperature Range	T_{STG}		-55 to +150	°C
DC Supply Voltage	V_{DD}		-0.5 to 3.8	V
	V_{DDA}		-0.5 to 3.8	V
	$V_{DD_{xtal}}$		-0.5 to 3.8	V
	V_{DDO}		-0.5 to 3.8	V
Input Voltage Range	V_I	XIN/XOUT	-0.3 to 1.3	V
Latch-up Tolerance	LU		JESD78 Compliant	
ESD Tolerance	HBM	100 pF, 1.5 k Ω	2.0	kV
Junction Temperature	T_{JCT}		-55 to 125	°C
Soldering Temperature	T_{PEAK}		260	°C
Soldering Temperature Time at T_{PEAK}	T_P		20 to 40	sec

Notes:

1. Permanent device damage may occur if the absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as specified in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. For more packaging information, go to www.silabs.com/support/quality/pages/RoHSInformation.aspx.
3. The device is compliant with JEDEC J-STD-020.

6. Pin Descriptions

6.1 Si52258A-D01AM Pin Descriptions (40-QFN)

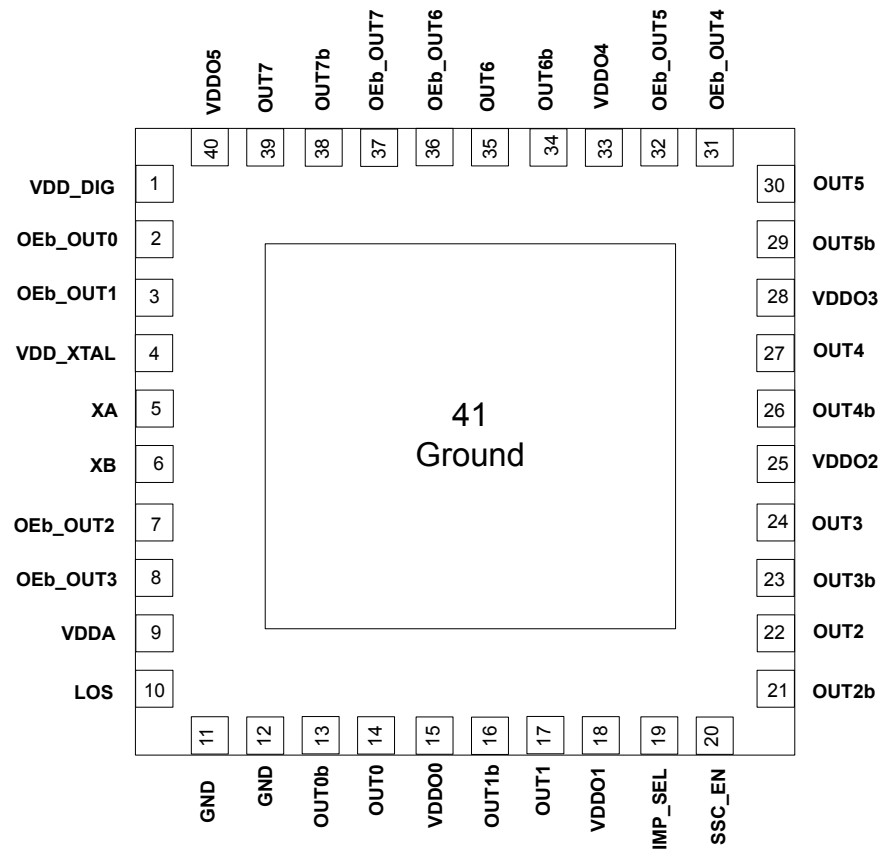


Figure 6.1. 40-QFN

Table 6.1. Si52258A-D01AM Pin Descriptions (40-QFN)

Pin Number	Pin Name	Pin Type	Function
1	VDD_DIG	P	Voltage supply for digital functions. Connect to 1.8–3.3 V. Part of internal core VDD voltage. Must be connected to same voltage as VDDA and VDD_XTAL. Refer to 4. Power Supply Filtering Recommendations for bypass capacitor recommendations.
2	OEb_OUT0	I	Output enable pin for OUT1. Low = output enabled High = output disabled
3	OEb_OUT1	I	Output enable pin for OUT1. Low = output enabled High = output disabled
4	VDD_XTAL	P	Voltage supply for crystal oscillator. Connect to 1.8–3.3 V. Part of internal core VDD voltage. Must be connected to same voltage as VDDA and VDD_DIG. Refer to 4. Power Supply Filtering Recommendations for bypass capacitor recommendations.
5	XA	I	Connect to 25 MHz input crystal. Refer to Section 5. Electrical Specifications for recommended crystal specifications.
6	XB	O	
7	OEb_OUT2	I	Output enable pin for OUT2. Low = output enabled High = output disabled
8	OEb_OUT3	I	Output enable pin for OUT3. Low = output enabled High = output disabled
9	VDDA	P	Core Supply Voltage. Connect to 1.8–3.3 V. Must be connected to same voltage as VDD_DIG and VDD_XTAL. Refer to 4. Power Supply Filtering Recommendations for bypass capacitor recommendations.
10	LOS	O	The LOS status pin indicates whether the reference input has dropped below approximately 10 MHz. LOS is active low, open drain output and requires an external pull-up resistor of 1 to 10 kΩ for proper operation. If LOS is not required, this pin can be left unconnected. 0 = reference input has dropped below approx. 10 MHz 1 = reference input is present (>10 MHz)
11	GND	—	Connect this pin to ground.
12	GND	—	Connect this pin to ground.
13	OUT0b	O	Output Clock 100 MHz HCSL output. Termination recommendations are provided in 3.3 HCSL Differential Output Terminations . Unused outputs should be left unconnected.
14	OUT0	O	

Pin Number	Pin Name	Pin Type	Function
15	VDDO0	P	Supply Voltage (1.8–3.3 V) for OUT0 Leave VDDOx pins of unused output drivers unconnected. An alternate option is to connect the VDDOx pin to a power supply and disable the output driver to minimize current consumption. Refer to 4. Power Supply Filtering Recommendations for bypass capacitor recommendations.
16	OUT1b	O	Output Clock
17	OUT1	O	100 MHz HCSL output. Termination recommendations are provided in 3.3 HCSL Differential Output Terminations . Unused outputs should be left unconnected.
18	VDDO1	P	Supply Voltage (1.8–3.3 V) for OUT1 Leave VDDOx pins of unused output drivers unconnected. An alternate option is to connect the VDDOx pin to a power supply and disable the output driver to minimize current consumption. Refer to 4. Power Supply Filtering Recommendations for bypass capacitor recommendations.
19	IMP_SEL	I	Impedance select pin for output drivers. IMP_SEL pin is sampled at power-up only. Low = 100 Ω High = 85 Ω
20	SSC_EN	I	Spread spectrum enable pin. Low = spread OFF High = spread ON (–0.5%)
21	OUT2b	O	Output Clock
22	OUT2	O	100 MHz HCSL output. Termination recommendations are provided in 3.3 HCSL Differential Output Terminations . Unused outputs should be left unconnected.
23	OUT3b	O	Output Clock
24	OUT3	O	Termination recommendations are provided in 3.3 HCSL Differential Output Terminations . Unused outputs should be left unconnected.
25	VDDO2	P	Supply Voltage (1.8–3.3 V) for OUT2 and OUT3 Leave VDDOx pins of unused output drivers unconnected. An alternate option is to connect the VDDOx pin to a power supply and disable the output driver to minimize current consumption. Refer to 4. Power Supply Filtering Recommendations for bypass capacitor recommendations.
26	OUT4b	O	Output Clock
27	OUT4	O	100 MHz HCSL output. Termination recommendations are provided in 3.3 HCSL Differential Output Terminations . Unused outputs should be left unconnected.
28	VDDO3	P	Supply Voltage (1.8–3.3 V) for OUT4 and OUT5 Leave VDDOx pins of unused output drivers unconnected. An alternate option is to connect the VDDOx pin to a power supply and disable the output driver to minimize current consumption. Refer to 4. Power Supply Filtering Recommendations for bypass capacitor recommendations.
29	OUT5b	O	Output Clock
30	OUT5	O	100 MHz HCSL output. Termination recommendations are provided in 3.3 HCSL Differential Output Terminations . Unused outputs should be left unconnected.

Pin Number	Pin Name	Pin Type	Function
31	OEb_OUT4	I	Output enable pin for OUT4. Low = output enabled High = output disabled
32	OEb_OUT5	I	Output enable pin for OUT5. Low = output enabled High = output disabled
33	VDDO4	P	Supply Voltage (1.8–3.3 V) for OUT6 Leave VDDOx pins of unused output drivers unconnected. An alternate option is to connect the VDDOx pin to a power supply and disable the output driver to minimize current consumption. Refer to 4. Power Supply Filtering Recommendations for bypass capacitor recommendations.
34	OUT6b	O	Output Clock 100 MHz HCSL output. Termination recommendations are provided in 3.3 HCSL Differential Output Terminations . Unused outputs should be left unconnected.
35	OUT6	O	
36	OEb_OUT6	I	Output enable pin for OUT6. Low = output enabled High = output disabled
37	OEb_OUT7	I	Output enable pin for OUT7. Low = output enabled High = output disabled
38	OUT7b	O	Output Clock 100 MHz HCSL output. Termination recommendations are provided in 3.3 HCSL Differential Output Terminations . Unused outputs should be left unconnected.
39	OUT7	O	
40	VDDO5	P	Supply Voltage (1.8–3.3 V) for OUT7 Leave VDDOx pins of unused output drivers unconnected. An alternate option is to connect the VDDOx pin to a power supply and disable the output driver to minimize current consumption. Refer to 4. Power Supply Filtering Recommendations for bypass capacitor recommendations.
41	GND PAD	P	Ground Pad This pad provides electrical and thermal connection to ground and must be connected for proper operation.

6.2 Si5224A-D01AM Pin Descriptions (32-QFN)

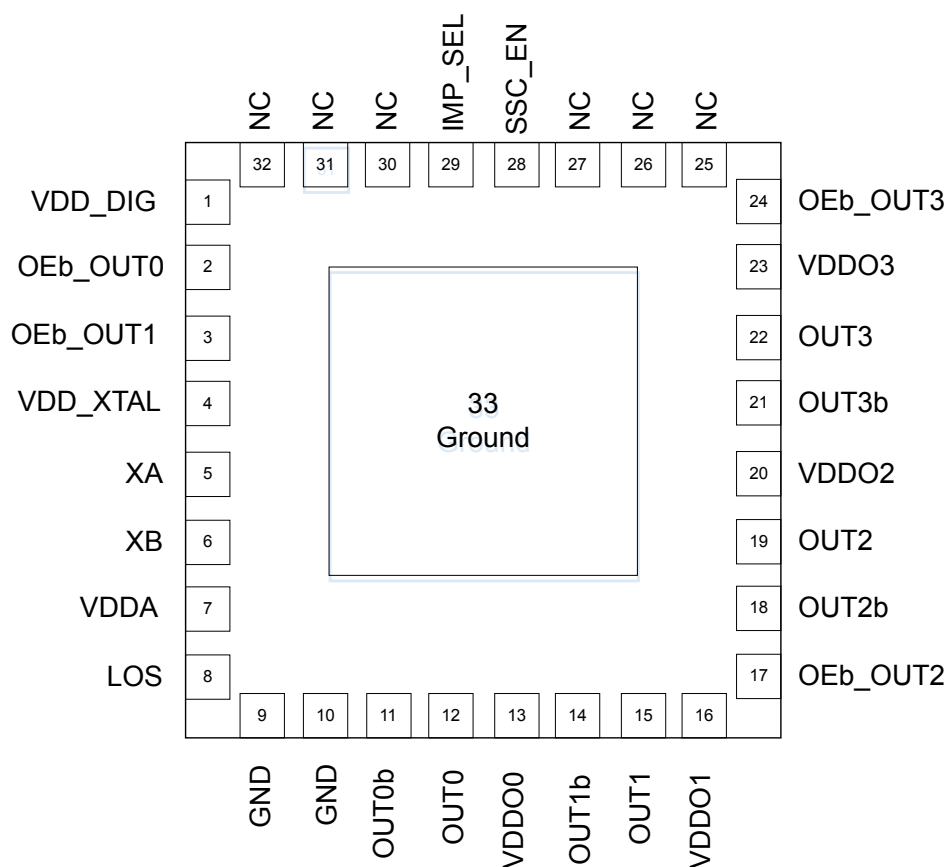


Figure 6.2. 32-QFN

Table 6.2. Si5224A-D01AM Pin Descriptions, (32-QFN)

Pin Number	Pin Name	Pin Type	Function
1	VDD_DIG	P	Voltage supply for digital functions. Connect to 1.8–3.3 V. Part of internal core VDD voltage. Must be connected to same voltage as VDDA and VDD_XTAL. Refer to 4. Power Supply Filtering Recommendations for by-pass capacitor recommendations.
2	OEb_OUT0	I	Output enable pin for OUT0. Low = output enabled High = output disabled
3	OEb_OUT1	I	Output enable pin for OUT1. Low = output enabled High = output disabled
4	VDD_XTAL	P	Voltage supply for crystal oscillator. Connect to 1.8–3.3 V. Part of internal core VDD voltage. Must be connected to same voltage as VDDA and VDD_DIG." Refer to 4. Power Supply Filtering Recommendations for by-pass capacitor recommendations.
5	XA	I	Refer to Section 5. Electrical Specifications for recommended crystal specifications.
6	XB	O	

Pin Number	Pin Name	Pin Type	Function
7	VDDA	P	<p>Core Supply Voltage. Connect to 1.8–3.3 V.</p> <p>See the Si5332-AM1/2/3 Family Reference Manual for power supply filtering recommendations.</p> <p>Must be connected to same voltage as VDD_DIG and VDD_XTAL.</p> <p>Refer to 4. Power Supply Filtering Recommendations for bypass capacitor recommendations.</p>
8	LOS	O	<p>The LOS status pin indicates whether the reference input has dropped below approximately 10 MHz. LOS is active low, open drain output and requires an external pull-up resistor of 1 to 10 kΩ for proper operation. If LOS is not required, this pin can be left unconnected.</p> <p>0 = reference input has dropped below approx. 10 MHz</p> <p>1 = reference input is present (>10 MHz)</p>
9	GND	P	Connect these pins to ground.
10	GND	P	
11	OUT0b	O	Output Clock
12	OUT0	O	100 MHz HCSL output. Termination recommendations are provided in 3.3 HCSL Differential Output Terminations . Unused outputs should be left unconnected.
13	VDDO0	P	<p>Supply Voltage (1.8–3.3 V) for OUT0</p> <p>See the Si5332-AM1/2/3 Family Reference Manual for power supply filtering recommendations.</p> <p>Leave VDDOx pins of unused output drivers unconnected. An alternate option is to connect the VDDOx pin to a power supply and disable the output driver to minimize current consumption. Refer to 4. Power Supply Filtering Recommendations for bypass capacitor recommendations.</p>
14	OUT1b	O	Output Clock
15	OUT1	O	100 MHz HCSL output. Termination recommendations are provided in 3.3 HCSL Differential Output Terminations . Unused outputs should be left unconnected.
16	VDDO1	P	<p>Supply Voltage (1.8–3.3 V) for OUT1</p> <p>Leave VDDOx pins of unused output drivers unconnected. An alternate option is to connect the VDDOx pin to a power supply and disable the output driver to minimize current consumption. Refer to 4. Power Supply Filtering Recommendations for bypass capacitor recommendations.</p>
17	OEb_OUT2	I	<p>Output enable pin for OUT2.</p> <p>Low = output enabled</p> <p>High = output disabled</p>
18	OUT2b	O	Output Clock
19	OUT2	O	100 MHz HCSL output. Termination recommendations are provided in 3.3 HCSL Differential Output Terminations . Unused outputs should be left unconnected.

Pin Number	Pin Name	Pin Type	Function
20	VDDO2	P	Supply Voltage (1.8–3.3 V) for OUT2 Leave VDDOx pins of unused output drivers unconnected. An alternate option is to connect the VDDOx pin to a power supply and disable the output driver to minimize current consumption. Refer to 4. Power Supply Filtering Recommendations for bypass capacitor recommendations.
21	OUT3b	O	Output Clock
22	OUT3	O	100 MHz HCSL output. Termination recommendations are provided in 3.3 HCSL Differential Output Terminations . Unused outputs should be left unconnected.
23	VDDO3	P	Supply Voltage (1.8–3.3 V) for OUT3 Leave VDDOx pins of unused output drivers unconnected. An alternate option is to connect the VDDOx pin to a power supply and disable the output driver to minimize current consumption. Refer to 4. Power Supply Filtering Recommendations for bypass capacitor recommendations.
24	OEb_OUT3	I	Output enable pin for OUT3. Low = output enabled High = output disabled
25	NC	—	Do not connect these pins to anything.
26	NC	—	
27	NC	—	
28	SSC_EN	I	Spread spectrum enable pin. Low = spread OFF High = spread ON (–0.5%)
29	IMP_SEL	I	Impedance select pin for output drivers. IMP_SEL pin is sampled at power-up only. Low = 100 Ω High = 85 Ω
30	NC	—	Do not connect these pins to anything.
31	NC	—	
32	NC	—	
33	GND PAD	P	Ground Pad This pad provides electrical and thermal connection to ground and must be connected for proper operation.

7. Package Outline

7.1 Si52258A-D01AM 6x6 mm 40-QFN Package Diagram

The figure below illustrates the package details for the Si52258A-D01AM in 40-QFN. The table below lists the values for the dimensions shown in the illustration.

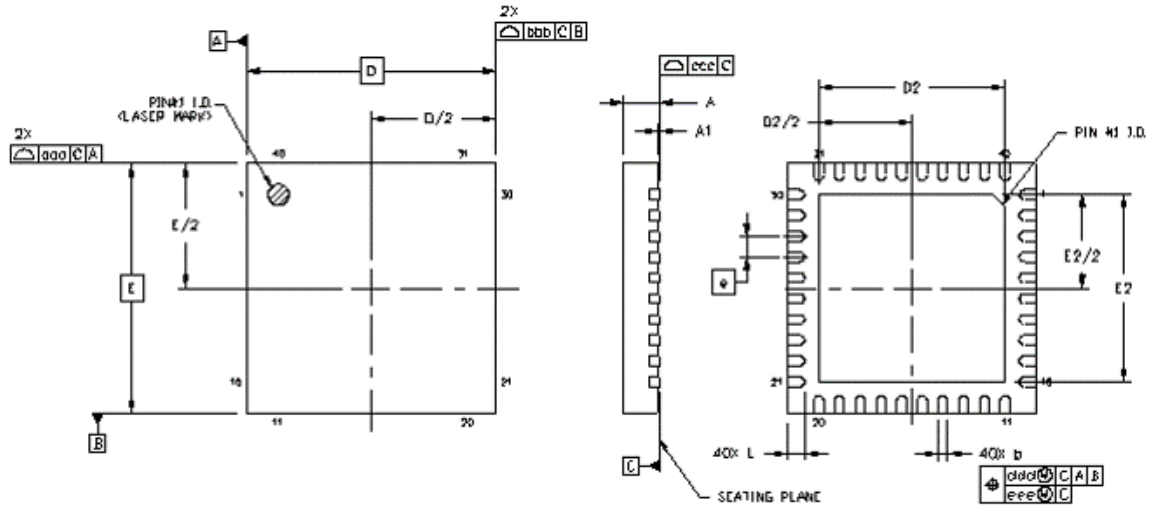


Figure 7.1. 40-Pin Quad Flat No-Lead (QFN)

Table 7.1. Package Dimensions

Dimension	Min	Nom	Max
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
b	0.18	0.25	0.30
D	6.00 BSC		
D2	4.35	4.50	4.65
e	0.50 BSC		
E	6.00 BSC		
E2	4.35	4.50	4.65
L	0.30	0.40	0.50
aaa	—	—	0.15
bbb	—	—	0.15
ccc	—	—	0.08
ddd	—	—	0.10
eee	—	—	0.05

Dimension	Min	Nom	Max
<p>Notes:</p> <ol style="list-style-type: none">1. All dimensions shown are in millimeters (mm) unless otherwise noted.2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.3. This drawing conforms to the JEDEC Solid State Outline MO-220.4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.			

7.2 Si52254A-D01AM 5x5 mm 32-QFN Package Diagram

The figure below illustrates the package details for the Si52254A-D01AM 32-QFN option. The table below lists the values for the dimensions shown in the illustration.

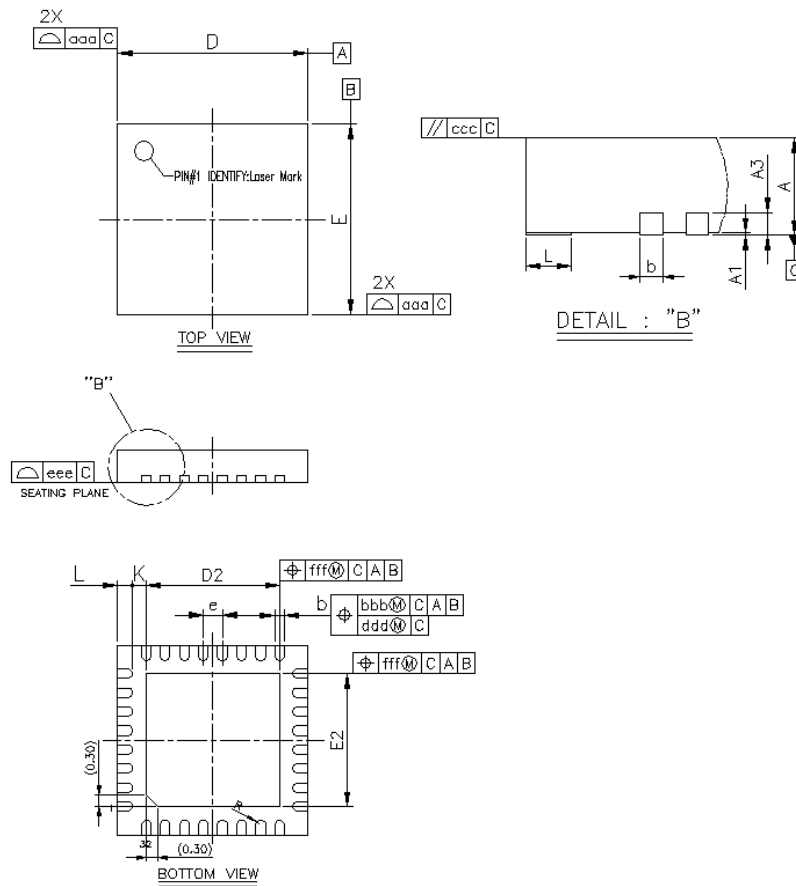


Figure 7.2. 32-Pin Quad Flat No-Lead (QFN)

Table 7.2. Package Dimensions

Dimension	MIN	NOM	MAX
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
A3	0.20 REF		
b	0.18	0.25	0.30
D/E	4.90	5.00	5.10
D2/E2	3.40	3.50	3.60
e	0.50 BSC		
L	0.30	0.40	0.50
K	0.20	---	---
R	0.09	---	0.14
aaa	0.15		
bbb	0.10		
ccc	0.10		

Dimension	MIN	NOM	MAX
ddd		0.05	
eee		0.08	
fff		0.10	

Notes:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to the JEDEC Solid State Outline MO-220, Variation VKKD-4.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

8. PCB Land Pattern

8.1 Si52258A-D01AM 40-QFN Land Pattern

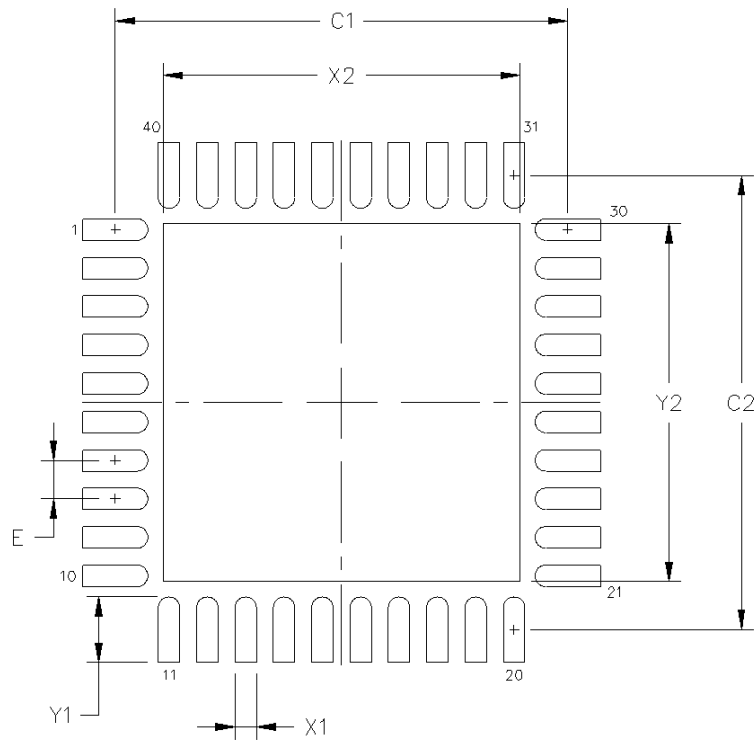


Figure 8.1. 40-QFN Land Pattern

Table 8.1. PCB Land Pattern Dimensions

Dimension	mm
C1	5.90
C2	5.90
e	0.50 BSC
X1	0.30
Y1	0.85
X2	4.65
Y2	4.65

Dimension	mm
<p>Notes:</p> <p>General</p> <ol style="list-style-type: none">1. All dimensions shown are in millimeters (mm) unless otherwise noted.2. This Land Pattern Design is based on the IPC-7351 guidelines. <p>Solder Mask Design</p> <ol style="list-style-type: none">1. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 μm minimum, all the way around the pad. <p>Stencil Design</p> <ol style="list-style-type: none">1. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.2. The stencil thickness should be 0.125 mm (5 mils).3. The ratio of stencil aperture to land pad size can be 1:1 for all perimeter pads.4. A 3\times3 array of 0.85 mm square openings on a 1.00 mm pitch can be used for the center ground pad. <p>Card Assembly</p> <ol style="list-style-type: none">1. A No-Clean, Type-3 solder paste is recommended.2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.	

8.2 Si52254A-D01AM 32-QFN Land Pattern

The figure below illustrates the PCB land pattern details for Si52254A-D01AM in 32-QFN package. The table below lists the values for the dimensions shown in the illustration.

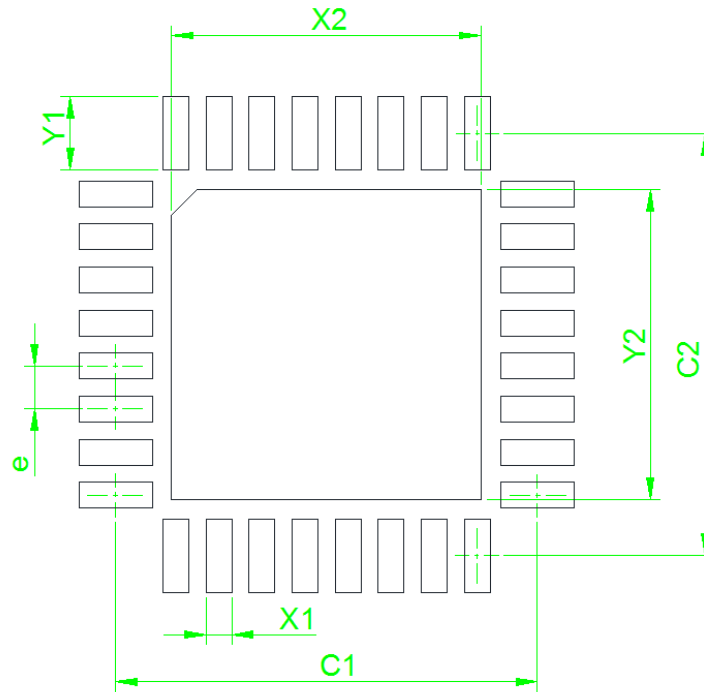


Figure 8.2. 32-QFN Land Pattern

Table 8.2. PCB Land Pattern Dimensions

Dimension	mm
C1	4.90
C2	4.90
e	0.50 BSC
X1	0.30
Y1	0.85
X2	3.60
Y2	3.60

Dimension	mm
<p>Notes:</p> <p>General</p> <ol style="list-style-type: none">1. All dimensions shown are in millimeters (mm) unless otherwise noted.2. This Land Pattern Design is based on the IPC-7351 guidelines. <p>Solder Mask Design</p> <ol style="list-style-type: none">1. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 μm minimum, all the way around the pad. <p>Stencil Design</p> <ol style="list-style-type: none">1. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.2. The stencil thickness should be 0.125 mm (5 mils).3. The ratio of stencil aperture to land pad size can be 1:1 for all perimeter pads.4. A 3\times3 array of 0.85 mm square openings on a 1.00 mm pitch can be used for the center ground pad. <p>Card Assembly</p> <ol style="list-style-type: none">1. A No-Clean, Type-3 solder paste is recommended.2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.	

9. Top Marking

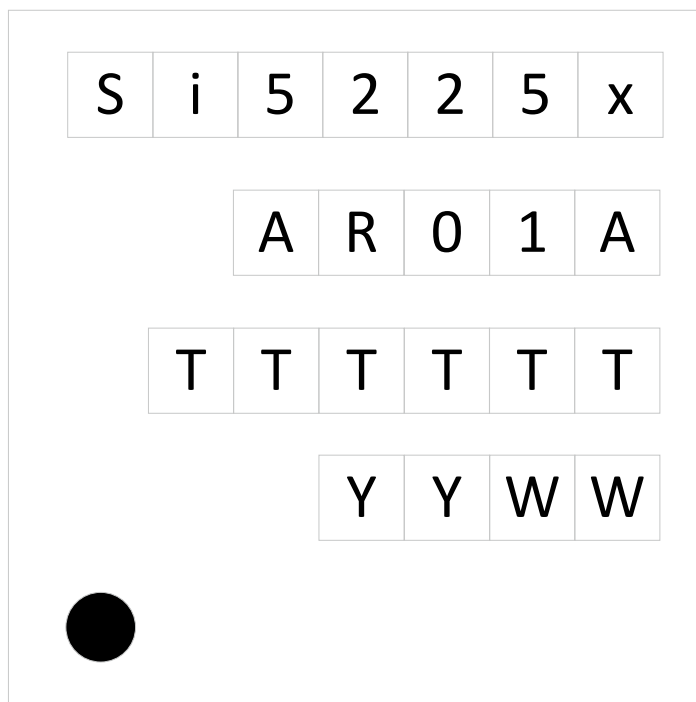


Figure 9.1. Top Marking

Table 9.1. Top Marking Explanation

Line	Characters	Description
1	Si52258 Si52254	Base part number
2	AR01A	A = Grade R = Product revision (reference ordering section for latest revision) 01 = Product identification, single input A = Automotive temperature grade. Package (QFN)
3	TTTTTT	Manufacturing trace code.
4	YYWW	Year (YY) and work week (WW) of package assembly

10. Revision History

Revision 1.0

January, 2021

- Updated [Table 5.4 Differential Clock Output Specifications](#) on page 9.
- Updated [Table 6.1 Si52258A-D01AM Pin Descriptions \(40-QFN\)](#) on page 15.
 - Removed "Default low" from hardware input pin function descriptions.
- Updated [Table 6.2 Si5224A-D01AM Pin Descriptions, \(32-QFN\)](#) on page 18.
 - Removed "Default low" from hardware input pin function descriptions.
- Updated [9. Top Marking](#).
- Updated Typ/Max performance specs in [Table 5.6 PCI-Express Clock Outputs \(100 MHz HCSL\)](#) on page 11.

Revision 0.7

September, 2019

- Initial release.

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