7.2 Requirements for Reading Array Data

To read array data from the outputs, the system must drive the CE# and OE# pins to V_{IL}. CE# is the power control and selects the device. OE# is the output control and gates array data to the output pins. WE# should remain at V_{IH}. The BYTE# pin determines whether the device outputs array data in words or bytes.

The internal state machine is set for reading array data upon device power-up, or after a hardware reset. This ensures that no spurious alteration of the memory content occurs during the power transition. No command is necessary in this mode to obtain array data. Standard microprocessor read cycles that assert valid addresses on the device-address inputs produce valid data on the device-data outputs. The device remains enabled for read access until the command register contents are altered.

See Reading Array Data on page 32 for more information. Refer to the AC Read Operations on page 49 table for timing specifications and to Figure 17.1 on page 49 for the timing diagram. I_{CC1} in the DC Characteristics table represents the active current specification for reading array data.

7.3 Writing Commands/Command Sequences

To write a command or command sequence (which includes programming data to the device and erasing sectors of memory), the system must drive WE# and CE# to V_{IL}, and OE# to V_{IH}.

For program operations, the BYTE# pin determines whether the device accepts program data in bytes or words. Refer to Word/Byte Configuration (Models 03, 04 Only) on page 12 for more information.

The device features an Unlock Bypass mode to facilitate faster programming. Once the device enters the Unlock Bypass mode, only two write cycles are required to program a word or byte, instead of four. Word/Byte Program Command Sequence on page 33 has details on programming data to the device using both standard and Unlock Bypass command sequences.

An erase operation can erase one sector, multiple sectors, or the entire device. Table 7.3 on page 15 and Table 7.5 on page 17 indicate the address space that each sector occupies. A *sector address* consists of the address bits required to uniquely select a sector. The Command Definitions on page 32 contains details on erasing a sector or the entire chip, or suspending/resuming the erase operation.

After the system writes the autoselect command sequence, the device enters the autoselect mode. The system can then read autoselect codes from the internal register (which is separate from the memory array) on DQ7–DQ0. Standard read cycle timings apply in this mode. Refer to Autoselect Mode on page 21 and Autoselect Command Sequence on page 32 for more information.

I_{CC2} in the DC Characteristics table represents the active current specification for the write mode. AC Characteristics on page 49 contains timing specification tables and timing diagrams for write operations.

7.4 Program and Erase Operation Status

During an erase or program operation, the system may check the status of the operation by reading the status bits on DQ7–DQ0. Standard read cycle timings and I_{CC} read specifications apply. Refer to Write Operation Status on page 40 for more information, and to AC Characteristics on page 49 for timing diagrams.

7.5 Accelerated Program Operation

The device offers accelerated program operations through the ACC function. This is one of two functions provided by the WP#/ACC (ACC on Model 00) pin. This function is primarily intended to allow faster manufacturing throughput at the factory.

If the system asserts V_{HH} on this pin, the device automatically enters the previously mentioned Unlock Bypass mode, temporarily unprotects any protected sectors, and uses the higher voltage on the pin to reduce the time required for program operations. The system would use a two-cycle program command sequence as required by the Unlock Bypass mode. Removing V_{HH} from the WP#/ACC pin returns the device to normal operation. Note that the WP#/ACC pin must not be at V_{HH} for operations other than accelerated programming, or device damage may result. In addition, the WP#/ACC pin must not be left floating or unconnected; inconsistent behavior of the device may result.

7.6 Standby Mode

When the system is not reading or writing to the device, it can place the device in the standby mode. In this mode, current consumption is greatly reduced, and the outputs are placed in the high impedance state, independent of the OE# input.

The device enters the CMOS standby mode when the CE# and RESET# pins are both held at $V_{CC} \pm 0.3$ V. (Note that this is a more restricted voltage range than V_{IH}.) If CE# and RESET# are held at V_{IH}, but not within $V_{CC} \pm 0.3$ V, the device will be in the standby mode, but the standby current will be greater. The device requires standard access time (t_{CE}) for read access when the device is in either of these standby modes, before it is ready to read data.

If the device is deselected during erasure or programming, the device draws active current until the operation is completed.

In the DC Characteristics table, I_{CC3} and I_{CC4} represents the standby current specification.

7.7 Automatic Sleep Mode

The automatic sleep mode minimizes Flash device energy consumption. The device automatically enables this mode when addresses remain stable for t_{ASM}. The automatic sleep mode is independent of the CE#, WE#, and OE# control signals. Standard address access timings provide new data when addresses are changed. While in sleep mode, output data is latched and always available to the system. I_{CC4} in DC Characteristics on page 46 represents the automatic sleep mode current specification.

Table 7.2 Automatic Sleep Mode Timing

Parameter	Description	Max.	Unit
t_{ASM}	Automatic Sleep Mode	t_{ACC}+30	ns

7.8 RESET#: Hardware Reset Pin

The RESET# pin provides a hardware method of resetting the device to reading array data. When the system drives the RESET# pin to V_{IL} for at least a period of t_{RP}, the device immediately terminates any operation in progress, tristates all data output pins, and ignores all read/write attempts for the duration of the RESET# pulse. The device also resets the internal state machine to reading array data. The operation that was interrupted should be reinitiated once the device is ready to accept another command sequence, to ensure data integrity.

Current is reduced for the duration of the RESET# pulse. When RESET# is held at V_{SS}±0.3 V, the device draws CMOS standby current (I_{CC4}). If RESET# is held at V_{IL} but not within V_{SS}±0.3 V, the standby current will be greater.

The RESET# pin may be tied to the system reset circuitry. A system reset would thus also reset the Flash memory, enabling the system to read the boot-up firmware from the Flash memory.

If RESET# is asserted during a program or erase operation, the RY/BY# pin remains a *0* (busy) until the internal reset operation is complete, which requires a time of t_{READY} (during Embedded Algorithms). The system can thus monitor RY/BY# to determine whether the reset operation is complete. If RESET# is asserted when a program or erase operation is not executing (RY/BY# pin is *1*), the reset operation is completed within a time of t_{READY} (not during Embedded Algorithms). The system can read data t_{RH} after the RESET# pin returns to V_{IH}.

Refer to AC Characteristics on page 49 for RESET# parameters and to Figure 17.2 on page 50 for the timing diagram.

7.9 Output Disable Mode

When the OE# input is at V_{IH}, output from the device is disabled. The output pins are placed in the high impedance state.

7.10 Sector Addresss Tables

Table 7.3 Model 00 Sector Addresses (Sheet 1 of 2)

Sector	A21	A20	A19	A18	A17	A16	Address Range (in hexadecimal)
SA0	0	0	0	0	0	0	000000–00FFFF
SA1	0	0	0	0	0	1	010000–01FFFF
SA2	0	0	0	0	1	0	020000–02FFFF
SA3	0	0	0	0	1	1	030000–03FFFF
SA4	0	0	0	1	0	0	040000–04FFFF
SA5	0	0	0	1	0	1	050000–05FFFF
SA6	0	0	0	1	1	0	060000–06FFFF
SA7	0	0	0	1	1	1	070000–07FFFF
SA8	0	0	1	0	0	0	080000–08FFFF
SA9	0	0	1	0	0	1	090000–09FFFF
SA10	0	0	1	0	1	0	0A0000–0AFFFF
SA11	0	0	1	0	1	1	0B0000–0BFFFF
SA12	0	0	1	1	0	0	0C0000–0CFFFF
SA13	0	0	1	1	0	1	0D0000–0DFFFF
SA14	0	0	1	1	1	0	0E0000–0EFFFF
SA15	0	0	1	1	1	1	0F0000–0FFFFF
SA16	0	1	0	0	0	0	100000–10FFFF
SA17	0	1	0	0	0	1	110000–11FFFF
SA18	0	1	0	0	1	0	120000–12FFFF
SA19	0	1	0	0	1	1	130000–13FFFF
SA20	0	1	0	1	0	0	140000–14FFFF
SA21	0	1	0	1	0	1	150000–15FFFF
SA22	0	1	0	1	1	0	160000–16FFFF
SA23	0	1	0	1	1	1	170000–17FFFF
SA24	0	1	1	0	0	0	180000–18FFFF
SA25	0	1	1	0	0	1	190000–19FFFF
SA26	0	1	1	0	1	0	1A0000–1AFFFF
SA27	0	1	1	0	1	1	1B0000–1BFFFF
SA28	0	1	1	1	0	0	1C0000–1CFFFF
SA29	0	1	1	1	0	1	1D0000–1DFFFF
SA30	0	1	1	1	1	0	1E0000–1EFFFF
SA31	0	1	1	1	1	1	1F0000–1FFFFF
SA32	1	0	0	0	0	0	200000–20FFFF
SA33	1	0	0	0	0	1	210000–21FFFF
SA34	1	0	0	0	1	0	220000–22FFFF
SA35	1	0	0	0	1	1	230000–23FFFF
SA36	1	0	0	1	0	0	240000–24FFFF
SA37	1	0	0	1	0	1	250000–25FFFF
SA38	1	0	0	1	1	0	260000–26FFFF
SA39	1	0	0	1	1	1	270000–27FFFF
SA40	1	0	1	0	0	0	280000–28FFFF
SA41	1	0	1	0	0	1	290000–29FFFF
SA42	1	0	1	0	1	0	2A0000–2AFFFF

Table 7.3 Model 00 Sector Addresses (Sheet 2 of 2)

Sector	A21	A20	A19	A18	A17	A16	Address Range (in hexadecimal)
SA43	1	0	1	0	1	1	2B0000–2BFFFF
SA44	1	0	1	1	0	0	2C0000–2CFFFF
SA45	1	0	1	1	0	1	2D0000–2DFFFF
SA46	1	0	1	1	1	0	2E0000–2EFFFF
SA47	1	0	1	1	1	1	2F0000–2FFFFF
SA48	1	1	0	0	0	0	300000–30FFFF
SA49	1	1	0	0	0	1	310000–31FFFF
SA50	1	1	0	0	1	0	320000–32FFFF
SA51	1	1	0	0	1	1	330000–33FFFF
SA52	1	1	0	1	0	0	340000–34FFFF
SA53	1	1	0	1	0	1	350000–35FFFF
SA54	1	1	0	1	1	0	360000–36FFFF
SA55	1	1	0	1	1	1	370000–37FFFF
SA56	1	1	1	0	0	0	380000–38FFFF
SA57	1	1	1	0	0	1	390000–39FFFF
SA58	1	1	1	0	1	0	3A0000–3AFFFF
SA59	1	1	1	0	1	1	3B0000–3BFFFF
SA60	1	1	1	1	0	0	3C0000–3CFFFF
SA61	1	1	1	1	0	1	3D0000–3DFFFF
SA62	1	1	1	1	1	0	3E0000–3EFFFF
SA63	1	1	1	1	1	1	3F0000–3FFFFF

Note

All sectors are 64 Kbytes in size.

Table 7.4 Model 00 Secured Silicon Sector Addresses

Sector Address A21–A7	Sector Size (bytes)	(x8) Address Range
000000000000000	128	000000h–00007fh
000000000001000	128	000400h-00047Fh

Table 7.5 Model 03 Sector Addresses (Sheet 1 of 2)

Sector	Sector Address A20–A12	Sector Size (Kbytes/ Kwords)	(x8) Address Range	(x16) Address Range
SA0	000000xxx	64/32	000000h–00FFFFh	000000h–07FFFh
SA1	000001xxx	64/32	010000h–01FFFFh	008000h–0FFFFh
SA2	000010xxx	64/32	020000h–02FFFFh	010000h–17FFFh
SA3	000011xxx	64/32	030000h–03FFFFh	018000h–01FFFFh
SA4	000100xxx	64/32	040000h–04FFFFh	020000h–027FFFh
SA5	000101xxx	64/32	050000h–05FFFFh	028000h–02FFFFh
SA6	000110xxx	64/32	060000h–06FFFFh	030000h–037FFFh
SA7	000111xxx	64/32	070000h–07FFFFh	038000h–03FFFFh
SA8	001000xxx	64/32	080000h–08FFFFh	040000h–047FFFh
SA9	001001xxx	64/32	090000h–09FFFFh	048000h–04FFFFh
SA10	001010xxx	64/32	0A0000h–0AFFFFh	050000h–057FFFh
SA11	001011xxx	64/32	0B0000h–0BFFFFh	058000h–05FFFFh
SA12	001100xxx	64/32	0C0000h–0CFFFFh	060000h–067FFFh
SA13	001101xxx	64/32	0D0000h–0DFFFFh	068000h–06FFFFh
SA14	001110xxx	64/32	0E0000h–0EFFFFh	070000h–077FFFh
SA15	001111xxx	64/32	0F0000h–0FFFFFh	078000h–07FFFFh
SA16	010000xxx	64/32	100000h–10FFFFh	080000h–087FFFh
SA17	010001xxx	64/32	110000h–11FFFFh	088000h–08FFFFh
SA18	010010xxx	64/32	120000h–12FFFFh	090000h–097FFFh
SA19	010011xxx	64/32	130000h–13FFFFh	098000h–09FFFFh
SA20	010100xxx	64/32	140000h–14FFFFh	0A0000h–0A7FFFh
SA21	010101xxx	64/32	150000h–15FFFFh	0A8000h–0AFFFFh
SA22	010110xxx	64/32	160000h–16FFFFh	0B0000h–0B7FFFh
SA23	010111xxx	64/32	170000h–17FFFFh	0B8000h–0BFFFFh
SA24	011000xxx	64/32	180000h–18FFFFh	0C0000h–0C7FFFh
SA25	011001xxx	64/32	190000h–19FFFFh	0C8000h–0CFFFFh
SA26	011010xxx	64/32	1A0000h–1AFFFFh	0D0000h–0D7FFFh
SA27	011011xxx	64/32	1B0000h–1BFFFFh	0D8000h–0DFFFFh
SA28	011100xxx	64/32	1C0000h–1CFFFFh	0E0000h–0E7FFFh
SA29	011101xxx	64/32	1D0000h–1DFFFFh	0E8000h–0EFFFFh
SA30	011110xxx	64/32	1E0000h–1EFFFFh	0F0000h–0F7FFFh
SA31	011111xxx	64/32	1F0000h–1FFFFFh	0F8000h–0FFFFFh
SA32	100000xxx	64/32	200000h–20FFFFh	100000h–107FFFh
SA33	100001xxx	64/32	210000h–21FFFFh	108000h–10FFFFh
SA34	100010xxx	64/32	220000h–22FFFFh	110000h–117FFFh
SA35	100011xxx	64/32	230000h–23FFFFh	118000h–11FFFFh
SA36	100100xxx	64/32	240000h–24FFFFh	120000h–127FFFh
SA37	100101xxx	64/32	250000h–25FFFFh	128000h–12FFFFh
SA38	100110xxx	64/32	260000h–26FFFFh	130000h–137FFFh
SA39	100111xxx	64/32	270000h–27FFFFh	138000h–13FFFFh
SA40	101000xxx	64/32	280000h–28FFFFh	140000h–147FFFh
SA41	101001xxx	64/32	290000h–29FFFFh	148000h–14FFFFh
SA42	101010xxx	64/32	2A0000h–2AFFFFh	150000h–157FFFh

Table 7.5 Model 03 Sector Addresses (Sheet 2 of 2)

Sector	Sector Address A20–A12	Sector Size (Kbytes/ Kwords)	(x8) Address Range	(x16) Address Range
SA43	101011xxx	64/32	2B0000h–2BFFFFh	158000h–15FFFFh
SA44	101100xxx	64/32	2C0000h–2CFFFFh	160000h–167FFFh
SA45	101101xxx	64/32	2D0000h–2DFFFFh	168000h–16FFFFh
SA46	101110xxx	64/32	2E0000h–2EFFFFh	170000h–177FFFh
SA47	101111xxx	64/32	2F0000h–2FFFFFh	178000h–17FFFFh
SA48	110000xxx	64/32	300000h–30FFFFh	180000h–187FFFh
SA49	110001xxx	64/32	310000h–31FFFFh	188000h–18FFFFh
SA50	110010xxx	64/32	320000h–32FFFFh	190000h–197FFFh
SA51	110011xxx	64/32	330000h–33FFFFh	198000h–19FFFFh
SA52	110100xxx	64/32	340000h–34FFFFh	1A0000h–1A7FFFh
SA53	110101xxx	64/32	350000h–35FFFFh	1A8000h–1AFFFFh
SA54	110110xxx	64/32	360000h–36FFFFh	1B0000h–1B7FFFh
SA55	110111xxx	64/32	370000h–37FFFFh	1B8000h–1BFFFFh
SA56	111000xxx	64/32	380000h–38FFFFh	1C0000h–1C7FFFh
SA57	111001xxx	64/32	390000h–39FFFFh	1C8000h–1CFFFFh
SA58	111010xxx	64/32	3A0000h–3AFFFFh	1D0000h–1D7FFFh
SA59	111011xxx	64/32	3B0000h–3BFFFFh	1D8000h–1DFFFFh
SA60	111100xxx	64/32	3C0000h–3CFFFFh	1E0000h–1E7FFFh
SA61	111101xxx	64/32	3D0000h–3DFFFFh	1E8000h–1EFFFFh
SA62	111110xxx	64/32	3E0000h–3EFFFFh	1F0000h–1F7FFFh
SA63	111111000	8/4	3F0000h–3F1FFFh	1F8000h–1F8FFFh
SA64	111111001	8/4	3F2000h–3F3FFFh	1F9000h–1F9FFFh
SA65	111111010	8/4	3F4000h–3F5FFFh	1FA000h–1FAFFFh
SA66	111111011	8/4	3F6000h–3F7FFFh	1FB000h–1FBFFFh
SA67	111111100	8/4	3F8000h–3F9FFFh	1FC000h–1FCFFFh
SA68	111111101	8/4	3FA000h–3FBFFFh	1FD000h–1FDFFFh
SA69	111111110	8/4	3FC000h–3FDFFFh	1FE000h–1FEFFFh
SA70	111111111	8/4	3FE000h–3FFFFFh	1FF000h–1FFFFFh

Note
The address range is A20:A-1 in byte mode (BYTE#=V_{IL}) or A20:A0 in word mode (BYTE#=V_{IH}).

Table 7.6 Model 03 Secured Silicon Sector Addresses

Sector Address A20–A12	Sector Size (bytes/words)	(x8) Address Range	(x16) Address Range
111111111	256/128	3FFF00h–3FFFFFh	1FFF80h–1FFFFFh

Table 7.7 Model 04 Sector Addresses (Sheet 1 of 2)

Sector	Sector Address A20–A12	Sector Size (Kbytes/ Kwords)	(x8) Address Range	(x16) Address Range
SA0	000000000	8/4	000000h-001FFFh	000000h–000FFFh
SA1	000000001	8/4	002000h-003FFFh	001000h–001FFFh
SA2	000000010	8/4	004000h-005FFFh	002000h–002FFFh
SA3	000000011	8/4	006000h-007FFFh	003000h–003FFFh
SA4	000000100	8/4	008000h-009FFFh	004000h–004FFFh
SA5	000000101	8/4	00A000h-00BFFFh	005000h–005FFFh
SA6	000000110	8/4	00C000h-00DFFFh	006000h–006FFFh
SA7	000000111	8/4	00E000h-00FFFFh	007000h–007FFFh
SA8	000001xxx	64/32	010000h-01FFFFh	008000h–00FFFFh
SA9	000010xxx	64/32	020000h-02FFFFh	010000h–017FFFh
SA10	000011xxx	64/32	030000h-03FFFFh	018000h–01FFFFh
SA11	000100xxx	64/32	040000h-04FFFFh	020000h–027FFFh
SA12	000101xxx	64/32	050000h-05FFFFh	028000h–02FFFFh
SA13	000110xxx	64/32	060000h-06FFFFh	030000h–037FFFh
SA14	000111xxx	64/32	070000h-07FFFFh	038000h–03FFFFh
SA15	001000xxx	64/32	080000h-08FFFFh	040000h–047FFFh
SA16	001001xxx	64/32	090000h-09FFFFh	048000h–04FFFFh
SA17	001010xxx	64/32	0A0000h-0AFFFFh	050000h–057FFFh
SA18	001011xxx	64/32	0B0000h-0BFFFFh	058000h–05FFFFh
SA19	001100xxx	64/32	0C0000h-0CFFFFh	060000h–067FFFh
SA20	001101xxx	64/32	0D0000h-0DFFFFh	068000h–06FFFFh
SA21	001110xxx	64/32	0E0000h-0EFFFFh	070000h–077FFFh
SA22	001111xxx	64/32	0F0000h-0FFFFFh	078000h–07FFFFh
SA23	010000xxx	64/32	100000h-10FFFFh	080000h–087FFFh
SA24	010001xxx	64/32	110000h-11FFFFh	088000h–08FFFFh
SA25	010010xxx	64/32	120000h-12FFFFh	090000h–097FFFh
SA26	010011xxx	64/32	130000h-13FFFFh	098000h–09FFFFh
SA27	010100xxx	64/32	140000h-14FFFFh	0A0000h–0A7FFFh
SA28	010101xxx	64/32	150000h-15FFFFh	0A8000h–0AFFFFh
SA29	010110xxx	64/32	160000h-16FFFFh	0B0000h–0B7FFFh
SA30	010111xxx	64/32	170000h-17FFFFh	0B8000h–0BFFFFh
SA31	011000xxx	64/32	180000h-18FFFFh	0C0000h–0C7FFFh
SA32	011001xxx	64/32	190000h-19FFFFh	0C8000h–0CFFFFh
SA33	011010xxx	64/32	1A0000h-1AFFFFh	0D0000h–0D7FFFh
SA34	011011xxx	64/32	1B0000h-1BFFFFh	0D8000h–0DFFFFh
SA35	011100xxx	64/32	1C0000h-1CFFFFh	0E0000h–0E7FFFh
SA36	011101xxx	64/32	1D0000h-1DFFFFh	0E8000h–0EFFFFh
SA37	011110xxx	64/32	1E0000h-1EFFFFh	0F0000h–0F7FFFh
SA38	011111xxx	64/32	1F0000h-1FFFFFh	0F8000h–0FFFFFh
SA39	100000xxx	64/32	200000h-20FFFFh	100000h–107FFFh
SA40	100001xxx	64/32	210000h-21FFFFh	108000h–10FFFFh
SA41	100010xxx	64/32	220000h-22FFFFh	110000h–117FFFh
SA42	100011xxx	64/32	230000h-23FFFFh	118000h–11FFFFh

Table 7.7 Model 04 Sector Addresses (Sheet 2 of 2)

Sector	Sector Address A20–A12	Sector Size (Kbytes/ Kwords)	(x8) Address Range	(x16) Address Range
SA43	100100xxx	64/32	240000h-24FFFFh	120000h–127FFFh
SA44	100101xxx	64/32	250000h-25FFFFh	128000h–12FFFFh
SA45	100110xxx	64/32	260000h-26FFFFh	130000h–137FFFh
SA46	100111xxx	64/32	270000h-27FFFFh	138000h–13FFFFh
SA47	101000xxx	64/32	280000h-28FFFFh	140000h–147FFFh
SA48	101001xxx	64/32	290000h-29FFFFh	148000h–14FFFFh
SA49	101010xxx	64/32	2A0000h-2AFFFFh	150000h–157FFFh
SA50	101011xxx	64/32	2B0000h-2BFFFFh	158000h–15FFFFh
SA51	101100xxx	64/32	2C0000h-2CFFFFh	160000h–167FFFh
SA52	101101xxx	64/32	2D0000h-2DFFFFh	168000h–16FFFFh
SA53	101110xxx	64/32	2E0000h-2EFFFFh	170000h–177FFFh
SA54	101111xxx	64/32	2F0000h-2FFFFFh	178000h–17FFFFh
SA55	111000xxx	64/32	300000h-30FFFFh	180000h–187FFFh
SA56	110001xxx	64/32	310000h-31FFFFh	188000h–18FFFFh
SA57	110010xxx	64/32	320000h-32FFFFh	190000h–197FFFh
SA58	110011xxx	64/32	330000h-33FFFFh	198000h–19FFFFh
SA59	110100xxx	64/32	340000h-34FFFFh	1A0000h–1A7FFFh
SA60	110101xxx	64/32	350000h-35FFFFh	1A8000h–1AFFFFh
SA61	110110xxx	64/32	360000h-36FFFFh	1B0000h–1B7FFFh
SA62	110111xxx	64/32	370000h-37FFFFh	1B8000h–1BFFFFh
SA63	111000xxx	64/32	380000h-38FFFFh	1C0000h–1C7FFFh
SA64	111001xxx	64/32	390000h-39FFFFh	1C8000h–1CFFFFh
SA65	111010xxx	64/32	3A0000h-3AFFFFh	1D0000h–1D7FFFh
SA66	111011xxx	64/32	3B0000h-3BFFFFh	1D8000h–1DFFFFh
SA67	111100xxx	64/32	3C0000h-3CFFFFh	1E0000h–1E7FFFh
SA68	111101xxx	64/32	3D0000h-3DFFFFh	1E8000h–1EFFFFh
SA69	111110xxx	64/32	3E0000h-3EFFFFh	1F0000h–1F7FFFh
SA70	111111xxx	64/32	3F0000h-3FFFFFh	1F8000h–1FFFFFh

Note

The address range is A20:A-1 in byte mode (BYTE#=V_{IL}) or A20:A0 in word mode (BYTE#=V_{IH}).

Table 7.8 Model 04 Secured Silicon Sector Addresses

Sector Address A20–A12	Sector Size (bytes/words)	(x8) Address Range	(x16) Address Range
000000000	256/128	000000h-0000FFh	00000h-0007Fh

7.11 Autoselect Mode

The autoselect mode provides manufacturer and device identification, and sector protection verification, through identifier codes output on DQ7–DQ0. This mode is primarily intended for programming equipment to automatically match a device to be programmed with its corresponding programming algorithm. However, the autoselect codes can also be accessed in-system through the command register.

When using programming equipment, the autoselect mode requires V_{ID} (11.5 V to 12.5 V) on address pin A9. Address pins A6, A1, and A0 must be as shown in Table 7.9. In addition, when verifying sector protection, the sector address must appear on the appropriate highest order address bits (see Table 7.3 on page 15 and Table 7.5 on page 17). Table 7.9 shows the remaining address bits that are don't care. When all necessary bits have been set as required, the programming equipment may then read the corresponding identifier code on DQ7-DQ0.

To access the autoselect codes in-system, the host system can issue the autoselect command via the command register, as shown in Table 11.2 on page 38. This method does not require V_{ID}. See Command Definitions for details on using the autoselect mode.

Table 7.9 S29AL032D Autoselect Codes (High Voltage Method)

Description	Mode	CE#	OE#	WE#	A21 to A12	A11 to A10	A9	A8 to A7	A6	A5 to A4	A3 to A2	A1	A0	DQ8 to DQ15	DQ7 to DQ0
Manufacturer ID: Spansion		L	L	H	X	X	V_{ID}	X	L	X	L	L	L	X	01h
Device ID: S29AL032D (Model 00)	Byte	L	L	H	X	X	V_{ID}	X	L	X	L	L	H	N/A	A3h
Device ID: S29AL032D (Model 03)	Word	L	L	H	X	X	V_{ID}	X	L	X	L	L	H	22h	F6h
	Byte	L	L	H										X	F6h
Device ID: S29AL032D (Model 04)	Word	L	L	H	X	X	V_{ID}	X	L	X	L	L	H	22h	F9h
	Byte	L	L	H										X	F9h
Sector Protection Verification		L	L	H	SA	X	V_{ID}	X	L	X	L	H	L	X	01h (protected)
														X	00h (unprotected)
Secured Silicon Sector Indicator Bit (DQ7) (Model 00)		L	L	H	X	X	V_{ID}	X	L	X	L	H	H	X	85 (factory locked)
														X	05 (not factory locked)
Secured Silicon Sector Indicator Bit (DQ7) (Model 03)		L	L	H	X	X	V_{ID}	X	L	X	L	H	H	X	8D (factory locked)
														X	1D (not factory locked)
Secured Silicon Sector Indicator Bit (DQ7) (Model 04)		L	L	H	X	X	V_{ID}	X	L	X	L	H	H	X	9D (factory locked)
														X	0D (not factory locked)

Legend

L = Logic Low = V_{IL}, H = Logic High = V_{IH}, SA = Sector Address, X = Don't care.

Note

The autoselect codes may also be accessed in-system via command sequences. See Table 11.2 on page 38.

7.12 Sector Protection/Unprotection

The hardware sector protection feature disables both program and erase operations in any sector. The hardware sector unprotection feature re-enables both program and erase operations in previously protected sectors.

The device is shipped with all sectors unprotected. Spansion offers the option of programming and protecting sectors at its factory prior to shipping the device through the Spansion ExpressFlash™ Service. Contact a Spansion representative for further details.

It is possible to determine whether a sector is protected or unprotected. See Autoselect Mode for details.

Sector protection/unprotection can be implemented via two methods.

The primary method requires V_{ID} on the RESET# pin only, and can be implemented either in-system or via programming equipment. Figure 7.1 on page 25 shows the algorithms and Figure 17.13 on page 57 shows the timing diagram. This method uses standard microprocessor bus cycle timing. For sector unprotect, all unprotected sectors must first be protected prior to the first sector unprotect write cycle.

The alternate method intended only for programming equipment requires V_{ID} on address pin A9 and OE#. This method is compatible with programmer routines written for earlier 3.0-volt-only Spansion flash devices. Details on this method are provided in a supplement, publication number 21468. Contact a Spansion representative to request a copy.

Table 7.10 Sector Block Addresses for Protection/Unprotection — Model 00

Sector/Sector Block	A21–A16	Sector/Sector Block Size
SA0	000000	64 Kbytes
SA1-SA3	000001, 000010, 000011	192 (3x64) Kbytes
SA4-SA7	000100, 000101, 000110, 000111	256 (4x64) Kbytes
SA8-SA11	001000, 001001, 001010, 001011	256 (4x64) Kbytes
SA12-SA15	001100, 001101, 001110, 001111	256 (4x64) Kbytes
SA16-SA19	010000, 010001, 010010, 010011	256 (4x64) Kbytes
SA20-SA23	010100, 010101, 010110, 010111	256 (4x64) Kbytes
SA24-SA27	011000, 011001, 011010, 011011	256 (4x64) Kbytes
SA28-SA31	011100, 011101, 011110, 011111	256 (4x64) Kbytes
SA32-SA35	100000, 100001, 100010, 100011	256 (4x64) Kbytes
SA36-SA39	100100, 100101, 100110, 100111	256 (4x64) Kbytes
SA40-SA43	101000, 101001, 101010, 101011	256 (4x64) Kbytes
SA44-SA47	101100, 101101, 101110, 101111	256 (4x64) Kbytes
SA48-SA51	110000, 110001, 110010, 110011	256 (4x64) Kbytes
SA52-SA55	110100, 110101, 110110, 110111	256 (4x64) Kbytes
SA56-SA59	111000, 111001, 111010, 111011	256 (4x64) Kbytes
SA60-SA62	111100, 111101, 111110	192 (4x64) Kbytes
SA63	111111	64 Kbytes

Table 7.11 Sector Block Addresses for Protection/Unprotection — Model 03

Sector / Sector Block	A20–A 12	Sector/Sector Block Size
SA0-SA3	000000XXX, 000001XXX, 000010XXX, 000011XXX	256 (4x64) Kbytes
SA4-SA7	0001XXXXX	256 (4x64) Kbytes
SA8-SA11	0010XXXXX	256 (4x64) Kbytes
SA12-SA15	0011XXXXX	256 (4x64) Kbytes
SA16-SA19	0100XXXXX	256 (4x64) Kbytes
SA20-SA23	0101XXXXX	256 (4x64) Kbytes
SA24-SA27	0110XXXXX	256 (4x64) Kbytes
SA28-SA31	0111XXXXX	256 (4x64) Kbytes
SA32-SA35	1000XXXXX	256 (4x64) Kbytes
SA36-SA39	1001XXXXX	256 (4x64) Kbytes
SA40-SA43	1010XXXXX	256 (4x64) Kbytes
SA44-SA47	1011XXXXX	256 (4x64) Kbytes
SA48-SA51	1100XXXXX	256 (4x64) Kbytes
SA52-SA55	1101XXXXX	256 (4x64) Kbytes
SA56-SA59	1110XXXXX	256 (4x64) Kbytes
SA60-SA62	111100XXX, 111101XXX, 111110XXX	192 (3x64) Kbytes
SA63	111111000	8 Kbytes
SA64	111111001	8 Kbytes
SA65	111111010	8 Kbytes
SA66	111111011	8 Kbytes
SA67	111111100	8 Kbytes
SA68	111111101	8 Kbytes
SA69	111111110	8 Kbytes
SA70	111111111	8 Kbytes

Table 7.12 Sector Block Addresses for Protection/Unprotection — Model 04

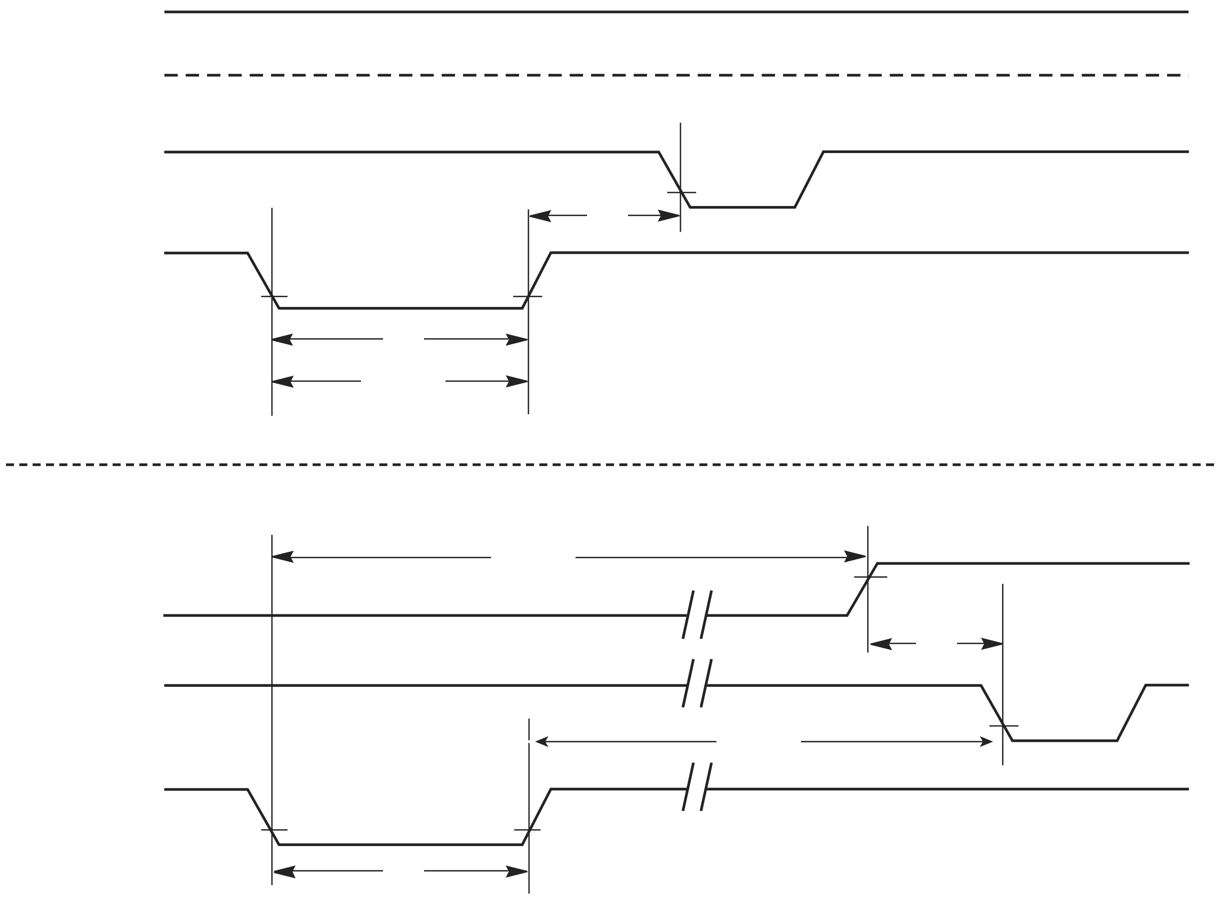
Sector / Sector Block	A20–A12	Sector/Sector Block Size
SA70-SA67	111111XXX, 111110XXX, 111101XXX, 111100XXX	256 (4x64) Kbytes
SA66-SA63	1110XXXXX	256 (4x64) Kbytes
SA62-SA59	1101XXXXX	256 (4x64) Kbytes
SA58-SA55	1100XXXXX	256 (4x64) Kbytes
SA54-SA51	1011XXXXX	256 (4x64) Kbytes
SA50-SA47	1010XXXXX	256 (4x64) Kbytes
SA46-SA43	1001XXXXX	256 (4x64) Kbytes
SA42-SA39	1000XXXXX	256 (4x64) Kbytes
SA38-SA35	0111XXXXX	256 (4x64) Kbytes
SA34-SA31	0110XXXXX	256 (4x64) Kbytes
SA30-SA27	0101XXXXX	256 (4x64) Kbytes
SA26-SA23	0100XXXXX	256 (4x64) Kbytes
SA22–SA19	0011XXXXX	256 (4x64) Kbytes
SA18-SA15	0010XXXXX	256 (4x64) Kbytes
SA14-SA11	0001XXXXX	256 (4x64) Kbytes
SA10-SA8	000011XXX, 000010XXX, 000001XXX	192 (3x64) Kbytes
SA7	000000111	8 Kbytes
SA6	000000110	8 Kbytes
SA5	000000101	8 Kbytes
SA4	000000100	8 Kbytes
SA3	000000011	8 Kbytes
SA2	000000010	8 Kbytes
SA1	000000001	8 Kbytes
SA0	000000000	8 Kbytes

17.2 Hardware Reset (RESET#)

Parameter		Description	Test Setup		All Speed Options	Unit
JEDEC	Std.					
	t_{READY}	RESET# Pin Low (During Embedded Algorithms) to Read or Write (See Note)		Max	20	µs
	t_{READY}	RESET# Pin Low (NOT During Embedded Algorithms) to Read or Write (See Note)		Max	500	ns
	t_{RP}	RESET# Pulse Width		Min	500	ns
	t_{RH}	RESET# High Time Before Read (See Note)		Min	50	ns
	t_{RPD}	RESET# Low to Standby Mode		Min	20	µs
	t_{RB}	RY/BY# Recovery Time		Min	0	ns

Note
Not 100% tested.

Figure 17.2 RESET# Timings



17.3 Word/Byte Configuration (BYTE#) (Models 03, 04 Only)

Parameter		Description		Speed Options		Unit
JEDEC	Std.			70	90	
	t_{ELFL}/t_{ELFH}	CE# to BYTE# Switching Low or High	Max	5		ns
	t_{FLQZ}	BYTE# Switching Low to Output HIGH Z	Max	16		ns
	t_{FHQV}	BYTE# Switching High to Output Active	Min	70	90	ns

Figure 17.3 BYTE# Timings for Read Operations

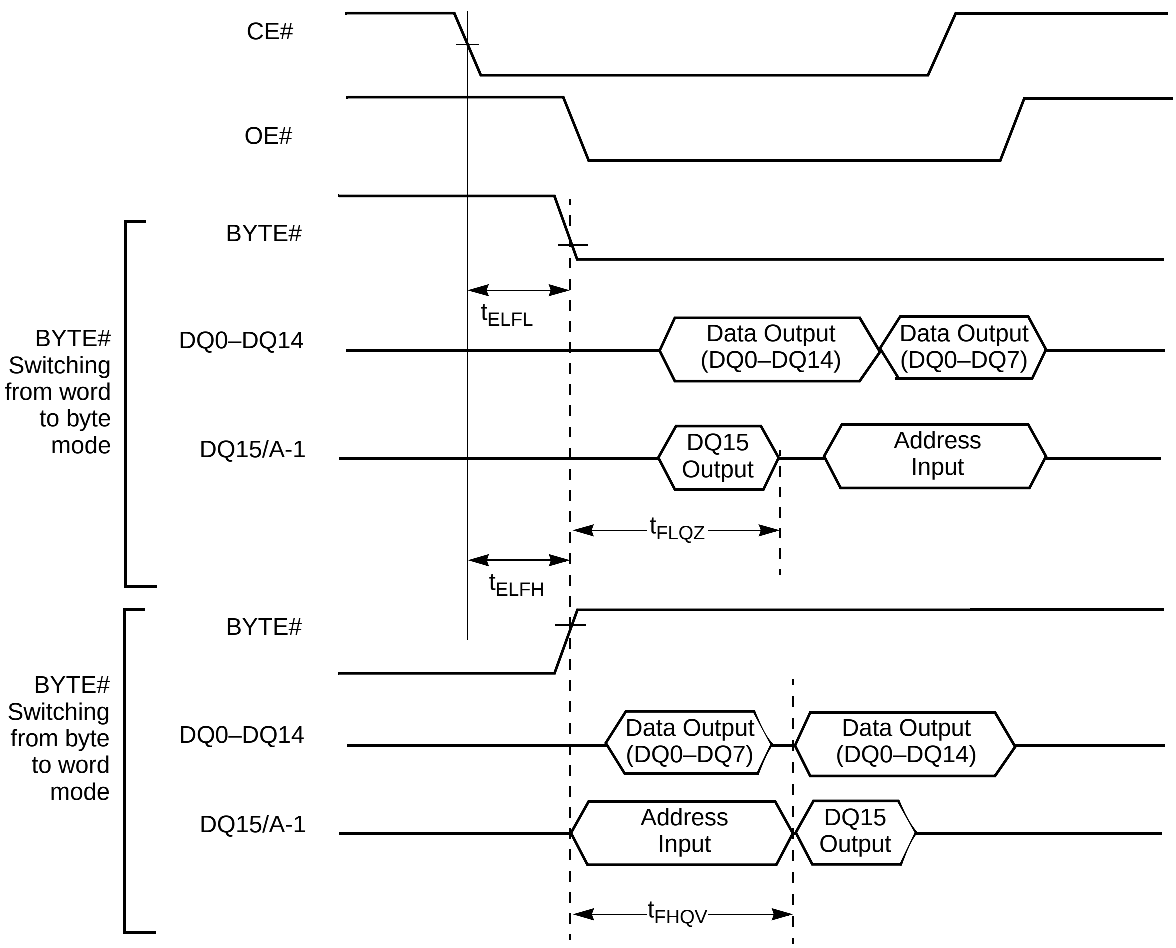
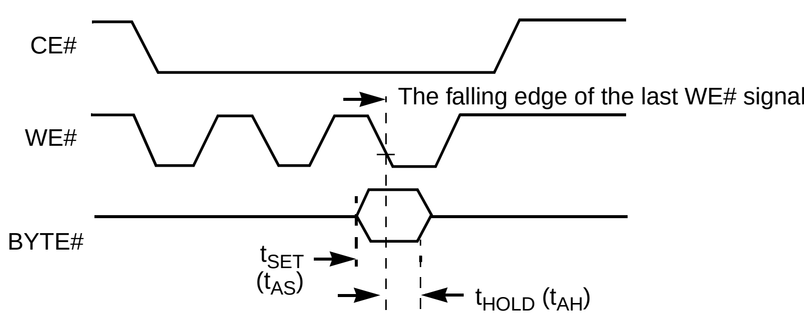


Figure 17.4 BYTE# Timings for Write Operations



Note

Refer to the Erase/Program Operations table for t_{AS} and t_{AH} specifications.

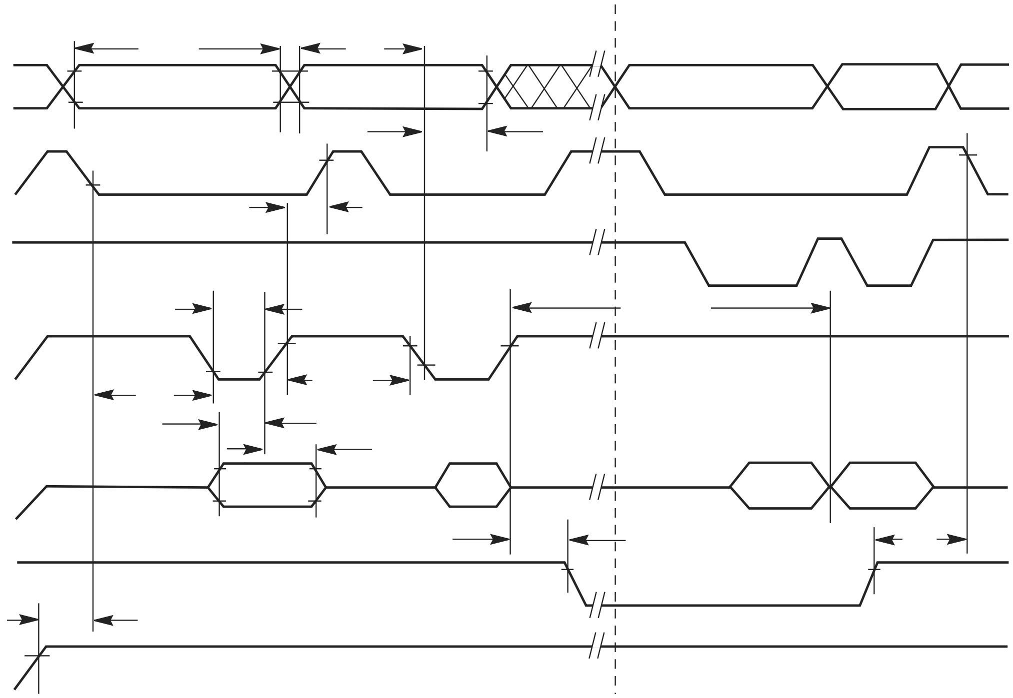
17.4 Erase/Program Operations

Table 17.1 Erase/Program Operations

Parameter		Description			Speed Options		Unit
JEDEC	Std.				70	90	
t_{AVAV}	t_{WC}	Write Cycle Time (Note 1)		Min	70	90	ns
t_{AVWL}	t_{AS}	Address Setup Time		Min	0		ns
t_{WLAX}	t_{AH}	Address Hold Time		Min	45	45	ns
t_{DVWH}	t_{DS}	Data Setup Time		Min	35	45	ns
t_{WHDX}	t_{DH}	Data Hold Time		Min	0		ns
	t_{OES}	Output Enable Setup Time		Min	0		ns
t_{GHWL}	t_{GHWL}	Read Recovery Time Before Write (OE# High to WE# Low)		Min	0		ns
t_{ELWL}	t_{CS}	CE# Setup Time		Min	0		ns
t_{WHEH}	t_{CH}	CE# Hold Time		Min	0		ns
t_{WLWH}	t_{WP}	Write Pulse Width		Min	35	35	ns
t_{WHWL}	t_{WPH}	Write Pulse Width High		Min	30		ns
	$t_{SR/W}$	Latency Between Read and Write Operations		Min	20		ns
t_{WHWH1}	t_{WHWH1}	Programming Operation (Note 2)	Byte	Typ	9		µs
			Word	Typ	11		
t_{WHWH1}	t_{WHWH1}	Accelerated Programming Operation, Word or Byte (Note 2)		Typ	7		µs
t_{WHWH2}	t_{WHWH2}	Sector Erase Operation (Note 2)		Typ	0.7		sec
	t_{VCS}	V_{CC} Setup Time (Note 1)		Min	50		µs
	t_{RB}	Recovery Time from RY/BY#		Min	0		ns
	t_{BUSY}	Program/Erase Valid to RY/BY# Delay		Max	90		ns

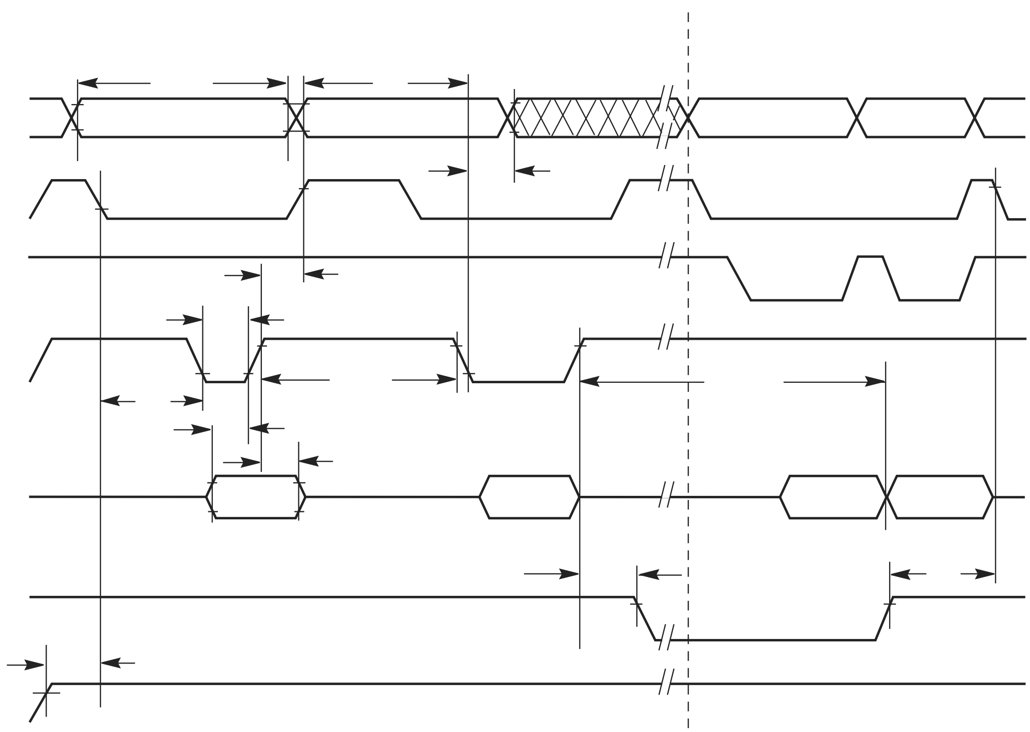
Notes
1. *Not 100% tested.*
2. *See Erase and Programming Performance on page 60 for more information.*

Figure 17.5 Program Operation Timings



Notes
1. *PA = program address, PD = program data, D_{OUT} is the true data at the program address.*
2. *Illustration shows device in word mode.*

Figure 17.6 Chip/Sector Erase Operation Timings



Notes
1. *SA = sector address (for Sector Erase), VA = Valid Address for reading status data (see Write Operation Status on page 40).*
2. *Illustration shows device in word mode.*

Figure 17.7 Back to Back Read/Write Cycle Timing

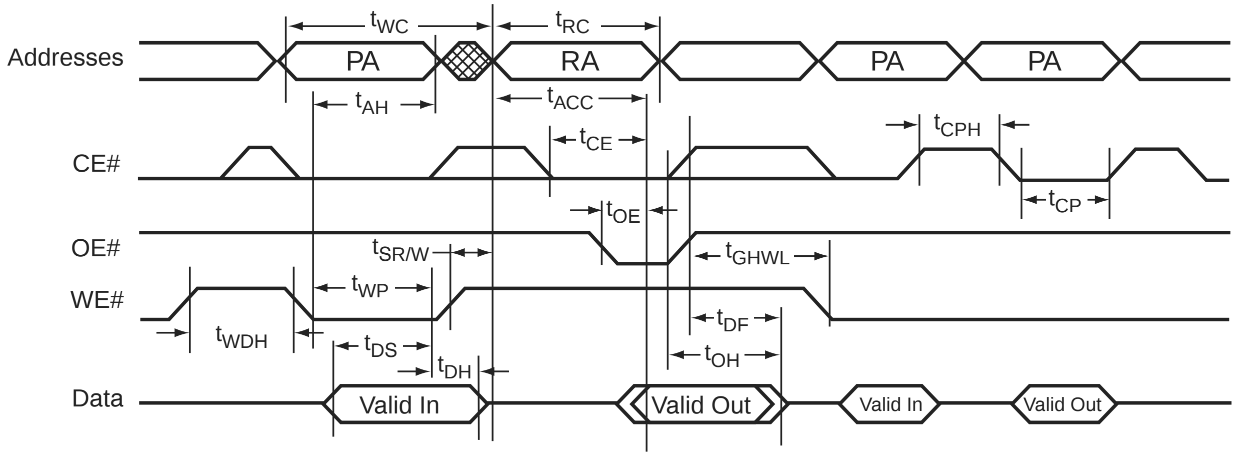
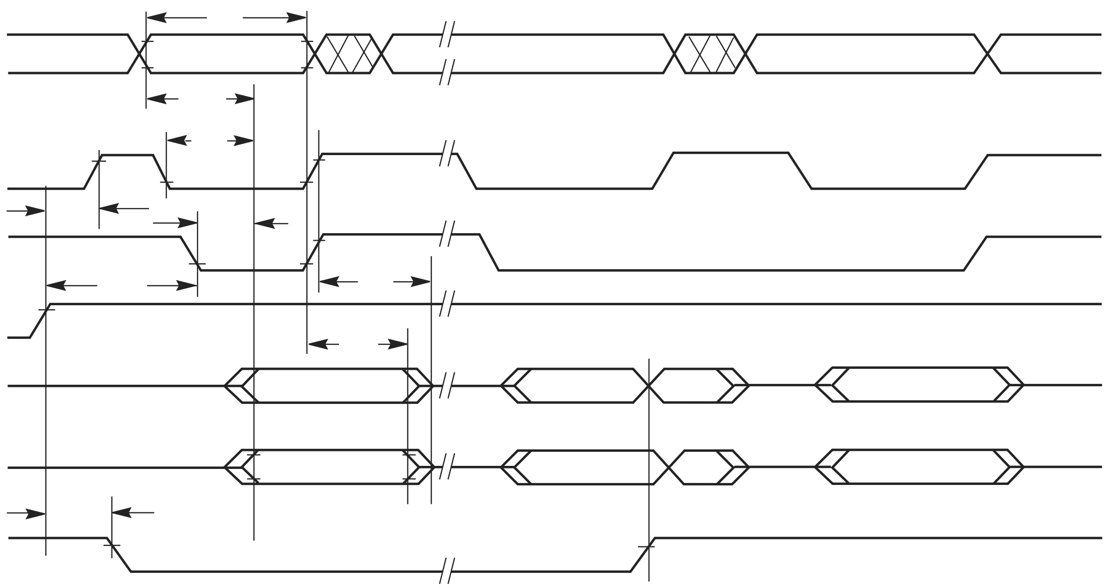


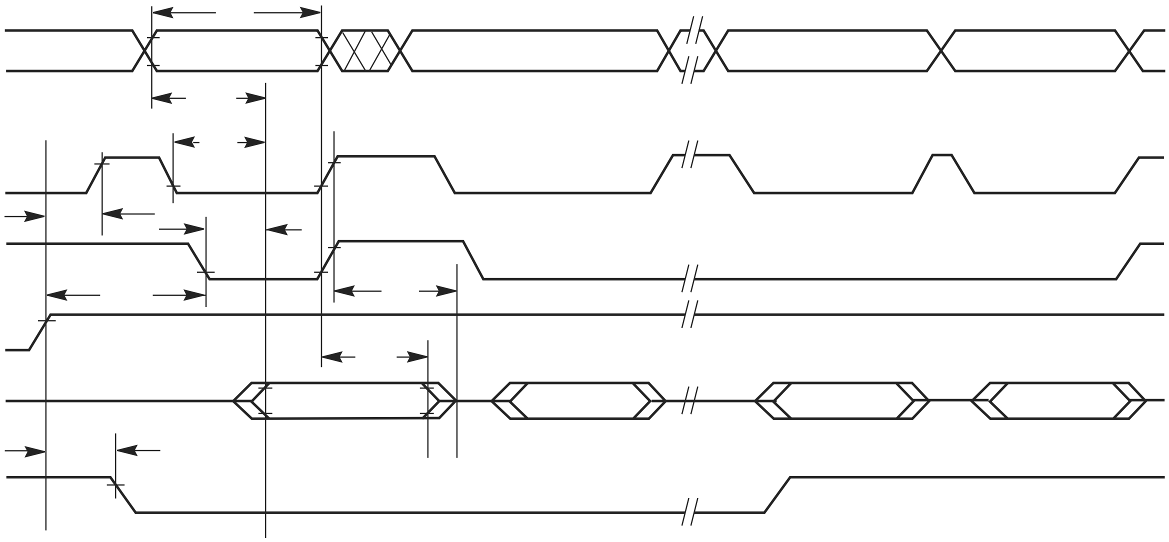
Figure 17.8 Data# Polling Timings (During Embedded Algorithms)



Note

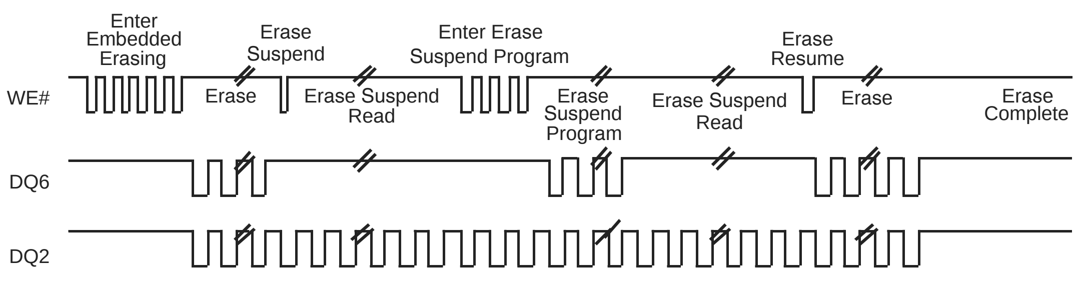
VA = Valid address. Illustration shows first status cycle after command sequence, last status read cycle, and array data read cycle.

Figure 17.9 Toggle Bit Timings (During Embedded Algorithms)



Note
VA = Valid address; not required for DQ6. Illustration shows first two status cycle after command sequence, last status read cycle, and array data read cycle.

Figure 17.10 DQ2 vs. DQ6 for Erase and Erase Suspend Operations



Note
The system may use CE# or OE# to toggle DQ2 and DQ6. DQ2 toggles only when read at an address within an erase-suspended sector.

17.5 Temporary Sector Unprotect

Table 17.2 Temporary Sector Unprotect

Parameter		Description		All Speed Options	Unit
JEDEC	Std.				
	t_{VIDR}	V_{ID} Rise and Fall Time (See Note)	Min	500	ns
	t_{RSP}	RESET# Setup Time for Temporary Sector Unprotect	Min	4	µs

Note
Not 100% tested.

Figure 17.11 Temporary Sector Unprotect Timing Diagram

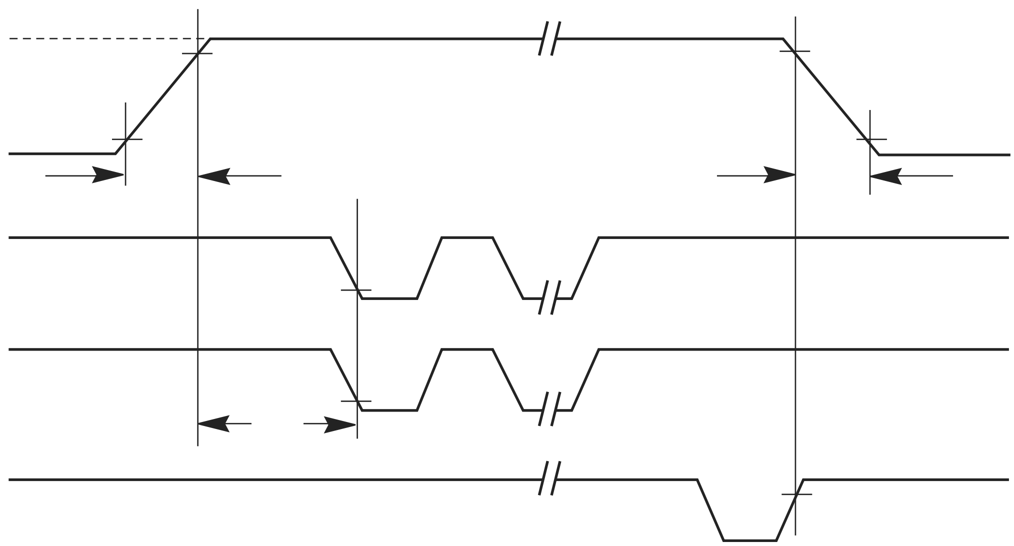


Figure 17.12 Accelerated Program Timing Diagram

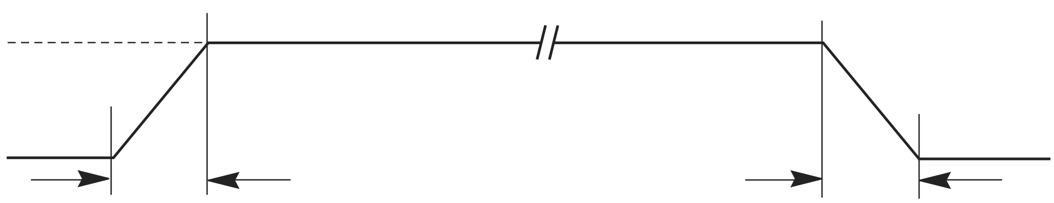
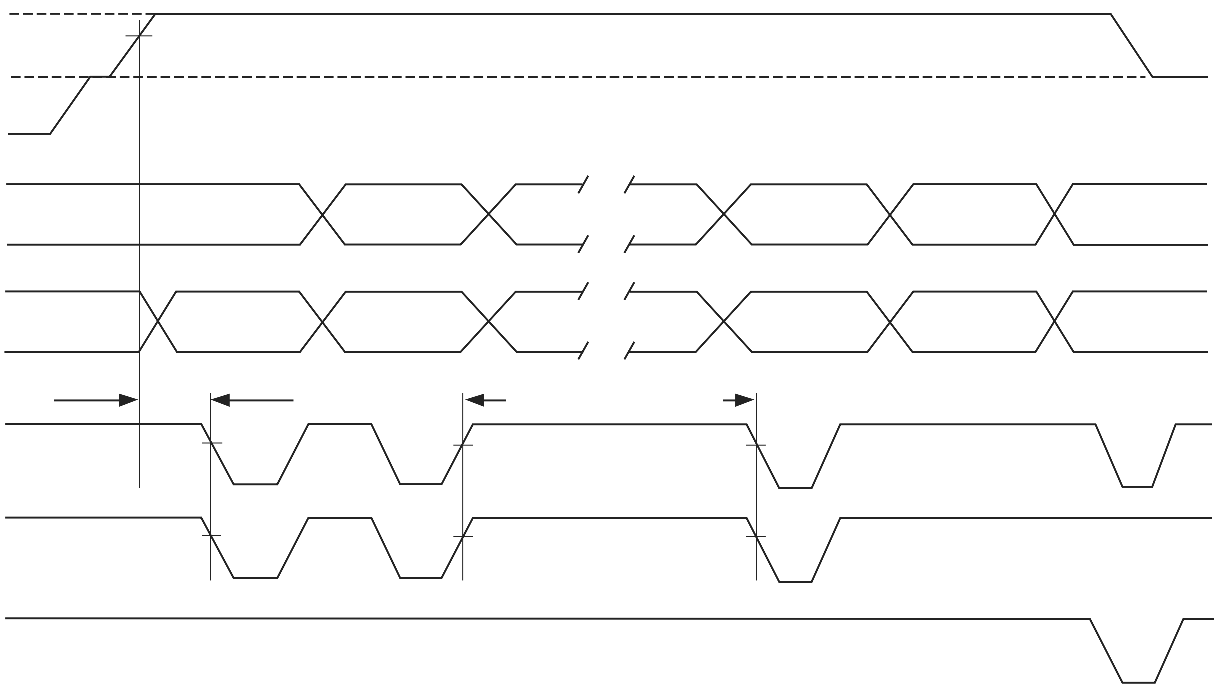


Figure 17.13 Sector Protect/Unprotect Timing Diagram



Note

For sector protect, A6 = 0, A1 = 1, A0 = 0. For sector unprotect, A6 = 1, A1 = 1, A0 = 0.

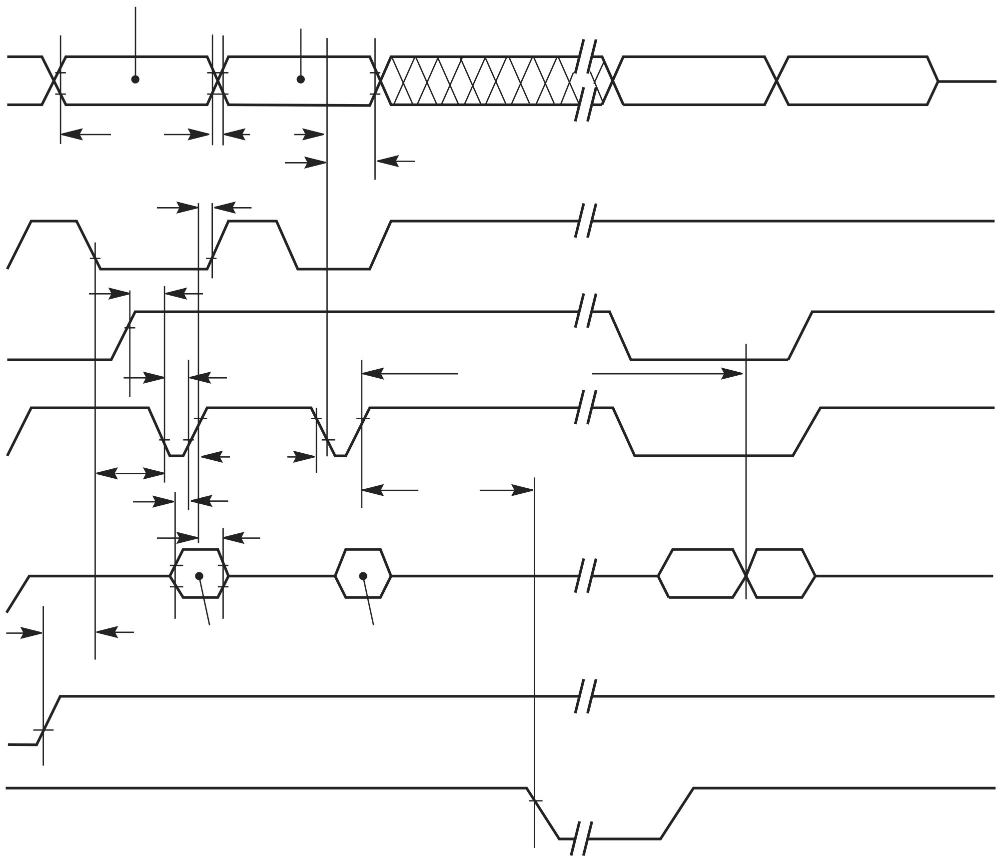
17.6 Alternate CE# Controlle d Erase/Program Operations

Table 17.3 Alternate CE# Controlled Erase/Program Operations

Parameter		Description			Speed Options		Unit
JEDEC	Std.				70	90	
t_{AVAV}	t_{WC}	Write Cycle Time (Note 1)		Min	70	90	ns
t_{AVEL}	t_{AS}	Address Setup Time		Min	0		ns
t_{ELAX}	t_{AH}	Address Hold Time		Min	45	45	ns
t_{DVEH}	t_{DS}	Data Setup Time		Min	35	45	ns
t_{EHDX}	t_{DH}	Data Hold Time		Min	0		ns
	t_{OES}	Output Enable Setup Time		Min	0		ns
t_{GHEL}	t_{GHEL}	Read Recovery Time Before Write (OE# High to WE# Low)		Min	0		ns
t_{WLEL}	t_{WS}	WE# Setup Time		Min	0		ns
t_{EHWH}	t_{WH}	WE# Hold Time		Min	0		ns
t_{ELEH}	t_{CP}	CE# Pulse Width		Min	35	35	ns
t_{EHEL}	t_{CPH}	CE# Pulse Width High		Min	30		ns
	$t_{SR/W}$	Latency Between Read and Write Operations		Min	20		ns
t_{WHWH1}	t_{WHWH1}	Programming Operation (Note 2)	Byte	Typ	9		µs
			Word	Typ	11		
t_{WHWH1}	t_{WHWH1}	Accelerated Programming Operation, Word or Byte (Note 2)		Typ	7		µs
t_{WHWH2}	t_{WHWH2}	Sector Erase Operation (Note 2)		Typ	0.7		sec

Notes
1. *Not 100% tested.*
2. *See the Erase and Programming Performance on page 60 section for more information.*

Figure 17.14 Alternate CE# Controlled Write Operation Timings



Notes

1. *PA = program address, PD = program data, DQ7# = complement of the data written to the device, D_{OUT} = data written to the device.*
2. *Figure indicates the last two bus cycles of the command sequence.*
3. *Word mode address used as an example.*

18. Erase and Programming Performance

Parameter		Typ (Note 1)	Max (Note 2)	Unit	Comments
Sector Erase Time (Note 7)		0.7	10	s	Excludes 00h programming prior to erasure (Note 4)
Chip Erase Time (Note 8)		45		s	
Byte Programming Time		9	300	µs	Excludes system level overhead (Note 5)
Word Programming Time		11	360	µs	
Accelerated Byte/Word Programming Time		7	210	µs	
Chip Programming Time (Note 3)	Byte Mode	36	108	s	
	Word Mode	24	72	s	

Notes

1. *Typical program and erase times assume the following conditions: 25°C, V_{CC} = 3.0 V, 100,000 cycles, checkerboard data pattern.*
2. *Under worst case conditions of 90°C, V_{CC} = 2.7 V, 1,000,000 cycles.*
3. *The typical chip programming time is considerably less than the maximum chip programming time listed, since most bytes program faster than the maximum program times listed.*
4. *In the pre-programming step of the Embedded Erase algorithm, all bytes are programmed to 00h before erasure.*
5. *System-level overhead is the time required to execute the two- or four-bus-cycle sequence for the program command. See Table 11.2 for further information on command definitions.*
6. *The device has a minimum erase and program cycle endurance of 100,000 cycles per sector.*
7. *At extended temperature range (>+85°C), typical erase time is 1.75 s and maximum erase time is 25 s.*
8. *At extended temperature range (>+85°C), typical erase time is 112 s.*

19. TSOP and BGA Pin Capacitance

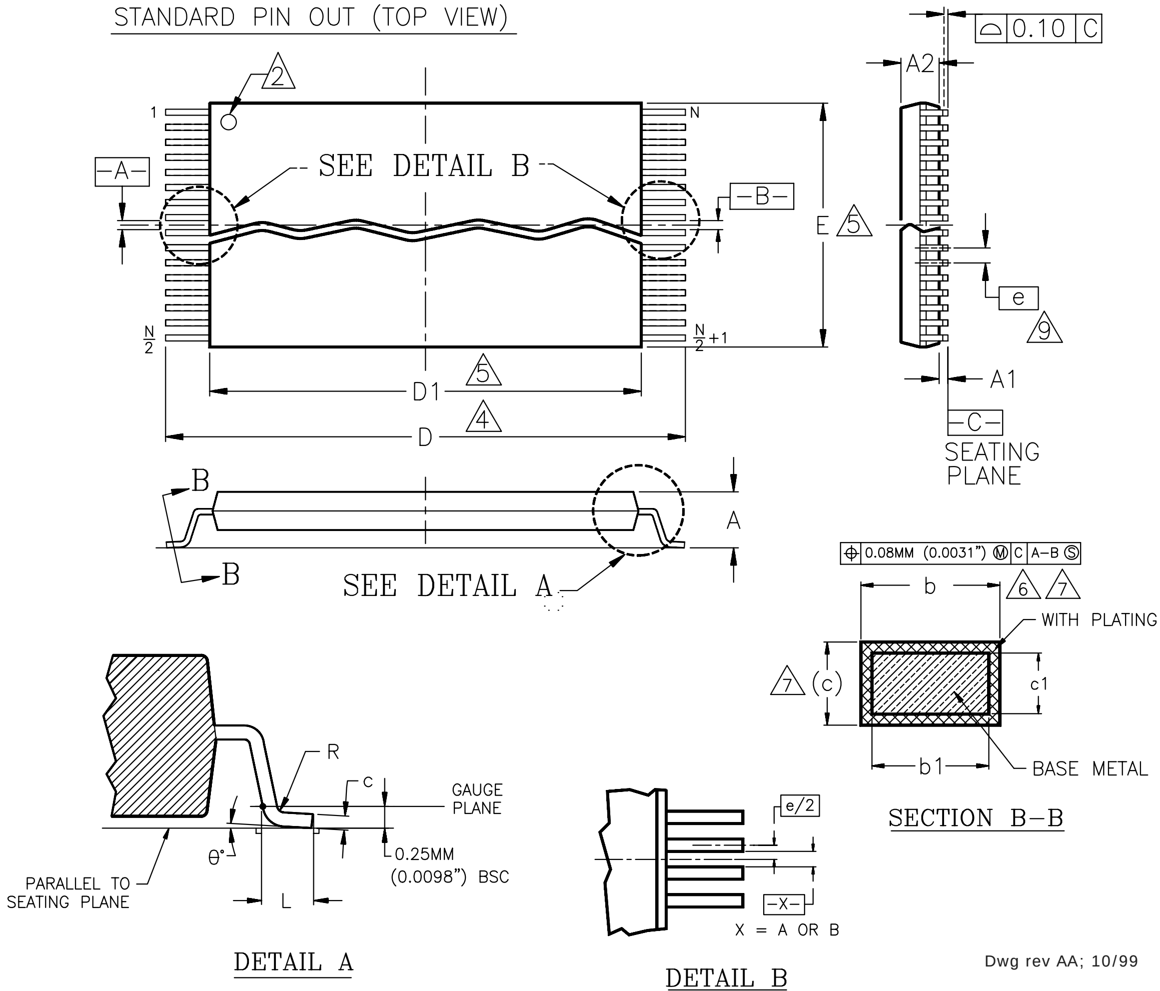
Parameter Symbol	Parameter Description	Test Setup	Package	Typ	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0	TSOP	6	7.5	pF
			BGA	4.2	5.0	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0	TSOP	8.5	12	pF
			BGA	5.4	6.5	pF
C_{IN2}	Control Pin Capacitance	V_{IN} = 0	TSOP	7.5	9	pF
			BGA	3.9	4.7	pF

Notes

1. *Sampled, not 100% tested.*
2. *Test conditions T_A = 25°C, f = 1.0 MHz.*

20. Physical Dimensions

20.1 TS040—40-Pin Standard TSOP

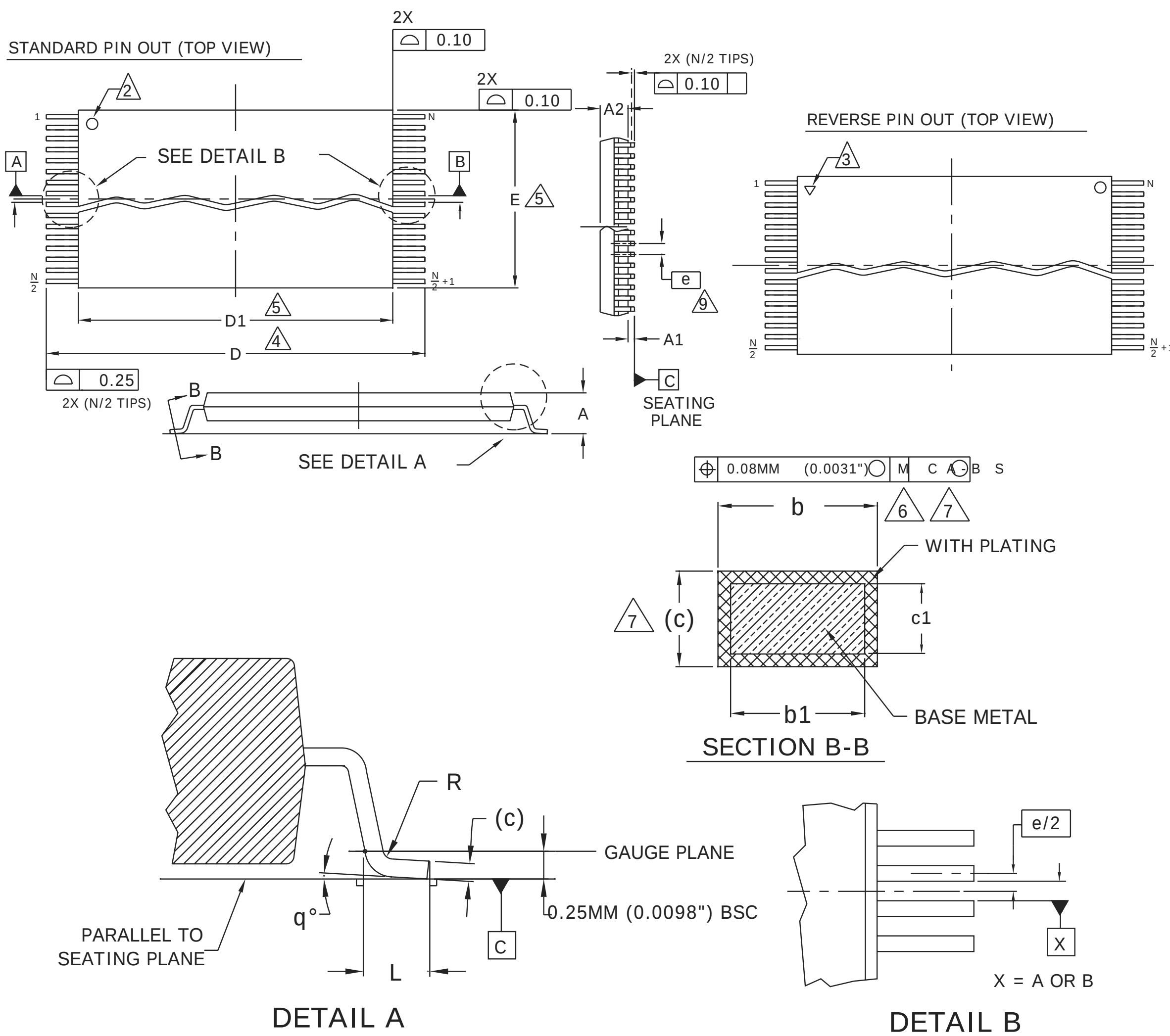


Package	TS 40		
Jedec	MO-142 (B) CD		
Symbol	MIN	NOM	MAX
A	—	—	1.20
A1	0.05	—	0.15
A2	0.95	1.00	1.05
b1	0.17	0.20	0.23
b	0.17	0.22	0.27
c1	0.10	—	0.16
c	0.10	—	0.21
D	19.80	20.00	20.20
D1	18.30	18.40	18.50
E	9.90	10.00	10.10
e	0.50 BASIC		
L	0.50	0.60	0.70
θ	0°	3°	5°
R	0.08	—	0.20
N	40		

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (mm). (DIMENSIONING AND TOLERANCING CONFORMS TO ANSI Y14.5M-1982)
2. PIN 1 IDENTIFIER FOR STANDARD PIN OUT (DIE UP).
3. PIN 1 IDENTIFIER FOR REVERSE PIN OUT (DIE DOWN): INK OR LASER MARK.
4. TO BE DETERMINED AT THE SEATING PLANE -C- . THE SEATING PLANE IS DEFINED AS THE PLANE OF CONTACT THAT IS MADE WHEN THE PACKAGE LEADS ARE ALLOWED TO REST FREELY ON A FLAT HORIZONTAL SURFACE.
5. DIMENSIONS D1 AND E DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTUSION IS 0.15mm (.0059") PER SIDE.
6. DIMENSION b DOES NOT INCLUDE DAMBAR PROTUSION. ALLOWABLE DAMBAR PROTUSION SHALL BE 0.08mm (0.0031") TOTAL IN EXCESS OF b DIMENSION AT MAX. MATERIAL CONDITION. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD TO BE 0.07mm (0.0028").
7. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm (.0039") AND 0.25mm (0.0098") FROM THE LEAD TIP.
8. LEAD COPLANARITY SHALL BE WITHIN 0.10mm (0.004") AS MEASURED FROM THE SEATING PLANE.
9. DIMENSION "e" IS MEASURED AT THE CENTERLINE OF THE LEADS.

20.2 TS 048—48-Pin Standard TSOP



Jedec	MO-142 (D) DD		
Symbol	MIN	NOM	MAX
A	—	—	1.20
A1	0.05	—	0.15
A2	0.95	1.00	1.05
b1	0.17	0.20	0.23
b	0.17	0.22	0.27
c1	0.10	—	0.16
c	0.10	—	0.21
D	19.80	20.00	20.20
D1	18.30	18.40	18.50
E	11.90	12.00	12.10
e	0.50 BASIC		
L	0.50	0.60	0.70
θ	0°	—	8
R	0.08	—	0.20
N	48		

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (mm). (DIMENSIONING AND TOLERANCING CONFORMS TO ANSI Y14.5M-1982)
2. PIN 1 IDENTIFIER FOR REVERSE PIN OUT (DIE UP).
3. PIN 1 IDENTIFIER FOR REVERSE PIN OUT (DIE DOWN), INK OR LASER MARK.
4. TO BE DETERMINED AT THE SEATING PLANE -C- . THE SEATING PLANE IS DEFINED AS THE PLANE OF CONTACT THAT IS MADE WHEN THE PACKAGE LEADS ARE ALLOWED TO REST FREELY ON A FLAT HORIZONTAL SURFACE.
5. DIMENSIONS D1 AND E DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTUSION IS 0.15mm (.0059") PER SIDE.
6. DIMENSION b DOES NOT INCLUDE DAMBAR PROTUSION. ALLOWABLE DAMBAR PROTUSION SHALL BE 0.08 (0.0031") TOTAL IN EXCESS OF b DIMENSION AT MAX. MATERIAL CONDITION. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD TO BE 0.07 (0.0028").
7. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10MM (.0039") AND 0.25MM (0.0098") FROM THE LEAD TIP.
8. LEAD COPLANARITY SHALL BE WITHIN 0.10mm (0.004") AS MEASURED FROM THE SEATING PLANE.
9. DIMENSION "e" IS MEASURED AT THE CENTERLINE OF THE LEADS.

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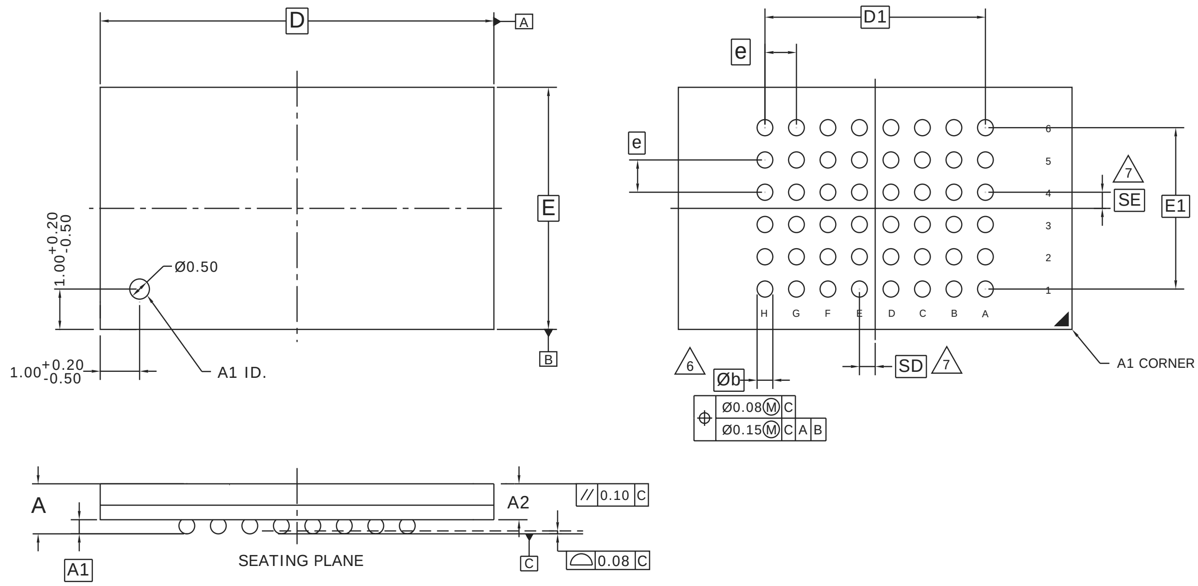
** For reference only. BSC is an ANSI standard for Basic Space Centering.*

20.3 VBN048—48-Ball Fine-Pitch Ball Grid Array (FBGA) 10.0 x 6.0 mm



PACKAGE	VBN 048			
JEDEC	N/A			
	10.00 mm x 6.00 mm NOM PACKAGE			
SYMBOL	MIN	NOM	MAX	NOTE
A	---	---	1.00	OVERALL THICKNESS
A1	0.17	---	---	BALL HEIGHT
A2	0.62	---	0.73	BODY THICKNESS
D	10.00 BSC.			BODY SIZE
E	6.00 BSC.			BODY SIZE
D1	5.60 BSC.			BALL FOOTPRINT
E1	4.00 BSC.			BALL FOOTPRINT
MD	8			ROW MATRIX SIZE D DIRECTION
ME	6			ROW MATRIX SIZE E DIRECTION
N	48			TOTAL BALL COUNT
fb	0.35	---	0.45	BALL DIAMETER
e	0.80 BSC.			BALL PITCH
SD / SE	0.40 BSC.			SOLDER BALL PLACEMENT
	NONE			DEPOPULATED SOLDER BALLS

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. BALL POSITION DESIGNATION PER JESD 95-1, SPP-010 (EXCEPT AS NOTED).
4. e REPRESENTS THE SOLDER BALL GRID PITCH.
5. SYMBOL "MD" IS THE BALL ROW MATRIX SIZE IN THE "D" DIRECTION.

   SYMBOL "ME" IS THE BALL COLUMN MATRIX SIZE IN THE "E" DIRECTION.

   N IS THE TOTAL NUMBER OF SOLDER BALLS.
6. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
7. SD AND SE ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.

   WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW PARALLEL TO THE D OR E DIMENSION, RESPECTIVELY, SD OR SE = 0.000.

   WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, SD OR SE = e/2
8. NOT USED.
9. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED BALLS.
10. A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK, METALLIZED MARK INDENTATION OR OTHER MEANS.

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21. Revision History

Section	Description
Revision A0 (January 31, 2005)	
	Initial release.
Revision A1 (March 16, 2005)	
Distinctive Characteristics	Revised Secured Silicon Sector with 128-word information.
Common Flash Memory Interface — (CFI)	Modified Primary Vendor-Specific Extended Query table information for 45h address..
Revision A2 (April 19, 2005)	
Valid Combinations Table	Clarified available packing types for TSOP and FBGA package. Modified Note 1.
Device Bus Operations	Added Secured Silicon Sector Addresses—Model 00 table Modified Top Boot Secured Silicon Sector Addresses—Model 03 and Bottom Boot Secured Silicon Sector Addresses—Model 04 tables
S29AL032D Command Definitions Model 00 table	Added Secured Silicon Sector Factory Protect information.
Accelerated Program Operation	Added section.
Secured Silicon Sector	Added section.
AC Characteristics	Added ACC programming timing diagram.
Revision A3 (June 13, 2005)	
Autoselect Mode	Updated Table 8 to include models 00, 03, and 04.
Common Flash Memory Interface	Updated table headings in table 12, 13, 14, and 15.
Absolute Maximum Rating	Updated figure 8.
DC Characteristics	Updated CMOS Compatible table.
AC Characteristics	Updated Erase/Program Operations table. Added new figure: Back-to-Back Read/Write Cycle Timing. Updated Alternate CE# Controlled Erase/Program Operations table.
Revision A4 (July 29, 2005)	
DS Status	Change of DS status to “Preliminary” from “Advance Information”.
Output Disable Mode	Updated Model 00 Secured Silicon Sector Analysis table.
Autoselect Mode	Updated S29AL032D Autoselect Codes (High Voltage Method) table.
Revision A5 (September 21, 2005)	
DS Status	Change of DS status to “Preliminary” from “Advance Information”.
Sector Protection/Unprotection	Corrected “In-System Sector Protect/Unprotect Algorithms” figure.
Revision A6 (May 22, 2006)	
AC Characteristics	Added $t_{SR/W}$ parameter to read and erase/program operations tables. Added back-to-back read/write cycle timing diagram. Changed maximum value for t_{DF} and t_{FLQZ}.
Revision A7 (June 19, 2006)	
Ordering Information	Added extended temperature range options to valid combinations.
Common Flash Memory Interface (CFI)	*Primary Vendor-Specific Extended Query table:* Change description for data at address 4Fh (address 9Eh on Models 03, 04).
DC Characteristics	Changed Note 4.
Read Operations Timings figure	Connected end of t_{RC} period to start of t_{OH} period.
Erase and Programming Performance	Added Notes 7 and 8 to table.
Revision A8 (November 2, 2006)	
Valid Combinations	Updated table.
Revision A9 (January 19, 2007)	
Autoselect Code (High Voltage Method) table; Command Definitions, x8 Mode—Models 03, 04 table	Corrected data for Secured Silicon Sector Sector Indicator Bit.

Colophon

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