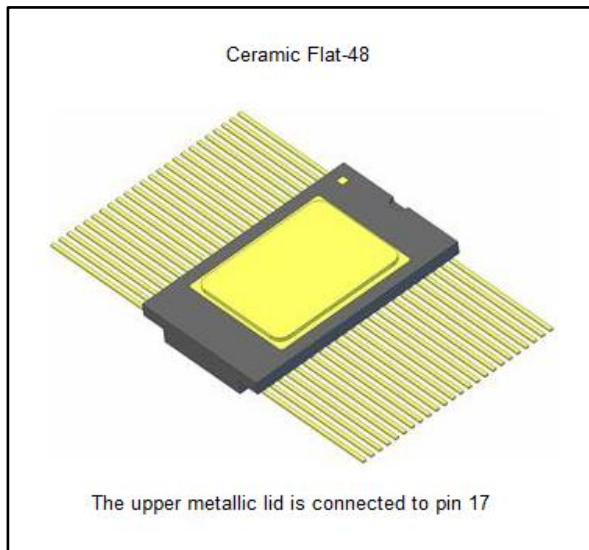


## Rad-hard LVDS serializer

Datasheet - preliminary data



### Description

The RHFLVDS217 serializer converts 21 bits of CMOS/TTL data into three LVDS (low voltage differential signaling) data streams. A phase-locked transmitter clock is transmitted in parallel with the data streams over a fourth LVDS link. With every cycle of the transmitter clock, 21 bits of input data are sampled and transmitted.

At a transmitter clock frequency of 75 MHz, 21 bits of TTL data are transmitted at a rate of 525 Mbps per LVDS data channel. Using a 75 MHz clock, the data throughput is 1.575 Gbit/s (197 Mbytes/s).

The RHFLVDS217 serializer allows the use of wide, high speed TTL interfaces while reducing overall EMI and cable size.

All pins have cold spare buffers. These buffers are high impedance when  $V_{CC}$  is tied to 0 V.

### Features

- 15 to 75 MHz shift clock support
- Fail-safe function
- 8 kV HBM on LVDS pins
- Power-down mode < 216  $\mu$ W (max)
- Cold sparing all pins
- Narrow bus reduces cable size and cost
- Up to 1.575 Gbps throughput
- Up to 197 Mbytes/s bandwidth
- 325 mV (typ) LVDS swing
- PLL requires no external components
- Rising edge strobe
- Operational environment: total dose irradiation testing to MIL-STD-883 method 1019
  - Total dose: 300 krad (Si)
  - Latchup immune (LET > 120 MeV-cm<sup>2</sup>/mg)
- Compatible with ANSI/TIA/EIA-644 standard

Table 1: Device summary

Parameter	RHFLVDS217K1
SMD <sup>(1)</sup>	—
Quality level	Engineering model
Package	Flat-48
Mass	1.22 g
EPPL <sup>(2)</sup>	—
Temp. range	-55 °C to 125 °C

#### Notes:

<sup>(1)</sup>SMD = standard microcircuit drawing

<sup>(2)</sup>EPPL = ESA preferred part list

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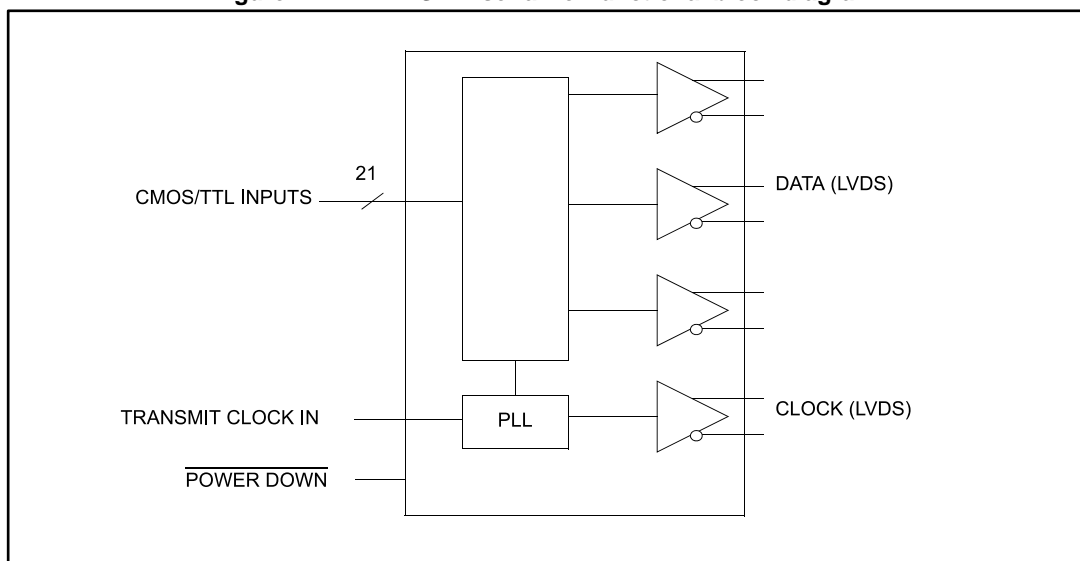
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# 1 Functional description

Figure 1: RHFLVDS217 serializer functional block diagram

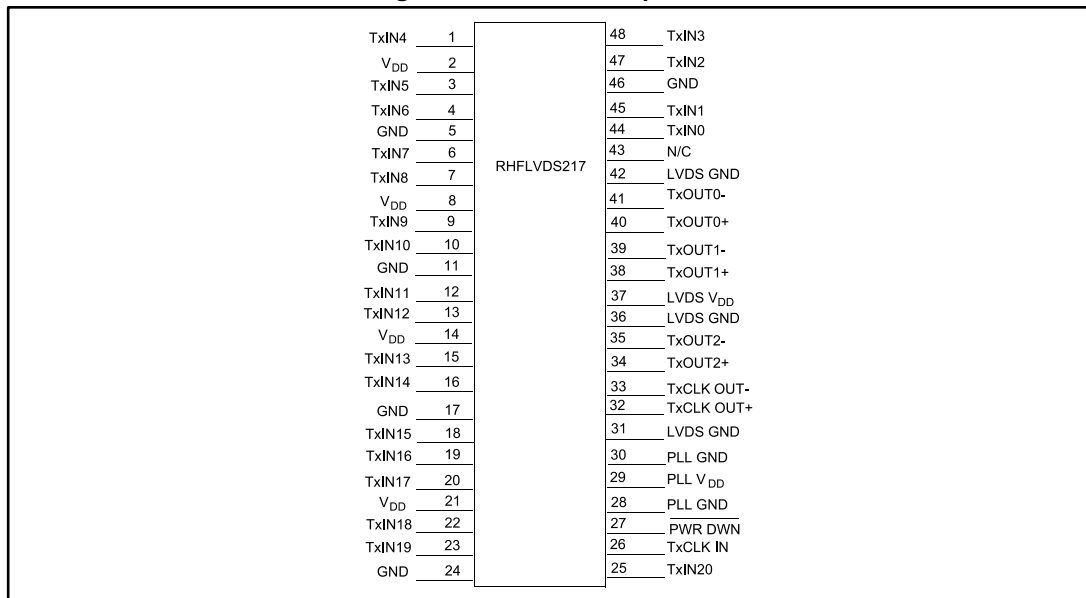


## 2 Pin configuration

Table 2: Pin description

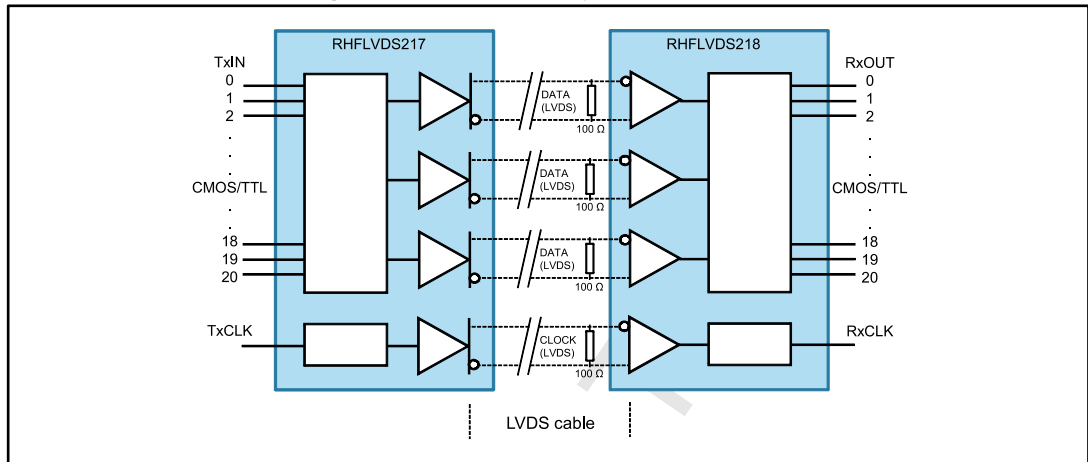
Pin name	I/O	No.	Description
TxIN	I	21	TTL level input
TxOUT+	O	3	Positive LVDS differential data output
TxOUT-	O	3	Negative LVDS differential data output
TxCLK IN	I	1	TTL level clock input. The rising edge acts as data strobe. Pin name TxCLK IN
TxCLK OUT+	O	1	Positive LVDS differential clock output
TxCLK OUT-	O	1	Negative LVDS differential clock output
$\overline{\text{PWR DWN}}$	I	1	TTL level input. Assertion (low input) TRISTATEs the clock and data outputs, ensuring low current at power down.
V <sub>CC</sub>	I	4	Power supply pins for TTL inputs and logic
GND	I	5	Ground pins for TTL inputs and logic
PLL V <sub>CC</sub>	I	1	Power supply pins for PLL
PLL GND	I	2	Ground pins for PPL
LVDS V <sub>CC</sub>	I	1	Power supply pin for LVDS output
LVDS GND	I	3	Ground pins for LVDS outputs

Figure 2: RHFLVDS217 pinout



### 3 Typical application

Figure 3: RHFLVDS217 typical application



## 4 Absolute maximum ratings and operating conditions

Stresses outside the listed absolute maximum ratings may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond the limits indicated in the operational sections of this specification are not recommended. Exposure to absolute maximum rating conditions for extended periods may affect device reliability and performance.

**Table 3: Absolute maximum ratings (references to GND)**

Symbol	Parameter		Value	Unit
V <sub>CC</sub>	Supply voltage <sup>(1)</sup>		4.8	V
V <sub>i</sub>	TTL inputs (operating or cold-spares)		-0.3 to 4.8	
T <sub>stg</sub>	Storage temperature range		-65 to 150	°C
T <sub>j</sub>	Maximum junction temperature		150	
R <sub>thjc</sub>	Thermal resistance junction to case <sup>(2)</sup>		22	°C/W
ESD	HBM: human body model	All pins except LVDS outputs	2	kV
		LVDS outputs vs. GND	8	
	CDM: charge device model		500	V

**Notes:**

<sup>(1)</sup>All voltages, except the differential I/O bus voltage, are with respect to the network ground terminal.

<sup>(2)</sup>Short-circuits can cause excessive heating. Destructive dissipation can result from short-circuits on the amplifiers.

**Table 4: Recommended operating conditions (referenced to GND)**

Symbol	Parameter	Min.	Typ.	Max.	Unit
V <sub>CC</sub>	Supply voltage	3	3.3	3.6	V
V <sub>IN</sub>	Driver DC input voltage (TTL inputs)	0		V <sub>CC</sub>	
T <sub>A</sub>	Ambient temperature range	-55		125	°C

## 5 Electrical characteristics

In [Table 5: "DC electrical characteristics"](#),  $V_{CC} = 3\text{ V to }3.6\text{ V}$ ,  $-55\text{ °C} < T_A < 125\text{ °C}$ , unless otherwise specified,  $T_A$  is per the temperature noted. Current into device pins is defined as positive. Current out of device pins is defined as negative. All voltages are referenced to ground.

**Table 5: DC electrical characteristics**

Symbol	Parameter	Condition	Min.	Max.	Unit
<b>CMOS/TTL DC specifications</b>					
$V_{IH}$	High-level input voltage		2.0	$V_{CC}$	V
$V_{IL}$	Low-level input voltage		GND	0.8	
$I_{IH}$	High-level input current	$V_{IN} = 3.6\text{ V}$ , $V_{CC} = 3.6\text{ V}$	-10	10	$\mu\text{A}$
$I_{IL}$	Low-level input current	$V_{IN} = 0\text{ V}$ , $V_{CC} = 3.6\text{ V}$	-10	10	
$V_{CL}$	Input clamp voltage	$I_{CL} = -18\text{ mA}$		-1.5	V
$I_{CS}$	Cold spare leakage current	$V_{IN} = 3.6\text{ V}$ , $V_{CC} = 0\text{ V}$	-20	20	$\mu\text{A}$
<b>LVDS output DC specifications (OUT+, OUT-)</b>					
$V_{OD}^{(1)}$	Differential output voltage	$R_L = 100\text{ ohm}$ (see <a href="#">Figure 14</a> )	250	400	mV
$DV_{OD}^{(1)}$	Change in $V_{OD}$ between complimentary output states	$R_L = 100\text{ ohm}$ (see <a href="#">Figure 14</a> )		35	
$V_{OS}^{(1)}$	Offset voltage	$R_L = 100\text{ ohm}$ , $V_{OS} = (V_{OH} + V_{OL})/2$	1.125	1.450	V
$DV_{OS}^{(2)}$	Change in $V_{OS}$ between complimentary output states	$R_L = 100\text{ohm}$		35	mV
$I_{OZ}$	Output three-state current	PWR DWN = 0 V $V_{OUT} = 0\text{ V or }V_{CC}$	-10	10	$\mu\text{A}$
$I_{OS}^{(1)(3)}$	Output short circuit current	$V_{OUT+}$ or $V_{OUT-} = 0\text{ V}$	3.5	9	mA
$I_{CSOUT}$	Cold spare leakage current	$V_{IN} = 3.6\text{ V}$ , $V_{CC} = 0\text{ V}$	-20	20	$\mu\text{A}$
<b>Supply current</b>					
$I_{CCL}^{(4)}$	Transmitter supply current with loads	$R_L = 100\text{ ohm}$ all channels (see <a href="#">Figure 5</a> ), $C_L = 5\text{ pF}$ , $f = 50\text{ MHz}$		65	mA
$I_{CCZ}$	Power down current	$D_{IN} = V_{SS}$ / PWR DWN = 0 V, $f = 0\text{ Hz}$		200	$\mu\text{A}$

**Notes:**

<sup>(1)</sup>Output short circuit current ( $I_{OS}$ ) is specified as magnitude only, minus sign indicates direction only. Only one output should be shorted at a time, for a maximum duration of one second.

<sup>(2)</sup>Clock outputs guaranteed by design.

<sup>(3)</sup>Guaranteed by characterization.

<sup>(4)</sup>Devices are tested at 3.6 V only.

In *Table 6: "AC switching characteristics"*,  $V_{CC} = 3\text{ V to }3.6\text{ V}$ ,  $-55\text{ }^{\circ}\text{C} < T_A < 125\text{ }^{\circ}\text{C}$ , unless otherwise specified,  $T_A$  is per the temperature noted. For devices procured with a total ionizing dose tolerance guarantee, the post-irradiation performance is guaranteed at  $25\text{ }^{\circ}\text{C}$  per MIL-STD-883 Method 1019, condition A up to the maximum TID level procured. The recommend transition time for TXCLK In is 1.0 to 6.0 ns (see *Figure 6*)

Table 6: AC switching characteristics

Symbol	Parameter	Min.	Max.	Unit
LLHT <sup>(1)</sup>	LVDS low-to-high transition time (see <i>Figure 5</i> )		1.5	ns
LHLT <sup>(1)</sup>	LVDS high-to-low transition time (see <i>Figure 5</i> )		1.5	
TPPos0 <sup>(1)</sup>	Transmitter output pulse position for bit 0 (see <i>Figure 13</i> )	-0.18	0.270	
TPPos1 <sup>(1)</sup>	Transmitter output pulse position for bit 1 (see <i>Figure 13</i> ), f = 75 MHz	1.72	2.17	
TPPos2 <sup>(1)</sup>	Transmitter output pulse position for bit 2 (see <i>Figure 13</i> ), f = 75 MHz	3.63	4.08	
TPPos3 <sup>(1)</sup>	Transmitter output pulse position for bit 3 (see <i>Figure 13</i> ), f = 75 MHz	5.53	5.98	
TPPos4 <sup>(1)</sup>	Transmitter output pulse position for bit 4 (see <i>Figure 13</i> ), f = 75 MHz	7.44	7.89	
TPPos5 <sup>(1)</sup>	Transmitter output pulse position for bit 5 (see <i>Figure 13</i> ), f = 75 MHz	9.34	9.79	
TPPos6 <sup>(1)</sup>	Transmitter output pulse position for bit 6 (see <i>Figure 13</i> ), f = 75 MHz	11.25	11.70	
TCCS <sup>(1)</sup>	Channel to channel skew (see <i>Figure 7</i> ), f = 75 MHz		0.45	
TCIP <sup>(1)</sup>	TxCLK IN period (see <i>Figure 8</i> )	13.3	66.7	
TCIH <sup>(2)</sup>	TxCLK IN high time (see <i>Figure 8</i> )	0.35 T <sub>cip</sub>	0.65 T <sub>cip</sub>	
TCIL <sup>(2)</sup>	TxCLK IN low time (see <i>Figure 8</i> )	0.35 T <sub>cip</sub>	0.65 T <sub>cip</sub>	
TSTC <sup>(1)</sup>	TxIN setup to TxCLK IN (see <i>Figure 8</i> ), 15 MHz	1.0		
	TxIN setup to TxCLK IN (see <i>Figure 8</i> ), 75 MHz	0.5		
THTC <sup>(1)</sup>	TxIN hold to TxCLK IN (see <i>Figure 8</i> ), 15MHz	0.7		
	TxIN hold to TxCLK IN (see <i>Figure 8</i> ), 75 MHz	0.5		
TCCD	TxCLK IN to TxCLK OUT delay (see <i>Figure 9</i> )	0.5	3	
TPLLS	Transmitter phase lock loop set (see <i>Figure 10</i> )		10	ms
TPDD	Transmitter power down delay (see <i>Figure 12</i> )		100	μs

**Notes:**

<sup>(1)</sup>Guaranteed by characterization.

<sup>(2)</sup>Guaranteed by design

**Cold sparing**

The RHFLVDS217 features a cold spare input and output buffer. In high reliability applications, cold sparing enables a redundant device to be tied to the data bus with its power supply at 0 V ( $V_{CC} = GND$ ) without affecting the bus signals or injecting current from the I/Os to the power supplies. Cold sparing also allows redundant devices to be kept powered off so that they can be switched on only when required. This has no impact on the application. Cold sparing is achieved by implementing a high impedance between the I/Os and VCC. ESD protection is ensured through a non-conventional dedicated structure.

**Fail-safe**

In many applications, inputs need a fail-safe function to avoid an uncertain output state when the inputs are not connected properly. In case of TTL floating inputs, the LVDS outputs remain in a stable logic-high state.

## 6 Radiations

### Total dose (MIL-STD-883 TM 1019)

The products guaranteed in radiation within the RHA QML-V system fully comply with the MIL-STD-883 TM 1019 specification.

The RHFLVDS217 is RHA QML-V, tested and characterized in full compliance with the MIL-STD-883 specification, between 50 and 300 rad/s only (full CMOS technology).

All parameters provided in [Table 5: "DC electrical characteristics"](#) apply to both pre- and post-irradiation, as follows:

- All test are performed in accordance with MIL-PRF-38535 and test method 1019 of MIL-STD-883 for total ionizing dose (TID).
- The initial characterization is performed in qualification only on both biased and unbiased parts.
- Each wafer lot is tested at high dose rate only, in the worst bias case condition, based on the results obtained during the initial qualification.

### Heavy ions

The behavior of the product when submitted to heavy ions is not tested in production. Heavy-ion trials are performed on qualification lots only.

**Table 7: Radiation**

Type	Characteristics	Value	Unit
TID	High-dose rate (50 - 300 rad/sec) up to:	300	krad
Heavy ions	SEL immune up to: (with a particle angle of 60 ° at 125 °C)	120	MeV.cm <sup>2</sup> /mg
	SEL immune up to: (with a particle angle of 0 ° at 125 °C)	60	

# 7 Test circuit and AC timing diagrams

Figure 4: Test pattern

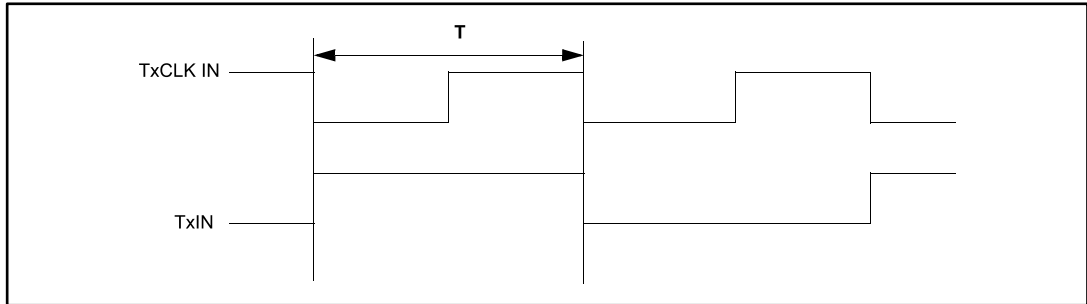


Figure 5: RHFLVDS217 output load and transition times

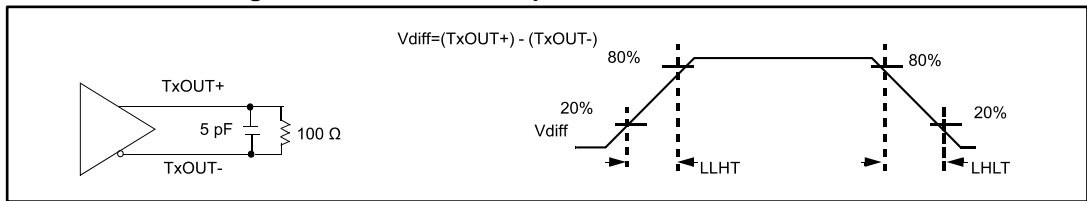


Figure 6: RHFLVDS217 input clock transition time

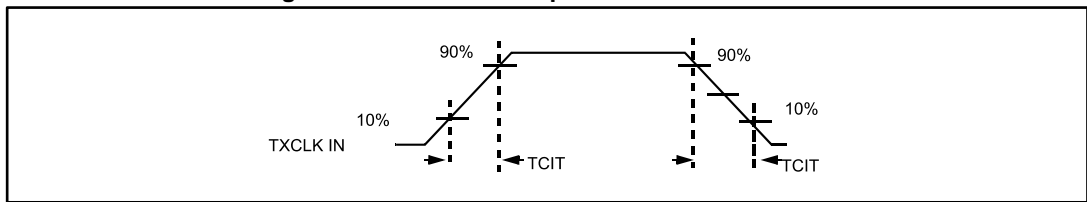
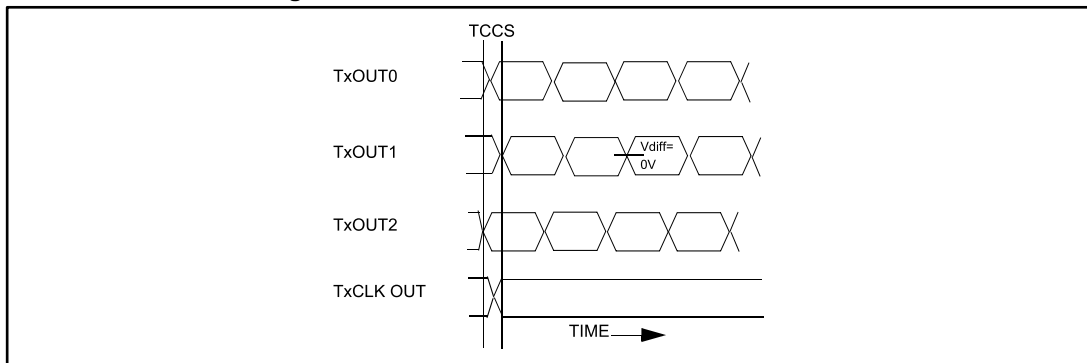


Figure 7: RHFLVDS217 channel-to-channel skew



1. Measurements at  $V_{DIFF} = 0\text{ V}$
2. TCCS measured between earliest and latest LVDS edges
3. TxCLK differential low-high edge

Figure 8: RHFLVDS217 setup/hold and high/low times

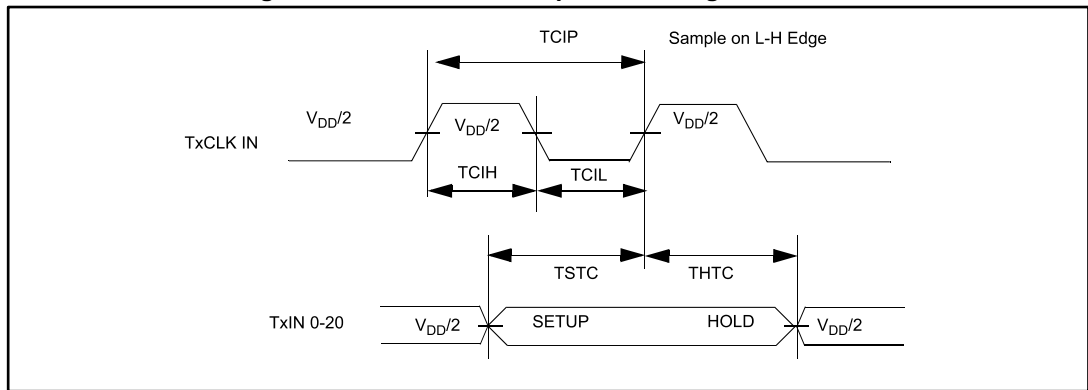


Figure 9: RHFLVDS217 clock-to-clock out delay

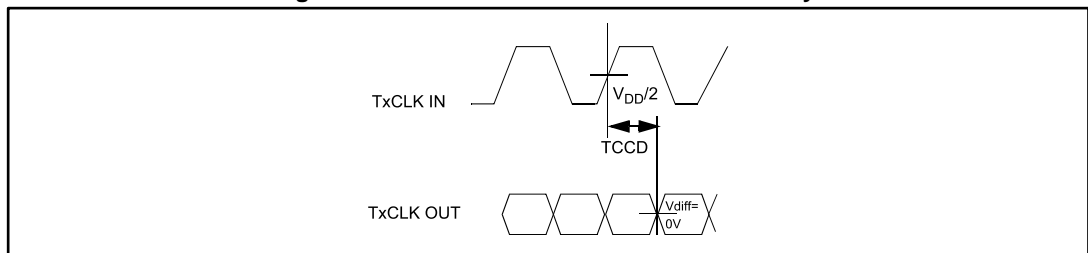


Figure 10: RHFLVDS217 phase-locked-loop set time

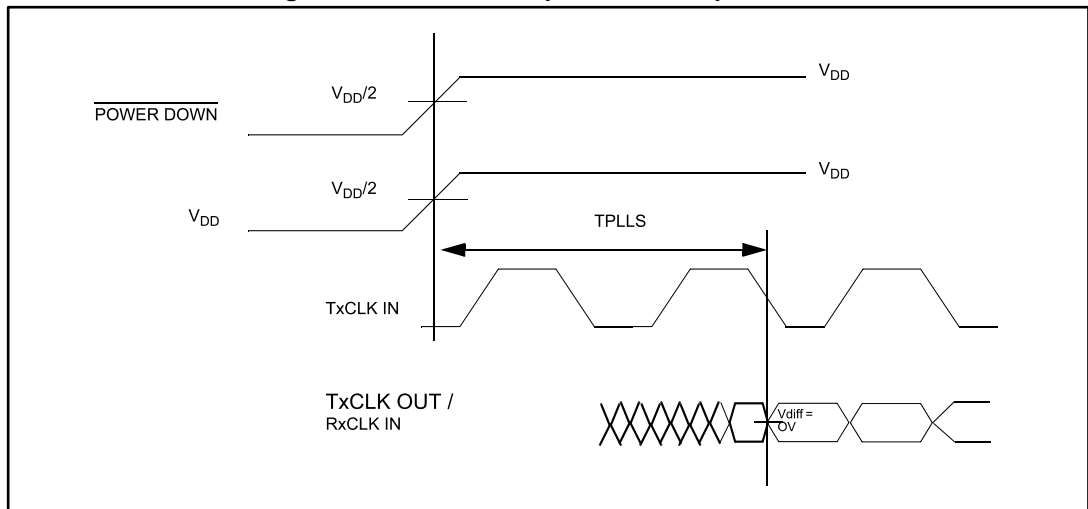


Figure 11: RHFLVDS217 parallel TTL data inputs mapped to LVDS outputs

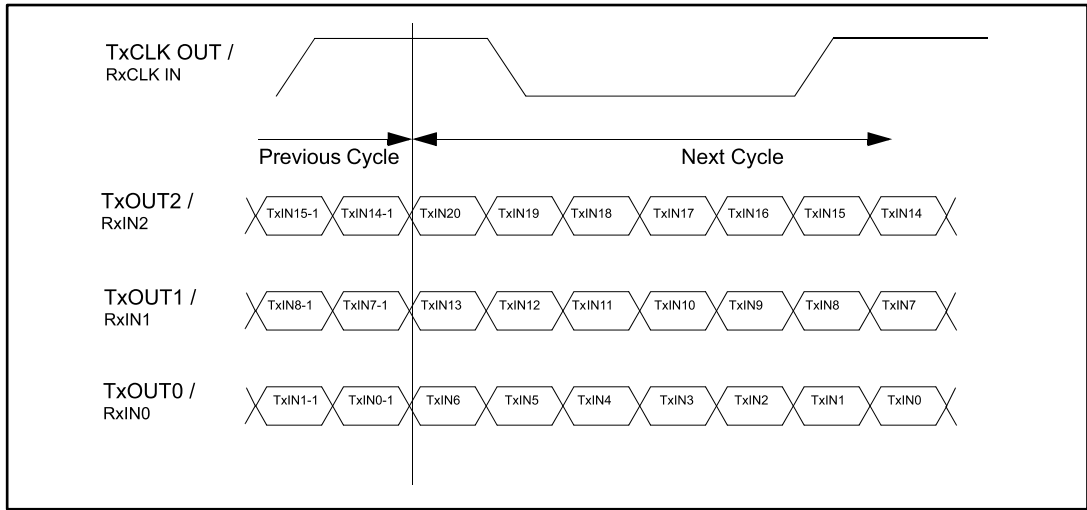


Figure 12: Transmitter powerdown delay

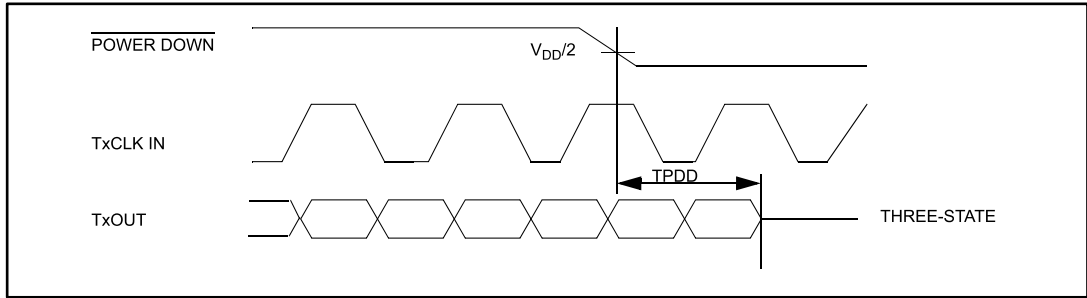


Figure 13: RHFLVDS output pulse position measurement

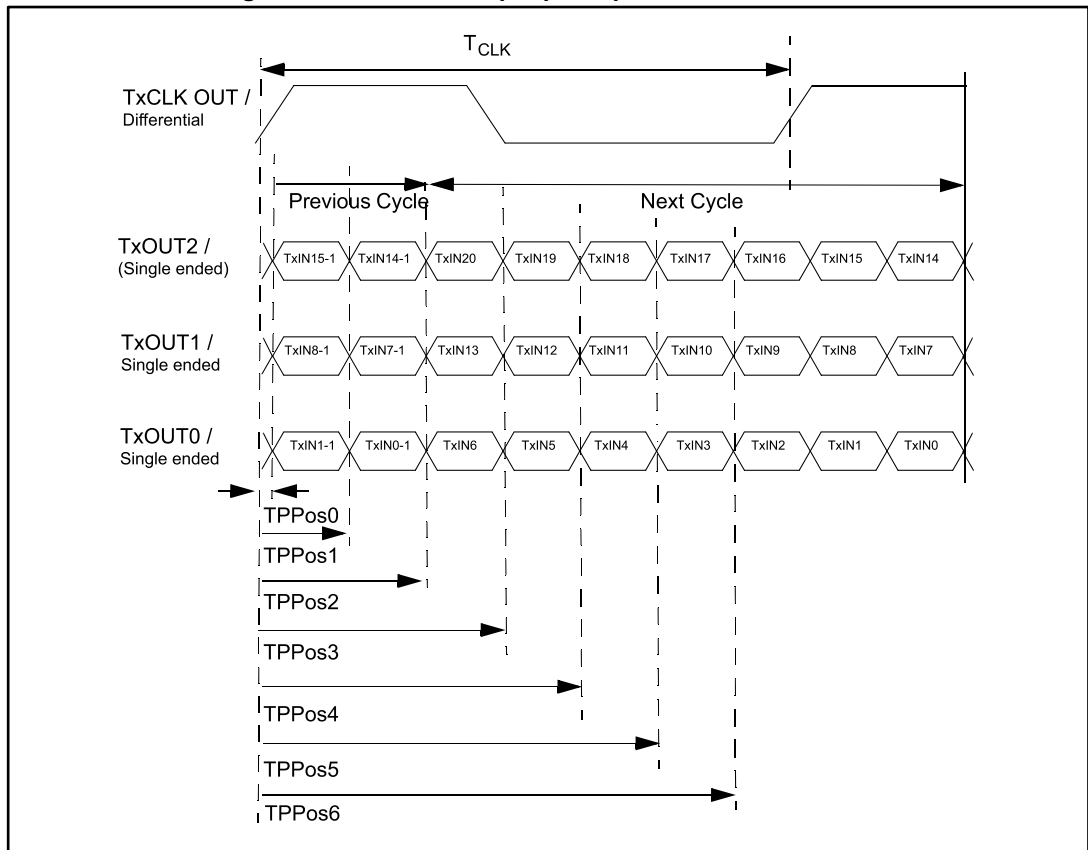
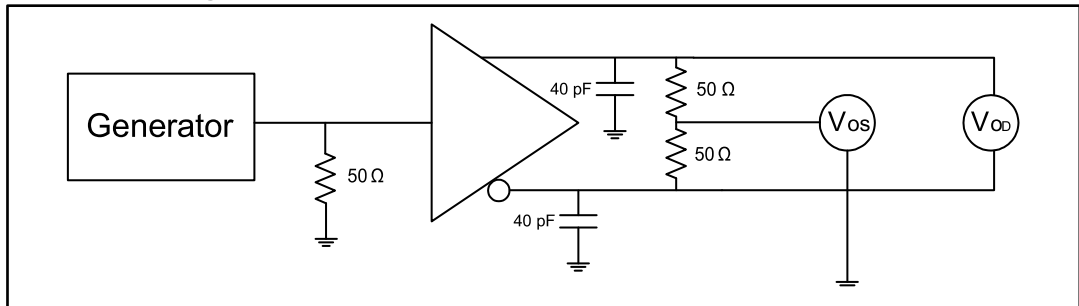


Figure 14: Driver VOD and VOS test circuit or equivalent circuit

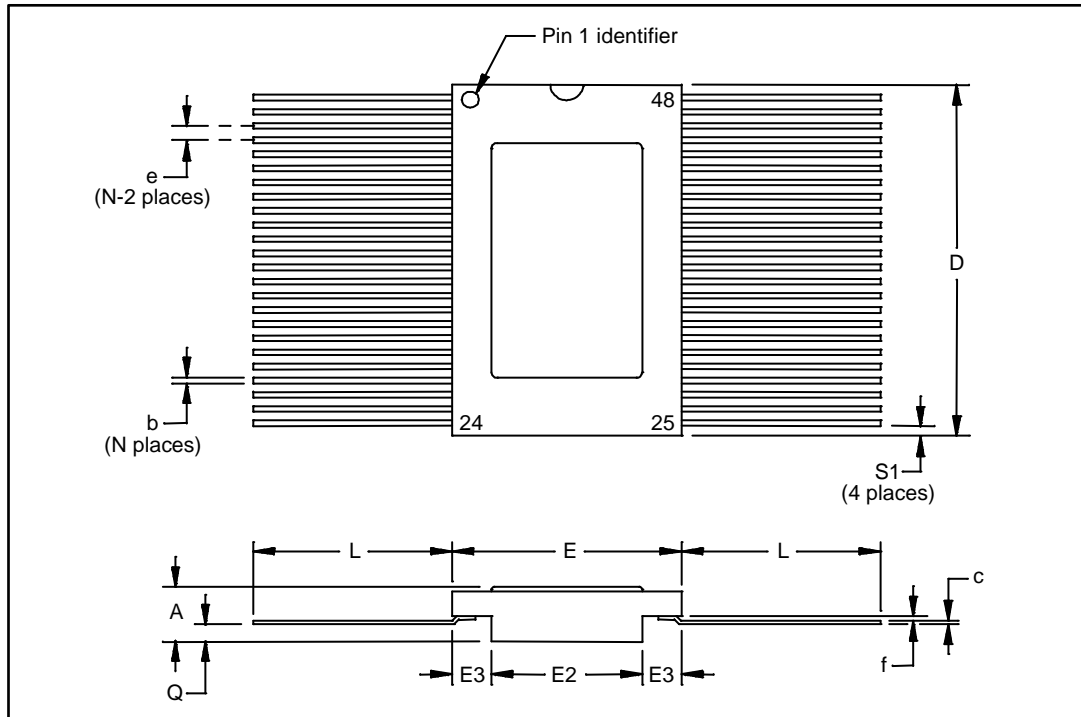


## 8 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK<sup>®</sup> packages, depending on their level of environmental compliance. ECOPACK<sup>®</sup> specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK<sup>®</sup> is an ST trademark.

### 8.1 Ceramic Flat-48 package information

Figure 15: Ceramic Flat-48 package outline



1. The upper metallic lid is connected to pin 17.

Table 8: Ceramic Flat-48 mechanical data

Dim	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A	2.47	2.18	2.72	0.097	0.086	0.107
b	0.254	0.20	0.30	0.010	0.008	0.012
c	0.15	0.12	0.18	0.006	0.005	0.007
D	15.75	15.57	15.92	0.620	0.613	0.627
E	9.65	9.52	9.78	0.380	0.375	0.385
E2	6.35	6.22	6.48	0.250	0.245	0.255
E3	1.65	1.52	1.78	0.065	0.060	0.070
e	0.635			0.025		
f	0.20			0.008		
L	8.38	6.85	9.40	0.330	0.270	0.370
Q	0.79	0.66	0.92	0.031	0.026	0.036
S1	0.43	0.25	0.61	0.017	0.010	0.024

## 9 Ordering information

**Table 9: Order codes**

Order code	Description	Temp. range	Package	Marking <sup>(1)</sup>	Packing
RHFLVDS217K1	Engineering model	-55 °C to 125 °C	Flat-48	RHFLVDS217K1	Strip pack

**Notes:**

<sup>(1)</sup>Specific marking only. Complete marking includes the following:

- ST logo
- Date code (date the package was sealed) in YYWWA (year, week, and lot index of week)
- Country of origin (FR = France)



Contact your ST sales office for information regarding the specific conditions for products in die form and QML-Q versions.

## 10 Other information

### 10.1 Date code

The date code is structured as follows: EM (engineering model) = xyywwz

Where:

x (EM only): 3, assembly location Rennes (France)

yy: last two digits year

ww: week digits

z: lot index in the week

## 11 Revision history

Table 10: Document revision history

Date	Revision	Changes
08-Apr-2016	1	Initial release

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