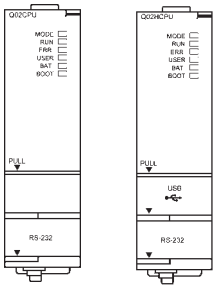
MELSEC Q Series High Performance Sequence CPUs

Key Features:

- Multiple CPU support; use up to four CPUs to combine sequence, process, motion & PC control on a single system in any combination
- Multiple program capability; allows up to 124 separate programs, depending on CPU type
- Multiple access to CPUs by several technicians simultaneously
- Very broad range of CPU capabilities
- Very high speed processing capability
- USB (Type B) connection to CPU for rapid upload/download of programs
- Up to 32MB of data storage by use of removable memory cards
- Supports floating point, PID and SFC programming
- Increased functionality in Version B or later (S/N 07032x)
  - SFC active step comment readout instruction
  - Increased multiple CPU shared memory flexibility
  - 1/1000 second resolution timestamp capability
  - Store sampling trace data in Standard RAM
  - Power supply error detection function



Required Manuals

Model Number	Description	Contents	Included with CPU?	Stocked Item
IB(NA)0800061	QCPU(Q mode) CPU Module User's Manual (Hardware)	General specs, CE compliance information, Installation, Safety requirements, Power supply wiring, Overview of system parts	No (included with base units)	–
SH(NA)080483ENG	QCPU (Q Mode) User's Manual (Hardware Design, Maintenance & Inspection)	CPU H/W specs, PSU specs, Base Unit specs, Memory Card specs, CE compliance information, Installation, Maintenance & inspection, Troubleshooting	No (purchase separately)	–
SH(NA)080484ENG	QCPU(Q Mode) User's Manual (Function Explanation, Program Fundamentals)	CPU specifications, System configuration, Programming basics, I/O assignments, Memory organization, CPU functions, Communication with intelligent function modules, Parameters & devices, Program up/downloads, Overview of multiple program architecture, Programming basics	No (purchase separately)	–
SH(NA)080485ENG	QCPU User's Manual (Multiple CPU System)	Outline, system configuration, concept for multiple CPU system, communication between CPU modules, processing time of QCPU in multiple CPU system, parameter added for multiple CPU system, precautions for use of AnS Series module, starting up the multiple CPU system	No (purchase separately)	–
SH(NA)080039	QCPU(Q Mode)/QnACPU Programming Manual (Common Instructions)	General Description, Instruction Tables, Configuration of Instructions, How To Read Instructions, Sequence Instructions, Basic Instructions, Application Instructions, Instructions For Data Link, QCPU Instructions, Redundant System Instructions, Error Codes	No (purchase separately)	–
SH(NA)080041	QCPU(Q Mode)/QnACPU Programming Manual (SFC)	General Description, System Configuration, Specifications, SFC Program Configuration, SFC Program Processing Sequence, SFC Program Execution	No (purchase separately)	–
SH(NA)080076	Q CPU (Q Mode) Programming Manual (MELSAP-L)	General Description, System Configuration, Specifications, SFC Program Configuration, SFC Program Processing Sequence, SFC Program Execution	No (purchase separately)	–
SH(NA)080040	QCPU(Q Mode)/QnACPU Programming Manual (PID Control Instructions)	General Description, System Configuration for PID Control, PID Control Specifications, Functions of PID Control, PID Control Procedure, PID Control Instructions, How To Read Explanations For Instructions, Incomplete Derivative PID Control Instructions and Program Examples, Complete Derivative PID Control Instructions and Program Examples	No (purchase separately)	–
SH(NA)080368	Programming Guide Book for Structured Text (ST)	Covers Structured Text programming method	No (purchase separately)	–

Note: Many of these manuals are available by free download from our website, www.meau.com

MELSEC Q Series High Performance Sequence CPUs

Model Number			Q02CPU	Q02HCPU	Q06HCPU	Q12HCPU	Q25HCPU
Stocked Item			S	S	S	S	–
Certification			UL• cUL • CE	UL • cUL • CE	UL • cUL • CE	UL • cUL • CE	UL • cUL • CE
Control System			Repeated operation using stored program				
I/O Control Method			Refresh mode				
Programming Language			Language dedicated to sequence control Relay symbol type (ladder), logic symbolic language				
Processing Speed (Sequence Instruc.)	LD (LD X10)		79ns	34ns			
	MOV (MOV D0 D1)		237ns	102ns			
Total Number of Instructions			360 (excluding intelligent function module dedicated instructions)				
Constant Scan (Program Start at Given Time Intervals)			0.5 to 2000ms (can be specified in 0.5ms increments)				
Program Capacity	Program Memory (Drive 0)		28k steps	28k steps	60k steps	124k steps	252k steps
Memory Capacity	Memory Card (RAM) (Drive 1)		Capacity of loading memory cards (2 Mbyte max.)				
	Memory Card (ROM) (Drive 2)		Installed memory card capacity (Flash card: 4 Mbyte max., ATA card: 32 Mbyte max.)				
	Standard RAM (Drive 3)		64 kbyte	128 kbyte	128 kbyte	256 kbyte	256 kbyte
	Standard ROM (Drive 4)		112 kbyte	112 kbyte	240 kbyte	496 kbyte	1008 kbyte
	CPU Shared Memory		8 kbyte (not latched)				
Maximum Number Of Stored Files	Program Memory		28	28	60	124	252
	Memory Card (RAM)		287				
	Memory Card (ROM)	Flash	288				
		ATA	512				
	Standard RAM		3				
	Standard ROM		28	28	60	124	252
Standard ROM Number of Writings			Max. 100,000 times				
Number of I/O Device Points			8192 points (X/Y0 to 1FFF) (*1)				
Number of I/O Points			4096 points (X/Y0 to FFF) (*2)				
Number of Device Points	Internal Relay [M]		Default 8192 points (M0 to 8191)				
	Latch Relay [L]		Default 8192 points (L0 to 8191)				
	Link Relay [B]		Default 8192 points (B0 to 1FFF)				
	Timer [T]		Default 2048 points (T0 to 2047) (used as low-speed or high-speed timer) Switching between low-speed and high-speed timers is set by instruction Low-speed/high-speed timer timing increments are parameter-set (Low-speed timer: 1 to 1000ms, 1ms increments, default 100ms) (High-speed timer: 0.1 to 100ms, 0.1ms increments, default 10ms)				
	Retentive Timer [ST]		Default 0 (ST0 to 2047) (used as low-speed or high-speed timer) Switching between low-speed and high-speed timers is set by instruction Low-speed/high-speed timer timing increments are parameter-set (Low-speed timer: 1 to 1000ms, 1ms increments, default 100ms) (High-speed timer: 0.1 to 100ms, 0.1ms increments, default 10ms)				
	Counter [C]		Normal counters Default 1024 points (C0 to 1023) Interrupt counters Max. 256 points. (Default 0 points, parameter setting)				
	Data Register [D]		Default 12288 points (D0 to 12287)				
	Link Register [W]		Default 8192 points (W0 to 1FFF)				
	Annunciator [F]		Default 2048 points (F0 to 2047)				
	Edge Relay [V]		Default 2048 points (V0 to 2047)				
	File Register [R]		When standard RAM is used: **Q02CPU:** 32768 points (R0 to 32767) **Q02HCPU, Q06HCPU:** The number of points of up to 65536 points can be used by block conversion in increments of 32768 points (R0 to 32767) **Q12HCPU, Q25HCPU:** The number of points of up to 131072 points can be used by block conversion in increments of 32768 points (R0 to 32767) • When a SRAM card (1 Mbyte) is used: The number of points of up to 517120 points can be used by block conversion increments of 32768 points (R0 to 32767) • When a SRAM card (2 Mbyte) is used: The number of points up to 1041408 points can be used by block conversion increments of 32768 points (R0 to 32767) • When a Flash card (2 Mbyte) is used: The number of points up to 1041408 points can be used by block conversion increments of 32768 points (R0 to 32767) • When a Flash card (4 Mbyte) is used: The number of points up to 1042432 points can be used by block conversion increments of 32768 points (R0 to 32767)				
	File Register [ZR]		When standard RAM is used: **Q02CPU:** 32768 points (ZR0 to 32767) **Q02HCPU, Q06HCPU:** 65536 points (ZR0 to 65535), No block conversion necessary **Q12HCPU, Q25HCPU:** 131072 points (ZR0 to 131071), No block conversion necessary • When a SRAM card (1 Mbyte) is used: 517120 points (ZR0 to 517119), No block conversion necessary • When a SRAM card (2 Mbyte) is used: 1041408 points (ZR0 to 1041407), No block conversion necessary • When a Flash card (2 Mbyte) is used: 1041408 points (ZR0 to 1041407), No block conversion necessary • When a Flash card (4 Mbyte) is used: 1042432 points (ZR0 to 1042431), No block conversion necessary				

MELSEC Q Series High Performance Sequence CPUs (continued)

Model Number		Q02CPU	Q02HCPU	Q06HCPU	Q12HCPU	Q25HCPU
Number of Device Points	Stocked Item	S	S	S	S	–
	Special Link Relay [SB]	[SB] 2048 points (SB0 to 7FF)				
	Special Link Register [SW]	[SW] 2048 points (SW0 to 7FF)				
	Step Relay [S]	8192 points (S0 to 8191)				
	Index Register [Z]	16 points (Z0 to 15)				
	Pointer [P]	4096 points (P0 to 4095), set in parameters the range in which the pointers/common pointers are used				
	Interrupt Pointer [I]	256 points (I0 to 255) In parameters, set the cyclic intervals of the system interrupt pointers I28 to I31 (0.5 to 1000ms, 0.5ms increments)				
	Special Relay [SM]	2048 points (SM0 to 2047)				
	Special Register [SD]	2048 points (SD0 to 2047)				
	Function Input [FX]	16 points (FX0 to F)				
	Function Output [FY]	16 points (FY0 to F)				
	Function Register [FD]	5 points (FD0 to 4)				
Link Direct Device		Device for direct access to link device. Specified format: J☐ ☐ \ ☐ ☐				
Intelligent Function Module Direct Device		Device for direct access to buffer memory of intelligent function module. Specified format: U☐ ☐ \ G ☐ ☐				
Latch (Power Failure Comp.) Range		L0 to 8191 (default) (Latch range setting can be made for B, F, V, T, ST, C, W and D)				
Remote RUN/PAUSE Contact		1 point can be set for each RUN and PAUSE contacts from X0-1FFF				
Clock Function		Year, month, day, hour, minute, second, day of week (Automatic leap year judgment) Accuracy –3.18 to +5.25 (TYP +2.12) s/d @ 0°C; Accuracy –3.93 to +5.25 (TYP +1.90) s/d @ 25°C Accuracy –14.69 to +3.53 (TYP –3.67) s/d @ 55°C				
Permissible Instantaneous Power Failure Time		Depends on power supply module				
5VDC Internal Current Consumption (A)		0.60	0.64	0.64	0.64	0.64
Weight (kg)		0.20	0.20	0.20	0.20	0.20
Dimensions (W x H x D) mm (in)		27.4 (1.08) x 98 (3.86) x 89.3 (3.52)				

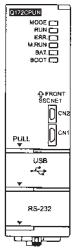
Notes:
1. Sum of the number of I/O points on the main/extension base directly controlled by the CPU module and the number of I/O points controlled as remote I/O by the remote I/O network.
2. Number of I/O points on the main/extension base directly controlled by the CPU module.

MELSEC Q Series Motion CPUs

Q Series motion CPUs offer the ability to integrate complex motion systems on a Q Series system alongside sequence, process & PC based functions. The motion CPUs allow costly, inflexible mechanical systems to be replaced by multiple axis motion control that is significantly easier and less expensive to design, build and re-configure.

Key Features:

- Up to 32 axes controlled by one CPU, allowing up to 96 axes per base rack
- Servo axes connect quickly and easily via daisy chain connection on SSCNET, eliminating complex, expensive wiring harnesses
- SSCNET offers high speed, deterministic control of each axis independently
- Allows integration with other automation technologies such as open language program control and Ethernet/Internet capabilities



Required Manuals

Model Number	Description	Contents	Included with CPU?	Stk Item
IB(NA)0300040	Q172CPU(N)/Q173CPU(N) User's Manual	Covers the Q172CPUN and Q173CPUN	No (purchase separately)	–

Note: Many of these manuals are available by free download from our website, www.meau.com

Q Motion CPUs

Model Number	Q173CPUN	Q172CPUN
Stocked Item	S	S
Number of Control Axes	32 axes	8 axes
Operation Cycle	Approx. 0.88ms	
Interpolation Function	Linear interpolation (Max.4-axes), Circular interpolation (2-axes), helical interpolation (3-axes) PTP (Point to Point), speed control, speed-position control, fixed-pitch feed, constant-speed control, position follow-up control, speed-switching control high speed oscillation control, synchronous control	
Acceleration/Deceleration Process	Automatic trapezoidal acceleration/deceleration, S-curve acceleration/deceleration	
Compensation Function	Backlash compensation, Electronic gear	
Program Language	Motion SFC, Dedicated instructions, Mechanical support language	
Program Capacity	14K steps	
Number of Positioning Points	3,200 points (Positioning data can be designated indirectly)	
Zeroing Function	Proximity DOG type, Count type, Data setting type	
JOG Operation Function	Available	
Sync. Encoder Operation Function	12 units can be connected	8 units can be connected
M-Function	M-code output function, M-code completion wait function	
Absolute Position System	Available by adding a battery to Servo Amplifier (Absolute or incremental system can be specified per axis)	
SSCNET I/F	5CH	2CH
Number of Modules Connected	Max. 64 modules (Number of Q-series Extension Base: Max. 7)	
Pulse Generator	Q172PX 4 modules can be used per CPU	Q172LX 1 module can be used per CPU
Synchronous Encoder	Q172EX 6 modules can be used per CPU	Q172EX 4 modules can be used per CPU
External Signal Input Module	Q173LX 4 modules can be used per CPU	Q173LX 3 modules can be used per CPU
Weight (kg)	0.23	0.22
Dimensions (W x H x D) mm (in)	27.4 (1.08) x 98 (3.86) x 114.3 (4.50)	27.4 (1.08) x 98 (3.86) x 114.3 (4.50)