PTMA180402EL
PTMA180402FL

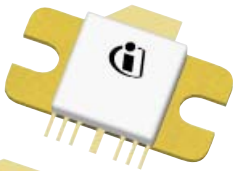
green Product

Wideband RF LDMOS Integrated Power Amplifier 40 W, 1800 – 2000 MHz

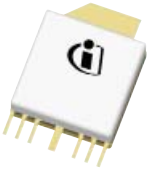
Description

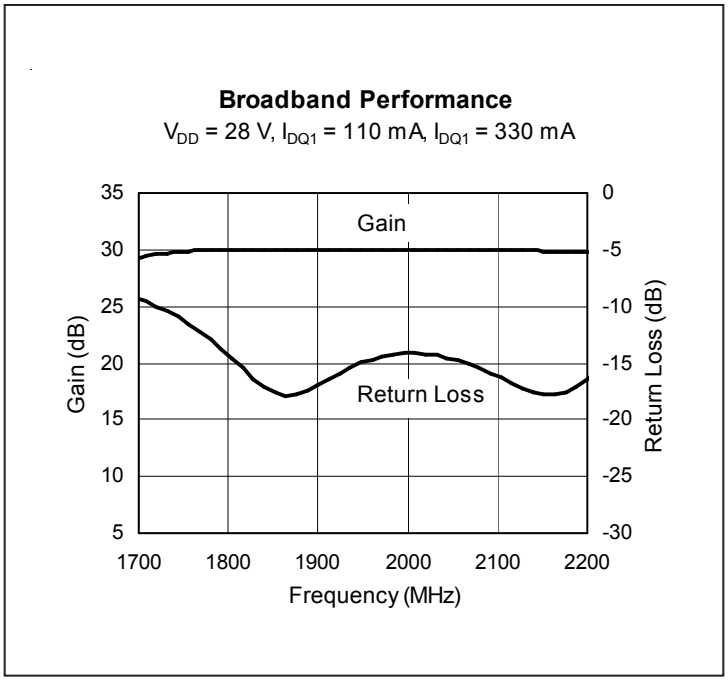
The PTMA180402EL and PTMA180402FL are matched, wideband 40-watt, 2-stage, LDMOS integrated amplifiers intended for use in all typical modulation formats from 1800 to 2000 MHz. These devices are offered in thermally-enhanced ceramic packages for cool and reliable operation.

PTMA180402EL
Package H-33265-8



PTMA180402FL
Package H-34265-8





Features

- Designed for wide RF and modulation bandwidths and low memory effects
- On-chip matching, integrated input DC block, 50-ohm input and > 5-ohm output
- Typical single-carrier CDMA performance at 1960 MHz, 28 V
  - Average output power = 4 W
  - Linear gain = 30 dB
  - Efficiency = 14%
  - Adjacent channel power = –53 dBc
- Typical 2-tone performance, 1960 MHz, 28 V
  - Output power (PEP) = 50 W at IM3 = –30 dBc
  - Efficiency = 33%
- Capable of handling 10:1 VSWR @ 28 V, 40 W (CW) output power
- Integrated ESD protection. Meets HBM Class 1B (minimum), per JESD22-A114F
- High-performance, thermally-enhanced packages, Pb-free and RoHS compliant, with solder-friendly plating

All published data at T_{CASE} = 25°C unless otherwise indicated

ESD: Electrostatic discharge sensitive device—observe handling precautions!

RF Characteristics

CDMA Measurements (tested in Infineon test fixture)
V_{DD} = 28 V, I_{DQ1} = 110 mA, I_{DQ2} = 335 mA, P_{OUT} = 4 W average, f = 1960 MHz

Characteristic	Symbol	Min	Typ	Max	Unit
Gain	G_{ps}	28.5	30	—	dB
Drain Efficiency	η_D	13	14	—	%
Adjacent Channel Power Ratio	ACPR	—	–53	–50	dBc

DC Characteristics

Stage 1 Characteristics	Conditions	Symbol	Min	Typ	Max	Unit
Drain Leakage Current	V_{DS} = 28 V, V_{GS} = 0 V	I_{DSS}	—	—	1.0	µA
	V_{DS} = 63 V, V_{GS} = 0 V	I_{DSS}	—	—	10.0	µA
Gate Leakage Current	V_{GS} = 10 V, V_{DS} = 0 V	I_{GSS}	—	—	1.0	µA
On-state Resistance	V_{GS} = 10 V, V_{DS} = 0.1 V	$R_{DS(on)}$	—	1.6	—	Ω
Operating Gate Voltage	V_{DS} = 28 V, I_{DQ} = 160 mA	V_{GS}	2.0	2.5	3.0	V

Stage 2 Characteristics	Conditions	Symbol	Min	Typ	Max	Unit
Drain-source Breakdown Voltage	V_{GS} = 0 V, I_{DS} = 10 mA	$V_{(BR)DSS}$	65	—	—	V
Drain Leakage Current	V_{DS} = 28 V, V_{GS} = 0 V	I_{DSS}	—	—	1.0	µA
	V_{DS} = 63 V, V_{GS} = 0 V	I_{DSS}	—	—	10.0	µA
Gate Leakage Current	V_{GS} = 10 V, V_{DS} = 0 V	I_{GSS}	—	—	1.0	µA
On-state Resistance	V_{GS} = 10 V, V_{DS} = 0.1 V	$R_{DS(on)}$	—	0.21	—	Ω
Operating Gate Voltage	V_{DS} = 28 V, I_{DQ} = 330 mA	V_{GS}	2.0	2.5	3.0	V

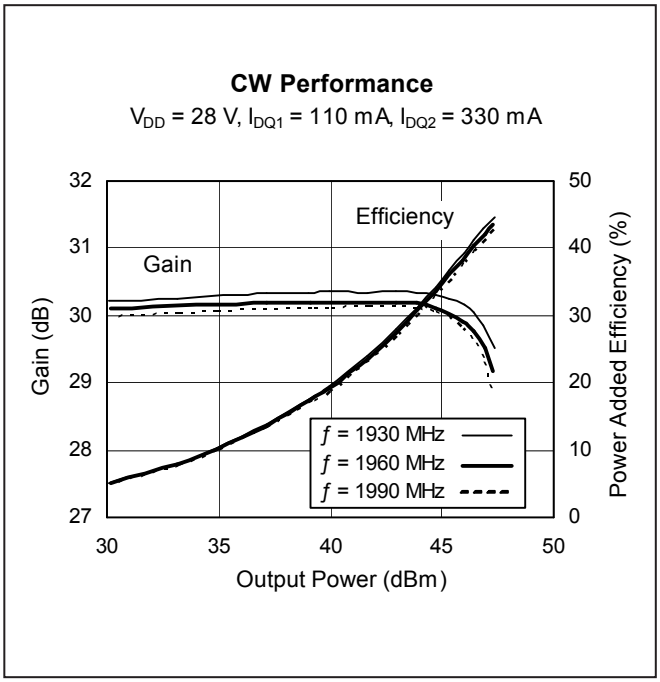
Maximum Ratings

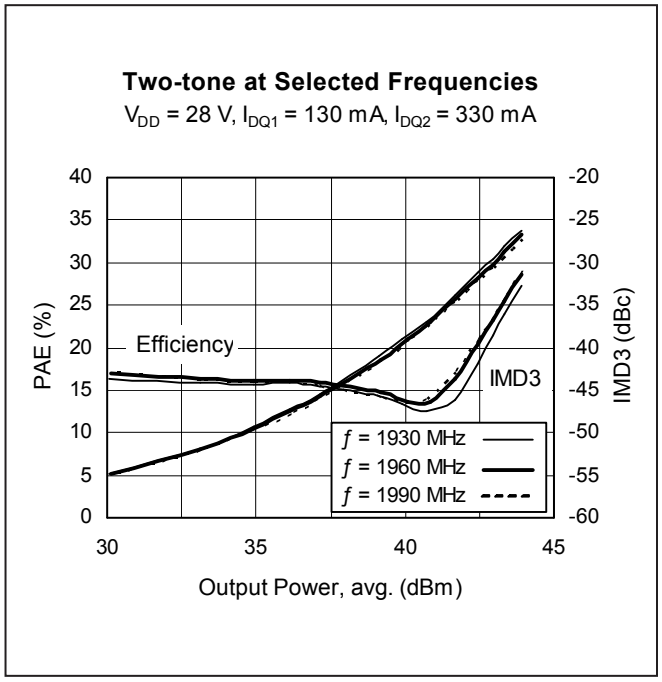
Parameter		Symbol	Value	Unit
Drain-Source Voltage		V_{DSS}	65	V
Gate-Source Voltage		V_{GS}	–0.5 to +12	V
Junction Temperature		T_J	200	°C
Storage Temperature Range		T_{STG}	–40 to +150	°C
Overall Thermal Resistance (T_{CASE} = 70°C)	1st Stage	$R_{\theta JC}$	5.0	°C/W
P_{OUT} = 40 W, I_{DQ1} = 160 mA, I_{DQ2} = 330 mA	2nd Stage	$R_{\theta JC}$	1.1	°C/W

Ordering Information

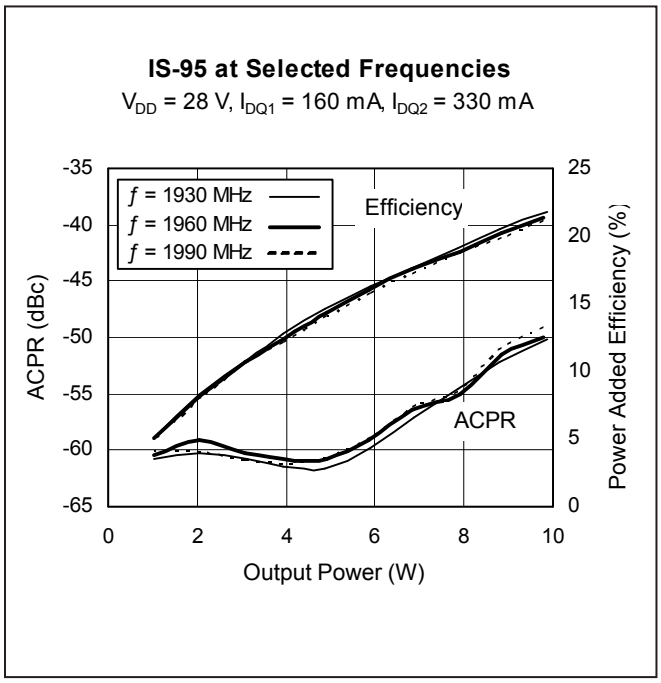
Type and Version	Package Type	Package Description	Shipping
PTMA180402EL V1	H-33265-8	Themally-enhanced, slotted flange	Tray
PTMA180402EL V1 R50	H-33265-8	Themally-enhanced, slotted flange	Tape
PTMA180402FL V1	H-34265-8	Themally-enhanced, earless flange	Tray
PTMA180402FL V1 R50	H-34265-8	Themally-enhanced, earless flange	Tape

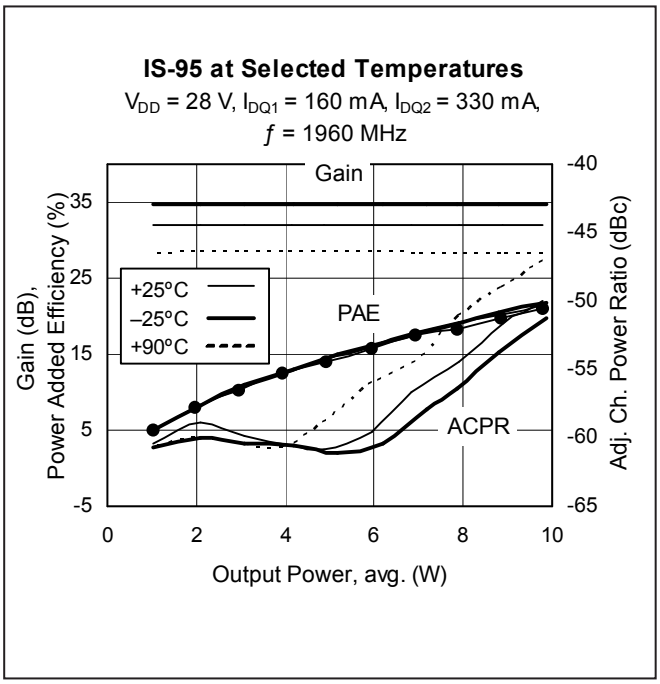
Typical Performance (data taken in a production test fixture)

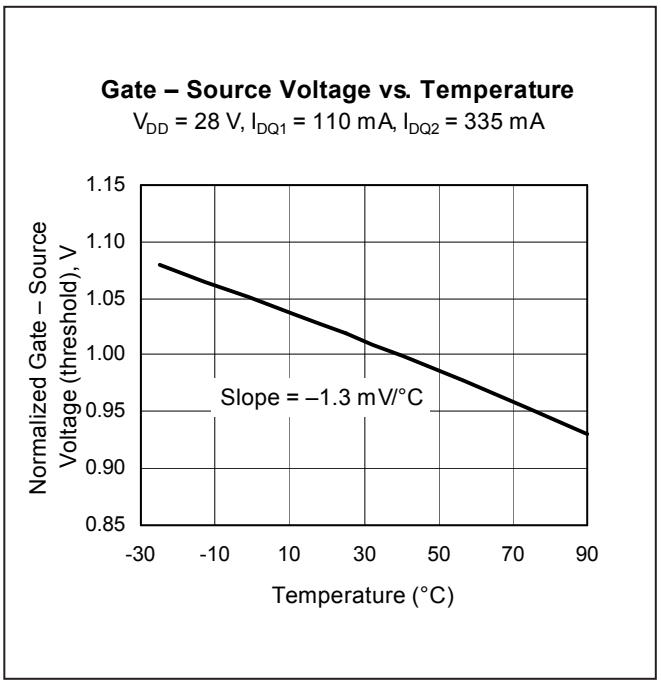


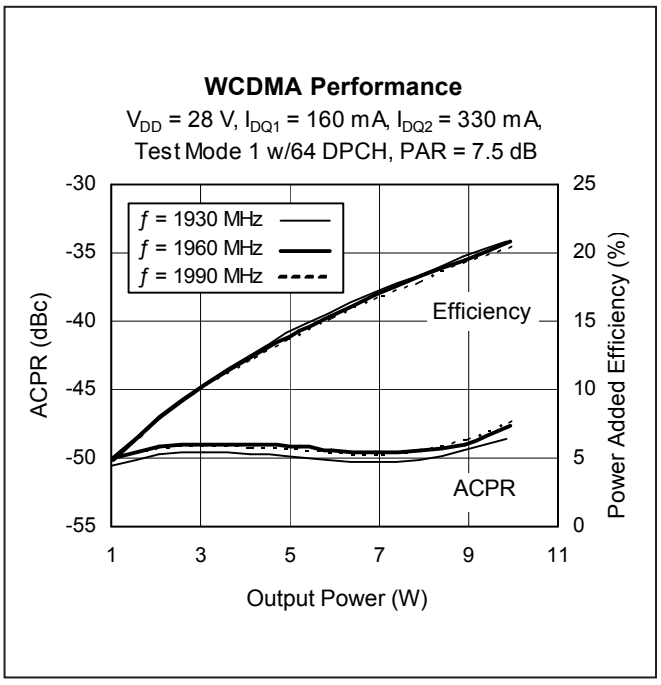


Typical Performance (cont.)

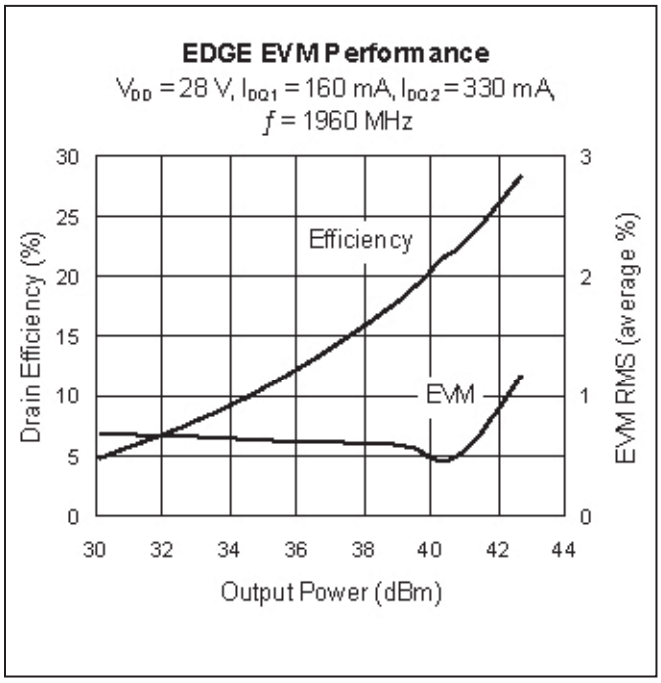


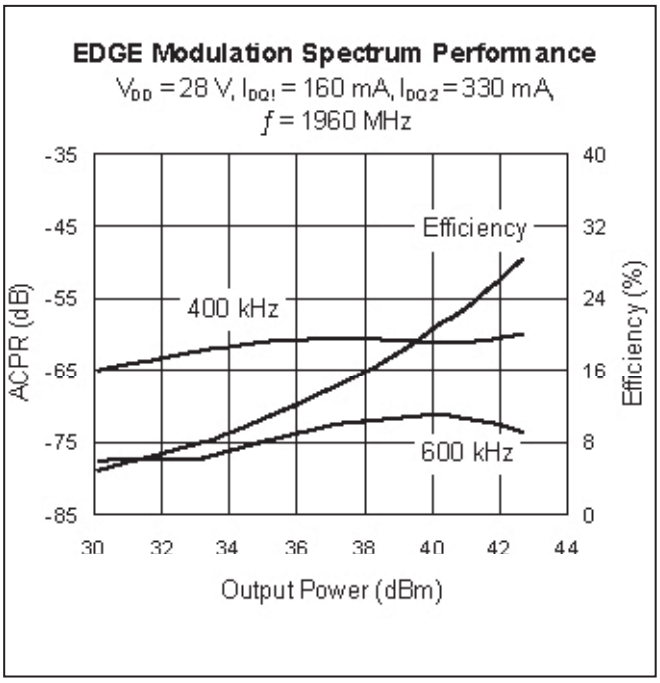


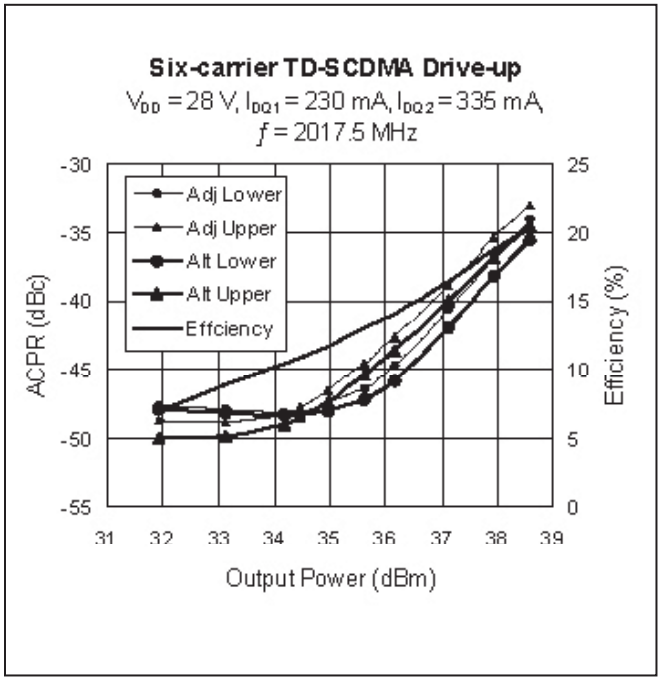




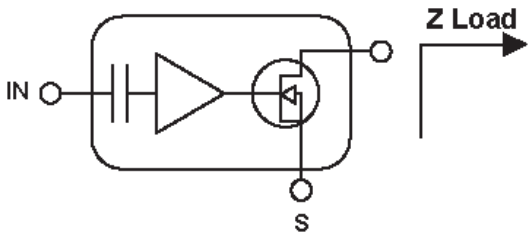
Typical Performance (cont.)



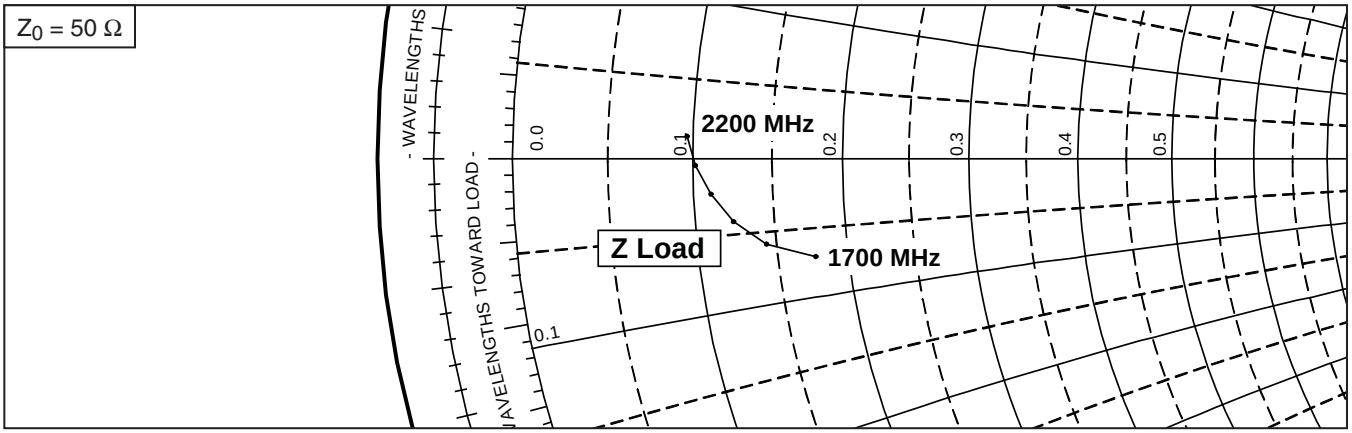




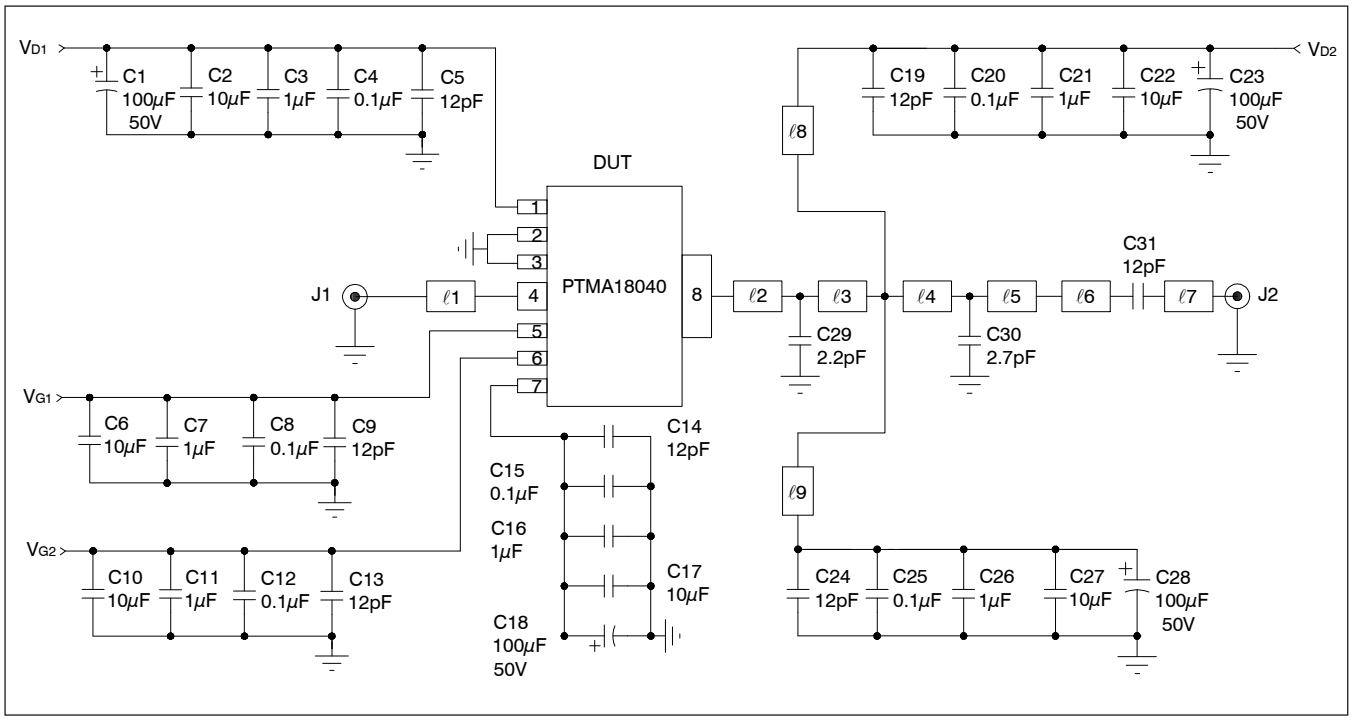
Broadband Circuit Impedance



Frequency	Z Load Ω	
MHz	R	jX
1700	8.89	–3.62
1800	7.27	–2.99
1900	6.26	–2.13
2000	5.59	–1.19
2100	5.14	–0.27
2200	4.89	0.67



Reference Circuit



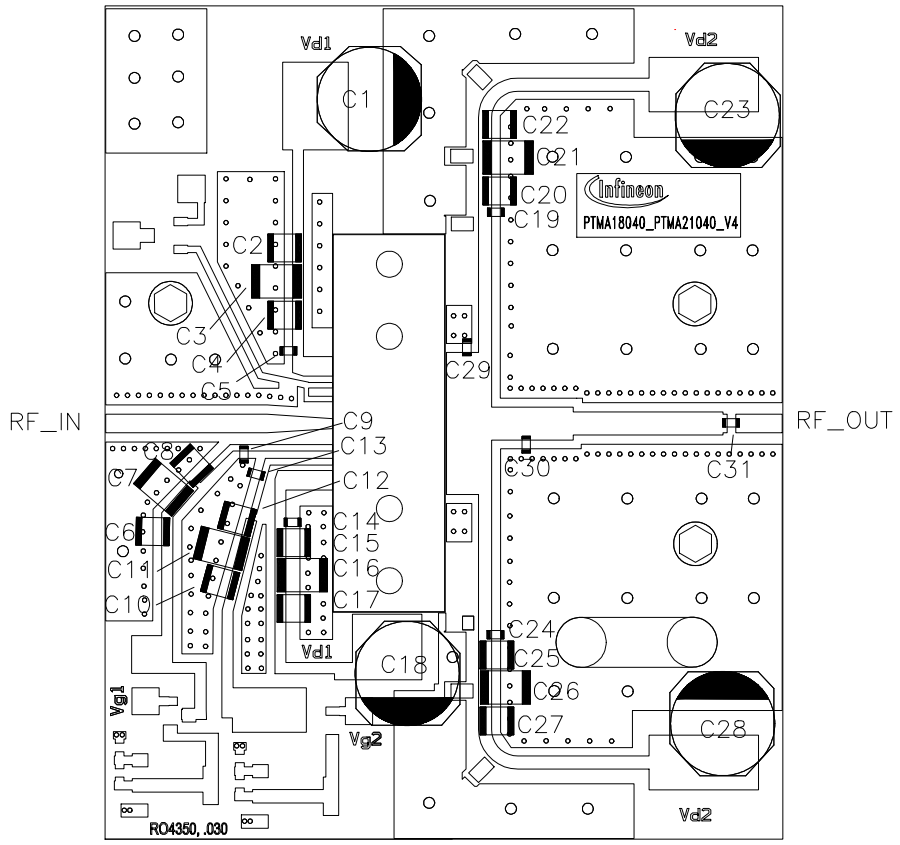
Reference circuit schematic for ƒ = 1930 – 1990 MHz

Circuit Assembly Specifications

DUT	PTMA180402EL or PTMA180402FL	LDMOS Integrated Power Amplifier
Test Fixture Part No.	LTN/PTMA180402EFL	
PCB	Rogers 4350, 0.76 mm [.030"] thick, 1 oz. copper, ε_r = 3.48	
Find Gerber files for this test fixture on the Infineon Web site at **http://www.infineon.com/rfpower**		

Microstrip	Electrical Characteristics at 1960 MHz	Dimensions: L x W (mm)	Dimensions: L x W (in.)
ℓ1	0.224 λ, 49.8 Ω	20.75 x 1.70	0.817 x 0.067
ℓ2	0.022 λ, 10.4 Ω	1.85 x 13.00	0.073 x 0.512
ℓ3	0.027 λ, 10.4 Ω	2.26 x` 13.00	0.089 x 0.512
ℓ4	0.035 λ, 34.1 Ω	3.18 x 3.00	0.125 x 0.118
ℓ5	0.048 λ, 34.1 Ω	4.29 x 3.00	0.169 x 0.118
ℓ6	0.153 λ, 44.5 Ω	14.07 x 2.03	0.554 x 0.080
ℓ7	0.046 λ, 49.8 Ω	4.27 x 1.70	0.168 x 0.067
ℓ8, ℓ9	0.136 λ, 61.1 Ω	12.83 x 1.19	0.505 x 0.047

Reference Circuit (cont.)



Reference circuit asembly diagram (not to scale)*

Component	Description	Suggested Supplier	P/N or Comment
C1, C18, C23, C28	Electrolytic capacitor, 100 µF, 50 V	Digi-Key	PCE3718CT-ND
C2, C6, C10, C17, C22, C27	Ceramic capacitor, 10 µF	Murata	GRM422Y5V106Z050AL
C3, C7, C11, C16, C21, C26	Ceramic capacitor, 1 µF	Digi-Key	445-1411-2-ND
C4, C8, C12, C15, C20, C25	Capacitor, 0.1 µF	Digi-Key	399-1267-2-ND
C5, C9, C13, C14, C19, C24, C31	Ceramic capacitor, 12 pF	ATC	600S120JT
C29	Ceramic capacitor, 2.2 pF	ATC	600S2R2CT
C30	Ceramic capacitor, 2.7 pF	ATC	600S2R7BT

Package Specifications

Package H-33265-8 Outline

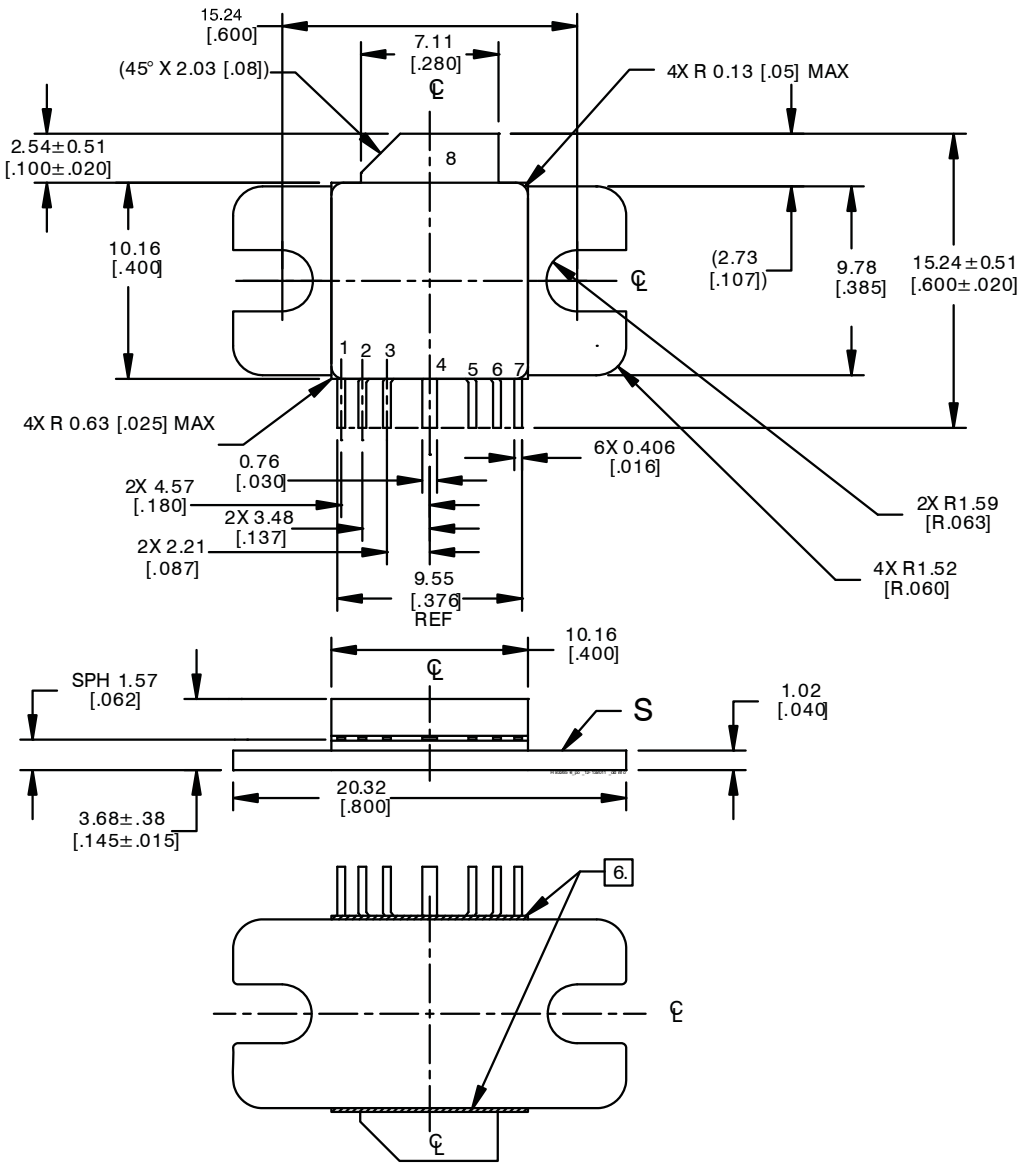
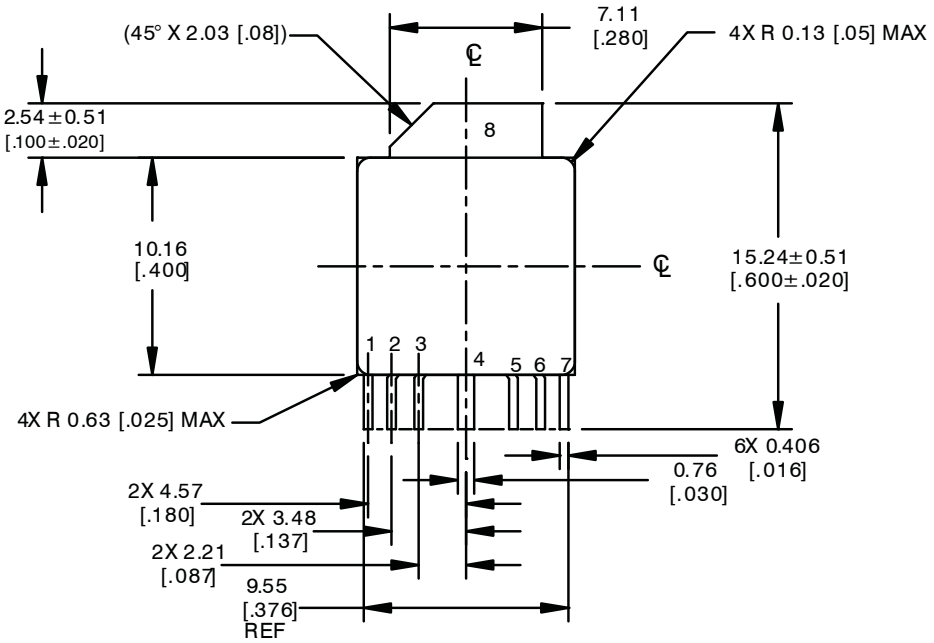


Diagram Notes—unless otherwise specified:

1. Interpret dimensions and tolerances per ASME Y14.5M-1994.
2. Pins: S = source; see page 11 for complete list and diagram.
3. Lead thickness: 0.127±0.025 [.005±0.001]
4. Gold plating less than 0.25 micron [10 microinch].
5. All tolerances ± 0.127 [.005] unless specified otherwise.
6. Exposed metal plane on bottom of ceramic insulator.
7. Primary dimensions are mm. Alternate dimensions are inches.

Package Specifications (cont.)

Package H-34265-8 Outline



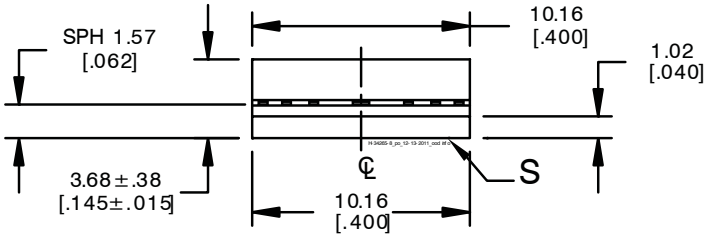


Diagram Notes—unless otherwise specified:

1. Interpret dimensions and tolerances per ASME Y14.5M-1994.
2. Pins: S = source; see page 11 for complete list and diagram.
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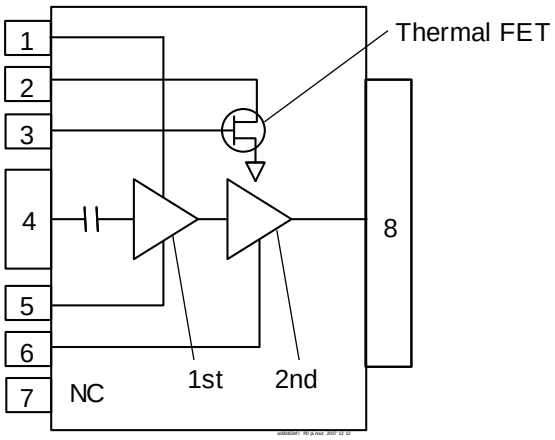
4. Gold plating less than 0.25 micron [10 microinch].
5. All tolerances ± 0.127 [.005] unless specified otherwise.
6. Primary dimensions are mm. Alternate dimensions are inches.

Package Specifications (cont.)

Pin Diagram for PTMA180402EL and PTMA180402FL Packages H-33265-8 and H-34265-8



Pin #	Function
S (flange, see Package Outlines)	Source
1	Drain 1
2	FET_D
3	FET_G
4	RF In
5	Gate 1
6	Gate 2
7	NC
8	RF Out/D2

Find the latest and most complete information about products and packaging at the Infineon Internet page
http://www.infineon.com/rfpower

Revision History:	2011-12-13	Data Sheet
Previous Version:	2009-08-31, Data Sheet	

Page	Subjects (major changes since last revision)
2	Separated the DC table into two stages, for clarity.

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highpowerRF@infineon.com

To request other information, contact us at:
+1 877 465 3667 (1-877-GO-LDMOS) USA
or +1 408 776 0600 International

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