



PSMNR67-30YLE

N-channel 30 V, 0.68 mOhm, ASFET with enhanced SOA in LFPAK56E

5 May 2022

Objective data sheet

1. General description

N-channel enhancement mode ASFET with enhanced SOA in LFPAK56E package optimized for low R_{DSon} and strong safe operating area optimized for hot-swap, inrush and linear-mode applications.

2. Features and benefits

- Fully optimized Safe Operating Area (SOA) for superior linear mode operation
- Optimized for low R_{DSon} / low I^2R conduction losses
- LFPAK56E package for applications that demand the highest performance and reliability in a 30 mm² footprint
- Low leakage < 1 μ A at 25 °C
- Copper-clip for low parasitic inductance and resistance
- High reliability LFPAK package, qualified to 175 °C

3. Applications

- Hot swap in 12 V-20 V applications
- e-Fuse
- DC switch
- Load switch
- Battery protection

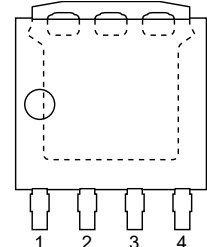
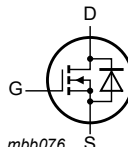
4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$25\text{ °C} \leq T_j \leq 175\text{ °C}$	-	-	30	V
I_D	drain current	$V_{GS} = 10\text{ V}; T_{mb} = 25\text{ °C}$	-	-	[tbd]	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}; \text{Fig. 1}$	-	-	[tbd]	W
T_j	junction temperature		-55	-	175	°C
Static characteristics						
R_{DSon}	drain-source on-state resistance	$V_{GS} = 10\text{ V}; I_D = 25\text{ A}; T_j = 25\text{ °C}$	-	0.62	0.68	m Ω
		$V_{GS} = 7\text{ V}; I_D = 25\text{ A}; T_j = 25\text{ °C}$	-	0.75	1	m Ω
Dynamic characteristics						
Q_{GD}	gate-drain charge	$I_D = 25\text{ A}; V_{DS} = 15\text{ V}; V_{GS} = 4.5\text{ V}$	[tbd]	[tbd]	[tbd]	nC
$Q_{G(tot)}$	total gate charge		[tbd]	[tbd]	[tbd]	nC
Source-drain diode						
S	softness factor	$I_S = 25\text{ A}; di_S/dt = -100\text{ A}/\mu\text{s}; V_{GS} = 0\text{ V}; V_{DS} = 15\text{ V}; \text{Fig. 3}$	-	[tbd]	-	

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source	 <p>LPAK56E; Power-SO8 (SOT1023)</p>	 <p>mbb076</p>
2	S	source		
3	S	source		
4	G	gate		
mb	D	mounting base; connected to drain		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PSMNR67-30YLE	LPAK56E; Power-SO8	plastic, single-ended surface-mounted package (LPAK56); 4 leads; 1.27 mm pitch	SOT1023

7. Marking

Table 4. Marking codes

Type number	Marking code
PSMNR67-30YLE	E67L30J

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage	$25\text{ °C} \leq T_j \leq 175\text{ °C}$	-	30	V
V_{DGR}	drain-gate voltage	$25\text{ °C} \leq T_j \leq 175\text{ °C}$; $R_{GS} = 20\text{ k}\Omega$	-	30	V
V_{GS}	gate-source voltage		-20	20	V
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}$; Fig. 1	-	[tbd]	W
I_D	drain current	$V_{GS} = 10\text{ V}$; $T_{mb} = 25\text{ °C}$	-	[tbd]	A
		$V_{GS} = 10\text{ V}$; $T_{mb} = 100\text{ °C}$	-	[tbd]	A
I_{DM}	peak drain current	pulsed; $t_p \leq 10\text{ }\mu\text{s}$; $T_{mb} = 25\text{ °C}$; Fig. 2	-	[tbd]	A
T_{stg}	storage temperature		-55	175	°C
T_j	junction temperature		-55	175	°C
$T_{sld(M)}$	peak soldering temperature		-	260	°C
Source-drain diode					
I_S	source current	$T_{mb} = 25\text{ °C}$	-	[tbd]	A

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Symbol	Parameter	Conditions	Min	Max	Unit
I_{SM}	peak source current	pulsed; $t_p \leq 10 \mu s$; $T_{mb} = 25 \text{ }^\circ\text{C}$	-	[tbd]	A
Avalanche ruggedness					
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$I_D = 25 \text{ A}$; $V_{sup} \leq 30 \text{ V}$; $R_{GS} = 50 \Omega$; $V_{GS} = 10 \text{ V}$; $T_{j(\text{init})} = 25 \text{ }^\circ\text{C}$; unclamped	-	[tbd]	mJ
I_{AS}	non-repetitive avalanche current	$V_{sup} \leq 30 \text{ V}$; $V_{GS} = 10 \text{ V}$; $T_{j(\text{init})} = 25 \text{ }^\circ\text{C}$; $R_{GS} = 50 \Omega$	[1]	[tbd]	A

[1] Protected by 100% test

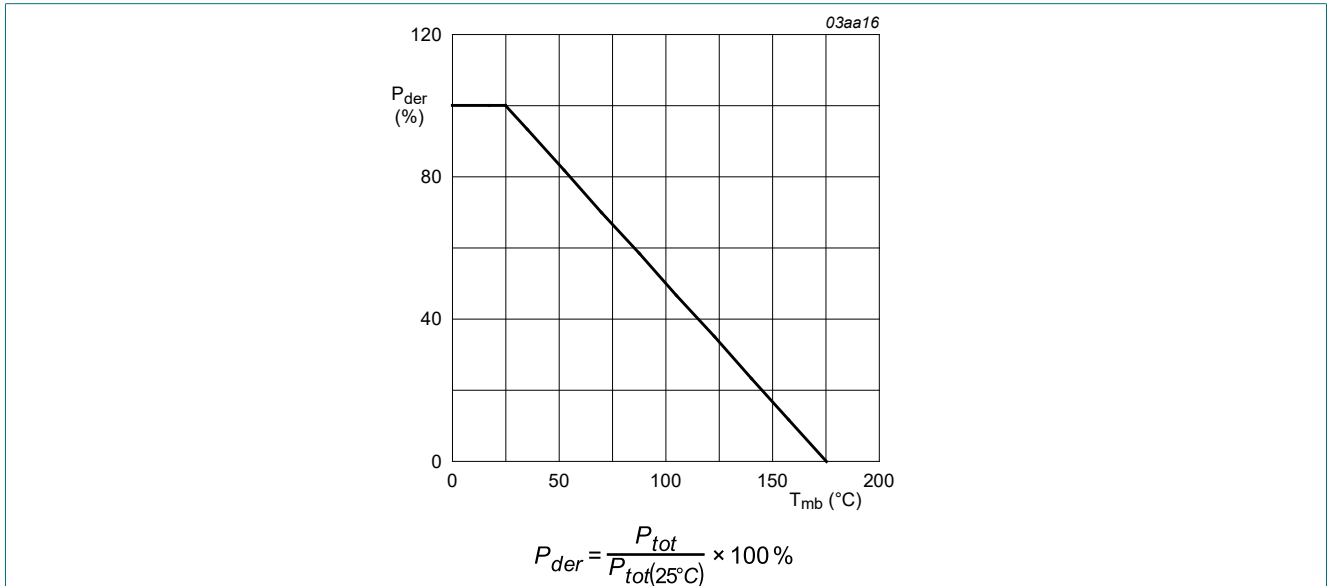


Fig. 1. Normalized total power dissipation as a function of mounting base temperature

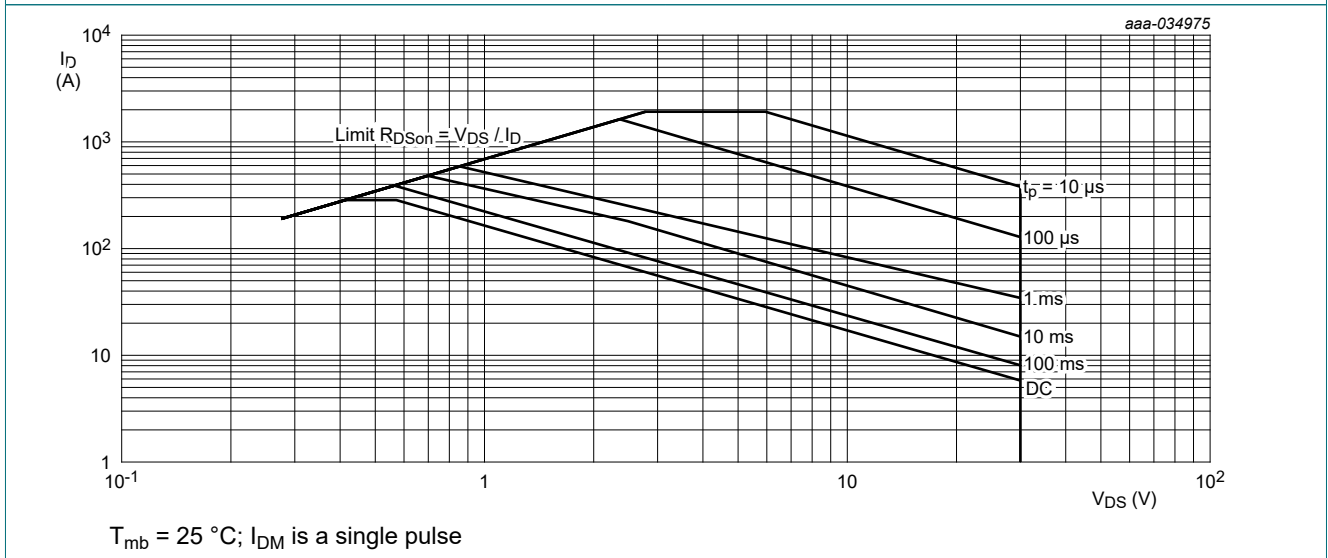


Fig. 2. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base		-	[tbd]	[tbd]	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient		-	42	-	K/W
			-	85	-	K/W

10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu A; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$	30	-	-	V
		$I_D = 250 \mu A; V_{GS} = 0 V; T_j = -55 \text{ }^\circ C$	27	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 25 \text{ }^\circ C$	1.2	[tbd]	2.2	V
$\Delta V_{GS(th)}/\Delta T$	gate-source threshold voltage variation with temperature	$25 \text{ }^\circ C \leq T_j \leq 150 \text{ }^\circ C$	-	[tbd]	-	mV/K
I_{DSS}	drain leakage current	$V_{DS} = 24 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$	-	-	1	μA
		$V_{DS} = 24 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 125 \text{ }^\circ C$	-	[tbd]	-	μA
I_{GSS}	gate leakage current	$V_{GS} = 16 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$	-	-	100	nA
		$V_{GS} = -16 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$	-	-	100	nA
R_{DSon}	drain-source on-state resistance	$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 25 \text{ }^\circ C$	-	0.62	0.68	m Ω
		$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 150 \text{ }^\circ C$	-	-	1.29	m Ω
		$V_{GS} = 7 \text{ V}; I_D = 25 \text{ A}; T_j = 25 \text{ }^\circ C$	-	0.75	1	m Ω
		$V_{GS} = 7 \text{ V}; I_D = 25 \text{ A}; T_j = 150 \text{ }^\circ C$	-	-	1.83	m Ω
R_G	gate resistance	$f = 1 \text{ MHz}; T_j = 25 \text{ }^\circ C$	[tbd]	[tbd]	[tbd]	Ω
Dynamic characteristics						
$Q_{G(tot)}$	total gate charge	$I_D = 25 \text{ A}; V_{DS} = 15 \text{ V}; V_{GS} = 4.5 \text{ V}$	[tbd]	[tbd]	[tbd]	nC
		$I_D = 25 \text{ A}; V_{DS} = 15 \text{ V}; V_{GS} = 10 \text{ V}$	[tbd]	[tbd]	[tbd]	nC
		$I_D = 0 \text{ A}; V_{DS} = 0 \text{ V}; V_{GS} = 10 \text{ V}$	-	[tbd]	-	nC
Q_{GS}	gate-source charge	$I_D = 25 \text{ A}; V_{DS} = 15 \text{ V}; V_{GS} = 4.5 \text{ V}$	[tbd]	[tbd]	[tbd]	nC
$Q_{GS(th)}$	pre-threshold gate-source charge		[tbd]	[tbd]	[tbd]	nC
$Q_{GS(th-pl)}$	post-threshold gate-source charge		[tbd]	[tbd]	[tbd]	nC
Q_{GD}	gate-drain charge		[tbd]	[tbd]	[tbd]	nC
$V_{GS(pl)}$	gate-source plateau voltage	$I_D = 25 \text{ A}; V_{DS} = 15 \text{ V}$	-	[tbd]	-	V
C_{iss}	input capacitance	$V_{DS} = 15 \text{ V}; V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}; T_j = 25 \text{ }^\circ C$	[tbd]	[tbd]	[tbd]	pF
C_{oss}	output capacitance		[tbd]	[tbd]	[tbd]	pF
C_{rss}	reverse transfer capacitance		[tbd]	[tbd]	[tbd]	pF

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Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{d(on)}$	turn-on delay time	$V_{DS} = 15\text{ V}; R_L = 0.6\ \Omega; V_{GS} = 4.5\text{ V}; R_{G(ext)} = 5\ \Omega$	-	[tbd]	-	ns
t_r	rise time		-	[tbd]	-	ns
$t_{d(off)}$	turn-off delay time		-	[tbd]	-	ns
t_f	fall time		-	[tbd]	-	ns
Q_{oss}	output charge	$V_{GS} = 0\text{ V}; V_{DS} = 15\text{ V}; f = 1\text{ MHz}; T_j = 25\text{ }^\circ\text{C}$	-	[tbd]	-	nC

Source-drain diode

V_{SD}	source-drain voltage	$I_S = 25\text{ A}; V_{GS} = 0\text{ V}; T_j = 25\text{ }^\circ\text{C}$	-	[tbd]	1	V	
t_{rr}	reverse recovery time	$I_S = 25\text{ A}; di_S/dt = -100\text{ A}/\mu\text{s}; V_{GS} = 0\text{ V}; V_{DS} = 15\text{ V};$ Fig. 3	-	[tbd]	-	ns	
Q_r	recovered charge		[1]	-	[tbd]	-	nC
t_a	reverse recovery rise time		-	[tbd]	-	ns	
t_b	reverse recovery fall time		-	[tbd]	-	ns	
S	softness factor		-	[tbd]	-		

[1] includes capacitive recovery

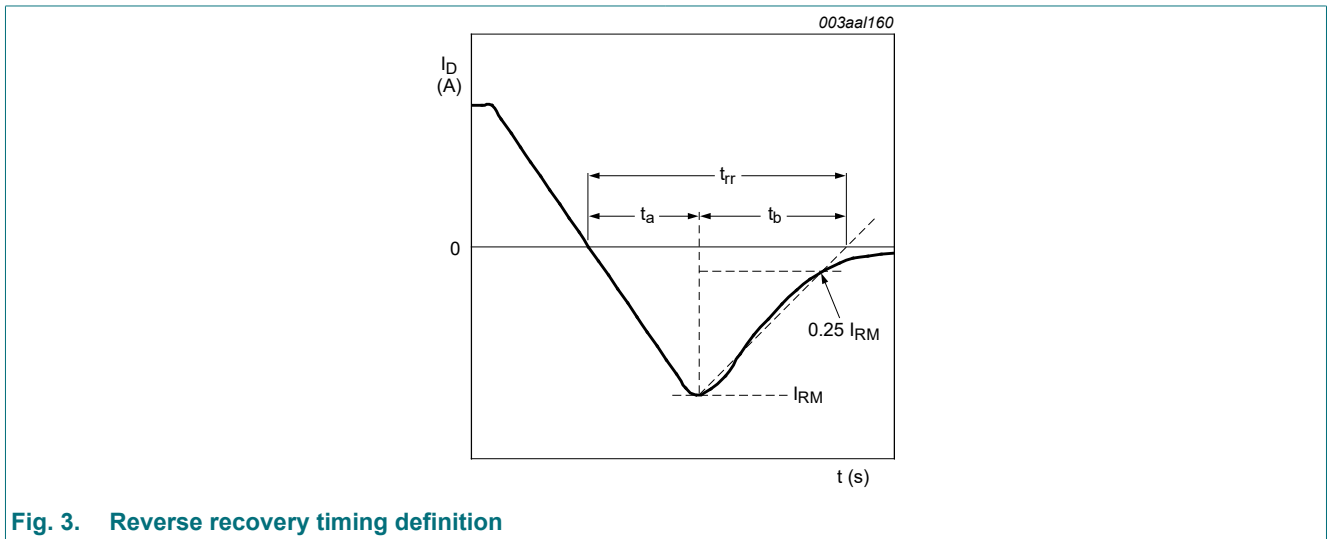


Fig. 3. Reverse recovery timing definition

11. Package outline

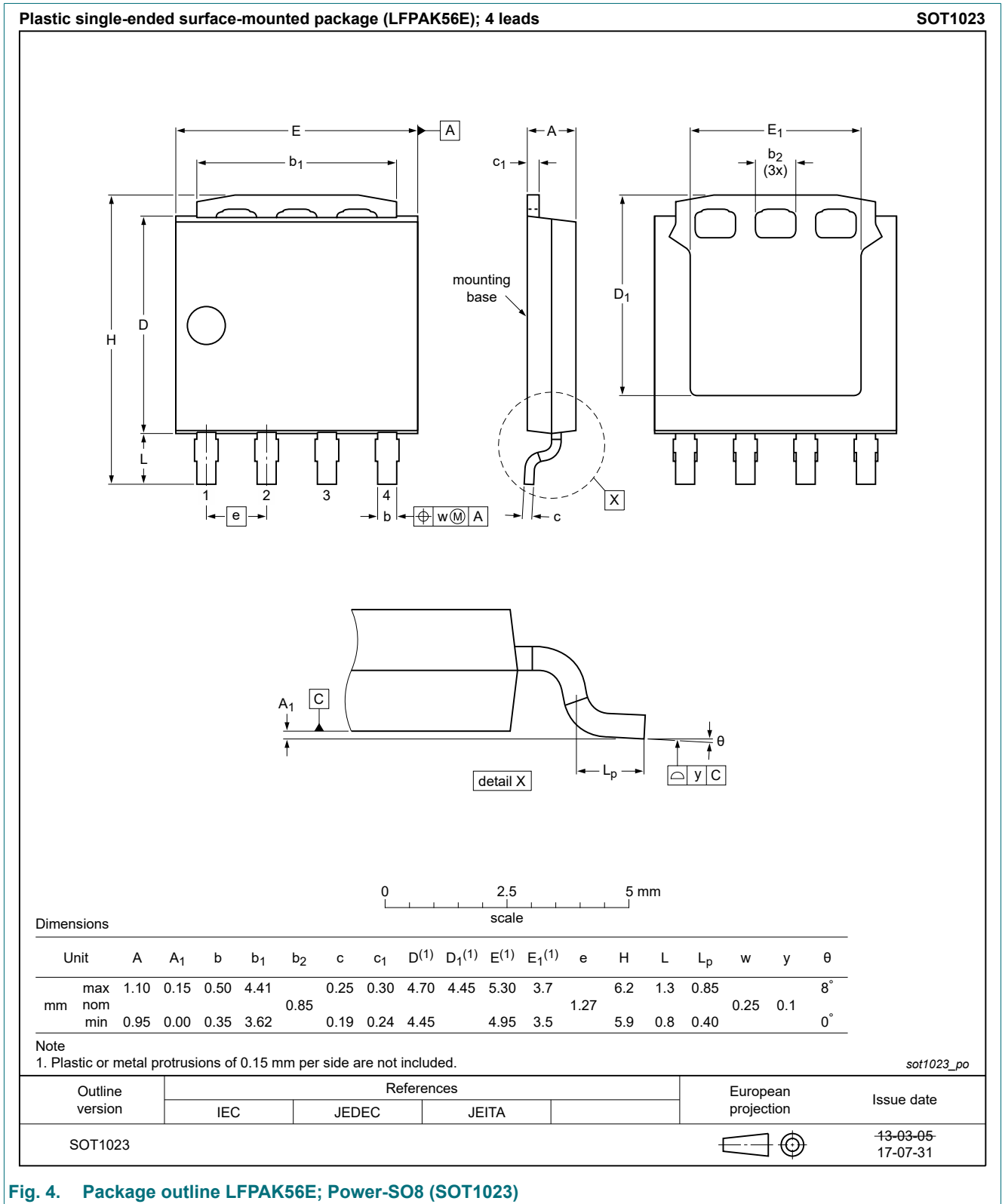


Fig. 4. Package outline LPAK56E; Power-SO8 (SOT1023)

12. Soldering

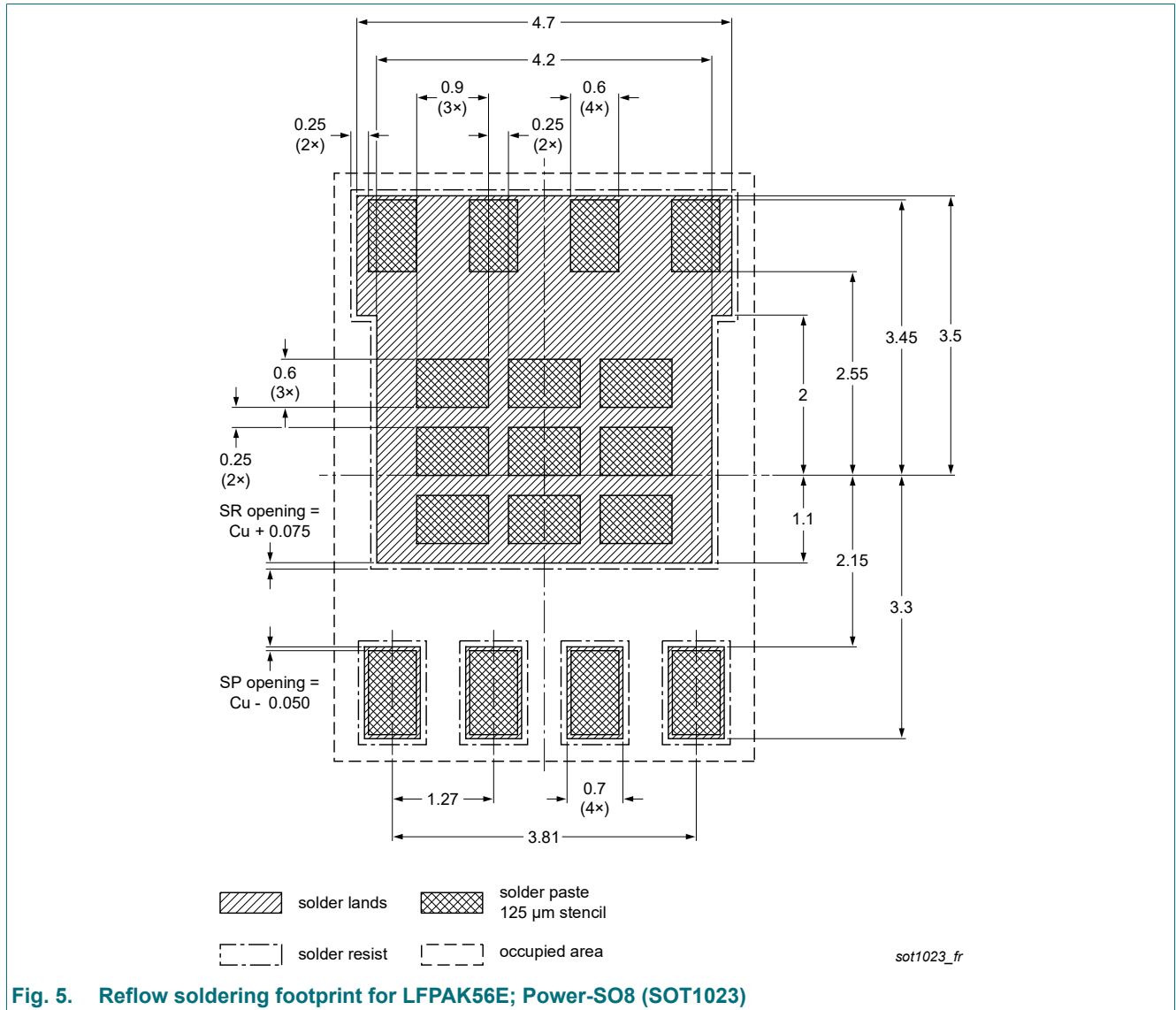


Fig. 5. Reflow soldering footprint for LPAK56E; Power-SO8 (SOT1023)

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Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
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