



# PSMN4R8-100YSE

N-channel 100 V, 4.8 mOhm, SuperSOA MOSFET in LFAK56E

2 October 2020

Objective data sheet

## 1. General description

SuperSOA N-channel enhancement mode MOSFET in a LFAK56E package qualified to 175 °C. Part of Nexperia's "NextPower Live" portfolio, the PSMN4R8-100YSE delivers very low  $R_{DS(on)}$  and a very strong linear-mode (SOA) performance in a high-reliability copper-clip LFAK56E package. PSMN4R8-100YSE complements the latest "hot-swap" controllers – robust enough to withstand substantial inrush currents during turn-on, low  $R_{DS(on)}$  to minimize  $I^2R$  losses and deliver optimum efficiency when turned fully ON.

## 2. Features and benefits

- Fully optimized Safe Operating Area (SOA) for superior linear mode operation
- Low  $R_{DS(on)}$  for low  $I^2R$  conduction losses
- LFAK56E package for applications that demand the highest performance and reliability in a 30 mm<sup>2</sup> footprint

## 3. Applications

- Hot swap
- Load switch
- Soft start
- E-fuse
- Telecommunication systems based on a 48 V backplane/supply rail

## 4. Quick reference data

Table 1. Quick reference data

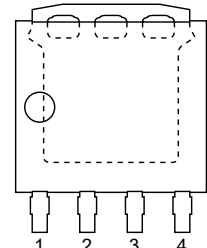
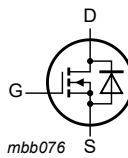
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{DS}$	drain-source voltage	$25\text{ °C} \leq T_j \leq 175\text{ °C}$	-	-	100	V
$I_D$	drain current	$V_{GS} = 10\text{ V}; T_{mb} = 25\text{ °C}; \text{Fig. 2}$	-	-	120	A
$P_{tot}$	total power dissipation	$T_{mb} = 25\text{ °C}; \text{Fig. 1}$	-	-	294	W
$T_j$	junction temperature		-55	-	175	°C
<b>Static characteristics</b>						
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}; I_D = 25\text{ A}; T_j = 25\text{ °C}$	-	3.6	4.8	mΩ
		$V_{GS} = 10\text{ V}; I_D = 25\text{ A}; T_j = 175\text{ °C}; \text{Fig. 7}$	-	8	11	mΩ
<b>Dynamic characteristics</b>						
$Q_{GD}$	gate-drain charge	$I_D = 25\text{ A}; V_{DS} = 50\text{ V}; V_{GS} = 10\text{ V}; T_j = 25\text{ °C}; \text{Fig. 8}; \text{Fig. 9}$	[tbd]	16	[tbd]	nC
$Q_{G(tot)}$	total gate charge		[tbd]	80	[tbd]	nC
<b>Avalanche ruggedness</b>						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$I_D = 52.6\text{ A}; V_{sup} \leq 100\text{ V}; R_{GS} = 50\text{ Ω}; V_{GS} = 10\text{ V}; T_{j(init)} = 25\text{ °C}; \text{unclamped}; \text{Fig. 4}$	[1]	-	325	mJ

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Source-drain diode</b>						
$Q_r$	recovered charge	$I_S = 25 \text{ A}$ ; $di_S/dt = -100 \text{ A}/\mu\text{s}$ ; $V_{GS} = 0 \text{ V}$ ; $V_{DS} = 50 \text{ V}$ ; $T_j = 25 \text{ }^\circ\text{C}$ ; <a href="#">Fig. 11</a>	-	44	-	nC

[1] Protected by 100% test

## 5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source	 <p>LPAK56E; Power-SO8 (SOT1023)</p>	 <p>mbb076</p>
2	S	source		
3	S	source		
4	G	gate		
mb	D	mounting base; connected to drain		

## 6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PSMN4R8-100YSE	LPAK56E; Power-SO8	plastic, single-ended surface-mounted package (LPAK56); 4 leads; 1.27 mm pitch	SOT1023

## 7. Limiting values

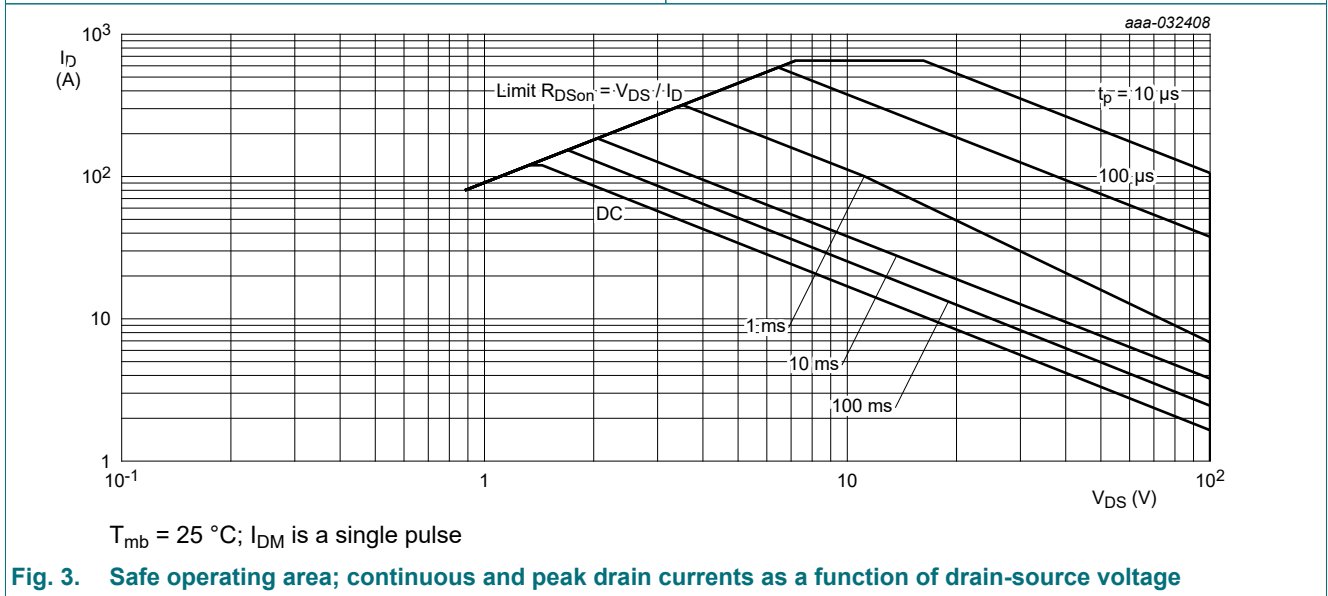
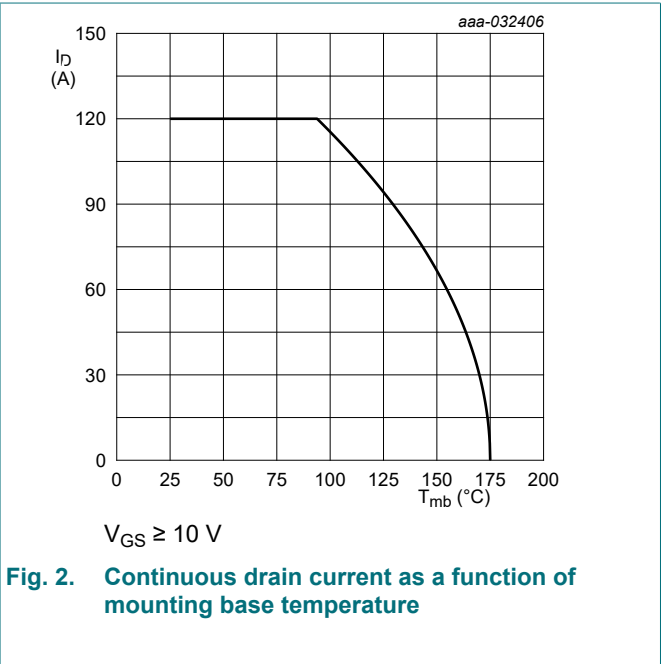
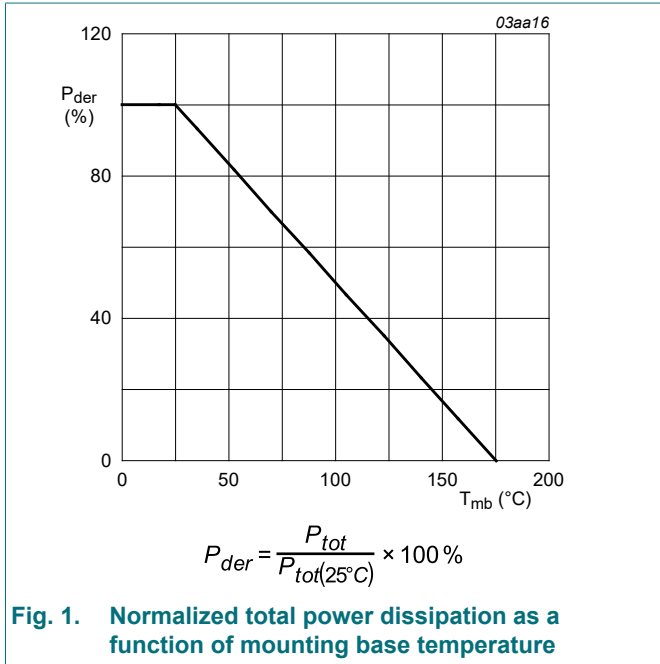
Table 4. Limiting values

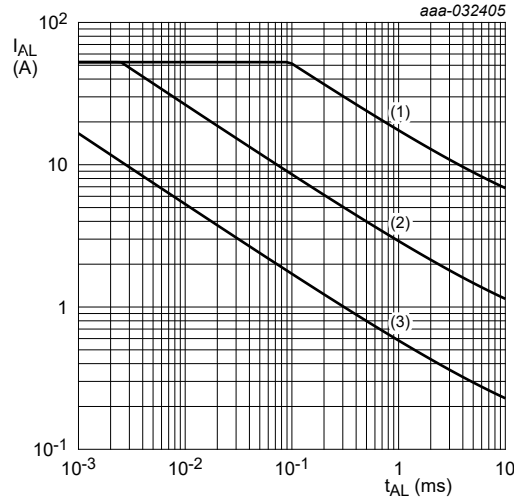
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DS}$	drain-source voltage	$25 \text{ }^\circ\text{C} \leq T_j \leq 175 \text{ }^\circ\text{C}$	-	100	V
$V_{DGR}$	drain-gate voltage	$25 \text{ }^\circ\text{C} \leq T_j \leq 175 \text{ }^\circ\text{C}$ ; $R_{GS} = 20 \text{ k}\Omega$	-	100	V
$V_{GS}$	gate-source voltage		-20	20	V
$P_{tot}$	total power dissipation	$T_{mb} = 25 \text{ }^\circ\text{C}$ ; <a href="#">Fig. 1</a>	-	294	W
$I_D$	drain current	$V_{GS} = 10 \text{ V}$ ; $T_{mb} = 25 \text{ }^\circ\text{C}$ ; <a href="#">Fig. 2</a>	-	120	A
		$V_{GS} = 10 \text{ V}$ ; $T_{mb} = 100 \text{ }^\circ\text{C}$ ; <a href="#">Fig. 2</a>	-	115	A
$I_{DM}$	peak drain current	pulsed; $t_p \leq 10 \text{ }\mu\text{s}$ ; $T_{mb} = 25 \text{ }^\circ\text{C}$ ; <a href="#">Fig. 3</a>	-	653	A
$T_{stg}$	storage temperature		-55	175	$^\circ\text{C}$
$T_j$	junction temperature		-55	175	$^\circ\text{C}$
$T_{sld(M)}$	peak soldering temperature		-	260	$^\circ\text{C}$
<b>Source-drain diode</b>					
$I_S$	source current	$T_{mb} = 25 \text{ }^\circ\text{C}$	-	120	A
$I_{SM}$	peak source current	pulsed; $t_p \leq 10 \text{ }\mu\text{s}$ ; $T_{mb} = 25 \text{ }^\circ\text{C}$	-	653	A

Symbol	Parameter	Conditions	Min	Max	Unit	
<b>Avalanche ruggedness</b>						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$I_D = 52.6 \text{ A}$ ; $V_{sup} \leq 100 \text{ V}$ ; $R_{GS} = 50 \Omega$ ; $V_{GS} = 10 \text{ V}$ ; $T_{j(\text{init})} = 25 \text{ }^\circ\text{C}$ ; unclamped; <a href="#">Fig. 4</a>	[1]	-	325	mJ
$I_{AS}$	non-repetitive avalanche current	$V_{sup} = 100 \text{ V}$ ; $V_{GS} = 10 \text{ V}$ ; $T_{j(\text{init})} = 25 \text{ }^\circ\text{C}$ ; $R_{GS} = 50 \Omega$ ; <a href="#">Fig. 4</a>	[1]	-	52.6	A

[1] Protected by 100% test





(1)  $T_{j\text{(init)}} = 25\text{ °C}$ ; (2)  $T_{j\text{(init)}} = 150\text{ °C}$ ; (3) Repetitive Avalanche

Fig. 4. Avalanche rating; avalanche current as a function of avalanche time

## 8. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 5	-	0.45	0.51	K/W

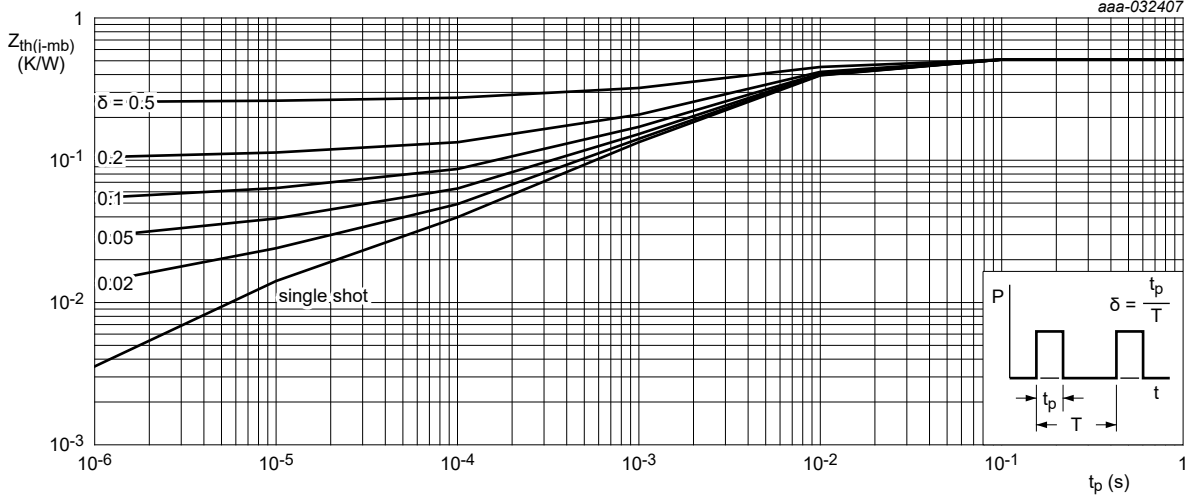


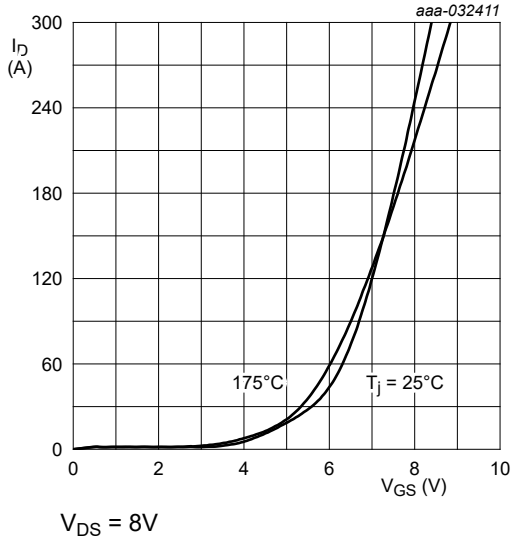
Fig. 5. Transient thermal impedance from junction to mounting base as a function of pulse duration

## 9. Characteristics

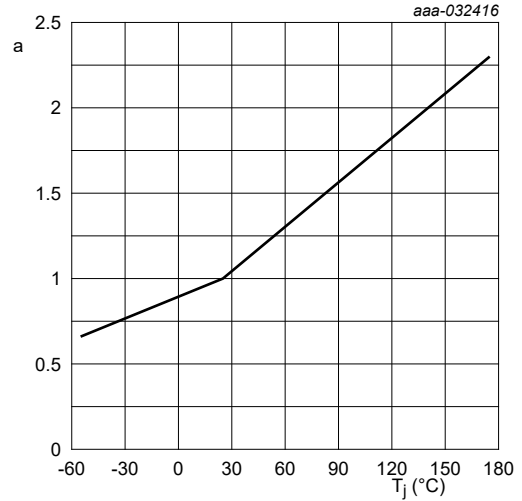
Table 6. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics</b>						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250\text{ }\mu\text{A}$ ; $V_{GS} = 0\text{ V}$ ; $T_j = 25\text{ °C}$	100	-	-	V
		$I_D = 250\text{ }\mu\text{A}$ ; $V_{GS} = 0\text{ V}$ ; $T_j = -55\text{ °C}$	90	-	-	V

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{DS}=V_{GS}; T_j = 25 \text{ }^\circ\text{C}$	2	2.6	4	V
		$I_D = 1 \text{ mA}; V_{DS}=V_{GS}; T_j = 175 \text{ }^\circ\text{C}$	-	1.4	-	V
		$I_D = 1 \text{ mA}; V_{DS}=V_{GS}; T_j = -55 \text{ }^\circ\text{C}$	-	3	-	V
$\Delta V_{GS(th)}/\Delta T$	gate-source threshold voltage variation with temperature	$25 \text{ }^\circ\text{C} \leq T_j \leq 150 \text{ }^\circ\text{C}$	-	[tbd]	-	mV/K
$I_{DSS}$	drain leakage current	$V_{DS} = 100 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	0.03	1	$\mu\text{A}$
		$V_{DS} = 100 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 175 \text{ }^\circ\text{C}$	-	-	500	$\mu\text{A}$
$I_{GSS}$	gate leakage current	$V_{GS} = 20 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	2	100	nA
		$V_{GS} = -20 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	2	100	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 25 \text{ }^\circ\text{C}$	-	3.6	4.8	m $\Omega$
		$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 100 \text{ }^\circ\text{C};$ <a href="#">Fig. 7</a>	-	5.6	7.7	m $\Omega$
		$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 175 \text{ }^\circ\text{C};$ <a href="#">Fig. 7</a>	-	8	11	m $\Omega$
$R_G$	gate resistance	$f = 1 \text{ MHz}; T_j = 25 \text{ }^\circ\text{C}$	[tbd]	0.8	[tbd]	$\Omega$
<b>Dynamic characteristics</b>						
$Q_{G(tot)}$	total gate charge	$I_D = 25 \text{ A}; V_{DS} = 50 \text{ V}; V_{GS} = 10 \text{ V};$ $T_j = 25 \text{ }^\circ\text{C};$ <a href="#">Fig. 8; Fig. 9</a>	[tbd]	80	[tbd]	nC
		$I_D = 0 \text{ A}; V_{DS} = 0 \text{ V}; V_{GS} = 10 \text{ V};$ $T_j = 25 \text{ }^\circ\text{C}$	-	42.4	-	nC
$Q_{GS}$	gate-source charge	$I_D = 25 \text{ A}; V_{DS} = 50 \text{ V}; V_{GS} = 10 \text{ V};$ $T_j = 25 \text{ }^\circ\text{C};$ <a href="#">Fig. 8; Fig. 9</a>	[tbd]	28.3	[tbd]	nC
$Q_{GS(th)}$	pre-threshold gate-source charge		-	15.3	-	nC
$Q_{GS(th-pl)}$	post-threshold gate-source charge		-	13	-	nC
$Q_{GD}$	gate-drain charge		[tbd]	16	[tbd]	nC
$V_{GS(pl)}$	gate-source plateau voltage	$I_D = 25 \text{ A}; V_{DS} = 50 \text{ V}; T_j = 25 \text{ }^\circ\text{C};$ <a href="#">Fig. 8; Fig. 9</a>	-	5.5	-	V
$C_{iss}$	input capacitance	$V_{DS} = 50 \text{ V}; V_{GS} = 0 \text{ V}; f = 1 \text{ MHz};$ $T_j = 25 \text{ }^\circ\text{C};$ <a href="#">Fig. 10</a>	[tbd]	5662	[tbd]	pF
$C_{oss}$	output capacitance		[tbd]	1313	[tbd]	pF
$C_{rss}$	reverse transfer capacitance		[tbd]	23	[tbd]	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 50 \text{ V}; R_L = 2 \text{ }^\circ\Omega; V_{GS} = 10 \text{ V};$ $R_{G(ext)} = 5 \text{ }^\circ\Omega; T_j = 25 \text{ }^\circ\text{C}$	-	22	-	ns
$t_r$	rise time		-	18	-	ns
$t_{d(off)}$	turn-off delay time		-	45	-	ns
$t_f$	fall time		-	23	-	ns
<b>Source-drain diode</b>						
$V_{SD}$	source-drain voltage	$I_S = 25 \text{ A}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	0.82	1.2	V
$t_{rr}$	reverse recovery time	$I_S = 25 \text{ A}; di_S/dt = -100 \text{ A}/\mu\text{s}; V_{GS} = 0 \text{ V};$ $V_{DS} = 50 \text{ V}; T_j = 25 \text{ }^\circ\text{C};$ <a href="#">Fig. 11</a>	-	43	-	ns
$Q_r$	recovered charge		-	44	-	nC

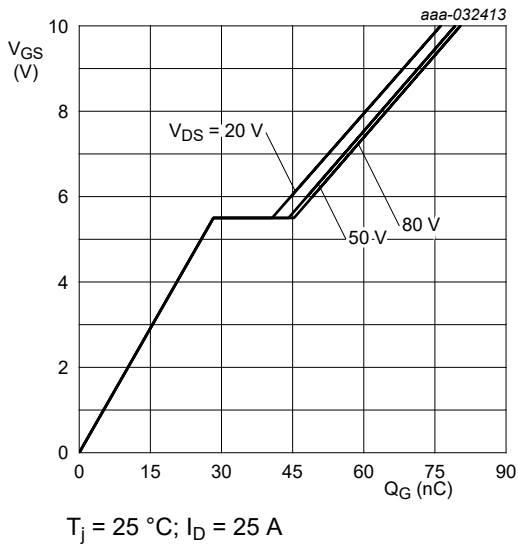


**Fig. 6. Transfer characteristics; drain current as a function of gate-source voltage; typical values**

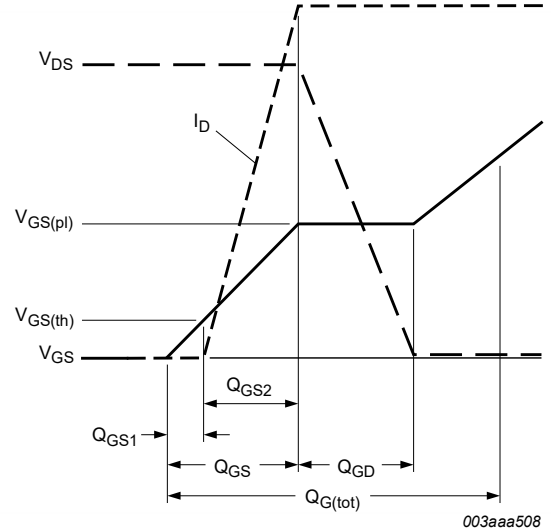


$$a = \frac{R_{DSon}}{R_{DSon}(25^{\circ}\text{C})}$$

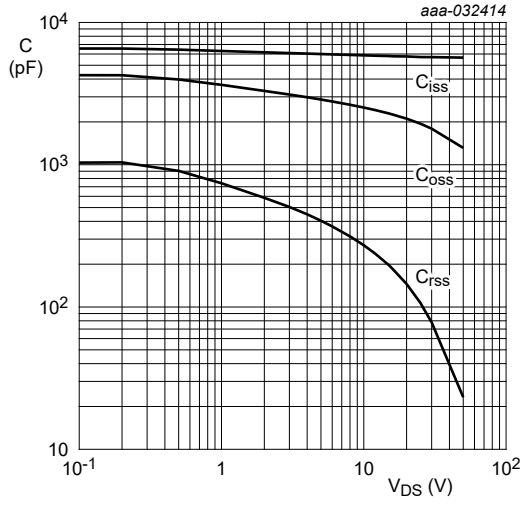
**Fig. 7. Normalized drain-source on-state resistance factor as a function of junction temperature**



**Fig. 8. Gate-source voltage as a function of gate charge; typical values**

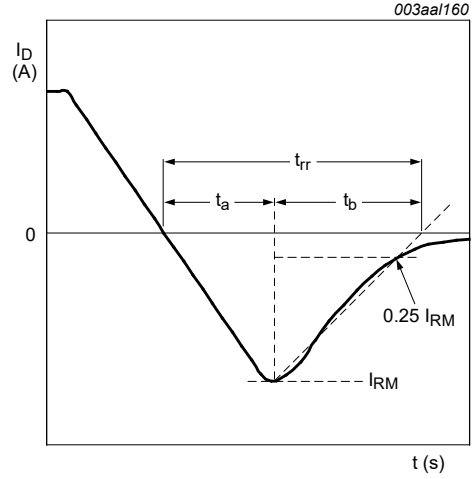


**Fig. 9. Gate charge waveform definitions**



$V_{GS} = 0$  V;  $f = 1$  MHz

**Fig. 10. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values**



**Fig. 11. Reverse recovery timing definition**

10. Package outline

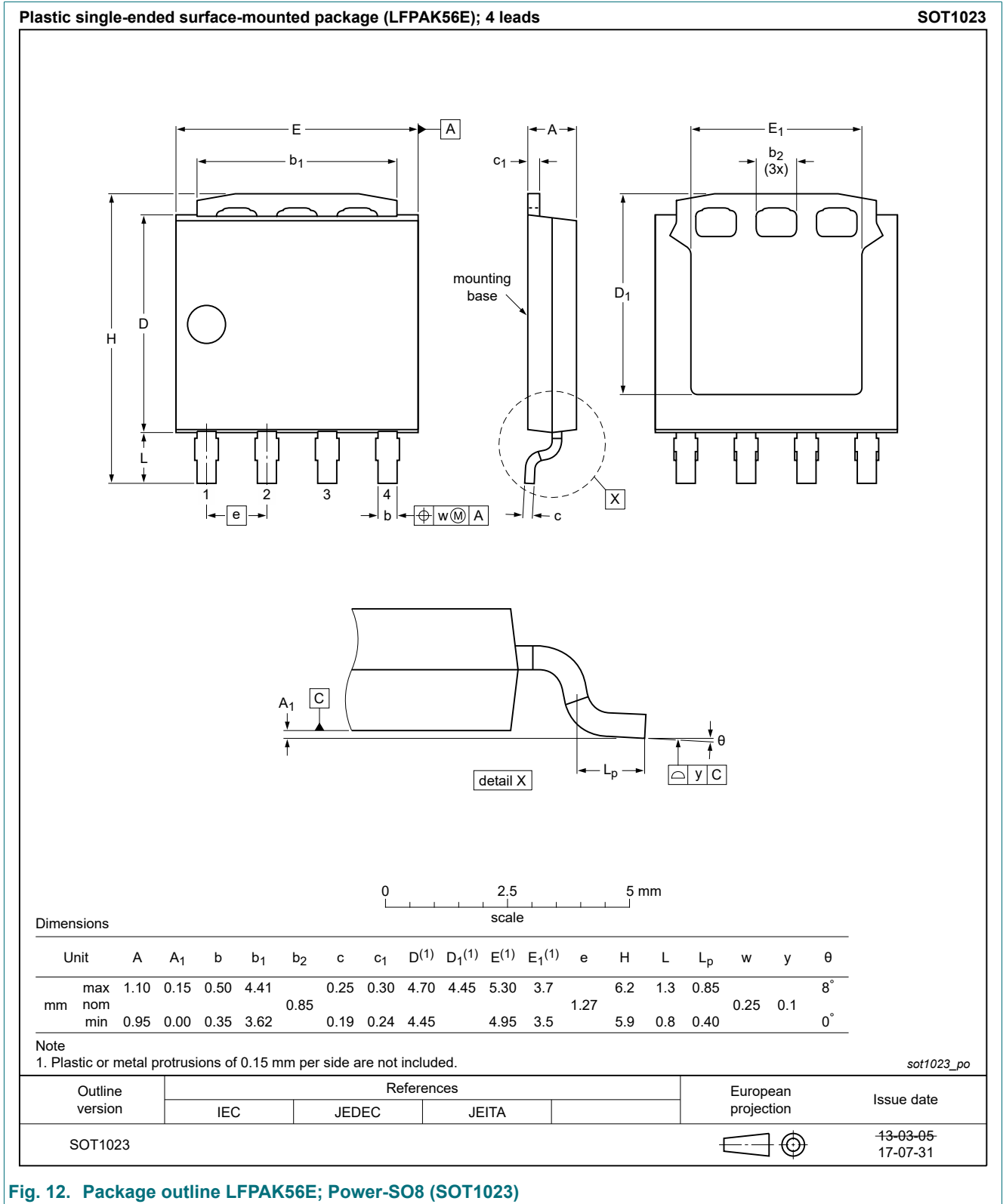


Fig. 12. Package outline LPAK56E; Power-SO8 (SOT1023)

### 11. Soldering

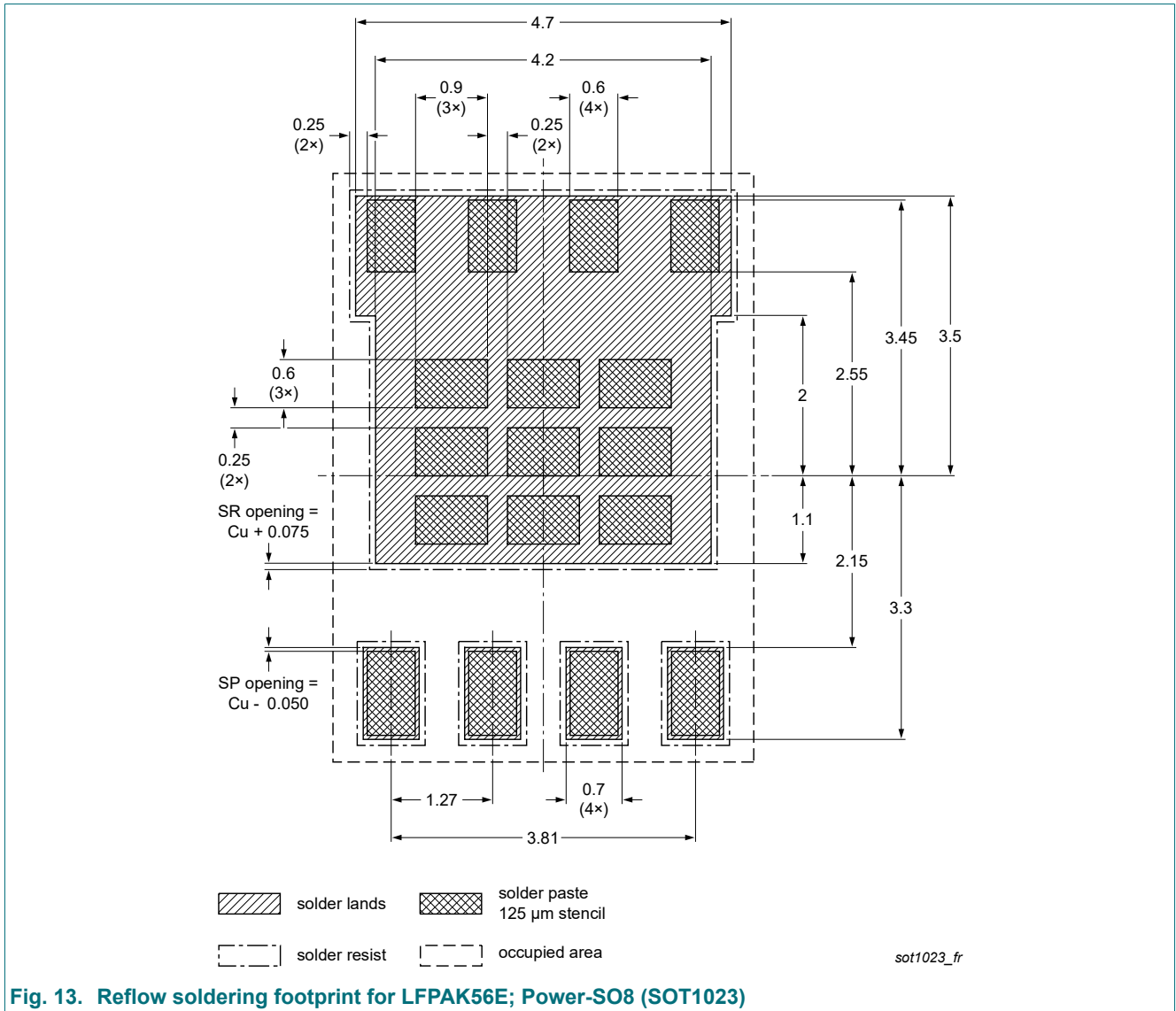


Fig. 13. Reflow soldering footprint for LPAK56E; Power-SO8 (SOT1023)

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Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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