
# PSMN4R2-80YSE

**N-channel 80 V, 4.2 mOhm, SuperSOA MOSFET in LFPAK56E**

**14 October 2020** **Objective data sheet**

## 1. General description

SuperSOA N-channel enhancement mode MOSFET in a LFPAK56E package qualified to 175 °C. Part of Nexperia's "NextPower Live" portfolio, the PSMN4R2-80YSE delivers very low $R_{DSon}$ and a very strong linear-mode (SOA) performance in a high-reliability copper-clip LFPAK56E package.

PSMN4R2-80YSE complements the latest "hot-swap" controllers – robust enough to withstand substantial inrush currents during turn-on, low $R_{DSon}$ to minimize $I^2R$ losses and deliver optimum efficiency when turned fully ON.

## 2. Features and benefits

- Fully optimized Safe Operating Area (SOA) for superior linear mode operation
- Low $R_{DSon}$ for low $I^2R$ conduction losses
- LFPAK56E package for applications that demand the highest performance and reliability in a 30 $mm^2$ footprint

## 3. Applications

- Hot swap
- Load switch
- Soft start
- E-fuse
- Telecommunication systems based on a 48 V backplane/supply rail

## 4. Quick reference data

**Table 1. Quick reference data**

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $V_{DS}$ | drain-source voltage | 25 °C ≤ $T_j$ ≤ 175 °C | | - | - | 80 | V |
| $I_D$ | drain current | $V_{GS}$ = 10 V; $T_{mb}$ = 25 °C; Fig. 2 | | - | - | 120 | A |
| $P_{tot}$ | total power dissipation | $T_{mb}$ = 25 °C; Fig. 1 | | - | - | 294 | W |
| $T_j$ | junction temperature | | | -55 | - | 175 | °C |
| **Static characteristics** | | | | | | | |
| $R_{DSon}$ | drain-source on-state resistance | $V_{GS}$ = 10 V; $I_D$ = 25 A; $T_j$ = 25 °C | | [tbd] | 3.4 | 4.2 | mΩ |
| | | $V_{GS}$ = 10 V; $I_D$ = 25 A; $T_j$ = 175 °C | | [tbd] | 7.3 | 9.2 | mΩ |
| **Dynamic characteristics** | | | | | | | |
| $Q_{GD}$ | gate-drain charge | $I_D$ = 25 A; $V_{DS}$ = 40 V; $V_{GS}$ = 10 V; $T_j$ = 25 °C; Fig. 6 | | [tbd] | 13 | [tbd] | nC |
| $Q_{G(tot)}$ | total gate charge | | | [tbd] | 73 | [tbd] | nC |
| **Avalanche ruggedness** | | | | | | | |
| $E_{DS(AL)S}$ | non-repetitive drain-source avalanche energy | $I_D$ = 57 A; $V_{sup}$ ≤ 80 V; $R_{GS}$ = 50 Ω; $V_{GS}$ = 10 V; $T_{j(init)}$ = 25 °C; unclamped; Fig. 4 | [1] | - | - | 372 | mJ |

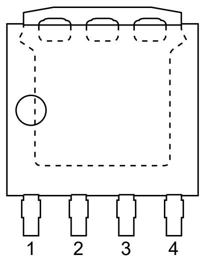
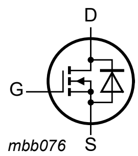
nexperia

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| **Source-drain diode** | | | | | | | |
| $Q_r$ | recovered charge | $I_S$ = 25 A; $dI_S/dt$ = -100 A/µs; $V_{GS}$ = 0 V; $V_{DS}$ = 40 V; $T_j$ = 25 °C; Fig. 7 | [2] | - | 44 | - | nC |

[1] Protected by 100% test
[2] includes capacitive recovery

## 5. Pinning information

**Table 2. Pinning information**

| Pin | Symbol | Description | Simplified outline | Graphic symbol |
|---|---|---|---|---|
| 1 | S | source |  **LFPAK56E; Power-SO8 (SOT1023)** |  |
| 2 | S | source | | |
| 3 | S | source | | |
| 4 | G | gate | | |
| mb | D | mounting base; connected to drain | | |

## 6. Ordering information

**Table 3. Ordering information**

| Type number | Package | | |
|---|---|---|---|
| | Name | Description | Version |
| PSMN4R2-80YSE | LFPAK56E; Power-SO8 | plastic, single-ended surface-mounted package (LFPAK56); 4 leads; 1.27 mm pitch | SOT1023 |

## 7. Limiting values

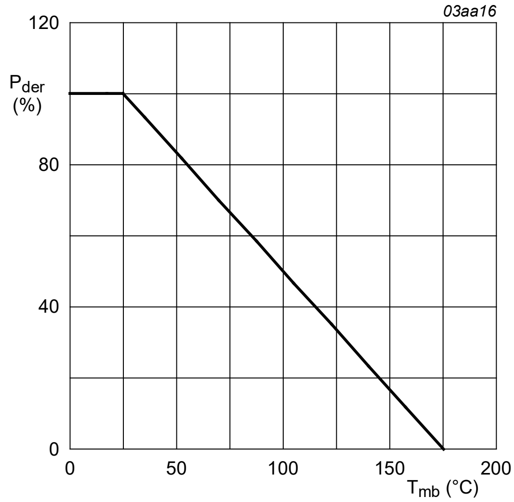
**Table 4. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134).*

| Symbol | Parameter | Conditions | | Min | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{DS}$ | drain-source voltage | 25 °C ≤ $T_j$ ≤ 175 °C | | - | 80 | V |
| $V_{DGR}$ | drain-gate voltage | 25 °C ≤ $T_j$ ≤ 175 °C; $R_{GS}$ = 20 kΩ | | - | 80 | V |
| $V_{GS}$ | gate-source voltage | | | -20 | 20 | V |
| $P_{tot}$ | total power dissipation | $T_{mb}$ = 25 °C; Fig. 1 | | - | 294 | W |
| $I_D$ | drain current | $V_{GS}$ = 10 V; $T_{mb}$ = 25 °C; Fig. 2 | | - | 120 | A |
| | | $V_{GS}$ = 10 V; $T_{mb}$ = 100 °C; Fig. 2 | | - | 120 | A |
| $I_{DM}$ | peak drain current | pulsed; $t_p$ ≤ 10 µs; $T_{mb}$ = 25 °C; Fig. 3 | | - | 698 | A |
| $T_{stg}$ | storage temperature | | | -55 | 175 | °C |
| $T_j$ | junction temperature | | | -55 | 175 | °C |
| $T_{sld(M)}$ | peak soldering temperature | | | - | 260 | °C |
| **Source-drain diode** | | | | | | |
| $I_S$ | source current | $T_{mb}$ = 25 °C | | - | 120 | A |

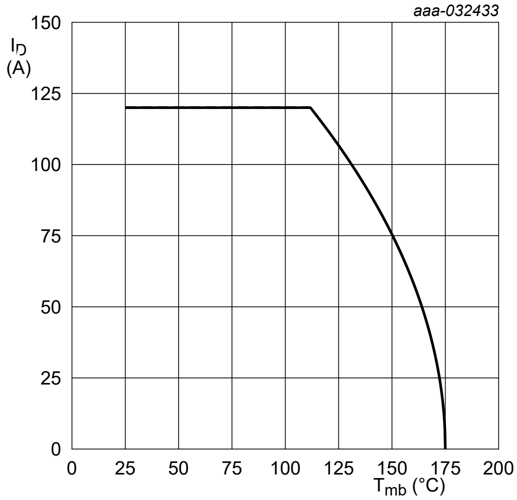
| Symbol | Parameter | Conditions | | Min | Max | Unit |
|---|---|---|---|---|---|---|
| $I_{SM}$ | peak source current | pulsed; $t_p \leq$ 10 μs; $T_{mb}$ = 25 °C | | - | 698 | A |
| **Avalanche ruggedness** | | | | | | |
| $E_{DS(AL)S}$ | non-repetitive drain-source avalanche energy | $I_D$ = 57 A; $V_{sup} \leq$ 80 V; $R_{GS}$ = 50 Ω; $V_{GS}$ = 10 V; $T_{j(init)}$ = 25 °C; unclamped; Fig. 4 | [1] | - | 372 | mJ |
| $I_{AS}$ | non-repetitive avalanche current | $V_{sup}$ = 80 V; $V_{GS}$ = 10 V; $T_{j(init)}$ = 25 °C; $R_{GS}$ = 50 Ω; Fig. 4 | [1] | - | 57 | A |

[1] Protected by 100% test



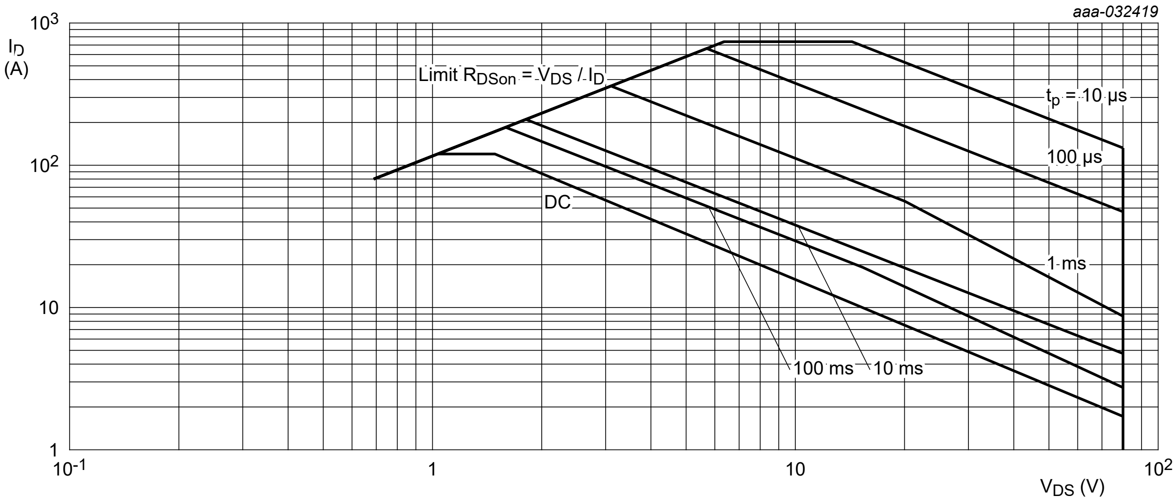

$$P_{der} = \frac{P_{tot}}{P_{tot(25°C)}} \times 100\,\%$$

**Fig. 1. Normalized total power dissipation as a function of mounting base temperature**



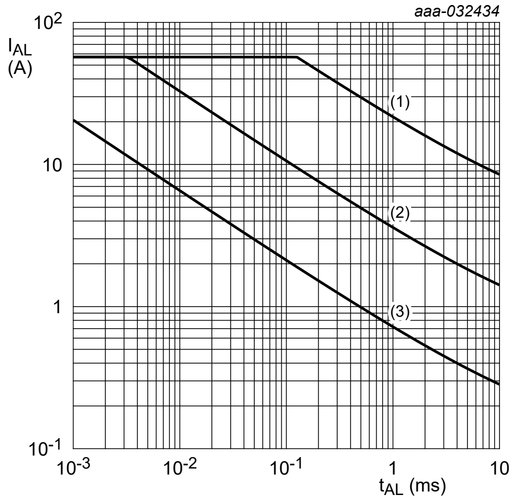

$V_{GS} \geq 10$ V

**Fig. 2. Continuous drain current as a function of mounting base temperature**




$T_{mb}$ = 25 °C; $I_{DM}$ is a single pulse

**Fig. 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage**




(1) $T_{j\ (init)}$ = 25 °C; (2) $T_{j\ (init)}$ = 150 °C; (3) Repetitive Avalanche

**Fig. 4. Avalanche rating; avalanche current as a function of avalanche time**

## 8. Thermal characteristics

**Table 5. Thermal characteristics**

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $R_{th(j-mb)}$ | thermal resistance from junction to mounting base | Fig. 5 | | - | 0.45 | 0.51 | K/W |

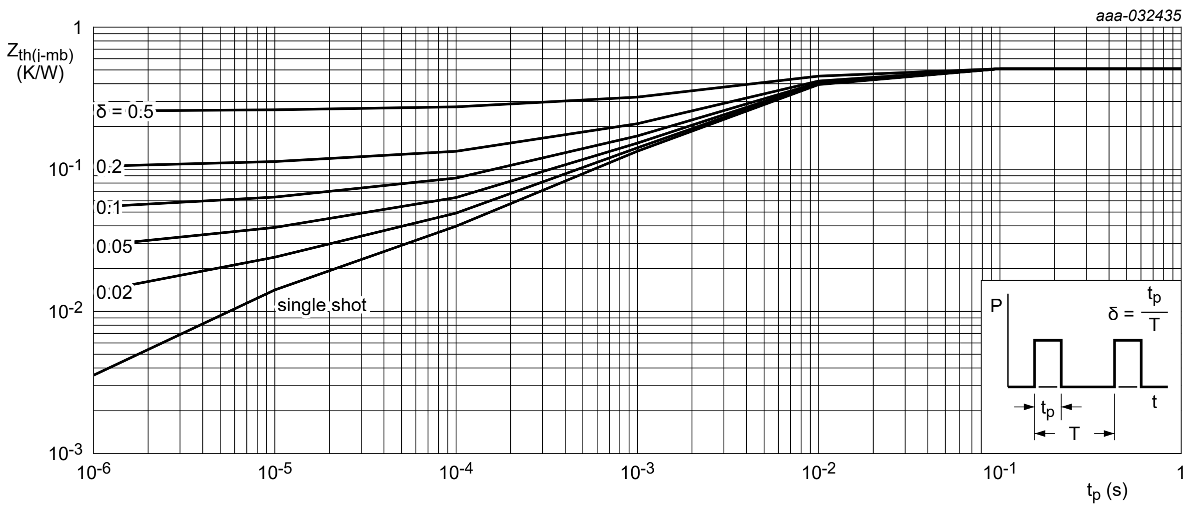



**Fig. 5. Transient thermal impedance from junction to mounting base as a function of pulse duration**

## 9. Characteristics

**Table 6. Characteristics**

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| **Static characteristics** | | | | | | | |
| $V_{(BR)DSS}$ | drain-source breakdown voltage | $I_D$ = 250 µA; $V_{GS}$ = 0 V; $T_j$ = 25 °C | | 80 | - | - | V |
| | | $I_D$ = 250 µA; $V_{GS}$ = 0 V; $T_j$ = -55 °C | | 72 | - | - | V |

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $V_{GS(th)}$ | gate-source threshold voltage | $I_D$ = 1 mA; $V_{DS}$=$V_{GS}$; $T_j$ = 25 °C | | 2 | 3 | 4 | V |
| | | $I_D$ = 1 mA; $V_{DS}$=$V_{GS}$; $T_j$ = 175 °C | | - | 1.9 | - | V |
| | | $I_D$ = 1 mA; $V_{DS}$=$V_{GS}$; $T_j$ = -55 °C | | - | 3.5 | - | V |
| $\Delta V_{GS(th)}/\Delta T$ | gate-source threshold voltage variation with temperature | 25 °C ≤ $T_j$ ≤ 150 °C | | - | [tbd] | - | mV/K |
| $I_{DSS}$ | drain leakage current | $V_{DS}$ = 80 V; $V_{GS}$ = 0 V; $T_j$ = 25 °C | | - | [tbd] | 25 | µA |
| | | $V_{DS}$ = 80 V; $V_{GS}$ = 0 V; $T_j$ = 125 °C | | - | [tbd] | [tbd] | µA |
| $I_{GSS}$ | gate leakage current | $V_{GS}$ = 20 V; $V_{DS}$ = 0 V; $T_j$ = 25 °C | | - | 2 | 100 | nA |
| | | $V_{GS}$ = -20 V; $V_{DS}$ = 0 V; $T_j$ = 25 °C | | - | 2 | 100 | nA |
| $R_{DSon}$ | drain-source on-state resistance | $V_{GS}$ = 10 V; $I_D$ = 25 A; $T_j$ = 25 °C | | [tbd] | 3.4 | 4.2 | mΩ |
| | | $V_{GS}$ = 10 V; $I_D$ = 25 A; $T_j$ = 100 °C | | [tbd] | 5.1 | 6.4 | mΩ |
| | | $V_{GS}$ = 10 V; $I_D$ = 25 A; $T_j$ = 175 °C | | [tbd] | 7.3 | 9.2 | mΩ |
| | | $V_{GS}$ = 7 V; $I_D$ = 25 A; $T_j$ = 25 °C | | [tbd] | [tbd] | [tbd] | mΩ |
| $R_G$ | gate resistance | f = 1 MHz; $T_j$ = 25 °C | | - | [tbd] | - | Ω |
| **Dynamic characteristics** | | | | | | | |
| $Q_{G(tot)}$ | total gate charge | $I_D$ = 25 A; $V_{DS}$ = 40 V; $V_{GS}$ = 10 V; $T_j$ = 25 °C; Fig. 6 | | [tbd] | 73 | [tbd] | nC |
| | | $I_D$ = 0 A; $V_{DS}$ = 0 V; $V_{GS}$ = 10 V; $T_j$ = 25 °C; Fig. 6 | | - | [tbd] | - | nC |
| $Q_{GS}$ | gate-source charge | $I_D$ = 25 A; $V_{DS}$ = 40 V; $V_{GS}$ = 10 V; $T_j$ = 25 °C; Fig. 6 | | [tbd] | 22 | [tbd] | nC |
| $Q_{GS(th)}$ | pre-threshold gate-source charge | | | - | 15 | - | nC |
| $Q_{GS(th-pl)}$ | post-threshold gate-source charge | | | - | 7 | - | nC |
| $Q_{GD}$ | gate-drain charge | | | [tbd] | 13 | [tbd] | nC |
| $V_{GS(pl)}$ | gate-source plateau voltage | $V_{DS}$ = 40 V; $T_j$ = 25 °C; Fig. 6 | | - | 4.5 | - | V |
| $C_{iss}$ | input capacitance | $V_{DS}$ = 40 V; $V_{GS}$ = 0 V; f = 1 MHz; $T_j$ = 25 °C | | [tbd] | 5702 | [tbd] | pF |
| $C_{oss}$ | output capacitance | | | [tbd] | 1370 | [tbd] | pF |
| $C_{rss}$ | reverse transfer capacitance | | | [tbd] | 23 | [tbd] | pF |
| $t_{d(on)}$ | turn-on delay time | $V_{DS}$ = 40 V; $R_L$ = 1.6 Ω; $V_{GS}$ = 10 V; $R_{G(ext)}$ = 5 Ω; $T_j$ = 25 °C | | - | 21 | - | ns |
| $t_r$ | rise time | | | - | 17 | - | ns |
| $t_{d(off)}$ | turn-off delay time | | | - | 46 | - | ns |
| $t_f$ | fall time | | | - | 24 | - | ns |
| **Source-drain diode** | | | | | | | |
| $V_{SD}$ | source-drain voltage | $I_S$ = 25 A; $V_{GS}$ = 0 V; $T_j$ = 25 °C | | - | [tbd] | 1.2 | V |
| $t_{rr}$ | reverse recovery time | $I_S$ = 25 A; $dI_S/dt$ = -100 A/µs; $V_{GS}$ = 0 V; $V_{DS}$ = 40 V; $T_j$ = 25 °C; Fig. 7 | | - | 43 | - | ns |
| $Q_r$ | recovered charge | | [1] | - | 44 | - | nC |

[1] includes capacitive recovery

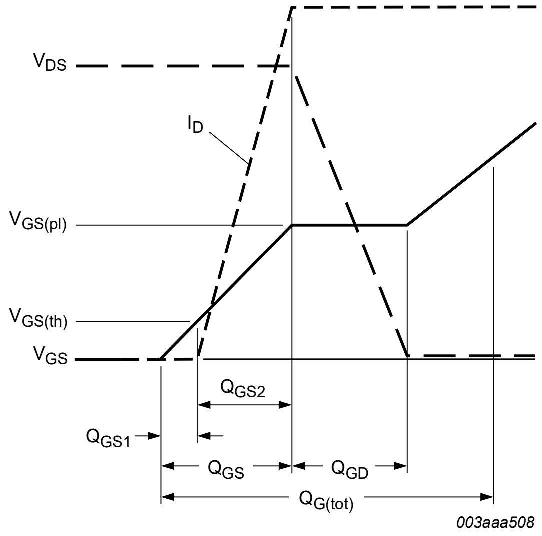



Fig. 6. Gate charge waveform definitions

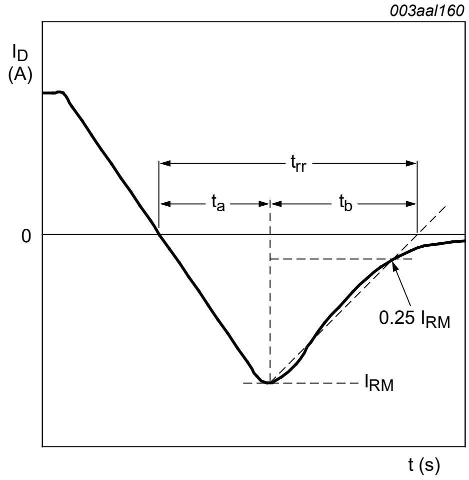
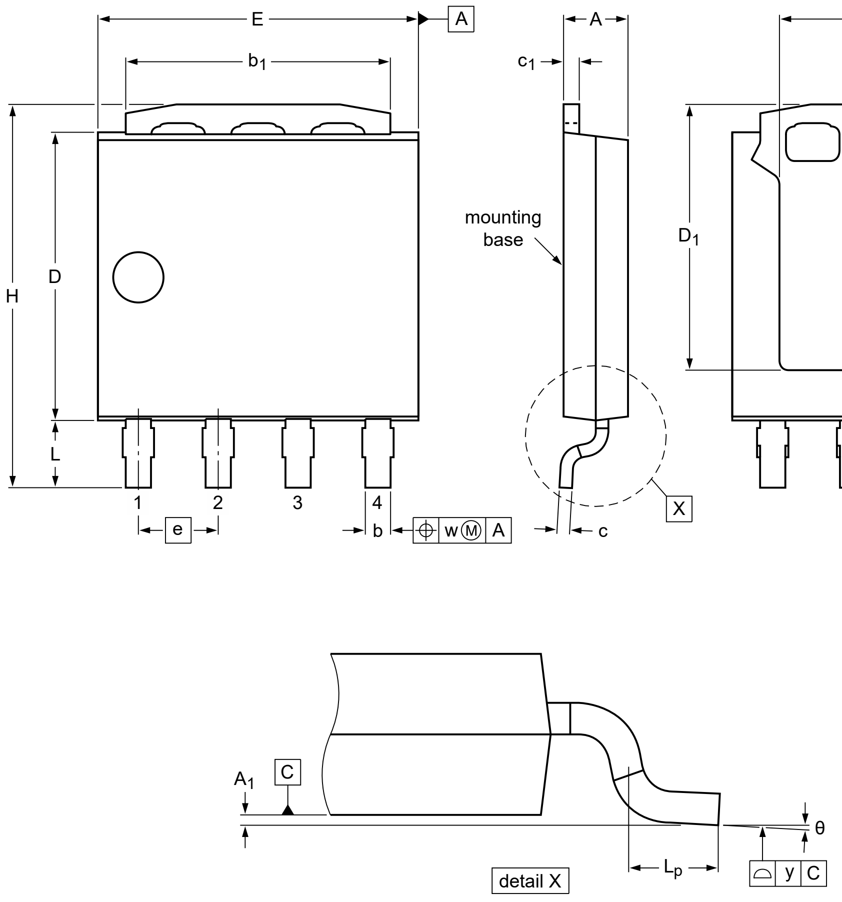



Fig. 7. Reverse recovery timing definition

## 10. Package outline

**Plastic single-ended surface-mounted package (LFPAK56E); 4 leads** **SOT1023**




0 2.5 5 mm

scale

Dimensions

| Unit | | A | $A_1$ | b | $b_1$ | $b_2$ | c | $c_1$ | D(1) | $D_1$(1) | E(1) | $E_1$(1) | e | H | L | $L_p$ | w | y | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | max | 1.10 | 0.15 | 0.50 | 4.41 | | 0.25 | 0.30 | 4.70 | 4.45 | 5.30 | 3.7 | | 6.2 | 1.3 | 0.85 | | | 8° |
| | nom | | | | | 0.85 | | | | | | | 1.27 | | | | 0.25 | 0.1 | |
| | min | 0.95 | 0.00 | 0.35 | 3.62 | | 0.19 | 0.24 | 4.45 | | 4.95 | 3.5 | | 5.9 | 0.8 | 0.40 | | | 0° |

Note

1. Plastic or metal protrusions of 0.15 mm per side are not included.

*sot1023_po*

| Outline version | References | | | | European projection | Issue date |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT1023 | | | | | | ~~13-03-05~~ 17-07-31 |

**Fig. 8. Package outline LFPAK56E; Power-SO8 (SOT1023)**

# 11. Soldering

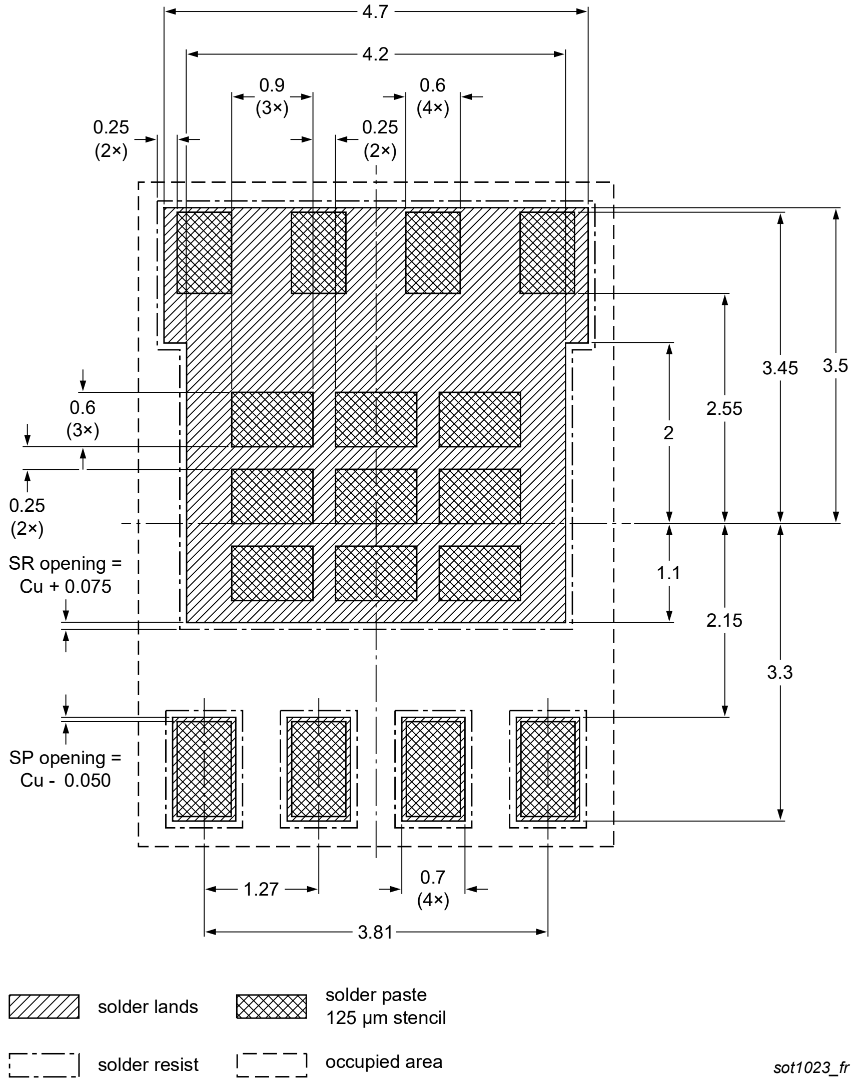



**Fig. 9. Reflow soldering footprint for LFPAK56E; Power-SO8 (SOT1023)**

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|---|---|---|
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[2] The term 'short data sheet' is explained in section "Definitions".
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