



PSMN2R3-100SSE

N-channel 100 V, 2.3 mΩ, SuperSOA MOSFET in LFPK88

11 September 2020

Objective data sheet

1. General description

SuperSOA N-channel enhancement mode MOSFET in a LFPK88 package qualified to 175 °C.

Part of Nexperia's "NextPower Live" portfolio, the PSMN2R3-100SSE delivers very low R_{DSon} and a very strong linear-mode (SOA) performance in a high-reliability copper-clip LFPK88 package.

PSMN2R3-100SSE complements the latest "hot-swap" controllers - robust enough to withstand substantial inrush currents during turn on, low R_{DSon} to minimize I^2R losses and deliver optimum efficiency when turned fully ON .

2. Features and benefits

- Fully optimized Safe Operating Area (SOA) for superior linear mode operation
- Low R_{DSon} for low I^2R conduction losses
- LFPK88 package for applications that demand the highest performance and reliability

3. Applications

- Hot swap
- Load switch
- Soft start
- E-fuse
- Telecommunication systems based on a 48 V backplane/supply rail

4. Quick reference data

Table 1. Quick reference data

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--------------------------------|--|---|-------|-----|-------|------|
| V_{DS} | drain-source voltage | $25\text{ °C} \leq T_j \leq 175\text{ °C}$ | - | - | 100 | V |
| I_D | drain current | $V_{GS} = 10\text{ V}; T_{mb} = 25\text{ °C}$ | - | - | 262 | A |
| P_{tot} | total power dissipation | $T_{mb} = 25\text{ °C};$ Fig. 1 | - | - | 341 | W |
| T_j | junction temperature | | -55 | - | 175 | °C |
| Static characteristics | | | | | | |
| R_{DSon} | drain-source on-state resistance | $V_{GS} = 10\text{ V}; I_D = 25\text{ A}; T_j = 25\text{ °C}$ | - | 1.7 | 2.2 | mΩ |
| | | $V_{GS} = 10\text{ V}; I_D = 25\text{ A}; T_j = 100\text{ °C}$ | - | 2.7 | 3.4 | mΩ |
| Dynamic characteristics | | | | | | |
| Q_{GD} | gate-drain charge | $I_D = 25\text{ A}; V_{DS} = 50\text{ V}; V_{GS} = 10\text{ V};$ Fig. 5 | [tbd] | 26 | [tbd] | nC |
| $Q_{G(tot)}$ | total gate charge | | [tbd] | 160 | [tbd] | nC |
| Avalanche ruggedness | | | | | | |
| $E_{DS(AL)S}$ | non-repetitive drain-source avalanche energy | $I_D = 82\text{ A}; V_{sup} \leq 100\text{ V}; R_{GS} = 50\text{ }\Omega;$ $V_{GS} = 10\text{ V}; T_{j(init)} = 25\text{ °C};$ unclamped | [1] | - | 732 | mJ |

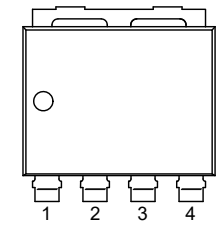
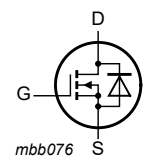
| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---------------------------|------------------|---|-----|-----|-----|------|
| Source-drain diode | | | | | | |
| Q_r | recovered charge | $I_S = 25 \text{ A}$; $di_S/dt = -100 \text{ A}/\mu\text{s}$; $V_{GS} = 0 \text{ V}$; $V_{DS} = 50 \text{ V}$; Fig. 6 | [2] | - | 32 | nC |

[1] Protected by 100% test

[2] includes capacitive recovery

5. Pinning information

Table 2. Pinning information

| Pin | Symbol | Description | Simplified outline | Graphic symbol |
|-----|--------|-----------------------------------|---|---|
| 1 | G | gate |  <p>LFAK88 (SOT1235)</p> |  <p>mbb076</p> |
| 2 | S | source | | |
| 3 | S | source | | |
| 4 | S | source | | |
| mb | D | mounting base; connected to drain | | |

6. Ordering information

Table 3. Ordering information

| Type number | Package | | Version |
|----------------|---------|--|---------|
| | Name | Description | |
| PSMN2R3-100SSE | LFAK88 | plastic, single-ended surface-mounted package (LFAK88); 4 leads; 2 mm pitch; 8 mm x 8 mm x 1.6 mm body | SOT1235 |

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---------------------------|----------------------------|---|-----|------|------------------|
| V_{DS} | drain-source voltage | $25 \text{ }^\circ\text{C} \leq T_j \leq 175 \text{ }^\circ\text{C}$ | - | 100 | V |
| V_{DGR} | drain-gate voltage | $25 \text{ }^\circ\text{C} \leq T_j \leq 175 \text{ }^\circ\text{C}$; $R_{GS} = 20 \text{ k}\Omega$ | - | 100 | V |
| V_{GS} | gate-source voltage | | -20 | 20 | V |
| P_{tot} | total power dissipation | $T_{mb} = 25 \text{ }^\circ\text{C}$; Fig. 1 | - | 341 | W |
| I_D | drain current | $V_{GS} = 10 \text{ V}$; $T_{mb} = 25 \text{ }^\circ\text{C}$ | - | 262 | A |
| | | $V_{GS} = 10 \text{ V}$; $T_{mb} = 100 \text{ }^\circ\text{C}$ | - | 185 | A |
| I_{DM} | peak drain current | pulsed; $t_p \leq 10 \text{ }\mu\text{s}$; $T_{mb} = 25 \text{ }^\circ\text{C}$; Fig. 2 | - | 1047 | A |
| T_{stg} | storage temperature | | -55 | 175 | $^\circ\text{C}$ |
| T_j | junction temperature | | -55 | 175 | $^\circ\text{C}$ |
| $T_{sld(M)}$ | peak soldering temperature | | - | 260 | $^\circ\text{C}$ |
| Source-drain diode | | | | | |
| I_S | source current | $T_{mb} = 25 \text{ }^\circ\text{C}$ | - | 262 | A |
| I_{SM} | peak source current | pulsed; $t_p \leq 10 \text{ }\mu\text{s}$; $T_{mb} = 25 \text{ }^\circ\text{C}$ | - | 1047 | A |

| Symbol | Parameter | Conditions | Min | Max | Unit | |
|-----------------------------|--|--|-----|-----|------|----|
| Avalanche ruggedness | | | | | | |
| $E_{DS(AL)S}$ | non-repetitive drain-source avalanche energy | $I_D = 82\text{ A}; V_{sup} \leq 100\text{ V}; R_{GS} = 50\ \Omega;$ $V_{GS} = 10\text{ V}; T_{j(\text{init})} = 25\text{ }^\circ\text{C};$ unclamped | [1] | - | 732 | mJ |
| I_{AS} | non-repetitive avalanche current | $V_{sup} \leq 100\text{ V}; V_{GS} = 10\text{ V}; T_{j(\text{init})} = 25\text{ }^\circ\text{C};$ $R_{GS} = 50\ \Omega$ | [1] | - | 82 | A |

[1] Protected by 100% test

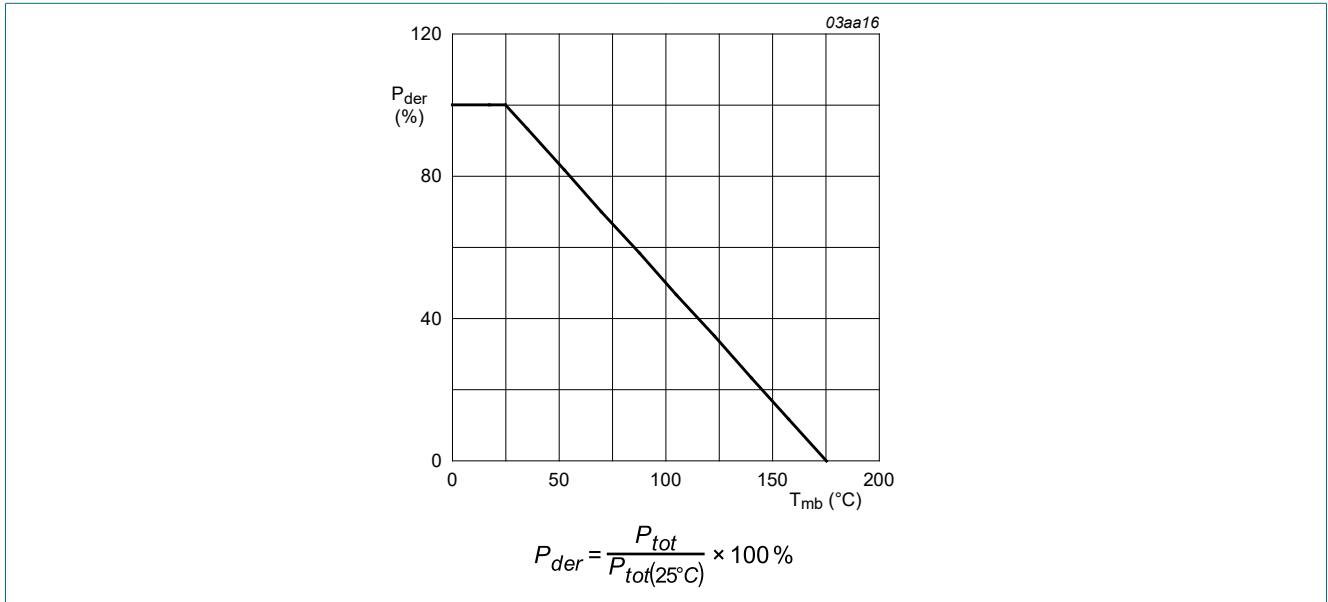


Fig. 1. Normalized total power dissipation as a function of mounting base temperature

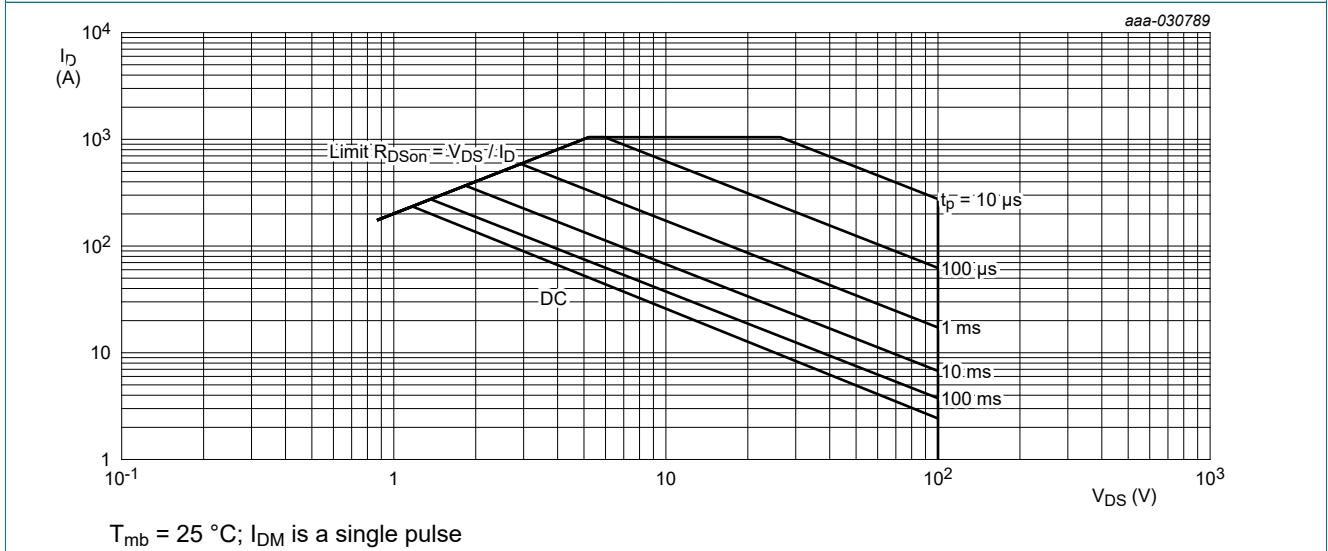


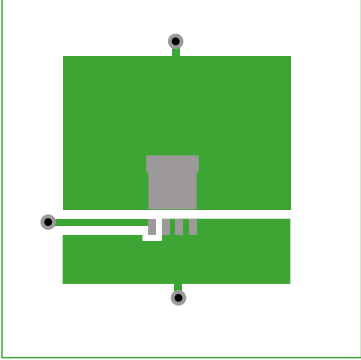
Fig. 2. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

8. Thermal characteristics

Table 5. Thermal characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|----------------|---|------------|-----|-------|------|------|
| $R_{th(j-mb)}$ | thermal resistance from junction to mounting base | | - | [tbd] | 0.44 | K/W |

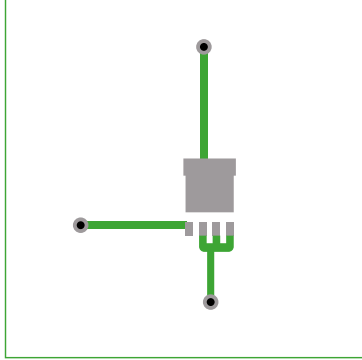
| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---------------|---|------------------------|-----|-----|-----|------|
| $R_{th(j-a)}$ | thermal resistance from junction to ambient | Fig. 3 | - | 35 | - | K/W |
| | | Fig. 4 | - | 70 | - | K/W |



aaa-029383

Copper square 25.4 mm x 25.4 mm; 70 μm thick on FR4 board

Fig. 3. PCB layout for resistance from junction to ambient



aaa-029384

70 μm thick copper on FR4 board

Fig. 4. PCB layout with minimum footprint for thermal resistance from junction to ambient

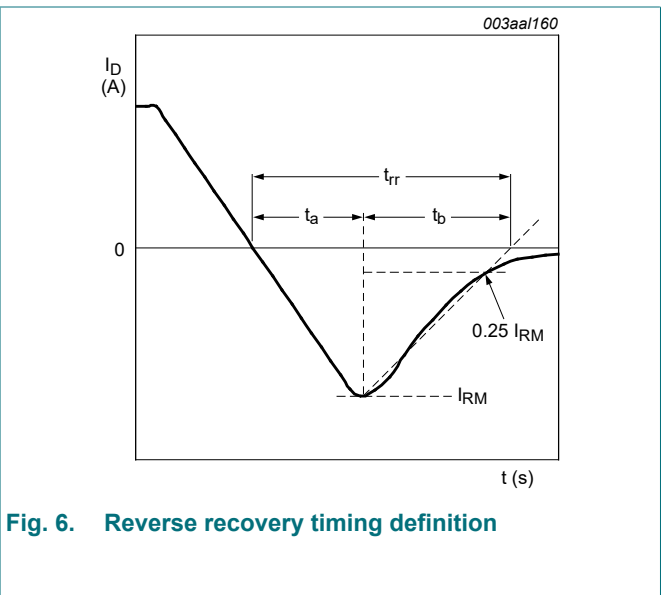
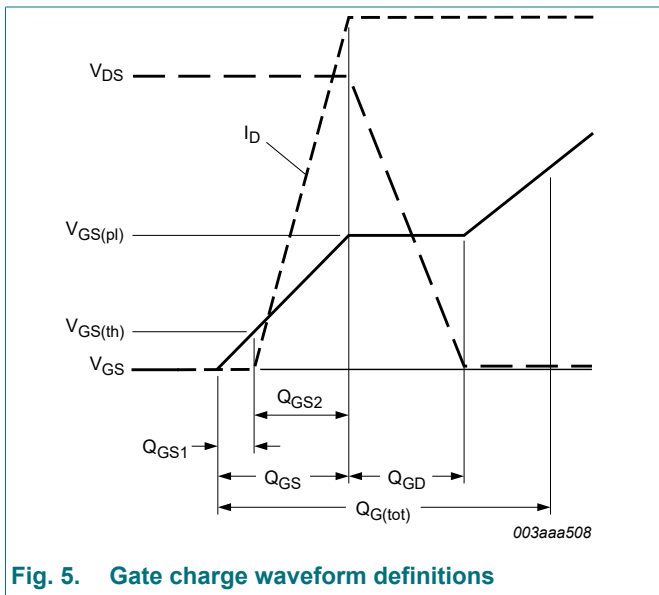
9. Characteristics

Table 6. Characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--------------------------------|--|---|-------|-------|-------|------|
| Static characteristics | | | | | | |
| $V_{(BR)DSS}$ | drain-source breakdown voltage | $I_D = 250 \mu A; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$ | 100 | - | - | V |
| | | $I_D = 250 \mu A; V_{GS} = 0 V; T_j = -55 \text{ }^\circ C$ | 90 | - | - | V |
| $V_{GS(th)}$ | gate-source threshold voltage | $I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 25 \text{ }^\circ C$ | 2 | 3 | 4 | V |
| | | $I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = -55 \text{ }^\circ C$ | - | [tbd] | - | V |
| | | $I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 175 \text{ }^\circ C$ | - | [tbd] | - | V |
| $\Delta V_{GS(th)}/\Delta T$ | gate-source threshold voltage variation with temperature | $25 \text{ }^\circ C \leq T_j \leq 150 \text{ }^\circ C$ | - | [tbd] | - | mV/K |
| I_{DSS} | drain leakage current | $V_{DS} = 100 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$ | - | 0.1 | 25 | μA |
| | | $V_{DS} = 100 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 125 \text{ }^\circ C$ | - | - | 100 | μA |
| I_{GSS} | gate leakage current | $V_{GS} = 20 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$ | - | 2 | 100 | nA |
| | | $V_{GS} = -20 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$ | - | 2 | 100 | nA |
| R_{DSon} | drain-source on-state resistance | $V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 25 \text{ }^\circ C$ | - | 1.7 | 2.2 | mΩ |
| | | $V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 100 \text{ }^\circ C$ | - | 2.7 | 3.4 | mΩ |
| | | $V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 175 \text{ }^\circ C$ | - | 4 | 5 | mΩ |
| R_G | gate resistance | $f = 1 \text{ MHz}; T_j = 25 \text{ }^\circ C$ | [tbd] | 1 | [tbd] | Ω |
| Dynamic characteristics | | | | | | |
| $Q_{G(tot)}$ | total gate charge | $I_D = 25 \text{ A}; V_{DS} = 50 \text{ V}; V_{GS} = 10 \text{ V};$ Fig. 5 | [tbd] | 160 | [tbd] | nC |
| | | $I_D = 0 \text{ A}; V_{DS} = 0 \text{ V}; V_{GS} = 10 \text{ V}$ | - | 83 | - | nC |

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---------------------------|-----------------------------------|--|-------|-------|-------|------|
| Q_{GS} | gate-source charge | $I_D = 25\text{ A}; V_{DS} = 50\text{ V}; V_{GS} = 10\text{ V};$ Fig. 5 | [tbd] | 54 | [tbd] | nC |
| $Q_{GS(th)}$ | pre-threshold gate-source charge | | - | 34 | - | nC |
| $Q_{GS(th-pl)}$ | post-threshold gate-source charge | | - | 20 | - | nC |
| Q_{GD} | gate-drain charge | | [tbd] | 26 | [tbd] | nC |
| $V_{GS(pl)}$ | gate-source plateau voltage | $I_D = 25\text{ A}; V_{DS} = 50\text{ V};$ Fig. 5 | - | 4.7 | - | V |
| C_{iss} | input capacitance | $V_{DS} = 50\text{ V}; V_{GS} = 0\text{ V}; f = 1\text{ MHz};$ $T_j = 25\text{ °C}$ | [tbd] | 12919 | [tbd] | pF |
| C_{oss} | output capacitance | | [tbd] | 3356 | [tbd] | pF |
| C_{rss} | reverse transfer capacitance | | [tbd] | 47 | [tbd] | pF |
| $t_{d(on)}$ | turn-on delay time | $V_{DS} = 50\text{ V}; R_L = 2\text{ }\Omega; V_{GS} = 10\text{ V};$ $R_{G(ext)} = 5\text{ }\Omega$ | - | 43 | - | ns |
| t_r | rise time | | - | 46 | - | ns |
| $t_{d(off)}$ | turn-off delay time | | - | 90 | - | ns |
| t_f | fall time | | - | 57 | - | ns |
| Source-drain diode | | | | | | |
| V_{SD} | source-drain voltage | $I_S = 25\text{ A}; V_{GS} = 0\text{ V}; T_j = 25\text{ °C}$ | - | 0.8 | 1.2 | V |
| t_{rr} | reverse recovery time | $I_S = 25\text{ A}; di_S/dt = -100\text{ A}/\mu\text{s}; V_{GS} = 0\text{ V};$ $V_{DS} = 50\text{ V};$ Fig. 6 | - | 40 | - | ns |
| Q_r | recovered charge | | [1] | - | 32 | - |

[1] includes capacitive recovery



10. Package outline

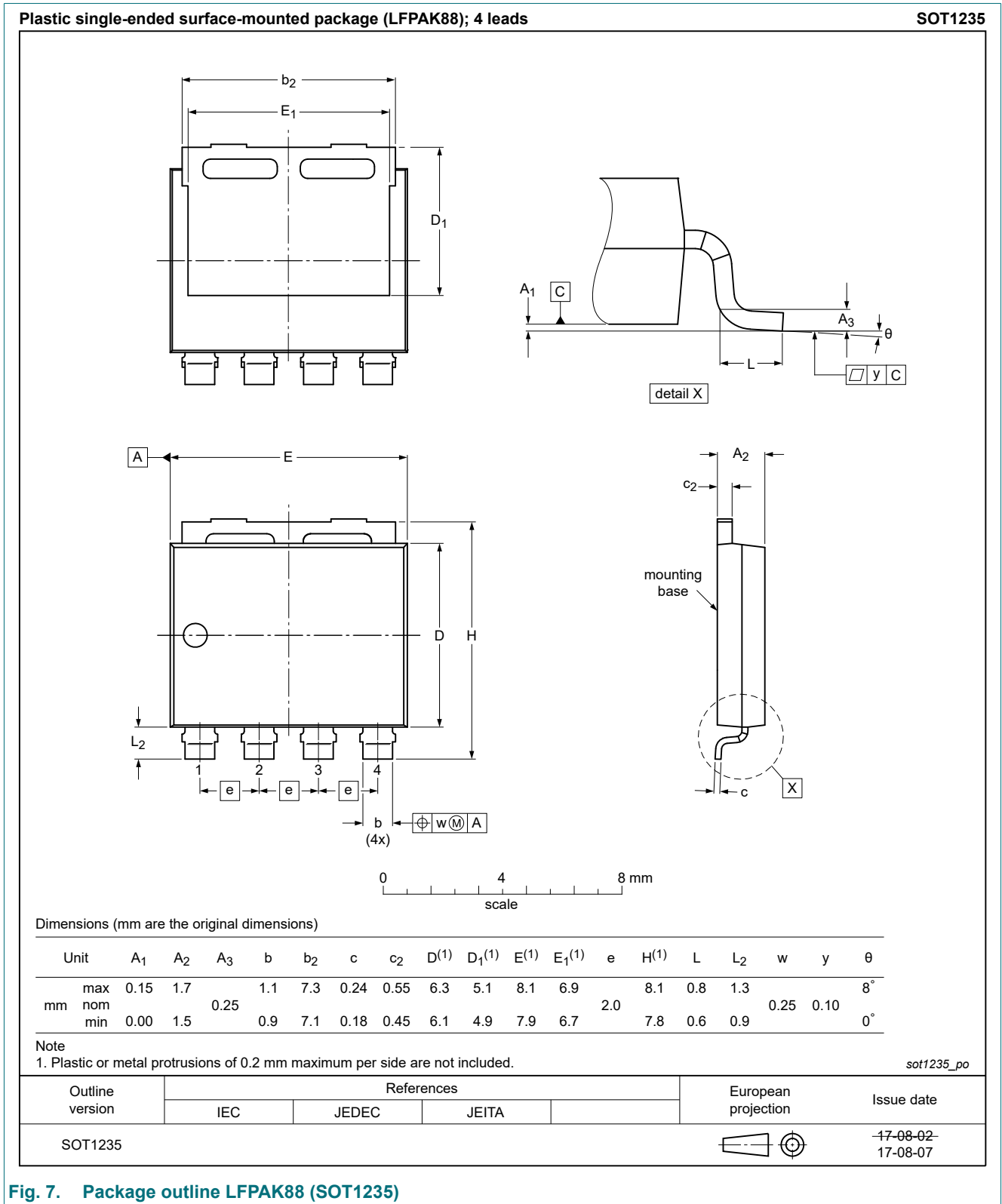


Fig. 7. Package outline LPAK88 (SOT1235)

11. Soldering

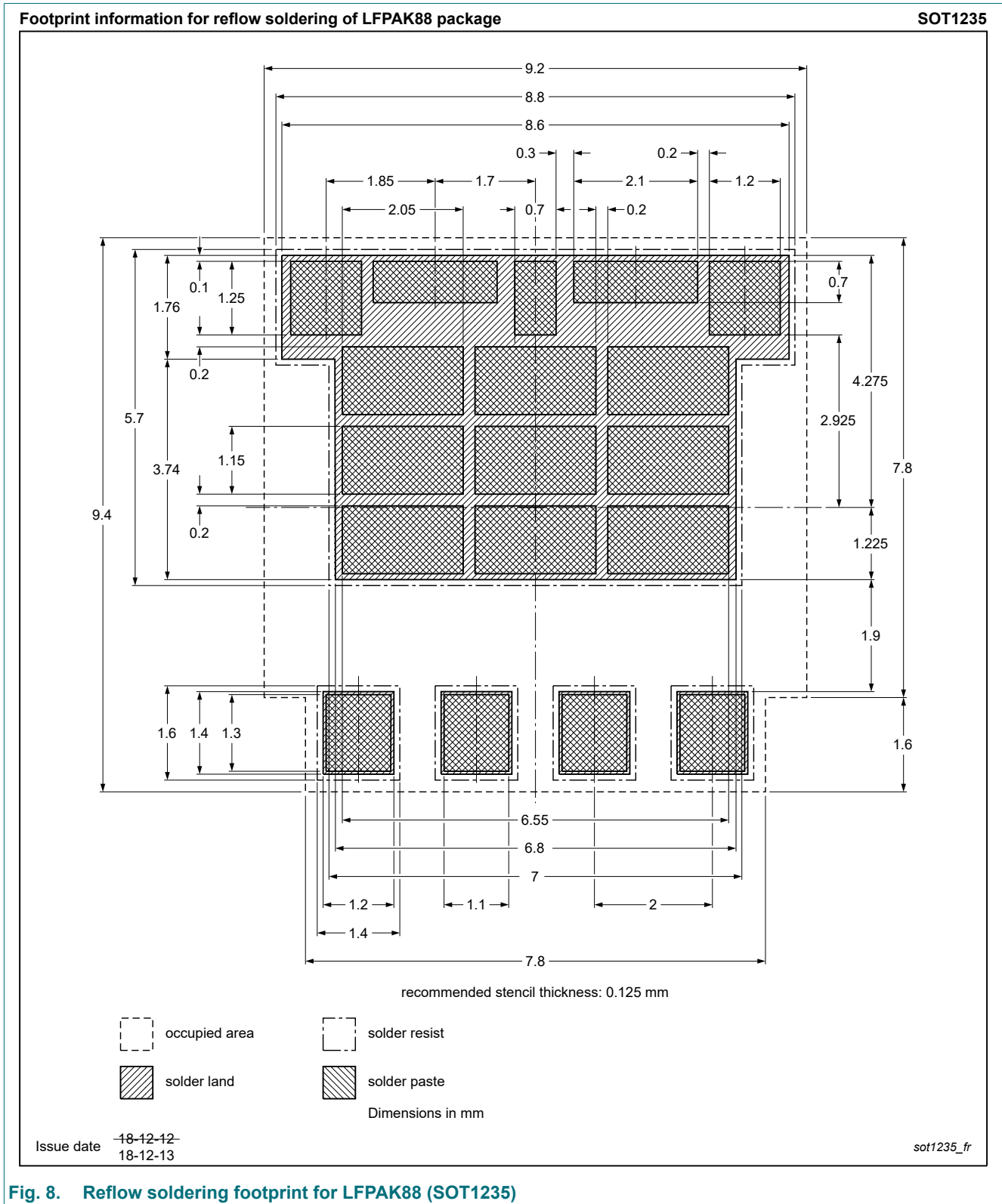


Fig. 8. Reflow soldering footprint for LPAK88 (SOT1235)

12. Legal information

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| Document status [1][2] | Product status [3] | Definition |
|--------------------------------|--------------------|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

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- [2] The term 'short data sheet' is explained in section "Definitions".
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