PSMN1R8-80SSF

NextPower 80 V, 1.8 mΩ, 215 Amp, N-channel MOSFET in LFPAK88 package

15 June 2020 **Objective data sheet**

1. General description

NextPower 80 V, standard level gate drive MOSFET. Qualified to 175 °C and recommended for industrial and consumer applications.

2. Features and benefits

- Low Q_{rr} for higher efficiency and lower spiking
- 215 Amps $I_{D(max)}$ continuous current rating
- Low $Q_G \times R_{DSon}$ FOM for high efficiency switching applications
- Strong avalanche energy rating (E_{as})
- Avalanche rated and 100% tested
- Ha-free and RoHS compliant LFPAK88 package

3. Applications

- Synchronous rectifier in AC-DC and DC-DC
- Primary side switch in DC-DC
- BLDC motor control
- Full-bridge and half-bridge applications
- Battery protection

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DS}	drain-source voltage	25 °C ≤ T_j ≤ 175 °C		-	-	80	V
I_D	drain current	V_{GS} = 10 V; T_{mb} = 25 °C		-	-	215	A
P_{tot}	total power dissipation	T_{mb} = 25 °C; Fig. 1		-	-	341	W
T_j	junction temperature			-55	-	175	°C
Static characteristics							
R_{DSon}	drain-source on-state resistance	V_{GS} = 10 V; I_D = 25 A; T_j = 25 °C		-	1.4	1.8	mΩ
		V_{GS} = 7 V; I_D = 25 A; T_j = 25 °C		-	[tbd]	[tbd]	mΩ
Dynamic characteristics							
Q_{GD}	gate-drain charge	I_D = 25 A; V_{DS} = 40 V; V_{GS} = 10 V; Fig. 4		[tbd]	27	[tbd]	nC
$Q_{G(tot)}$	total gate charge			[tbd]	156	[tbd]	nC
Avalanche ruggedness							
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	I_D = 90 A; V_{sup} ≤ 80 V; R_{GS} = 50 Ω; V_{GS} = 10 V; $T_{j(init)}$ = 25 °C; unclamped	[1]	-	-	920	mJ

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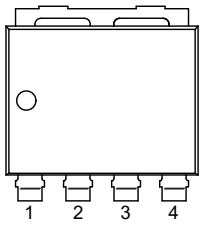
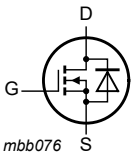
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Source-drain diode							
Q_r	recovered charge	I_S = 25 A; dI_S/dt = -100 A/µs; V_{GS} = 0 V; V_{DS} = 20 V		-	58	-	nC

[1] Protected by 100% test

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate	 LFPAK88 (SOT1235)	
2	S	Source		
3	S	Source		
4	S	Source		
mb	D	mounting base; connected to drain		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PSMN1R8-80SSF	LFPAK88	plastic, single-ended surface-mounted package (LFPAK88); 4 leads; 2 mm pitch; 8 mm x 8 mm x 1.6 mm body	SOT1235

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DS}	drain-source voltage	25 °C ≤ T_j ≤ 175 °C		-	80	V
V_{DGR}	drain-gate voltage	25 °C ≤ T_j ≤ 175 °C; R_{GS} = 20 kΩ		-	80	V
V_{GS}	gate-source voltage			-20	20	V
P_{tot}	total power dissipation	T_{mb} = 25 °C; Fig. 1		-	341	W
I_D	drain current	V_{GS} = 10 V; T_{mb} = 25 °C		-	215	A
		V_{GS} = 10 V; T_{mb} = 100 °C		-	151	A
I_{DM}	peak drain current	pulsed; t_p ≤ 10 µs; T_{mb} = 25 °C		-	860	A
T_{stg}	storage temperature			-55	175	°C
T_j	junction temperature			-55	175	°C
$T_{sld(M)}$	peak soldering temperature			-	260	°C
Source-drain diode						
I_S	source current	T_{mb} = 25 °C		-	215	A
I_{SM}	peak source current	pulsed; t_p ≤ 10 µs; T_{mb} = 25 °C		-	860	A

Symbol	Parameter	Conditions		Min	Max	Unit
Avalanche ruggedness						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	I_D = 90 A; $V_{sup} \leq$ 80 V; R_{GS} = 50 Ω; V_{GS} = 10 V; $T_{j(init)}$ = 25 °C; unclamped	[1]	-	920	mJ
I_{AS}	non-repetitive avalanche current	$V_{sup} \leq$ 100 V; V_{GS} = 10 V; $T_{j(init)}$ = 25 °C; R_{GS} = 50 Ω	[1]	-	90	A

[1] Protected by 100% test

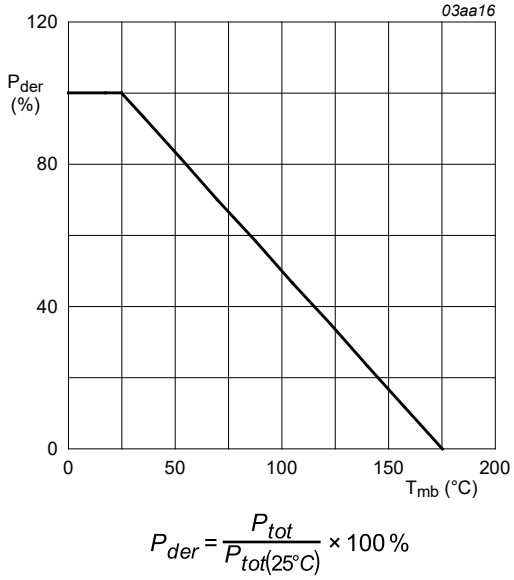
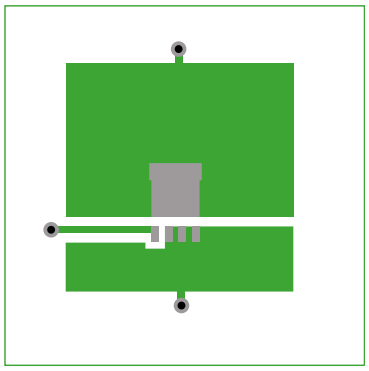


Fig. 1. Normalized total power dissipation as a function of mounting base temperature

8. Thermal characteristics

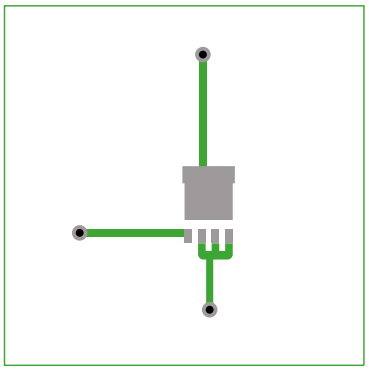
Table 5. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base			-	[tbd]	0.44	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	Fig. 2		-	35	-	K/W
		Fig. 3		-	70	-	K/W



Copper square 25.4 mm square; 70 µm thick on FR4 board

Fig. 2. PCB layout for thermal resistance from junction to ambient



70 µm thick copper on FR4 board

Fig. 3. PCB layout with minimum footprint for thermal resistance from junction to ambient

9. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 250 µA; V_{GS} = 0 V; T_j = 25 °C		80	-	-	V
		I_D = 250 µA; V_{GS} = 0 V; T_j = -55 °C		72	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA; V_{DS} = V_{GS}; T_j = 25 °C		2	3	4	V
		I_D = 1 mA; V_{DS} = V_{GS}; T_j = -55 °C		-	3.5	-	V
		I_D = 1 mA; V_{DS} = V_{GS}; T_j = 175 °C		-	1.6	-	V
$\Delta V_{GS(th)}/\Delta T$	gate-source threshold voltage variation with temperature	25 °C ≤ T_j ≤ 150 °C		-	[tbd]	-	mV/K
I_{DSS}	drain leakage current	V_{DS} = 80 V; V_{GS} = 0 V; T_j = 25 °C		-	0.06	25	µA
		V_{DS} = 80 V; V_{GS} = 0 V; T_j = 125 °C		-	-	100	µA
I_{GSS}	gate leakage current	V_{GS} = 20 V; V_{DS} = 0 V; T_j = 25 °C		-	0.7	100	nA
		V_{GS} = -20 V; V_{DS} = 0 V; T_j = 25 °C		-	0.7	100	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = 10 V; I_D = 25 A; T_j = 25 °C		-	1.4	1.8	mΩ
		V_{GS} = 7 V; I_D = 25 A; T_j = 25 °C		-	[tbd]	[tbd]	mΩ
		V_{GS} = 10 V; I_D = 25 A; T_j = 100 °C		-	2.2	2.9	mΩ
		V_{GS} = 10 V; I_D = 25 A; T_j = 175 °C		-	3.1	4.1	mΩ
R_G	gate resistance	f = 1 MHz; T_j = 25 °C		[tbd]	1.2	[tbd]	Ω
Dynamic characteristics							
$Q_{G(tot)}$	total gate charge	I_D = 25 A; V_{DS} = 40 V; V_{GS} = 10 V; Fig. 4		[tbd]	156	[tbd]	nC
		I_D = 0 A; V_{DS} = 0 V; V_{GS} = 10 V; Fig. 4		-	84	-	nC
Q_{GS}	gate-source charge	I_D = 25 A; V_{DS} = 40 V; V_{GS} = 10 V; Fig. 4		[tbd]	46	[tbd]	nC
$Q_{GS(th)}$	pre-threshold gate-source charge			[tbd]	31	[tbd]	nC
$Q_{GS(th-pl)}$	post-threshold gate-source charge			[tbd]	15	[tbd]	nC
Q_{GD}	gate-drain charge			[tbd]	27	[tbd]	nC

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$V_{GS(pl)}$	gate-source plateau voltage	I_D = 25 A; V_{DS} = 40 V; Fig. 4		-	[tbd]	-	V
C_{iss}	input capacitance	V_{DS} = 40 V; V_{GS} = 0 V; f = 1 MHz; T_j = 25 °C		[tbd]	12105	[tbd]	pF
C_{oss}	output capacitance			[tbd]	2909	[tbd]	pF
C_{rss}	reverse transfer capacitance			[tbd]	65	[tbd]	pF
$t_{d(on)}$	turn-on delay time	V_{DS} = 40 V; R_L = 1.6 Ω; V_{GS} = 10 V; $R_{G(ext)}$ = 5 Ω		-	43	-	ns
t_r	rise time			-	38	-	ns
$t_{d(off)}$	turn-off delay time			-	98	-	ns
t_f	fall time			-	52	-	ns
Source-drain diode							
V_{SD}	source-drain voltage	I_S = 25 A; V_{GS} = 0 V; T_j = 25 °C		-	-	1.2	V
t_{rr}	reverse recovery time	I_S = 25 A; dI_S/dt = -100 A/µs; V_{GS} = 0 V; V_{DS} = 20 V		-	54	-	ns
Q_r	recovered charge			-	58	-	nC

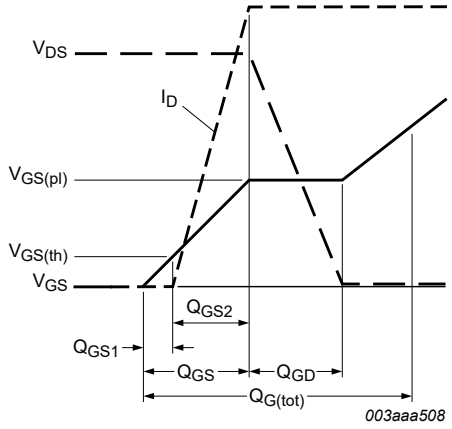
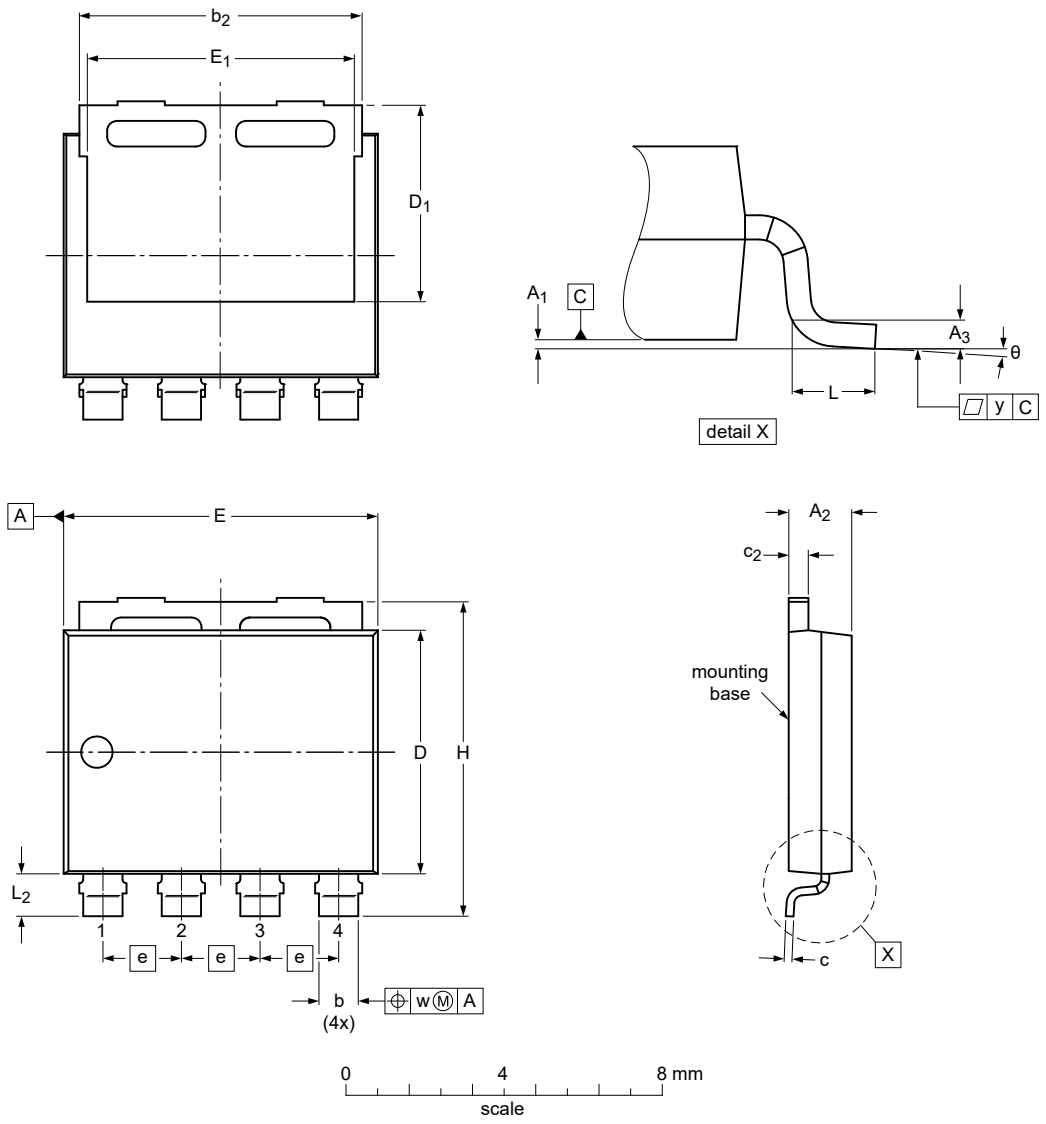


Fig. 4. Gate charge waveform definitions

10. Package outline

Plastic single-ended surface-mounted package (LFPAK88); 4 leads **SOT1235**



Dimensions (mm are the original dimensions)

Unit		A_1	A_2	A_3	b	b_2	c	c_2	$D^{(1)}$	$D_1^{(1)}$	$E^{(1)}$	$E_1^{(1)}$	e	$H^{(1)}$	L	L_2	w	y	θ
mm	max	0.15	1.7		1.1	7.3	0.24	0.55	6.3	5.1	8.1	6.9		8.1	0.8	1.3			8°
	nom			0.25									2.0				0.25	0.10	
	min	0.00	1.5		0.9	7.1	0.18	0.45	6.1	4.9	7.9	6.7		7.8	0.6	0.9			0°

Note
1. Plastic or metal protrusions of 0.2 mm maximum per side are not included.

sot1235_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1235						~~17-08-02~~ 17-08-07

Fig. 5. Package outline LFPAK88 (SOT1235)

11. Soldering

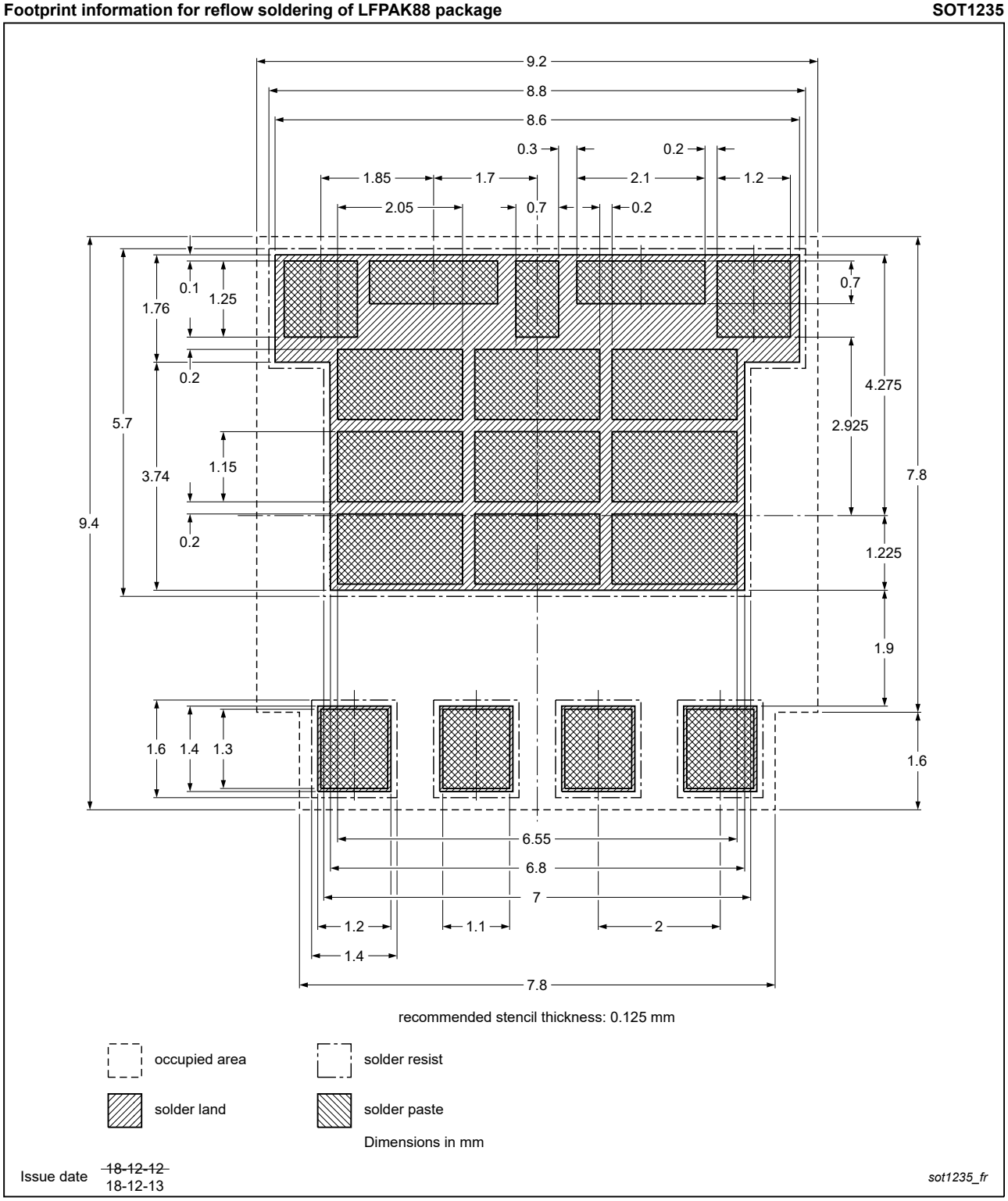


Fig. 6. Reflow soldering footprint for LFPAK88 (SOT1235)

12. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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