



PSMN1R0-30YLE

N-channel 30 V, 1.1 mOhm, ASFET for hotswap with enhanced SOA in LFAK56

13 October 2022

Product data sheet

1. General description

N-channel enhancement mode ASFET for hotswap with enhanced SOA in LFAK56 package optimized for low R_{DSon} and strong safe operating area, optimized for hot-swap, inrush and linear-mode applications.

2. Features and benefits

- Fully optimized Safe Operating Area (SOA) for superior linear mode operation
- Optimized for low R_{DSon} / low I^2R conduction losses
- LFAK56 package for applications that demand the highest performance and reliability in a 30 mm² footprint
- Low leakage <1 μ A at 25 °C
- Copper-clip for low parasitic inductance and resistance
- High reliability LFAK package, qualified to 175 °C

3. Applications

- Hot swap in 12 V - 20 V applications
- e-Fuse
- DC switch
- Load switch
- Battery protection

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$25\text{ °C} \leq T_j \leq 175\text{ °C}$		-	-	30	V
I_D	drain current	$V_{GS} = 10\text{ V}$; $T_{mb} = 25\text{ °C}$; Fig. 2	[1]	-	-	275	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}$; Fig. 1		-	-	224	W
T_j	junction temperature			-55	-	175	°C
Static characteristics							
R_{DSon}	drain-source on-state resistance	$V_{GS} = 10\text{ V}$; $I_D = 25\text{ A}$; $T_j = 25\text{ °C}$; #unique_6/unique_6_Connect_42_idaaa-035466		-	0.94	1.11	mΩ
		$V_{GS} = 7\text{ V}$; $I_D = 25\text{ A}$; $T_j = 25\text{ °C}$; #unique_6/unique_6_Connect_42_idaaa-035466		-	1.17	1.55	mΩ

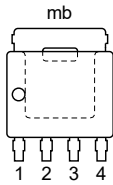
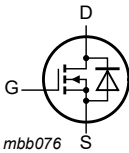
N-channel 30 V, 1.1 mOhm, ASFET for hotswap with enhanced SOA in LFPAK56

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Dynamic characteristics						
Q_{GD}	gate-drain charge	$I_D = 25\text{ A}$; $V_{DS} = 15\text{ V}$; $V_{GS} = 4.5\text{ V}$;	1.8	10	20	nC
$Q_{G(\text{tot})}$	total gate charge	$T_j = 25\text{ }^\circ\text{C}$; #unique_6/unique_6_Connect_42_idaaa-035468 ; #unique_6/unique_6_Connect_42_id003aaa508	15	33	54	nC
Source-drain diode						
S	softness factor	$I_S = 25\text{ A}$; $di_S/dt = -100\text{ A}/\mu\text{s}$; $V_{GS} = 0\text{ V}$; $V_{DS} = 15\text{ V}$; $T_j = 25\text{ }^\circ\text{C}$; #unique_6/unique_6_Connect_42_id003aal160	-	0.95	-	

[1] 275 A continuous current has been successfully demonstrated during application tests. Practically the current will be limited by PCB, thermal design and operating temperature.

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source	 <p>LFPAK56; Power-SO8 (SOT669)</p>	 <p>mbb076</p>
2	S	source		
3	S	source		
4	G	gate		
mb	D	mounting base; connected to drain		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PSMN1R0-30YLE	LFPAK56; Power-SO8	plastic, single-ended surface-mounted package; 4 terminals	SOT669

7. Marking

Table 4. Marking codes

Type number	Marking code
PSMN1R0-30YLE	1E0L30Y

8. Limiting values

Table 5. Limiting values

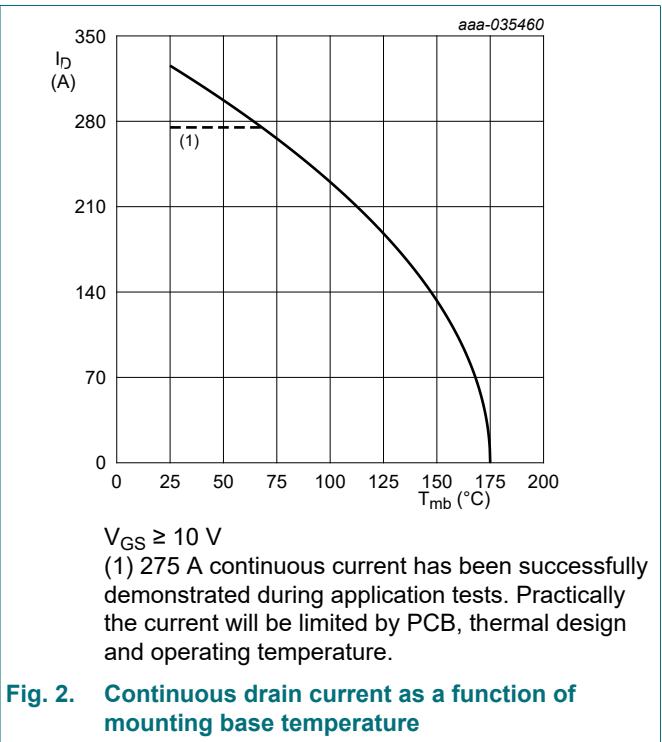
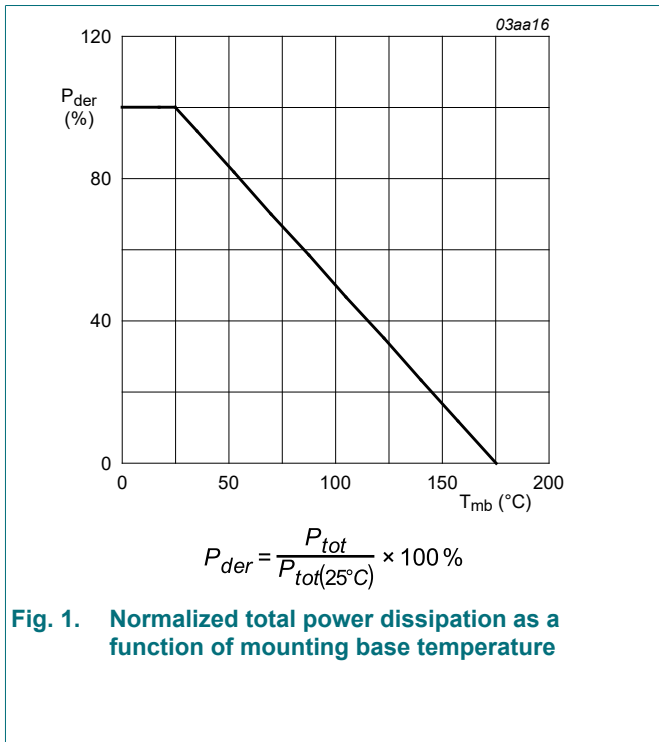
In accordance with the Absolute Maximum Rating System (IEC 60134). $T_j = 25\text{ }^\circ\text{C}$ unless otherwise stated.

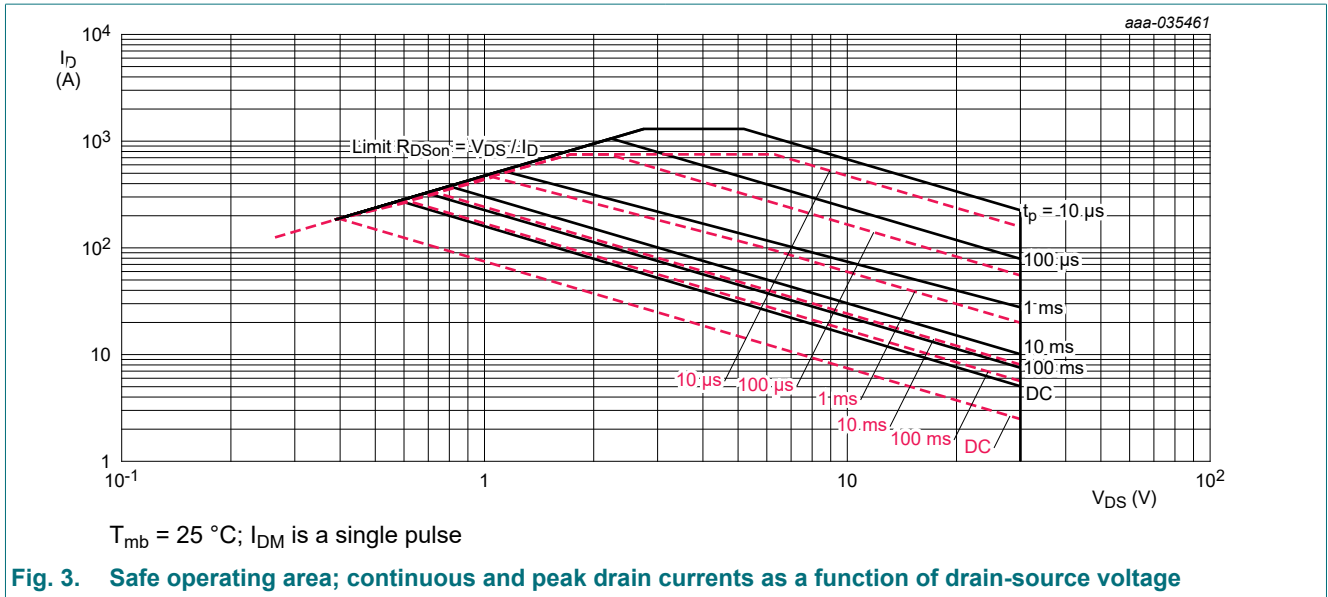
Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage	$25\text{ }^\circ\text{C} \leq T_j \leq 175\text{ }^\circ\text{C}$	-	30	V
V_{DGR}	drain-gate voltage	$25\text{ }^\circ\text{C} \leq T_j \leq 175\text{ }^\circ\text{C}$; $R_{GS} = 20\text{ k}\Omega$	-	30	V
V_{GS}	gate-source voltage		-20	20	V

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Symbol	Parameter	Conditions		Min	Max	Unit
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}$; Fig. 1		-	224	W
I_D	drain current	$V_{GS} = 10\text{ V}$; $T_{mb} = 25\text{ °C}$; Fig. 2	[1]	-	275	A
		$V_{GS} = 10\text{ V}$; $T_{mb} = 100\text{ °C}$; Fig. 2		-	230	A
I_{DM}	peak drain current	pulsed; $t_p \leq 10\text{ }\mu\text{s}$; $T_{mb} = 25\text{ °C}$; Fig. 3		-	1303	A
T_{stg}	storage temperature			-55	175	°C
T_J	junction temperature			-55	175	°C
$T_{slid(M)}$	peak soldering temperature			-	260	°C
Source-drain diode						
I_S	source current	$T_{mb} = 25\text{ °C}$		-	224	A
I_{SM}	peak source current	pulsed; $t_p \leq 10\text{ }\mu\text{s}$; $T_{mb} = 25\text{ °C}$		-	1303	A
Avalanche ruggedness						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$I_D = 25\text{ A}$; $V_{sup} \leq 30\text{ V}$; $R_{GS} = 50\text{ }\Omega$; $V_{GS} = 10\text{ V}$; $T_{j(init)} = 25\text{ °C}$; unclamped; $t_p = 3\text{ ms}$	[2]	-	1.5	J
I_{AS}	non-repetitive avalanche current	$V_{sup} \leq 30\text{ V}$; $V_{GS} = 10\text{ V}$; $T_{j(init)} = 25\text{ °C}$; $R_{GS} = 50\text{ }\Omega$	[2]	-	128	A

- [1] 275 A continuous current has been successfully demonstrated during application tests. Practically the current will be limited by PCB, thermal design and operating temperature.
- [2] Protected by 100% test.

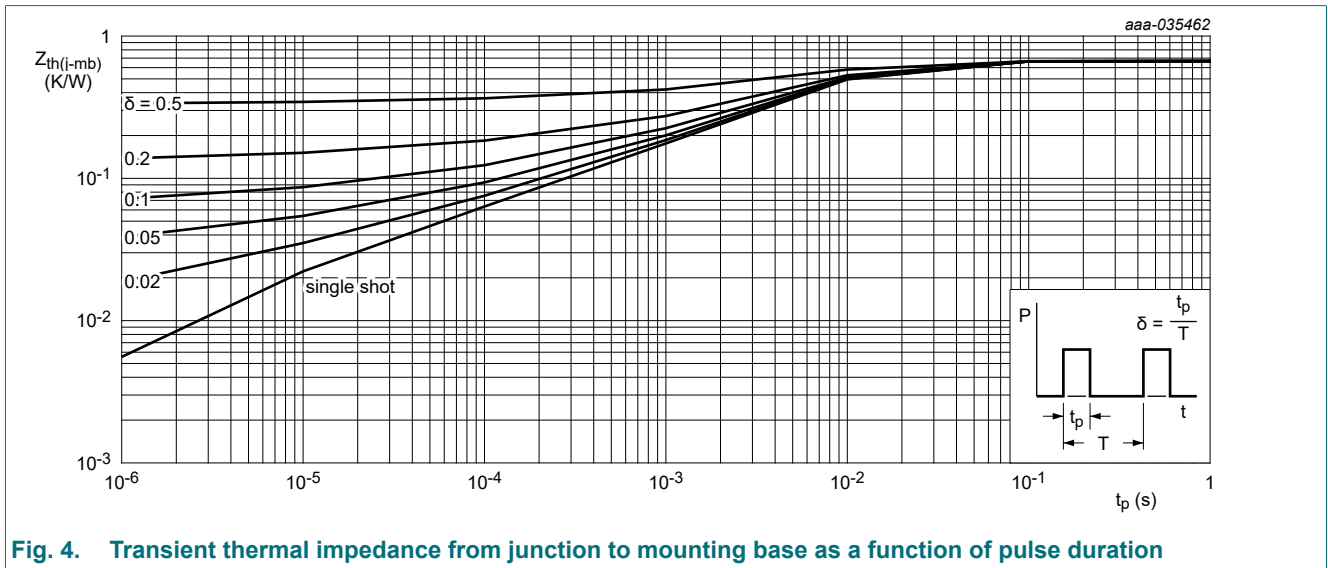


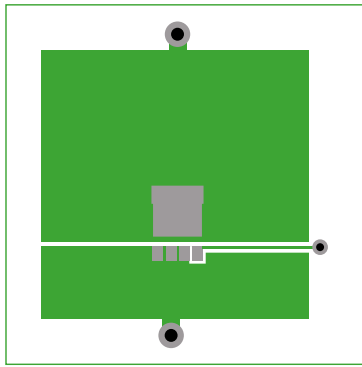


9. Thermal characteristics

Table 6. Thermal characteristics

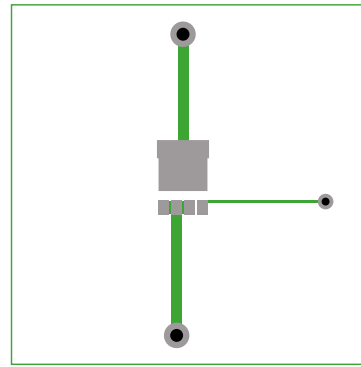
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 4	-	0.37	0.67	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	Fig. 5 Fig. 6	-	42	-	K/W
			-	85	-	K/W





Copper area 25.4 mm square; 70 μm thick on FR4 board

Fig. 5. PCB layout for thermal resistance from junction to ambient



70 μm thick copper on FR4 board

Fig. 6. PCB layout with minimum footprint for thermal resistance from junction to ambient

10. Package outline

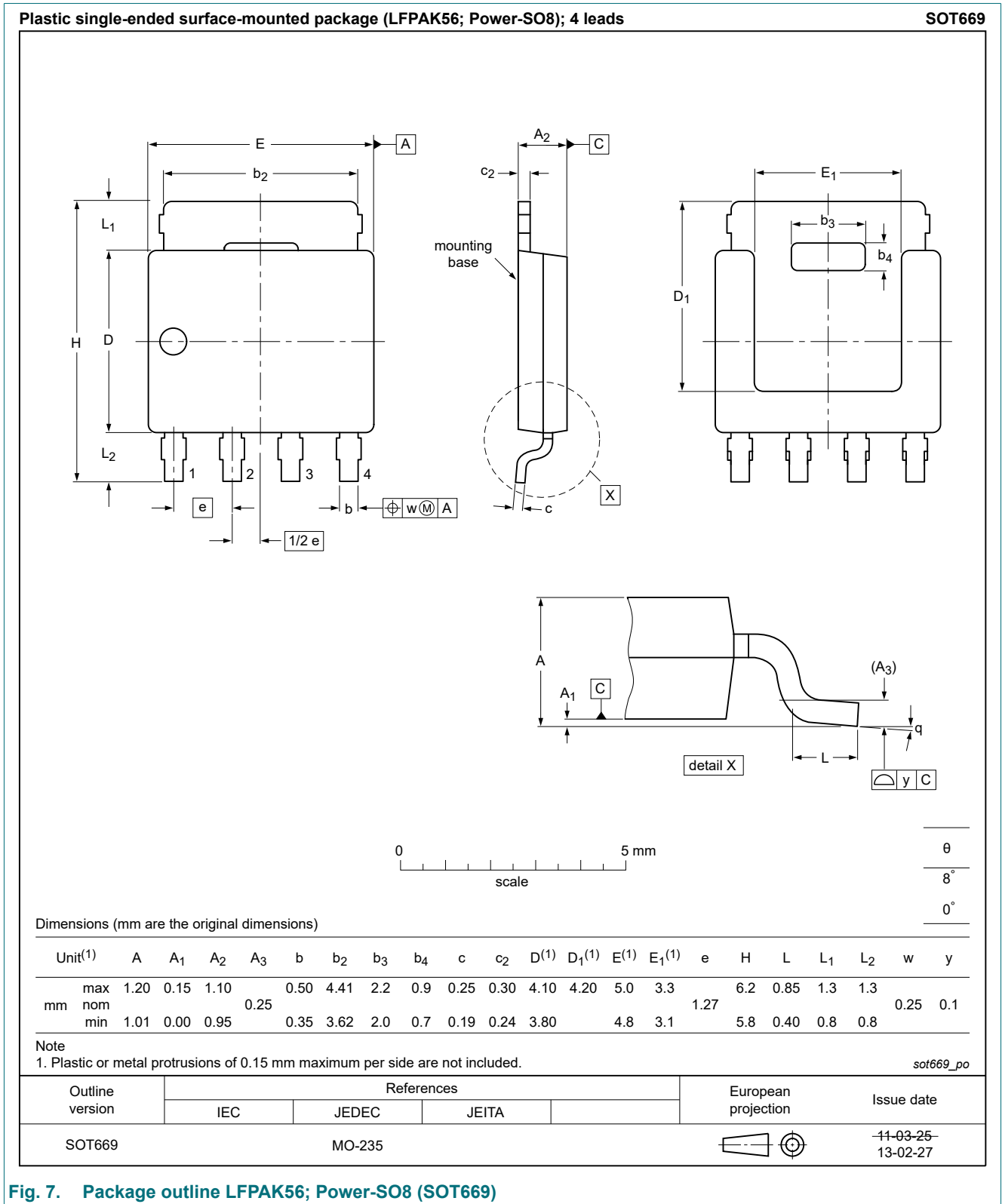


Fig. 7. Package outline LPAK56; Power-SO8 (SOT669)

11. Soldering

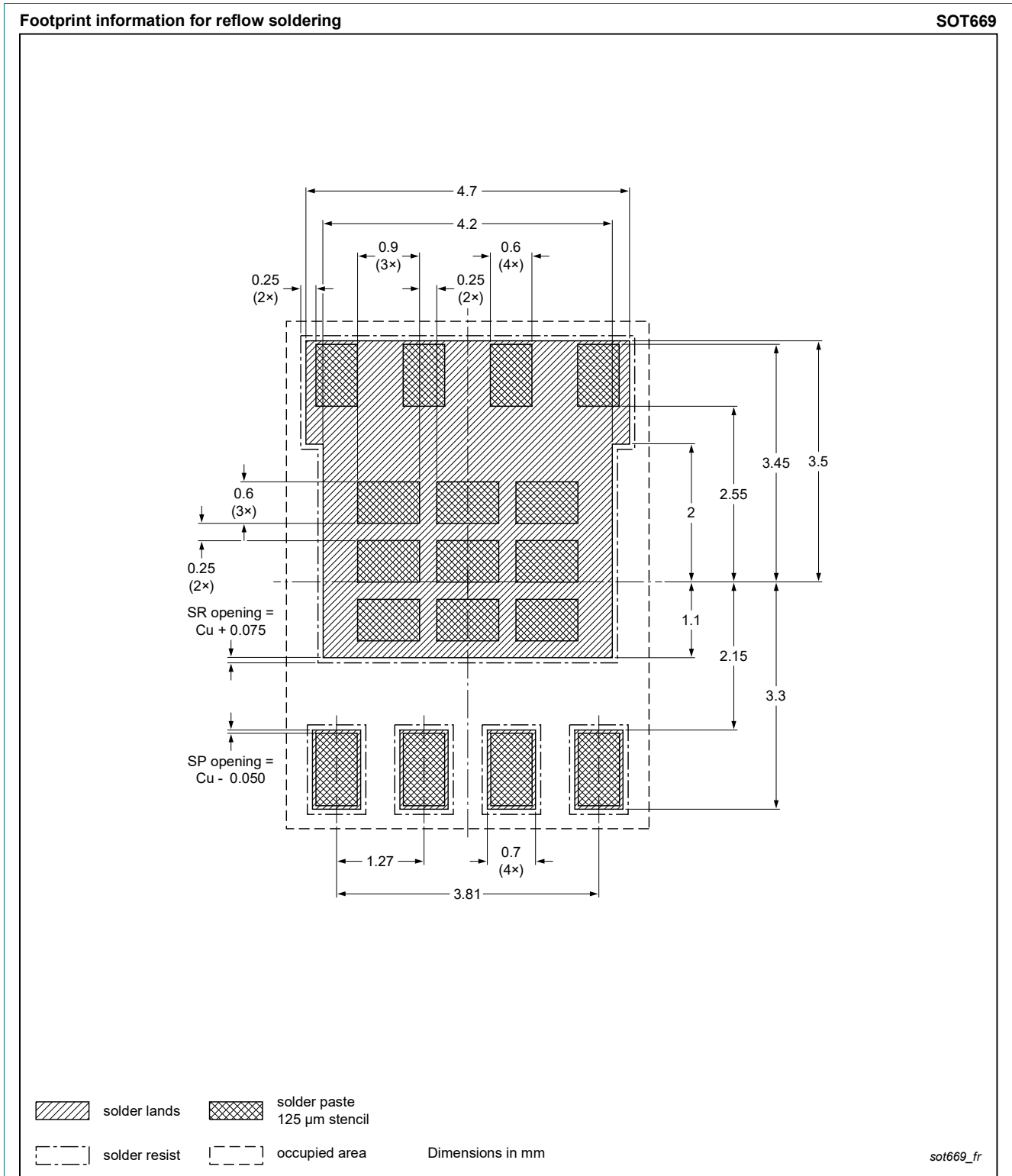
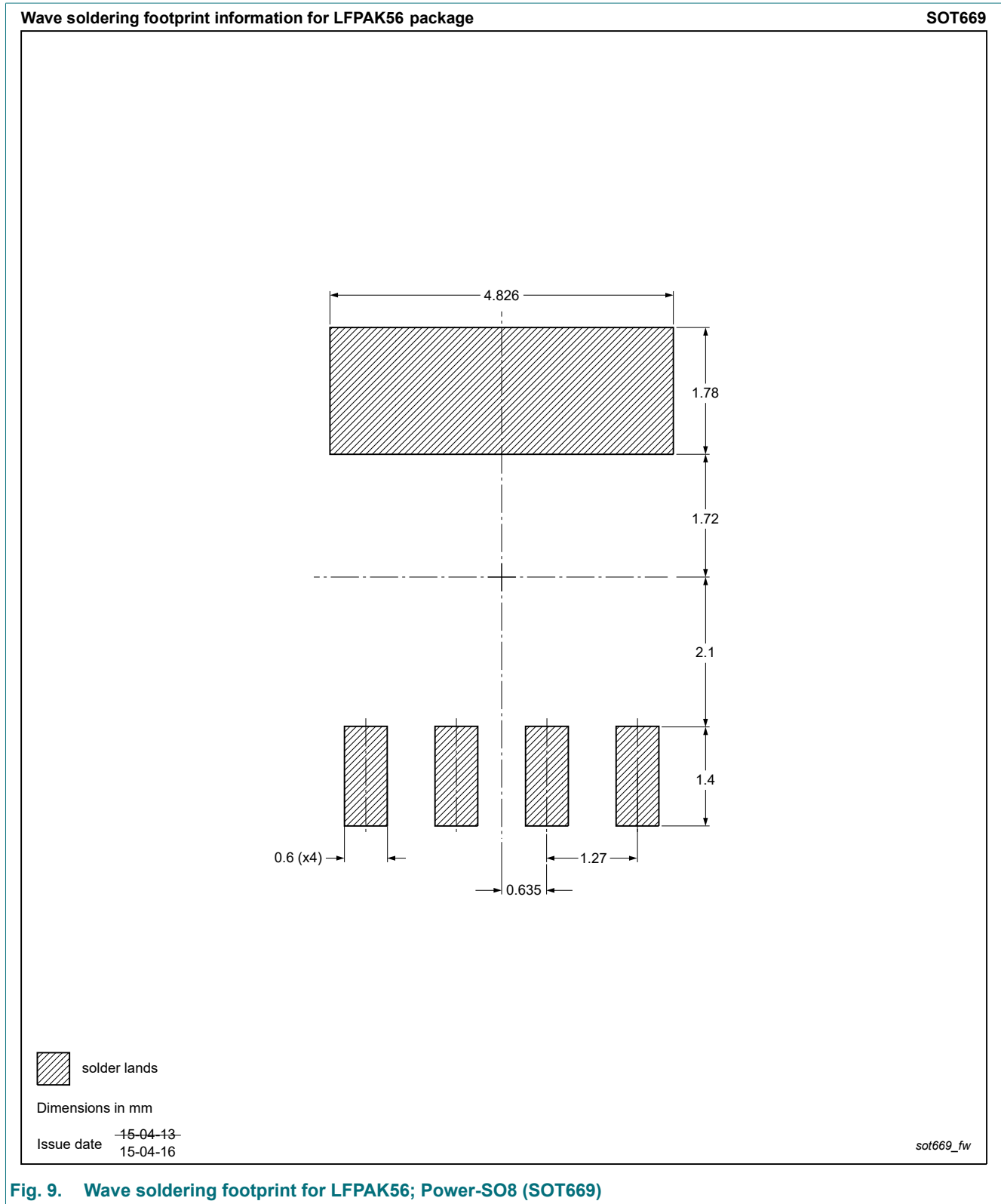


Fig. 8. Reflow soldering footprint for LFPAK56; Power-SO8 (SOT669)



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Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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- [2] The term 'short data sheet' is explained in section "Definitions".
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