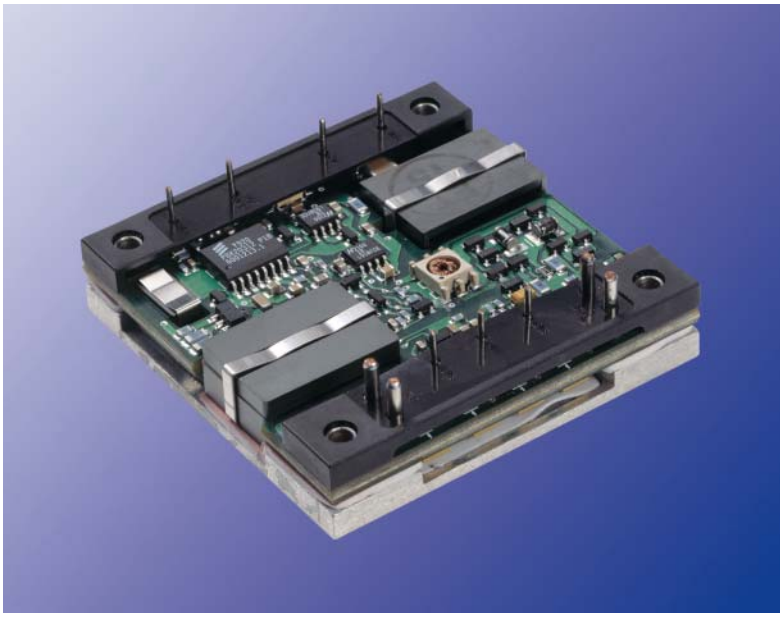
DC/DC converter
Input 36-75 Vdc
Output up to 80 A/300 W

Key Features

- "THE double P" extended Half-brick 61.5x61x12.7 mm (2.42x2.4x0.5 in)
- Low Output Ripple, 60 mVp-p Typ.
- Parallelable with no external components
- High efficiency, typ. 88 % at 1.8 Vout 80A (full) load
- 1500 Vdc input to output isolation, meets isolation requirements equivalent to Basic Insulation according to IEC/EN/UL 60950
- More than 3.7 million hours predicted MTBF at 90 °C case temperature



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The PKL 4000 Series of high efficiency DC/DC converters are designed to provide high quality on-board power solutions in distributed power architectures used in "Inter-networking" equipment in Wireless and Wired Communications and Datacom applications. The PKL 4000 Series is an extended version of the industry standard half brick footprint that has been enhanced to include two additional output pins for connection reliability and higher output current. The PKL Series uses the most advanced patented topology and synchronous rectification technology and achieves a typical efficiency up to 92%. This product features fast dynamic response times and low output ripple, which are important parameters when supplying low-voltage logics. Ericsson's PKL 4000 Series addresses the emerging telecom market for applications in the multi-service network by specifying the input voltage range in accordance with ETSI specifications. Included as standard features are over-voltage protection, under-voltage protection, over-temperature protection, soft-start, short circuit protection, remote sense, remote on/off, and industry standard output trim adjustment. The PKL 4000 Series also offers the flexibility of using optional heatsinks when needed, enabling reduced airflow, extended reliability, and higher ambient temperature operation. These converters are manufactured in highly automated manufacturing lines and meet world-class quality levels.
Ericsson Power Modules is an ISO 9001 (since 1991) and ISO14001 certified Supplier.

ERICSSON

Absolute Maximum Ratings

Characteristics		min	max	Unit
T_C	Operating Case Temperature PKL PKL4118B PIT	-40 -40	+100 +110	˚C
T_S	Storage temperature	-40	+125	˚C
V_I	Input voltage	-0.5	+80	Vdc
V_{ISO}	Isolation voltage (input to output test voltage)	1500		Vdc
V_{tr}	Input over voltage condition (100 ms)		100	Vdc
V_{RC}	Remote Control Voltage, pin 2	-0.5	15	Vdc
V_{adj}	Maximum input, pin 6. (measured from pin 1)	-0.5	$2xV_o$	Vdc

Note:

Stress in excess of Absolute Maximum Ratings may cause permanent damage. Absolute Maximum Ratings, sometimes referred to as no destruction limits, are normally tested with one parameter at a time exceeding the limits of Output data or Electrical Characteristics. If exposed to stress above these limits, function and performance may degrade in an unspecified manner.

Input T_C <$T_{C\ max}$ unless otherwise specified

Characteristics		Conditions	min	typ	max	Unit
V_I	Input voltage range [1)]		36		75	Vdc
V_{Ioff}	Turn-off input voltage	Ramping from higher voltage	30	32.5	35	Vdc
V_{Ion}	Turn-on input voltage	Ramping from lower voltage	32	34.4	36	Vdc
C_I	Input capacitance			2.18		µF
I_{Iac}	Reflected ripple current	5 Hz to 20 MHz, V_I = 53 V		10		A_{p-p}
P_{II}	Input idling power	I_o= 0, V_I = 53 V		4.14	4.46	W
P_{RC}	Input standby power (turned off with RC)	V_I = 53 V, RC activated			0.055	W

Environmental Characteristics

Characteristics			
Random Vibration	IEC 68-2-34E_d	Frequency Spectral density Duration	10 ... 500 Hz 0.025 g^2/Hz 10 min each direction
Sinusoidal Vibration	IEC 68-2-6 F_c	Frequency Amplitude Acceleration Number of cycles	10 ... 500 Hz 0.75 mm 10 g 10 in each axis
Shock (half sinus)	IEC 68-2-27 E_a	Peak acceleration Duration	100 g 6 ms
Temperature change	IEC 68-2-14 N_a	Temperature Number of cycles	-40 ... +100 ˚C 300
Heat/Humidity	IEC 68-2-3 C_a	Temperature Humidity Duration	+85 ˚C 85 % RH 1000 hours
Solder heat stability	IEC 68-2-20 1A	Temperature, solder Duration	260 ˚C 10 ...13 s
Resistance to cleaning solvents	IEC 68-2-45 XA Method 2	Water Isopropyl alcohol Glycol ether	+55 ±5 ˚C +35 ±5 ˚C +35 ±5 ˚C
Cold (in operation)	IEC 68-2-1 A_d	Temperature Duration	-45 ˚C 2 h
Storage test	IEC 68-2-2 B_a	Temperature Duration	+125 ˚C 1000 h

Safety

The PKL 4000 series DC/DC converters are designed in accordance with safety standards IEC/EN/UL 60 950, *Safety of Information Technology Equipment.*

The PKL 4000 series DC/DC converters are UL 60 950 recognized and certified in accordance with EN 60 950.

The DC/DC converter should be installed in the end-use equipment, in accordance with the requirements of the ultimate application. The input source must be isolated by minimum Basic Insulation from the primary circuit in accordance with IEC/EN/UL 60 950. If the input voltage to the DC/DC converter is 75 V dc or less, then the output remains SELV (Safety Extra Low Voltage) under normal and abnormal operating conditions. Single fault testing in the input power supply circuit should be performed with the DC/DC converter connected to demonstrate that the input voltage does not exceed 75 V dc. If the input power source circuit is a DC power system, the source may be treated as a TNV2 circuit and testing has demonstrated compliance with SELV limits and isolation requirements equivalent to Basic Insulation in accordance with IEC/EN/UL 60 950.

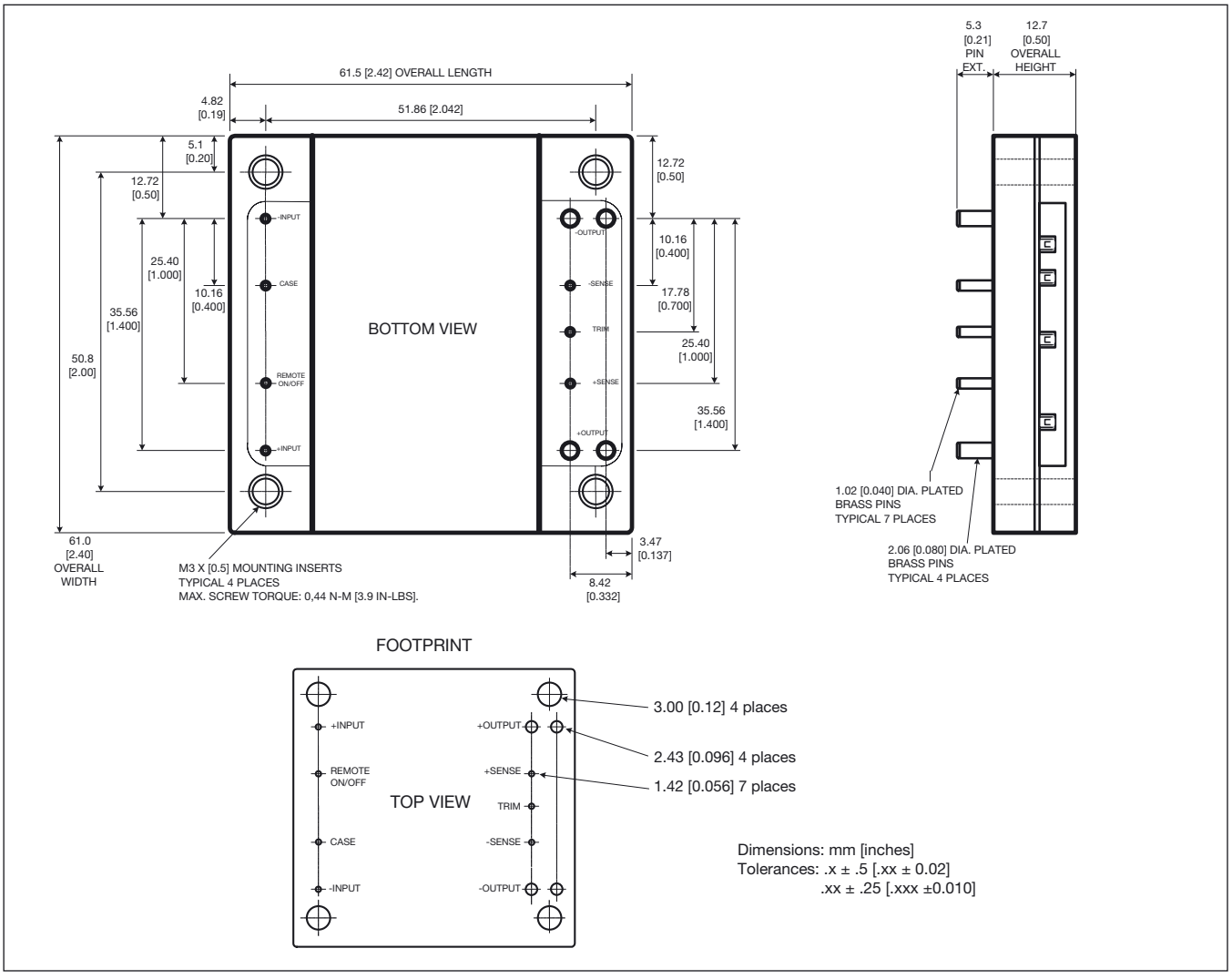
It is recommended that a fast blow fuse with a rating twice the maximum input current per selected product be used at the input of each DC/DC converter. If a fault occurs in the converter that imposes a short circuit on the input source, this fuse will provide the following functions:

- Isolate the faulty DC/DC converter from the input power source not to affect the operation of other parts of the system.
- Protect the distribution wiring from excessive current and power loss thus preventing hazardous overheating.

The galvanic isolation is verified in an electric strength test. The test voltage (V_{ISO}) between input and output is 1500 Vdc for 60 seconds. Leakage current is less than 1µA at nominal input voltage.

The flammability rating for all construction parts of the DC/DC converter meets UL 94V-0.

Mechanical Data

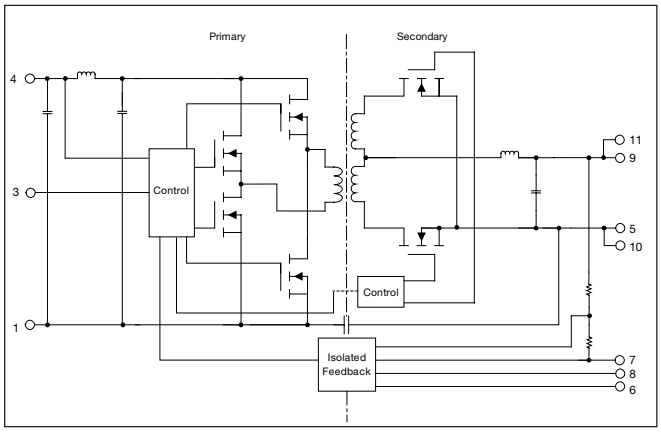


Connections

Pin	Designation	Function
1	- In	Negative Input
2	Case	Connected to baseplate
3	RC	Remote Control
4	+ In	Positive Input
5, 10	- Out	Negative Output
6	- Sen	Negative Sense
7	V_{adj}	Output voltage adjust
8	+ Sen	Positive Sense
9, 11	+ Out	Positive Output

For more information about the functions see Operating Information

Fundamental Circuit Diagram



Weight

PKL 4000 Series, 110 g

Pins

Material: Brass Alloy

Plating: Tin/Lead over Nickel

PKL 4118 PIT Output

T_C = —40…+100°C, V= 36 ...75V, sense pins connected to output pins unless otherwise specified.

Characteristics		Conditions	Output			Unit
			min	typ	max	
V_{Oi}	Output voltage initial setting and accuracy	T_C = +25 °C, V_I = 53 V, I_O = I_{Omax}	1.77	1.8	1.83	V
	Output adjust range	I_O = I_{Omax}	1.44		2.00	V
V_O	Output voltage tolerance band	I_O = 0.1...1 x I_{Omax}	1.746		1.854	V
	Idling voltage	I_O = 0	1.746		1.900	V
	Line regulation	I_O = I_{Omax}		5	15	mV
	Load regulation	V_I = 53 V, I_O = 0.01...1 x I_{Omax}		5	15	mV
V_{tr}	Load transient voltage deviation	I_O = 0.1...1 x I_{Omax} , V_I = 53 V Load step = 0.25 x I_{Omax} di/dt = 1A/µs		+200 -200		mV
t_{tr}	Load transient recovery time	I_O = 0.1...1 x I_{Omax} , V_I = 53 loadstep = 0.25x I_{Omax}		220		µs
t_r	Ramp-up time	I_O = 0.1...0.9 x V_O		12	16	ms
t_s	Start-up time	From V_I connected to V_O = 0.9 x V_{OI}		16	20	ms
I_O	Output current		0		60	A
P_{Omax}	Max output power	At V_O = V_{Onom}	108			W
I_{lim}	Current limit threshold	T_C < T_{Cmax}	65.2	66.5	68.5	A
I_{sc}	Short circuit current	T_C = 25 °C	69	70	71	A
V_{Oac}	Output ripple & noise	I_O = I_{Omax} , f < 4-20 MHz			100	mV_{p-p}
SVR	Supply voltage rejection (ac)	f = 100 Hz sinewave , 1 Vp-p , V_I = 53 V	53			dB
OVP	Over voltage protection	V_I = 53 V		2.51		V

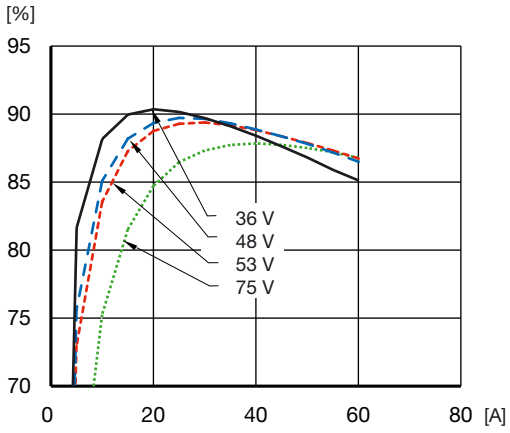
Miscellaneous

T_C = —40…+100°C, V= 36 ...75V, sense pins connected to output pins unless otherwise specified.

Characteristics		Conditions	min	typ	max	Unit
η	Efficiency - 50% load	T_C = +25 °C, V_I = 53 V, I_O = 0.5 x I_{Omax}		89		%
η	Efficiency - 100% load	T_C = +25 °C, V_I = 53 V, I_O = I_{Omax}		86.5		%
P_d	Power Dissipation	T_C = +25 °C, V_I = 53 V, I_O = I_{Omax}		18		W
f_s	Switching frequency	I_O = 0 ... 1.0 x I_{Omax}		150		kHz
I_{Imax}	Maximum input current	1.1 x V_{Oi} x I_{Omax} / η / V_{Imin}			3.9	A

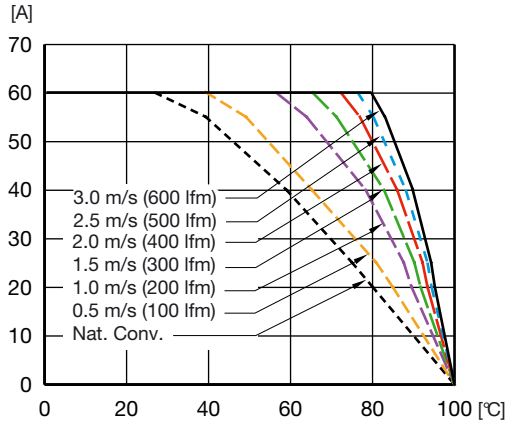
PKL 4118 PIT Typical Characteristics

Efficiency



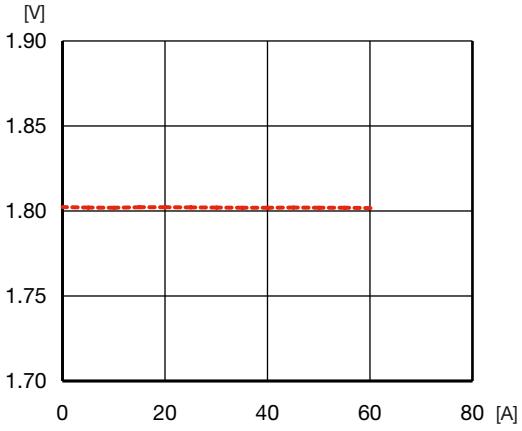
Efficiency vs. load current and input voltage at T_C = +25 °C

Output Current Derating



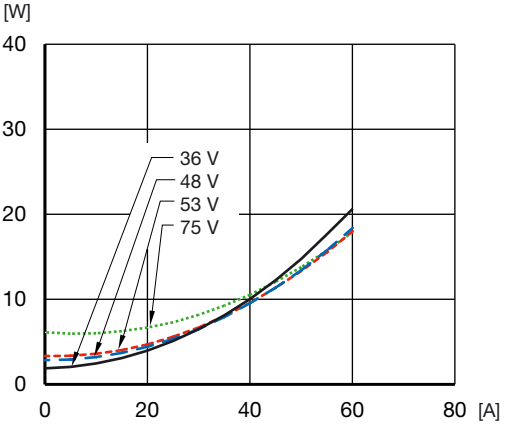
Available load current vs. ambient air temperature and airflow at V_{in} = 53 V.

Output Characteristic



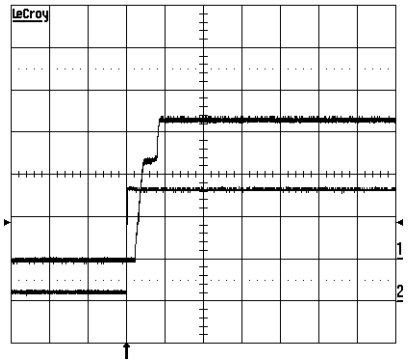
Output voltage vs. load current at T_C = +25 °C, V_{in} = 53 V.

Power Dissipation



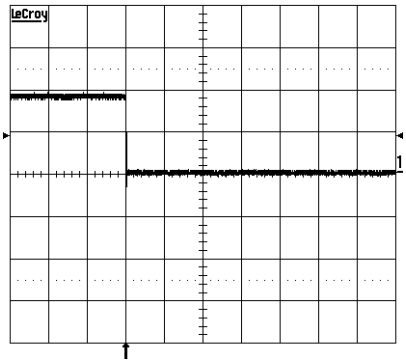
Dissipated power vs. load current and input voltage at T_C = +25 °C

Start-Up



Start-up at I_O = 60 A resistive load at T_C = +25 °C, V_{in} = 53 V. Start enabled by connecting V_{in}.
Top trace: output voltage (1 V/div.).
Bottom trace: input voltage (20 V/div.).
Time scale: 20 ms/div.

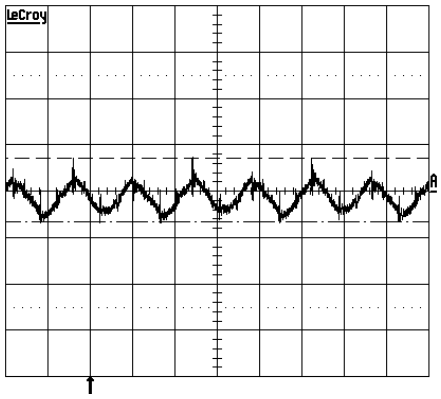
Turn-Off



Turn-off at I_O = 60 A resistive load at T_C = +25 °C, V_{in} = 53 V. Turn-off enabled by disconnecting V_{in}.
Trace: output voltage (1 V/div.).
Time scale: 5 ms/div.

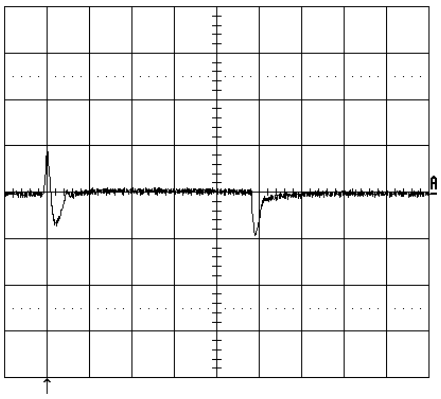
PKL 4118 PIT Typical Characteristics

Output Ripple



Output voltage ripple (50 mV/div.) at T_C = +25 °C
V_{in} = 53 V, I_O = 60 A resistive load.
Band width = 20 MHz.
Time scale: 2 µs/div.

Transient



Output voltage response to load current step-change (15-45-15 A) at T_C = +25 °C, V_{in} = 53 V.
Trace: output voltage (420 mV/div.).
dI/dt = 4 A/µs
Time scale: 100 µs/div.

Output Voltage Adjust

The resistor value for an adjusted output voltage is calculated by using the following equations:

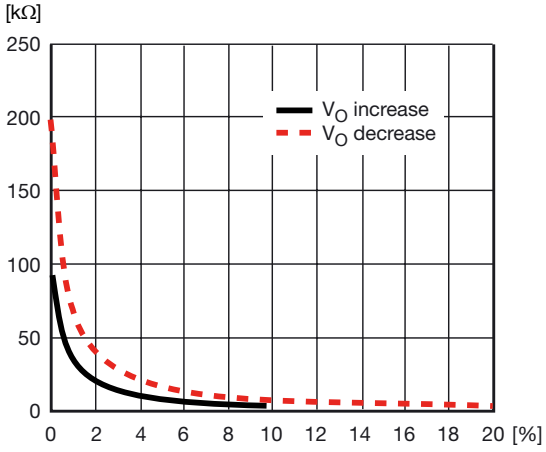
Output Voltage Adjust Upwards, Increase:
R_{adj}= [(V_O(100+Δ%)/(1.225Δ%))-(100+2Δ%)/Δ%] kOhm

Output Voltage Adjust Downwards, Decrease:
R_{adj}= [100/Δ%-2] kOhm

Ex. Increase 5% to: 1.89 V_{dc}
(1.8(100+5)/(1.225*5)-(100+2*5)/5 = 8.8 kOhm

Ex. Decrease 5% to: 1.71 V_{dc}
(100/5)-2= 18 kOhm

Output Voltage Adjust



Output voltage adjust resistor value vs. percentage change.

PKL 4118B PIT Output

T_C = —40…+110°C, V= 36 ...75V, sense pins connected to output pins unless otherwise specified.

Characteristics		Conditions	Output			Unit
			min	typ	max	
V_{Oi}	Output voltage initial setting and accuracy	T_C = +25 °C, V_I = 53 V, I_O = I_{Omax}	1.77	1.8	1.83	V
	Output adjust range	I_O = I_{Omax}	1.44		2.00	V
V_O	Output voltage tolerance band	I_O = 0.1...1 x I_{Omax}	1.746		1.854	V
	Idling voltage	I_O = 0	1.746		1.900	V
	Line regulation	I_O = I_{Omax}		5	15	mV
	Load regulation	V_I = 53 V, I_O = 0.01...1 x I_{Omax}		5	15	mV
V_{tr}	Load transient voltage deviation	I_O = 0.1...1 x I_{Omax} , V_I = 53 V Load step = 0.25 x I_{Omax} di/dt = 1A/µs		+200 -200		mV
t_{tr}	Load transient recovery time	I_O = 0.1...1 x I_{Omax} , V_I = 53 loadstep = 0.25x I_{Omax}		220		µs
t_r	Ramp-up time	I_O = 0.1...0.9 x V_O		16	20	ms
t_s	Start-up time	From V_I connected to V_O = 0.9 x V_{OI}		20	30	ms
I_O	Output current		0		80	A
P_{Omax}	Max output power	At V_O = V_{Onom}	144			W
I_{lim}	Current limit threshold	T_C < T_{Cmax}	92.5	93.0	93.5	A
I_{sc}	Short circuit current	T_C = 25 °C	96	97	98	A
V_{Oac}	Output ripple & noise	I_O = I_{Omax} , f < 4-20 MHz			100	mV_{p-p}
SVR	Supply voltage rejection (ac)	f = 100 Hz sinewave , 1 Vp-p , V_I = 53 V	53			dB
OVP	Over voltage protection	V_I = 53 V		2.51		V

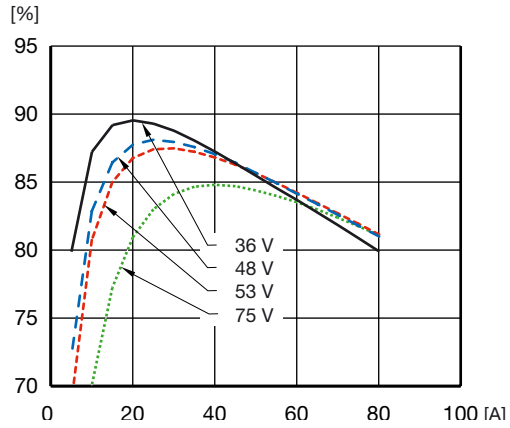
Miscellaneous

T_C = —40…+110°C, V= 36 ...75V, sense pins connected to output pins unless otherwise specified.

Characteristics		Conditions	min	typ	max	Unit
η	Efficiency - 50% load	T_C = +25 °C, V_I = 53 V, I_O = 0.5 x I_{Omax}		88		%
η	Efficiency - 100% load	T_C = +25 °C, V_I = 53 V, I_O = I_{Omax}		84.5		%
P_d	Power Dissipation	T_C = +25 °C, V_I = 53 V, I_O = I_{Omax}		33.6		W
f_s	Switching frequency	I_O = 0 ... 1.0 x I_{Omax}		150		kHz
I_{Imax}	Maximum input current	1.1 x V_{Oi} x I_{Omax} / η / V_{Imin}			5.2	A

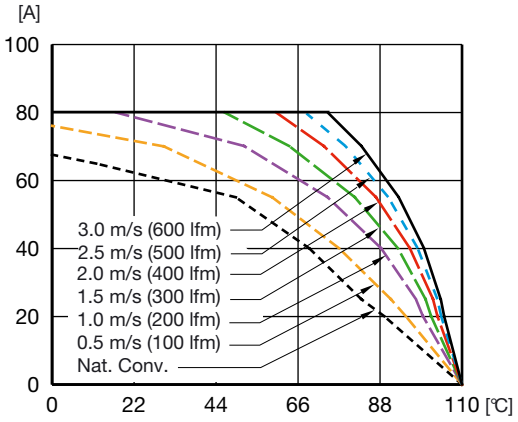
PKL 4118B PIT Typical Characteristics

Efficiency



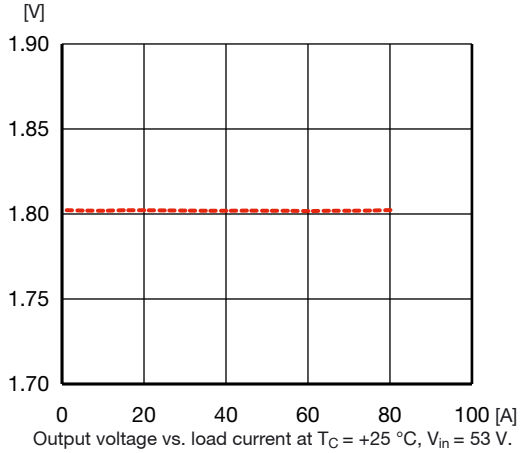
Efficiency vs. load current and input voltage at T_C = +25 °C

Output Current Derating



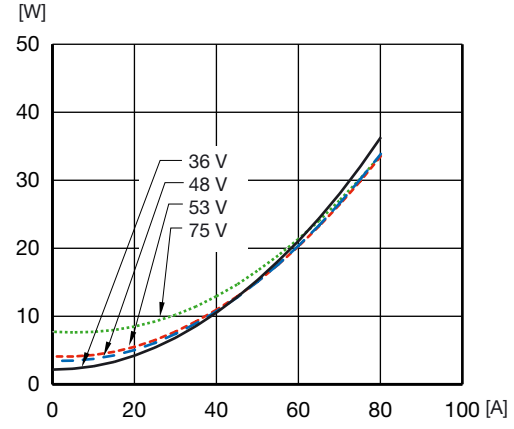
Available load current vs. ambient air temperature and airflow at V_{in} = 53 V.

Output Characteristic



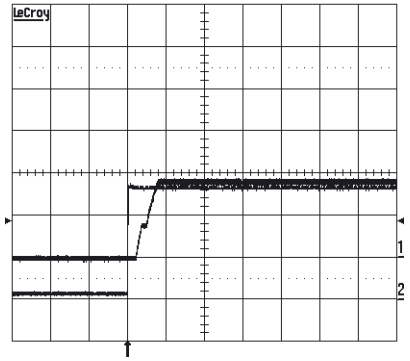
Output voltage vs. load current at T_C = +25 °C, V_{in} = 53 V.

Power Dissipation



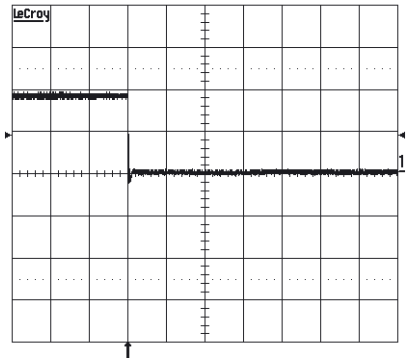
Dissipated power vs. load current and input voltage at T_C = +25 °C

Start-Up



Start-up at I_O = 80 A resistive load at T_C = +25 °C, V_{in} = 53 V. Start enabled by connecting V_{in}.
Top trace: output voltage (1 V/div.).
Bottom trace: input voltage (20 V/div.).
Time scale: 20 ms/div.

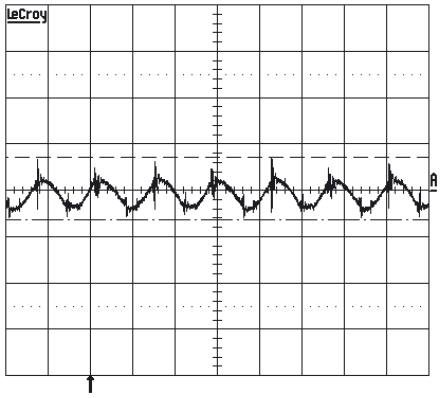
Turn-Off



Turn-off at I_O = 80 A resistive load at T_C = +25 °C, V_{in} = 53 V. Turn-off enabled by disconnecting V_{in}.
Trace: output voltage (1 V/div.).
Time scale: 1 ms/div.

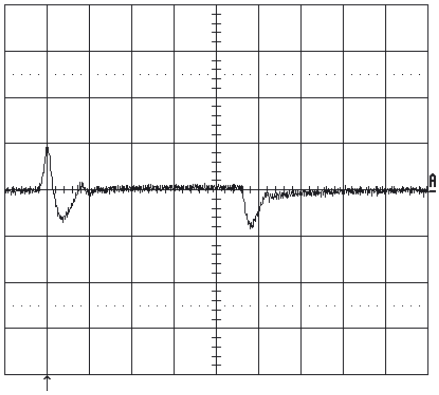
PKL 4118B PIT Typical Characteristics

Output Ripple



Output voltage ripple (100 mV/div.) at T_C = +25 °C
V_{in} = 53 V, I_O = 80 A resistive load.
Band width = 20 MHz.
Time scale: 2 µs / div.

Transient



Output voltage response to load current step-change (20-60-20 A) at T_C = +25 °C, V_{in} = 53 V.
Trace: output voltage (420 mV/div.).
dI/dt = 4 A/µs
Time scale: 50 µs/div.

Output Voltage Adjust

The resistor value for an adjusted output voltage is calculated by using the following equations:

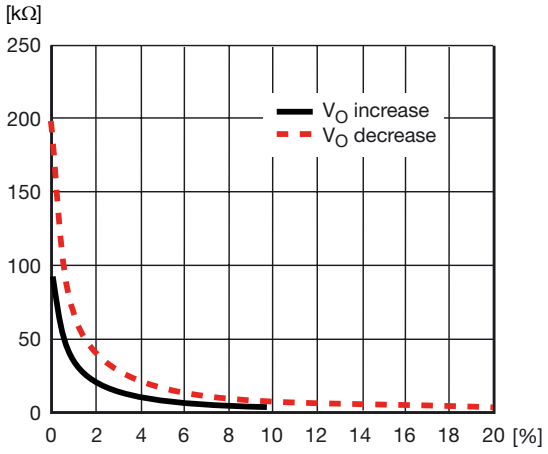
Output Voltage Adjust Upwards, Increase:
R_{adj}= [(V_O(100+Δ%)/(1.225Δ%))-(100+2Δ%)/Δ%] kOhm

Output Voltage Adjust Downwards, Decrease:
R_{adj}= [100/Δ%-2] kOhm

Ex. Increase 5% to: 1.89 V_{dc}
(1.8(100+5)/(1.225*5)-(100+2*5)/5 = 8.8 kOhm

Ex. Decrease 5% to: 1.71 V_{dc}
(100/5)-2= 18 kOhm

Output Voltage Adjust



Output voltage adjust resistor value vs. percentage change.

PKL 4119 PIT Output

T_C = —40…+100°C, V= 36 ...75V, sense pins connected to output pins unless otherwise specified.

Characteristics		Conditions	Output			Unit
			min	typ	max	
V_{Oi}	Output voltage initial setting and accuracy	T_C = +25 °C, V_I = 53 V, I_O = I_{Omax}	2.45	2.5	2.55	V
	Output adjust range	I_O = I_{Omax}	2.00		2.75	V
V_O	Output voltage tolerance band	I_O = 0.1...1 x I_{Omax}	2.42		2.58	V
	Idling voltage	I_O = 0	2.38		2.63	V
	Line regulation	I_O = I_{Omax}		5	15	mV
	Load regulation	V_I = 53 V, I_O = 0.01...1 x I_{Omax}		5	15	mV
V_{tr}	Load transient voltage deviation	I_O = 0.1...1 x I_{Omax} , V_I = 53 V Load step = 0.25 x I_{Omax} di/dt = 1A/µs		+200 -200		mV
t_{tr}	Load transient recovery time	I_O = 0.1...1 x I_{Omax} , V_I = 53 loadstep = 0.25x I_{Omax}		200		µs
t_r	Ramp-up time	I_O = 0.1...0.9 x V_O		30		ms
t_s	Start-up time	From V_I connected to V_O = 0.9 x V_{OI}		20	30	ms
I_O	Output current		0		50	A
P_{Omax}	Max output power	At V_O = V_{Onom}	125			W
I_{lim}	Current limit threshold	T_C < T_{Cmax}	51	54.5	62	A
I_{sc}	Short circuit current	T_C = 25 °C		55	69	A
V_{Oac}	Output ripple & noise	I_O = I_{Omax} , f < 4-20 MHz		80	150	mV_{p-p}
SVR	Supply voltage rejection (ac)	f = 100 Hz sinewave , 1 Vp-p , V_I = 53 V	50			dB
OVP	Over voltage protection	V_I = 53 V	3.0		4.0	V

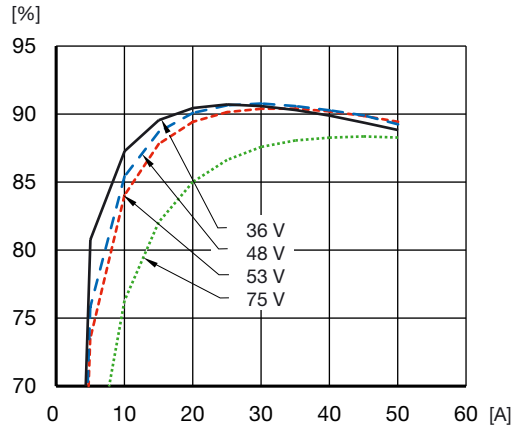
Miscellaneous

T_C = —40…+100°C, V= 36 ...75V, sense pins connected to output pins unless otherwise specified.

Characteristics		Conditions	min	typ	max	Unit
η	Efficiency - 50% load	T_C = +25 °C, V_I = 53 V, I_O = 0.5 x I_{Omax}		90		%
η	Efficiency - 100% load	T_C = +25 °C, V_I = 53 V, I_O = I_{Omax}		89		%
P_d	Power Dissipation	T_C = +25 °C, V_I = 53 V, I_O = I_{Omax}		15.4		W
f_s	Switching frequency	I_O = 0 ... 1.0 x I_{Omax}		200		kHz
I_{Imax}	Maximum input current	1.1 x V_{Oi} x I_{Omax} / η / V_{Imin}			4.3	A

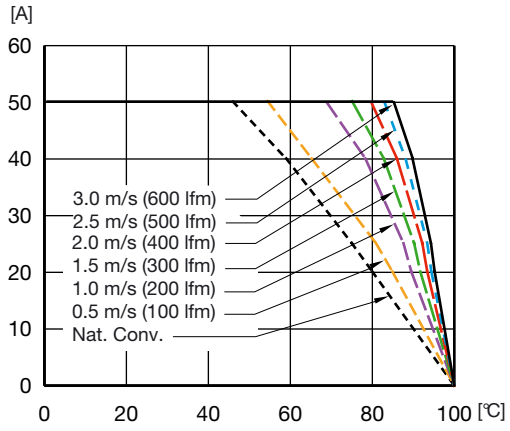
PKL 4119 PIT Typical Characteristics

Efficiency



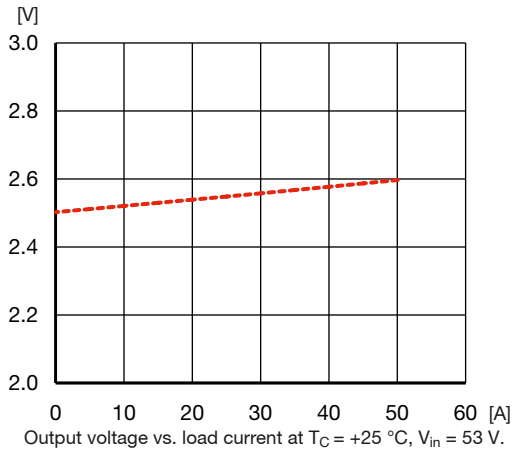
Efficiency vs. load current and input voltage at T_C = +25 °C

Output Current Derating



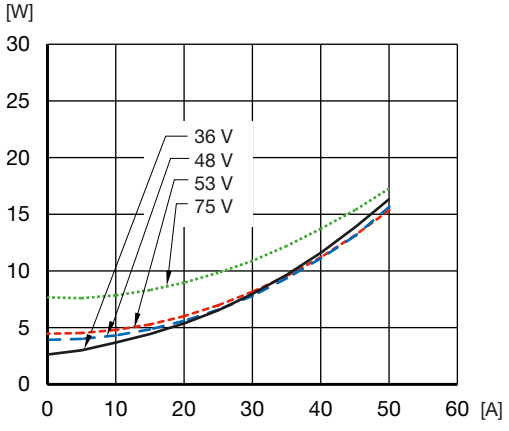
Available load current vs. ambient air temperature and airflow at V_{in} = 53 V.

Output Characteristic



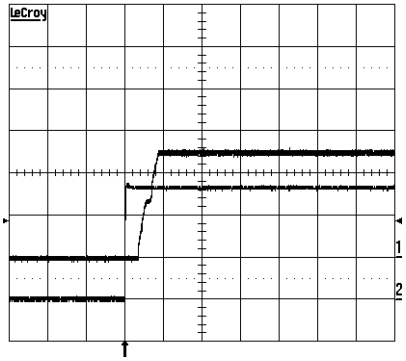
Output voltage vs. load current at T_C = +25 °C, V_{in} = 53 V.

Power Dissipation



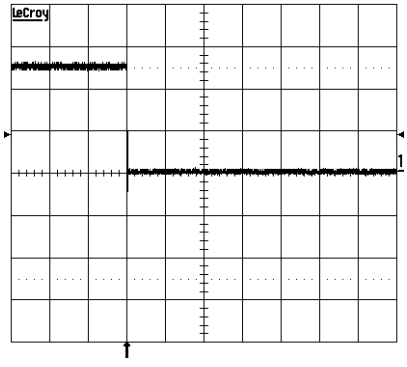
Dissipated power vs. load current and input voltage at T_C = +25 °C

Start-Up



Start-up at I_O = 80 A resistive load at T_C = +25 °C, V_{in} = 53 V. Start enabled by connecting V_{in}.
Top trace: output voltage (1 V/div.).
Bottom trace: input voltage (20 V/div.).
Time scale: 20 ms/div.

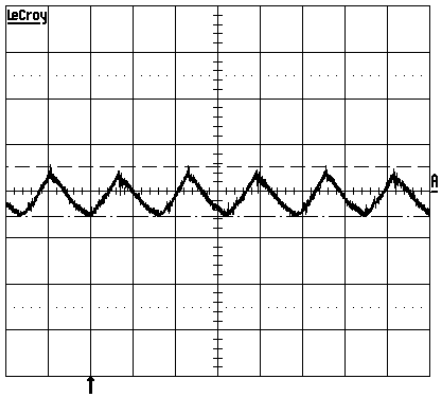
Turn-Off



Turn-off at I_O = 80 A resistive load at T_C = +25 °C, V_{in} = 53 V. Turn-off enabled by disconnecting V_{in}.
Trace: output voltage (1 V/div.).
Time scale: 5 ms/div.

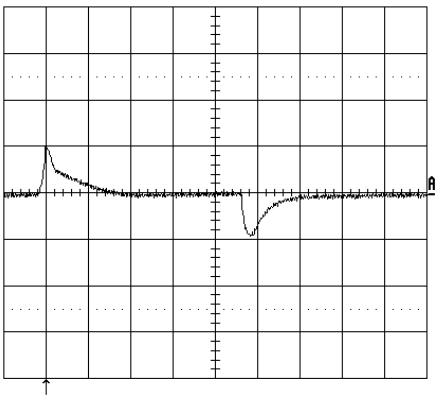
PKL 4119 PIT Typical Characteristics

Output Ripple



Output voltage ripple (50 mV/div.) at T_C = +25 °C
V_{in} = 53 V, I_O = 80 A resistive load.
Band width = 20 MHz.
Time scale: 2 µs / div.

Transient



Output voltage response to load current step-change (20-60-20 A) at T_C = +25 °C, V_{in} = 53 V.
Trace: output voltage (420 mV/div.).
dI/dt = 4 A/µs
Time scale: 100 µs/div.

Output Voltage Adjust

The resistor value for an adjusted output voltage is calculated by using the following equations:

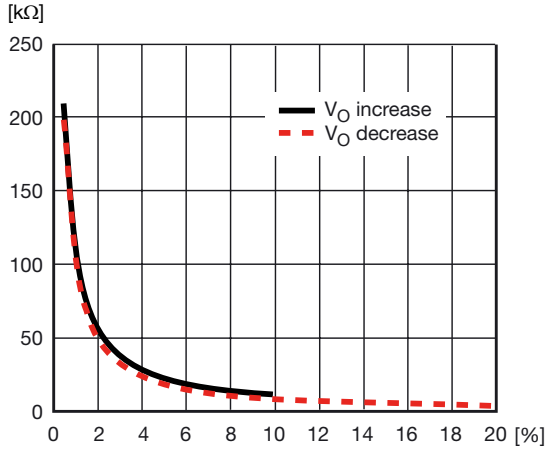
Output Voltage Adjust Upwards, Increase:
R_{adj}= [(V_O(100+Δ%)/(1.225Δ%))-(100+2Δ%)/Δ%] kOhm

Output Voltage Adjust Downwards, Decrease:
R_{adj}= [100/Δ%-2] kOhm

Ex. Increase 5% to: 2.625 V_{dc}
(2.5(100+5)/(1.225*5)-(100+2*5)/5 = 21 kOhm

Ex. Decrease 5% to: 2.375 V_{dc}
(100/5)-2= 18 kOhm

Output Voltage Adjust



Output voltage adjust resistor value vs. percentage change.

PKL 4119A PIT Output

T_C = —40…+100°C, V= 36 ...75V, sense pins connected to output pins unless otherwise specified.

Characteristics		Conditions	Output			Unit
			min	typ	max	
V_{Oi}	Output voltage initial setting and accuracy	T_C = +25 °C, V_I = 53 V, I_O = I_{Omax}	2.45	2.5	2.55	V
	Output adjust range	I_O = I_{Omax}	2.00		2.75	V
V_O	Output voltage tolerance band	I_O = 0.1...1 x I_{Omax}	2.42		2.58	V
	Idling voltage	I_O = 0	2.38		2.63	V
	Line regulation	I_O = I_{Omax}		5	15	mV
	Load regulation	V_I = 53 V, I_O = 0.01...1 x I_{Omax}		5	15	mV
V_{tr}	Load transient voltage deviation	I_O = 0.1...1 x I_{Omax} , V_I = 53 V Load step = 0.25 x I_{Omax} di/dt = 1A/µs		+200 -200		mV
t_{tr}	Load transient recovery time	I_O = 0.1...1 x I_{Omax} , V_I = 53 loadstep = 0.25x I_{Omax}		200		µs
t_r	Ramp-up time	I_O = 0.1...0.9 x V_O		30		ms
t_s	Start-up time	From V_I connected to V_O = 0.9 x V_{OI}		20	30	ms
I_O	Output current		0		60	A
P_{Omax}	Max output power	At V_O = V_{Onom}	150			W
I_{lim}	Current limit threshold	T_C < T_{Cmax}	61	64.5	72	A
I_{sc}	Short circuit current	T_C = 25 °C		65	79	A
V_{Oac}	Output ripple & noise	I_O = I_{Omax} , f < 4-20 MHz		80	150	mV_{p-p}
SVR	Supply voltage rejection (ac)	f = 100 Hz sinewave , 1 Vp-p , V_I = 53 V	50			dB
OVP	Over voltage protection	V_I = 53 V	3.0		4.0	V

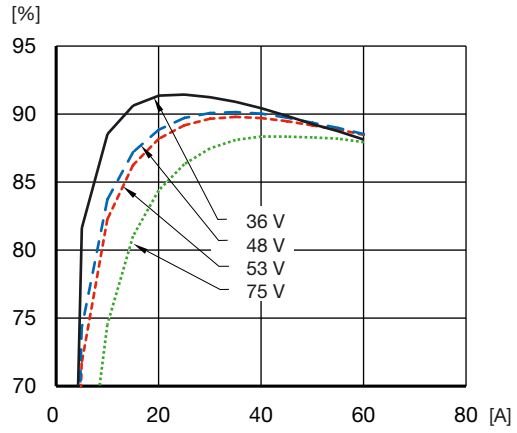
Miscellaneous

T_C = —40…+100°C, V= 36 ...75V, sense pins connected to output pins unless otherwise specified.

Characteristics		Conditions	min	typ	max	Unit
η	Efficiency - 50% load	T_C = +25 °C, V_I = 53 V, I_O = 0.5 x I_{Omax}		89.5		%
η	Efficiency - 100% load	T_C = +25 °C, V_I = 53 V, I_O = I_{Omax}		88.5		%
P_d	Power Dissipation	T_C = +25 °C, V_I = 53 V, I_O = I_{Omax}		19.5		W
f_s	Switching frequency	I_O = 0 ... 1.0 x I_{Omax}		200		kHz
I_{Imax}	Maximum input current	1.1 x V_{Oi} x I_{Omax} / η / V_{Imin}			5.2	A

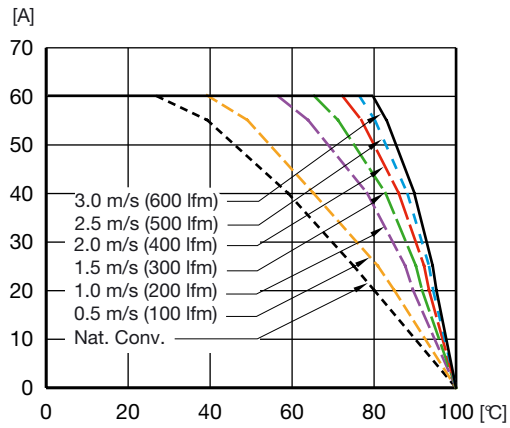
PKL 4119A PIT Typical Characteristics

Efficiency



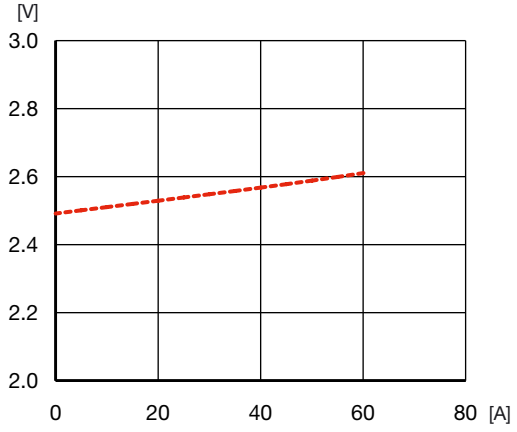
Efficiency vs. load current and input voltage at T_C = +25 °C

Output Current Derating



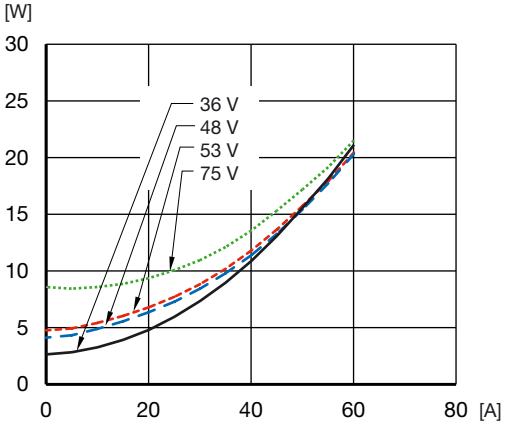
Available load current vs. ambient air temperature and airflow at V_{in} = 53 V.

Output Characteristic



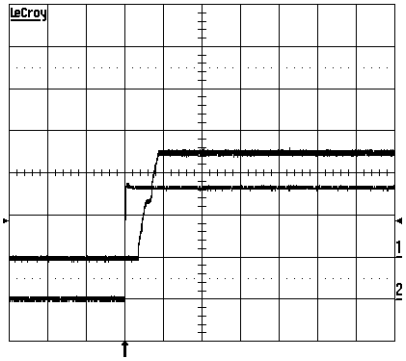
Output voltage vs. load current at T_C = +25 °C, V_{in} = 53 V.

Power Dissipation



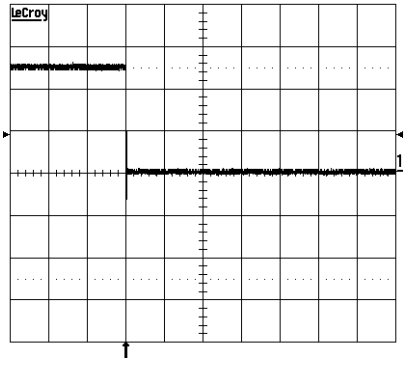
Dissipated power vs. load current and input voltage at T_C = +25 °C

Start-Up



Start-up at I_O = 50 A resistive load at T_C = +25 °C, V_{in} = 53 V. Start enabled by connecting V_{in}.
Top trace: output voltage (1 V/div.).
Bottom trace: input voltage (20 V/div.).
Time scale: 20 ms/div.

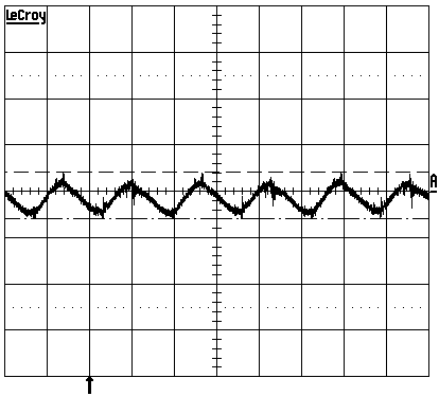
Turn-Off



Turn-off at I_O = 50 A resistive load at T_C = +25 °C, V_{in} = 53 V. Turn-off enabled by disconnecting V_{in}.
Trace: output voltage (1 V/div.).
Time scale: 5 ms/div.

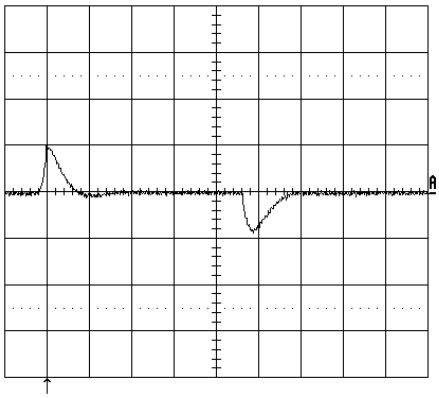
PKL 4119A PIT Typical Characteristics

Output Ripple



Output voltage ripple (50mV/div.) at T_C = +25 °C
V_{in} = 53 V, I_O = 50 A resistive load.
Band width = 20 MHz.
Time scale: 2 µs / div.

Transient



Output voltage response to load current step-change (12.5-37.5-12.5 A) at T_C = +25 °C, V_{in} = 53 V.
Trace: output voltage (420 mV/div.).
dI/dt = 4 A/µs
Time scale: 50 µs/div.

Output Voltage Adjust

The resistor value for an adjusted output voltage is calculated by using the following equations:

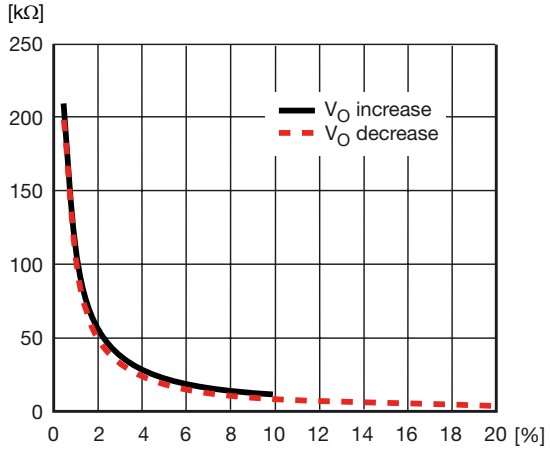
Output Voltage Adjust Upwards, Increase:
R_{adj}= [(V_O(100+Δ%)/(1.225Δ%))-(100+2Δ%)/Δ%] kOhm

Output Voltage Adjust Downwards, Decrease:
R_{adj}= [100/Δ%-2] kOhm

Ex. Increase 5% to: 2.625 V_{dc}
(2.5(100+5)/(1.225*5)-(100+2*5)/5 = 21 kOhm

Ex. Decrease 5% to: 2.375 V_{dc}
(100/5)-2= 18 kOhm

Output Voltage Adjust



Output voltage adjust resistor value vs. percentage change.

PKL 4219A PIT Output

T_C = —40…+100°C, V= 36 ...75V, sense pins connected to output pins unless otherwise specified.

Characteristics		Conditions	Output			Unit
			min	typ	max	
V_{Oi}	Output voltage initial setting and accuracy	T_C = +25 °C, V_I = 53 V, I_O = I_{Omax}	2.45	2.5	2.55	V
	Output adjust range	I_O = I_{Omax}	2.00		2.75	V
V_O	Output voltage tolerance band	I_O = 0.1...1 x I_{Omax}	2.42		2.58	V
	Idling voltage	I_O = 0	2.45		2.55	V
	Line regulation	I_O = I_{Omax}		5	15	mV
	Load regulation	V_I = 53 V, I_O = 0.01...1 x I_{Omax}		5	15	mV
V_{tr}	Load transient voltage deviation	I_O = 0.1...1 x I_{Omax} , V_I = 53 V Load step = 0.25 x I_{Omax} di/dt = 1A/µs		+120 -120		mV
t_{tr}	Load transient recovery time	I_O = 0.1...1 x I_{Omax} , V_I = 53 loadstep = 0.25x I_{Omax}		100		µs
t_r	Ramp-up time	I_O = 0.1...0.9 x V_O		20	40	ms
t_s	Start-up time	From V_I connected to V_O = 0.9 x V_{OI}		20	40	ms
I_O	Output current		0		80	A
P_{Omax}	Max output power	At V_O = V_{Onom}	200			W
I_{lim}	Current limit threshold	T_C < T_{Cmax}		92	97	A
I_{sc}	Short circuit current	T_C = 25 °C		95	98	A
V_{Oac}	Output ripple & noise	I_O = I_{Omax} , f < 4-20 MHz			110	mV_{p-p}
SVR	Supply voltage rejection (ac)	f = 100 Hz sinewave , 1 Vp-p , V_I = 53 V	50			dB
OVP	Over voltage protection	V_I = 53 V	3.0		4.0	V

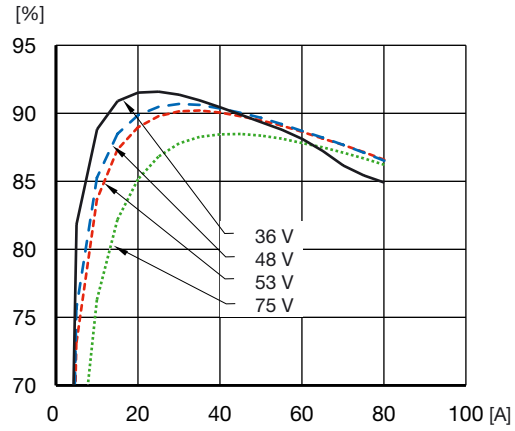
Miscellaneous

T_C = —40…+100°C, V= 36 ...75V, sense pins connected to output pins unless otherwise specified.

Characteristics		Conditions	min	typ	max	Unit
η	Efficiency - 50% load	T_C = +25 °C, V_I = 53 V, I_O = 0.5 x I_{Omax}		90		%
η	Efficiency - 100% load	T_C = +25 °C, V_I = 53 V, I_O = I_{Omax}		86.5		%
P_d	Power Dissipation	T_C = +25 °C, V_I = 53 V, I_O = I_{Omax}		32.5		W
f_s	Switching frequency	I_O = 0 ... 1.0 x I_{Omax}		180		kHz
I_{Imax}	Maximum input current	1.1 x V_{Oi} x I_{Omax} / η / V_{Imin}			7.0	A

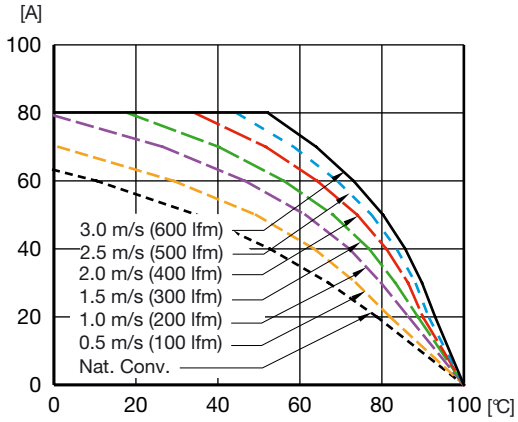
PKL 4219A PIT Typical Characteristics

Efficiency



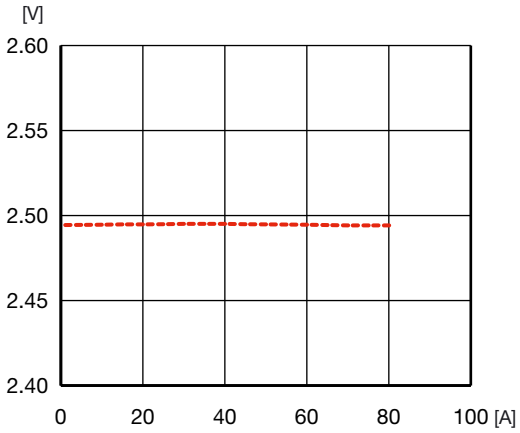
Efficiency vs. load current and input voltage at T_C = +25 °C

Output Current Derating



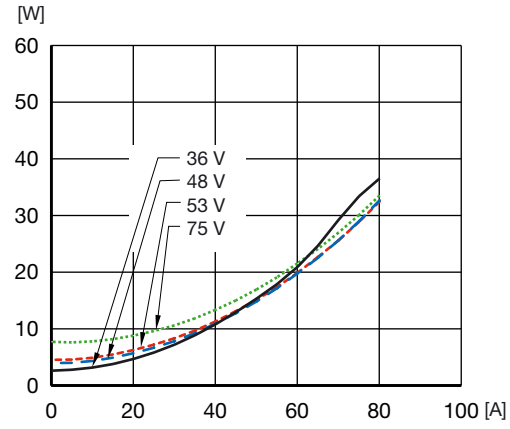
Available load current vs. ambient air temperature and airflow at V_{in} = 53 V.

Output Characteristic



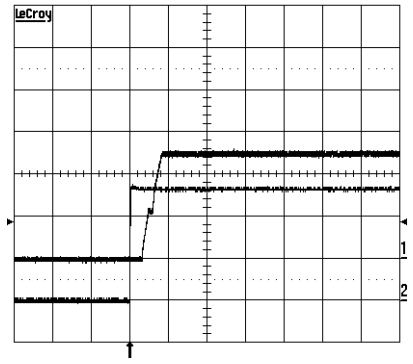
Output voltage vs. load current at T_C = +25 °C, V_{in} = 53 V.

Power Dissipation



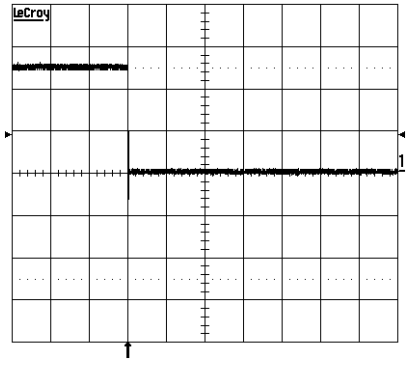
Dissipated power vs. load current and input voltage at T_C = +25 °C

Start-Up



Start-up at I_O = 60 A resistive load at T_C = +25 °C, V_{in} = 53 V. Start enabled by connecting V_{in}.
Top trace: output voltage (1 V/div.).
Bottom trace: input voltage (20 V/div.).
Time scale: 20 ms/div.

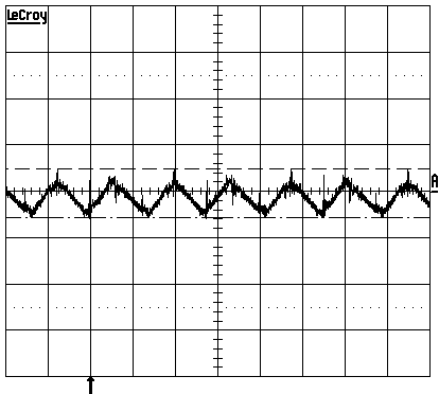
Turn-Off



Turn-off at I_O = 60 A resistive load at T_C = +25 °C, V_{in} = 53 V. Turn-off enabled by disconnecting Vin.
Trace: output voltage (1 V/div.).
Time scale: 5 ms/div.

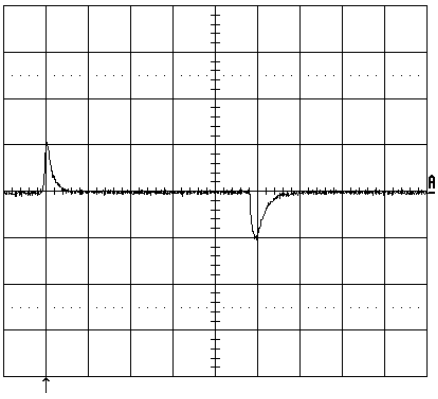
PKL 4219A PIT Typical Characteristics

Output Ripple



Output voltage ripple (50 mV/div.) at T_C = +25 °C
V_{in} = 53 V, I_O = 60 A resistive load.
Band width = 20 MHz.
Time scale: 2 µs / div.

Transient



Output voltage response to load current step-change (15-45-15 A) at T_C = +25 °C, V_{in} = 53 V.
Trace: output voltage (420 mV/div.).
dI/dt = 4 A/µs
Time scale: 50 µs/div.

Output Voltage Adjust

The resistor value for an adjusted output voltage is calculated by using the following equations:

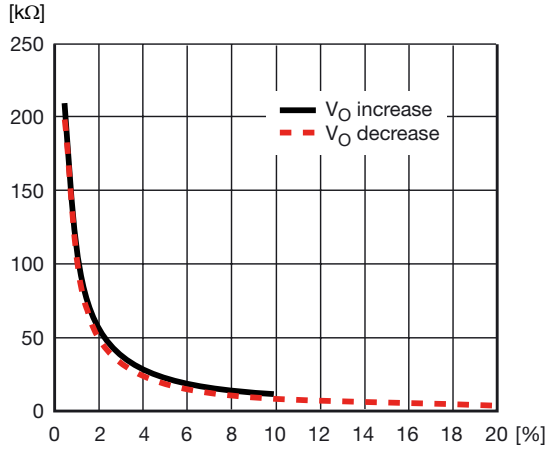
Output Voltage Adjust Upwards, Increase:
R_{adj}= [(V_O(100+Δ%)/(1.225Δ%))-(100+2Δ%)/Δ%] kOhm

Output Voltage Adjust Downwards, Decrease:
R_{adj}= [100/Δ%-2] kOhm

Ex. Increase 5% to: 2.625 V_{dc}
(2.5(100+5)/(1.225*5)-(100+2*5)/5 = 21 kOhm

Ex. Decrease 5% to: 2.375 V_{dc}
(100/5)-2= 18 kOhm

Output Voltage Adjust



Output voltage adjust resistor value vs. percentage change.

PKL 4110 PIT Output

T_C = —40…+100°C, V= 36 ...75V, sense pins connected to output pins unless otherwise specified.

Characteristics		Conditions	Output			Unit
			min	typ	max	
V_{Oi}	Output voltage initial setting and accuracy	T_C = +25 °C, V_I = 53 V, I_O = I_{Omax}	3.25	3.3	3.35	V
	Output adjust range	I_O = I_{Omax}	2.64		3.63	V
V_O	Output voltage tolerance band	I_O = 0.1...1 x I_{Omax}	3.2		3.4	V
	Idling voltage	I_O = 0	3.2		3.4	V
	Line regulation	I_O = I_{Omax}		5	15	mV
	Load regulation	V_I = 53 V, I_O = 0.01...1 x I_{Omax}		5	15	mV
V_{tr}	Load transient voltage deviation	I_O = 0.1...1 x I_{Omax} , V_I = 53 V Load step = 0.25 x I_{Omax} di/dt = 1A/µs		+250 -250		mV
t_{tr}	Load transient recovery time	I_O = 0.1...1 x I_{Omax} , V_I = 53 loadstep = 0.25x I_{Omax}		200		µs
t_r	Ramp-up time	I_O = 0.1...0.9 x V_O		10	30	ms
t_s	Start-up time	From V_I connected to V_O = 0.9 x V_{OI}		10	30	ms
I_O	Output current		0		50	A
P_{Omax}	Max output power	At V_O = V_{Onom}	165			W
I_{lim}	Current limit threshold	T_C < T_{Cmax}	51	54.5	62	A
I_{sc}	Short circuit current	T_C = 25 °C		59		A
V_{Oac}	Output ripple & noise	I_O = I_{Omax} , f < 4-20 MHz		70	150	mV_{p-p}
SVR	Supply voltage rejection (ac)	f = 100 Hz sinewave , 1 Vp-p , V_I = 53 V	50			dB
OVP	Over voltage protection	V_I = 53 V	3.9	4.4	5.0	V

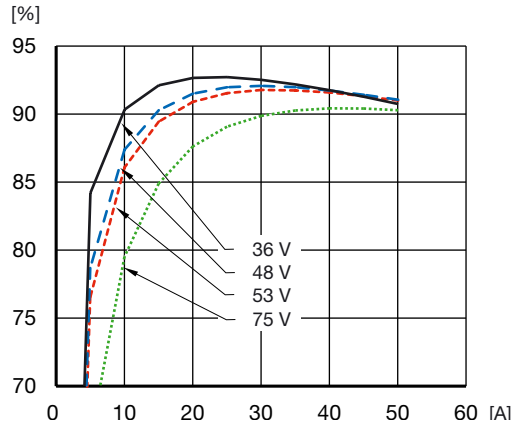
Miscellaneous

T_C = —40…+100°C, V= 36 ...75V, sense pins connected to output pins unless otherwise specified.

Characteristics		Conditions	min	typ	max	Unit
η	Efficiency - 50% load	T_C = +25 °C, V_I = 53 V, I_O = 0.5 x I_{Omax}		92		%
η	Efficiency - 100% load	T_C = +25 °C, V_I = 53 V, I_O = I_{Omax}		91		%
P_d	Power Dissipation	T_C = +25 °C, V_I = 53 V, I_O = I_{Omax}		22		W
f_s	Switching frequency	I_O = 0 ... 1.0 x I_{Omax}		150		kHz
I_{Imax}	Maximum input current	1.1 x V_{Oi} x I_{Omax} / η / V_{Imin}			5.6	A

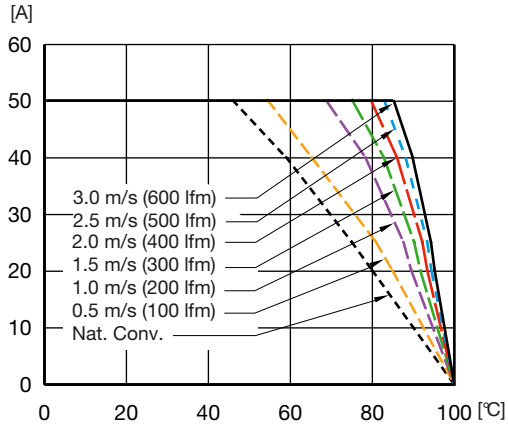
PKL 4110 PIT Typical Characteristics

Efficiency



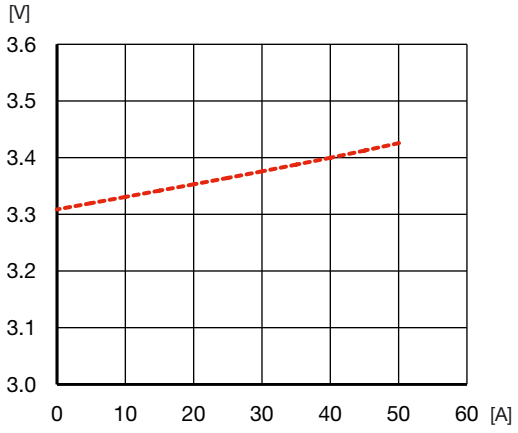
Efficiency vs. load current and input voltage at T_C = +25 °C

Output Current Derating



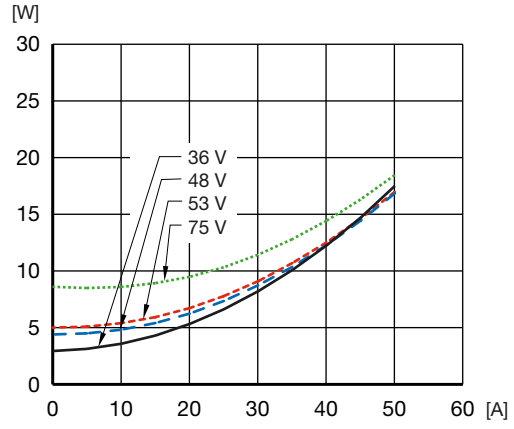
Available load current vs. ambient air temperature and airflow at V_{in} = 53 V.

Output Characteristic



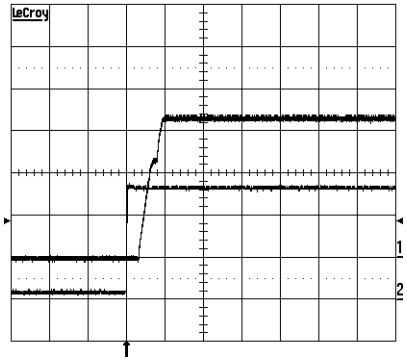
Output voltage vs. load current at T_C = +25 °C, V_{in} = 53 V.

Power Dissipation



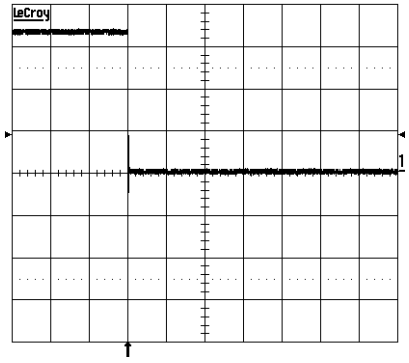
Dissipated power vs. load current and input voltage at T_C = +25 °C

Start-Up



Start-up at I_O = 50 A resistive load at T_C = +25 °C, V_{in} = 53 V. Start enabled by connecting V_{in}.
Top trace: output voltage (1 V/div.).
Bottom trace: input voltage (20 V/div.).
Time scale: 20 ms/div.

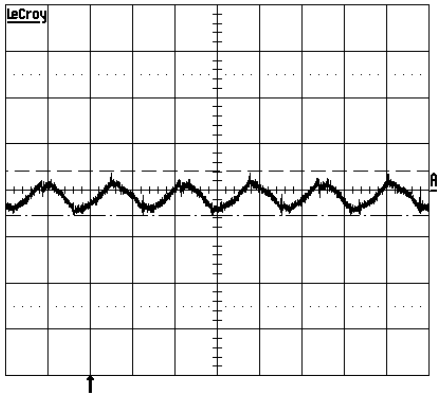
Turn-Off



Turn-off at I_O = 50 A resistive load at T_C = +25 °C, V_{in} = 53 V. Turn-off enabled by disconnecting V_{in}.
Trace: output voltage (1 V/div.).
Time scale: 5 ms/div.

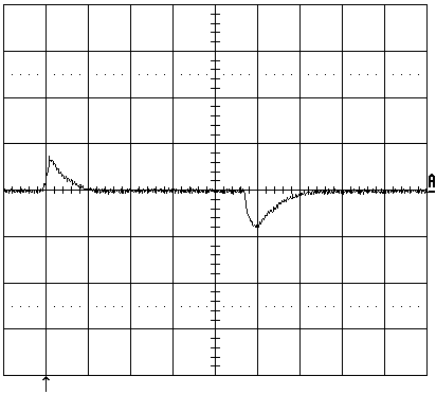
PKL 4110 PIT Typical Characteristics

Output Ripple



Output voltage ripple (50mV/div.) at T_C = +25 °C
V_{in} = 53 V, I_O = 50 A resistive load.
Band width = 20 MHz.
Time scale: 2 µs / div.

Transient



Output voltage response to load current step-change (12.5-37.5-12.5 A) at T_C = +25 °C, V_{in} = 53 V.
Trace: output voltage (420 mV/div.).
dI/dt = 4 A/µs
Time scale: 50 µs/div.

Output Voltage Adjust

The resistor value for an adjusted output voltage is calculated by using the following equations:

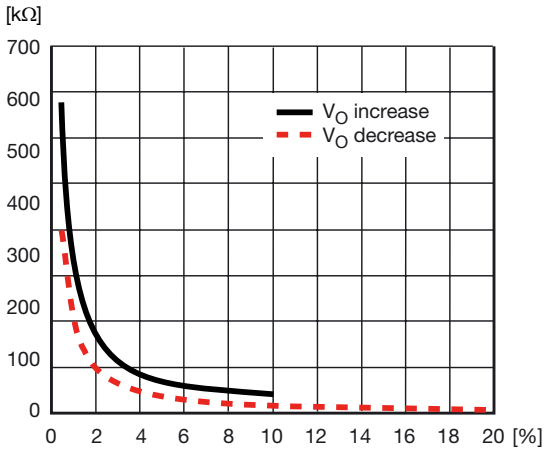
Output Voltage Adjust Upwards, Increase:
R_{adj}= [(15.9V_O+3.3)/(V_O-3.3)] kOhm

Output Voltage Adjust Downwards, Decrease:
R_{adj}= [(11V_O-3.3)/(3.3-V_O)] kOhm

Ex. Increase to: 3.35 V_{dc}
(15.9x3.35+3.3)/(3.35-3.3) = 1090 kOhm

Ex. Decrease to: 3.25 V_{dc}
(11x3.25-3.3)/(3.3-3.25) = 649 kOhm

Output Voltage Adjust



Output voltage adjust resistor value vs. percentage change.

PKL 4110A PIT Output

T_C = —40…+100°C, V= 36 ...75V, sense pins connected to output pins unless otherwise specified.

Characteristics		Conditions	Output			Unit
			min	typ	max	
V_{Oi}	Output voltage initial setting and accuracy	T_C = +25 °C, V_I = 53 V, I_O = I_{Omax}	3.25	3.3	3.35	V
	Output adjust range	I_O = I_{Omax}	2.64		3.63	V
V_O	Output voltage tolerance band	I_O = 0.1...1 x I_{Omax}	3.2		3.4	V
	Idling voltage	I_O = 0	3.2		3.4	V
	Line regulation	I_O = I_{Omax}		5	15	mV
	Load regulation	V_I = 53 V, I_O = 0.01...1 x I_{Omax}		5	15	mV
V_{tr}	Load transient voltage deviation	I_O = 0.1...1 x I_{Omax} , V_I = 53 V Load step = 0.25 x I_{Omax} di/dt = 1A/µs		+250 -250		mV
t_{tr}	Load transient recovery time	I_O = 0.1...1 x I_{Omax} , V_I = 53 loadstep = 0.25x I_{Omax}		200		µs
t_r	Ramp-up time	I_O = 0.1...0.9 x V_O		10	30	ms
t_s	Start-up time	From V_I connected to V_O = 0.9 x V_{OI}		10	30	ms
I_O	Output current		0		60	A
P_{Omax}	Max output power	At V_O = V_{Onom}	198			W
I_{lim}	Current limit threshold	T_C < T_{Cmax}	61	64.8	72	A
I_{sc}	Short circuit current	T_C = 25 °C		68		A
V_{Oac}	Output ripple & noise	I_O = I_{Omax} , f < 4-20 MHz		70	150	mV_{p-p}
SVR	Supply voltage rejection (ac)	f = 100 Hz sinewave , 1 Vp-p , V_I = 53 V	50			dB
OVP	Over voltage protection	V_I = 53 V	3.9	4.4	5.0	V

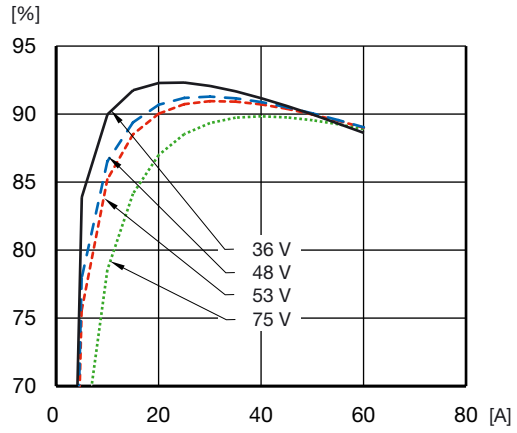
Miscellaneous

T_C = —40…+100°C, V= 36 ...75V, sense pins connected to output pins unless otherwise specified.

Characteristics		Conditions	min	typ	max	Unit
η	Efficiency - 50% load	T_C = +25 °C, V_I = 53 V, I_O = 0.5 x I_{Omax}		92		%
η	Efficiency - 100% load	T_C = +25 °C, V_I = 53 V, I_O = I_{Omax}		89		%
P_d	Power Dissipation	T_C = +25 °C, V_I = 53 V, I_O = I_{Omax}		24		W
f_s	Switching frequency	I_O = 0 ... 1.0 x I_{Omax}		150		kHz
I_{Imax}	Maximum input current	1.1 x V_{Oi} x I_{Omax} / η / V_{Imin}			6.8	A

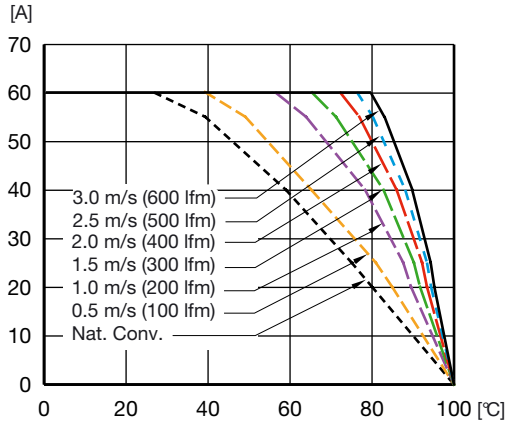
PKL 4110A PIT Typical Characteristics

Efficiency



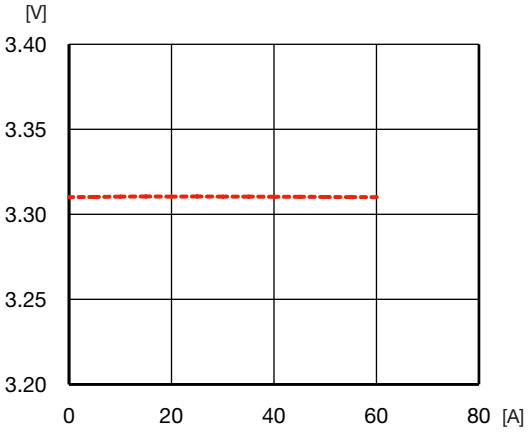
Efficiency vs. load current and input voltage at T_C = +25 °C

Output Current Derating



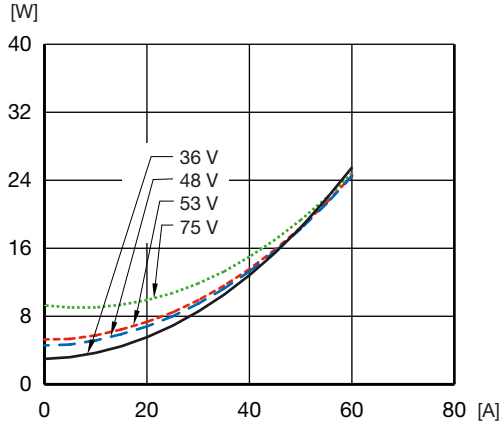
Available load current vs. ambient air temperature and airflow at V_{in} = 53 V.

Output Characteristic



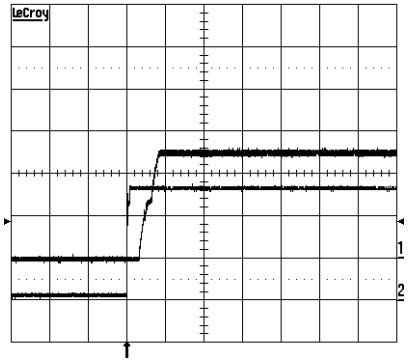
Output voltage vs. load current at T_C = +25 °C, V_{in} = 53 V.

Power Dissipation



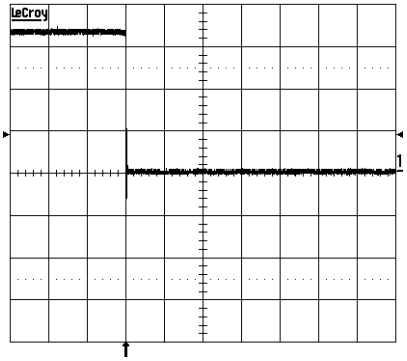
Dissipated power vs. load current and input voltage at T_C = +25 °C

Start-Up



Start-up at I_O = 60 A resistive load at T_C = +25 °C, V_{in} = 53 V. Start enabled by connecting V_{in}.
Top trace: output voltage (1 V/div.).
Bottom trace: input voltage (20 V/div.).
Time scale: 20 ms/div.

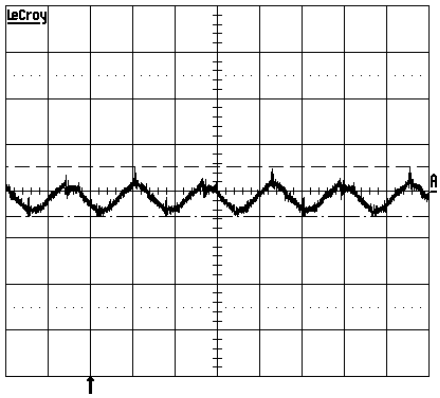
Turn-Off



Turn-off at I_O = 60 A resistive load at T_C = +25 °C, V_{in} = 53 V. Turn-off enabled by disconnecting V_{in}.
Trace: output voltage (1 V/div.).
Time scale: 5 ms/div.

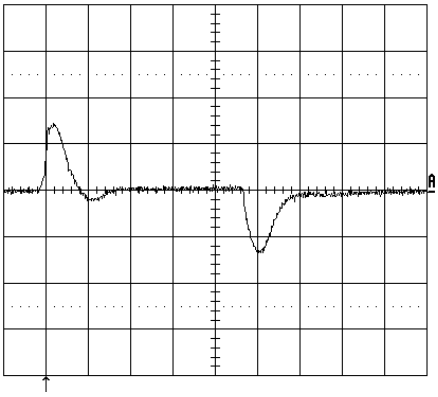
PKL 4110A PIT Typical Characteristics

Output Ripple



Output voltage ripple (50 mV/div.) at T_C = +25 °C
V_{in} = 53 V, I_O = 60 A resistive load.
Band width = 20 MHz.
Time scale: 2 µs / div.

Transient



Output voltage response to load current step-change (15-45-15 A) at T_C = +25 °C, V_{in} = 53 V.
Trace: output voltage (420 mV/div.).
dI/dt = 20 A/µs
Time scale: 50 µs/div.

Output Voltage Adjust

The resistor value for an adjusted output voltage is calculated by using the following equations:

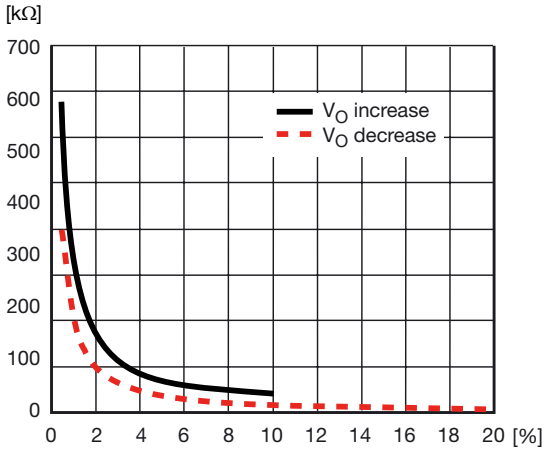
Output Voltage Adjust Upwards, Increase:
R_{adj}= [(15.9V_O+3.3)/(V_O-3.3)] kOhm

Output Voltage Adjust Downwards, Decrease:
R_{adj}= [(11V_O-3.3)/(3.3-V_O)] kOhm

Ex. Increase to: 3.35 V_{dc}
(15.9x3.35+3.3)/(3.35-3.3) = 1090 kOhm

Ex. Decrease to: 3.25 V_{dc}
(11x3.25-3.3)/(3.3-3.25) = 649 kOhm

Output Voltage Adjust



Output voltage adjust resistor value vs. percentage change.

PKL 4211 PIT Output

T_C = —40…+100°C, V= 36 ...75V, sense pins connected to output pins unless otherwise specified.

Characteristics		Conditions	Output			Unit
			min	typ	max	
V_{Oi}	Output voltage initial setting and accuracy	T_C = +25 °C, V_I = 53 V, I_O = I_{Omax}	4.9	5.0	5.1	V
	Output adjust range	I_O = I_{Omax}	4.0		5.5	V
V_O	Output voltage tolerance band	I_O = 0.1...1 x I_{Omax}	4.85		5.15	V
	Idling voltage	I_O = 0	4.85		5.15	V
	Line regulation	I_O = I_{Omax}		5	15	mV
	Load regulation	V_I = 53 V, I_O = 0.01...1 x I_{Omax}		5	15	mV
V_{tr}	Load transient voltage deviation	I_O = 0.1...1 x I_{Omax} , V_I = 53 V Load step = 0.25 x I_{Omax} di/dt = 1A/µs		+/-165		mV
t_{tr}	Load transient recovery time	I_O = 0.1...1 x I_{Omax} , V_I = 53 loadstep = 0.25x I_{Omax}		150		µs
t_r	Ramp-up time	I_O = 0.1...0.9 x V_O		15		ms
t_s	Start-up time	From V_I connected to V_O = 0.9 x V_{OI}		20		ms
I_O	Output current		0		50	A
P_{Omax}	Max output power	At V_O = V_{Onom}	250			W
I_{lim}	Current limit threshold	T_C < T_{Cmax}		56.5		A
I_{sc}	Short circuit current	T_C = 25 °C		70		A
V_{Oac}	Output ripple & noise	I_O = I_{Omax} , f < 4-20 MHz		70	110	mV_{p-p}
SVR	Supply voltage rejection (ac)	f = 100 Hz sinewave , 1 Vp-p , V_I = 53 V	50			dB
OVP	Over voltage protection	V_I = 53 V		5.9		V

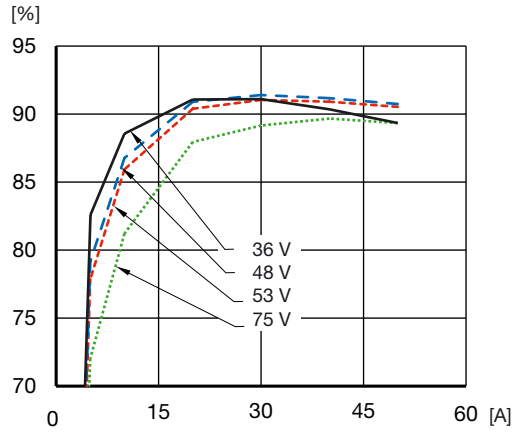
Miscellaneous

T_C = —40…+100°C, V= 36 ...75V, sense pins connected to output pins unless otherwise specified.

Characteristics		Conditions	min	typ	max	Unit
η	Efficiency - 50% load	T_C = +25 °C, V_I = 53 V, I_O = 0.5 x I_{Omax}		91		%
η	Efficiency - 100% load	T_C = +25 °C, V_I = 53 V, I_O = I_{Omax}		90.5		%
P_d	Power Dissipation	T_C = +25 °C, V_I = 53 V, I_O = I_{Omax}		27		W
f_s	Switching frequency	I_O = 0 ... 1.0 x I_{Omax}		200		kHz
I_{Imax}	Maximum input current	1.1 x V_{Oi} x I_{Omax} / η / V_{Imin}			8.5	A

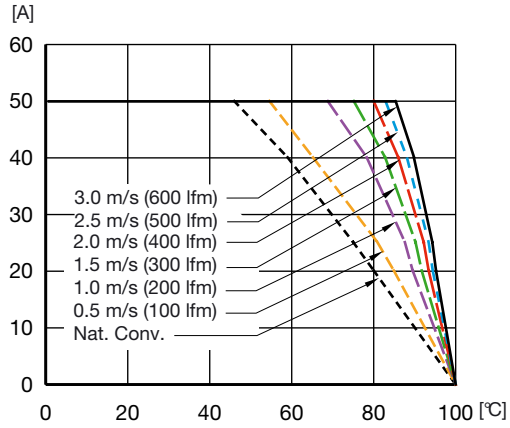
PKL 4211 PIT Typical Characteristics

Efficiency



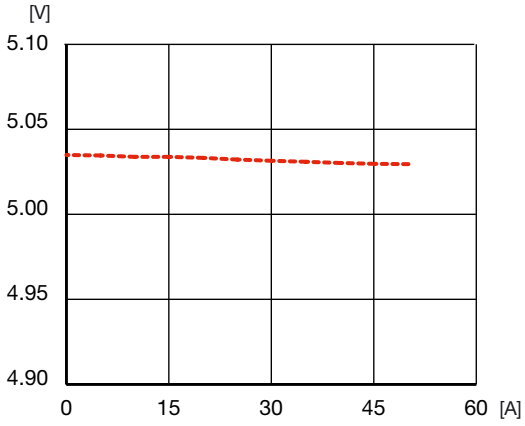
Efficiency vs. load current and input voltage at T_C = +25 °C

Output Current Derating



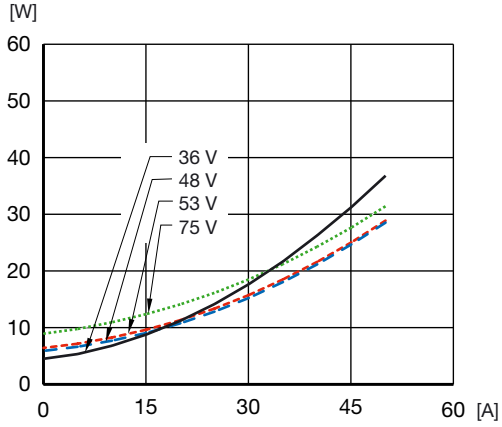
Available load current vs. ambient air temperature and airflow at V_{in} = 53 V.

Output Characteristic



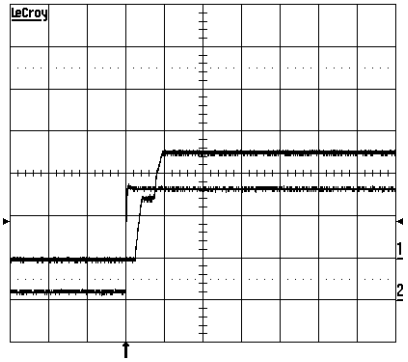
Output voltage vs. load current at T_C = +25 °C, V_{in} = 53 V.

Power Dissipation



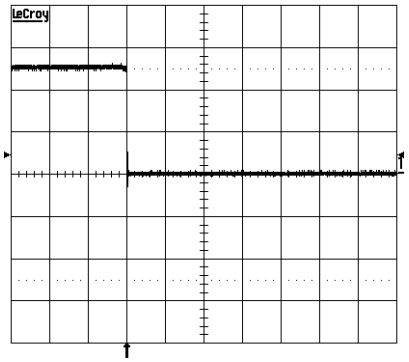
Dissipated power vs. load current and input voltage at T_C = +25 °C

Start-Up



Start-up at I_O = 50 A resistive load at T_C = +25 °C, V_{in} = 53 V. Start enabled by connecting Vin.
Top trace: output voltage (2 V/div.).
Bottom trace: input voltage (20 V/div.).
Time scale: 20 ms/div.

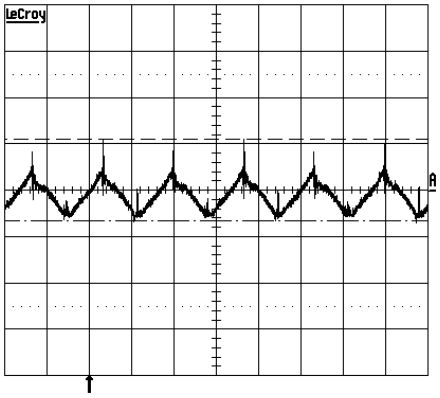
Turn-Off



Turn-off at I_O = 50 A resistive load at T_C = +25 °C, V_{in} = 53 V. Turn-off enabled by disconnecting V_{in}.
Trace: output voltage (2 V/div.).
Time scale: 5 ms/div.

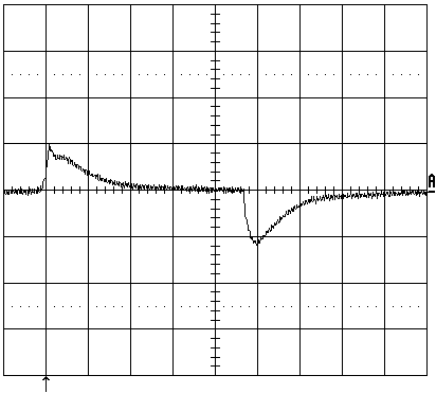
PKL 4211 PIT Typical Characteristics

Output Ripple



Output voltage ripple (50 mV/div.) at T_C = +25 °C
V_{in} = 53 V, I_O = 50 A resistive load.
Band width = 20 MHz.
Time scale: 2 µs/div.

Transient



Output voltage response to load current step-change (15-45-15 A) at T_C = +25 °C, V_{in} = 53 V.
Trace: output voltage (420 mV/div.).
dI/dt = 4 A/µs
Time scale: 50 µs/div.

Output Voltage Adjust

The resistor value for an adjusted output voltage is calculated by using the following equations:

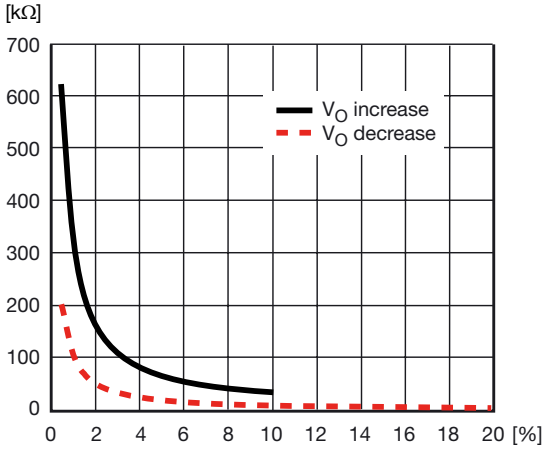
Output Voltage Adjust Upwards, Increase:
R_{adj}= [(V_O(100+Δ%)/(1.225Δ%))-(100+2Δ%)/Δ%] kOhm

Output Voltage Adjust Downwards, Decrease:
R_{adj}= [100/Δ%-2] kOhm

Ex. Increase 5% to: 5.25 V_{dc}
(5(100+5)/(1.225*5)-(100+2*5)/5 = 64 kOhm

Ex. Decrease 5% to: 4.75 V_{dc}
(100/5)-2= 18 kOhm

Output Voltage Adjust



Output voltage adjust resistor value vs. percentage change.

PKL 4311 PIT Output

T_C = —40…+100°C, V= 36 ...75V, sense pins connected to output pins unless otherwise specified.

Characteristics		Conditions	Output			Unit
			min	typ	max	
V_{Oi}	Output voltage initial setting and accuracy	T_C = +25 °C, V_I = 53 V, I_O = I_{Omax}	4.9	5.0	5.1	V
	Output adjust range	I_O = I_{Omax}	4.0		5.5	V
V_O	Output voltage tolerance band	I_O = 0.1...1 x I_{Omax}	4.85		5.15	V
	Idling voltage	I_O = 0	4.85		5.15	V
	Line regulation	I_O = I_{Omax}		5	15	mV
	Load regulation	V_I = 53 V, I_O = 0.01...1 x I_{Omax}		5	15	mV
V_{tr}	Load transient voltage deviation	I_O = 0.1...1 x I_{Omax} , V_I = 53 V Load step = 0.25 x I_{Omax} di/dt = 1A/µs		+/-165		mV
t_{tr}	Load transient recovery time	I_O = 0.1...1 x I_{Omax} , V_I = 53 loadstep = 0.25x I_{Omax}		150		µs
t_r	Ramp-up time	I_O = 0.1...0.9 x V_O		15		ms
t_s	Start-up time	From V_I connected to V_O = 0.9 x V_{OI}		20		ms
I_O	Output current		0		60	A
P_{Omax}	Max output power	At V_O = V_{Onom}	300			W
I_{lim}	Current limit threshold	T_C < T_{Cmax}		66.5		A
I_{sc}	Short circuit current	T_C = 25 °C		80		A
V_{Oac}	Output ripple & noise	I_O = I_{Omax} , f < 4-20 MHz		70	110	mV_{p-p}
SVR	Supply voltage rejection (ac)	f = 100 Hz sinewave , 1 Vp-p , V_I = 53 V	50			dB
OVP	Over voltage protection	V_I = 53 V		5.9		V

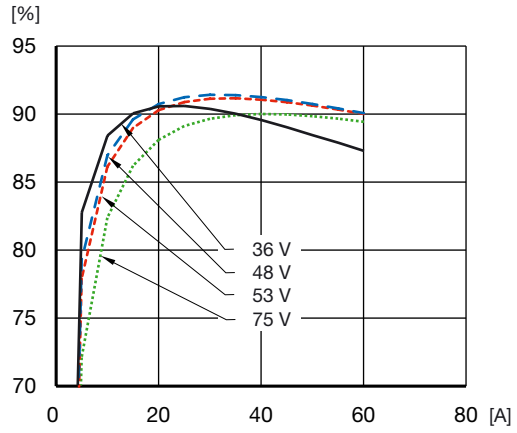
Miscellaneous

T_C = —40…+100°C, V= 36 ...75V, sense pins connected to output pins unless otherwise specified.

Characteristics		Conditions	min	typ	max	Unit
η	Efficiency - 50% load	T_C = +25 °C, V_I = 53 V, I_O = 0.5 x I_{Omax}		91		%
η	Efficiency - 100% load	T_C = +25 °C, V_I = 53 V, I_O = I_{Omax}		90		%
P_d	Power Dissipation	T_C = +25 °C, V_I = 53 V, I_O = I_{Omax}		34		W
f_s	Switching frequency	I_O = 0 ... 1.0 x I_{Omax}		200		kHz
I_{Imax}	Maximum input current	1.1 x V_{Oi} x I_{Omax} / η / V_{Imin}			10.2	A

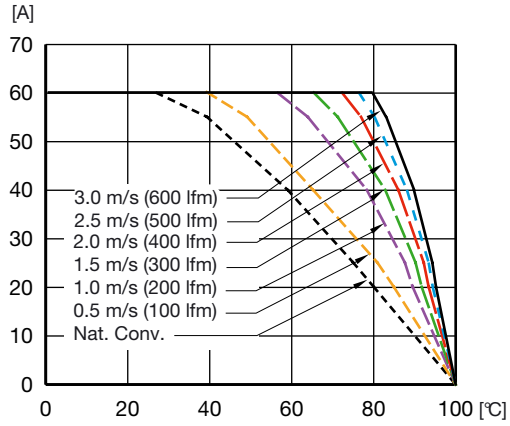
PKL 4311 PIT Typical Characteristics

Efficiency



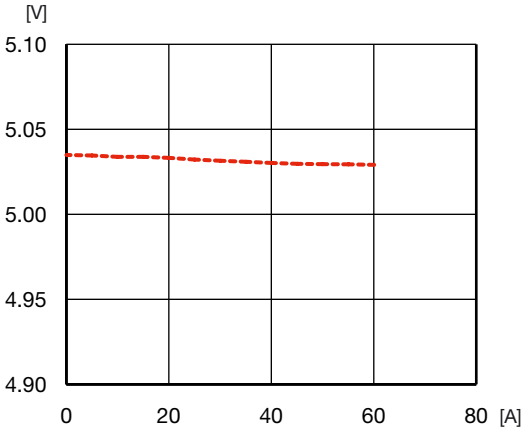
Efficiency vs. load current and input voltage at T_C = +25 °C

Output Current Derating



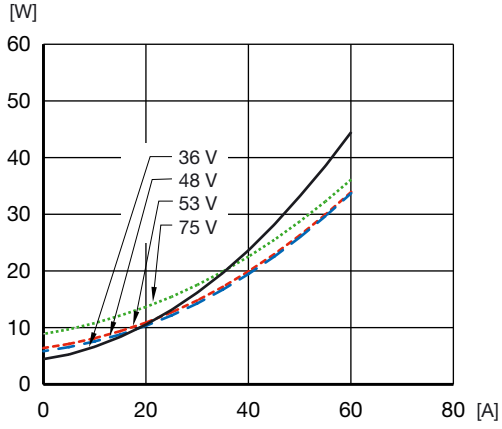
Available load current vs. ambient air temperature and airflow at V_{in} = 53 V.

Output Characteristic



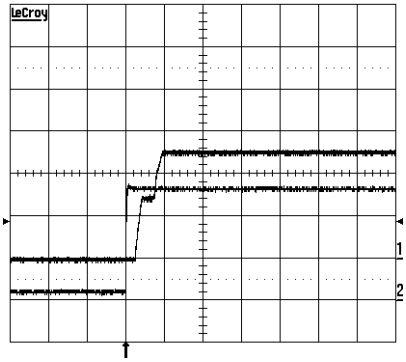
Output voltage vs. load current at T_C = +25 °C, V_{in} = 53 V.

Power Dissipation



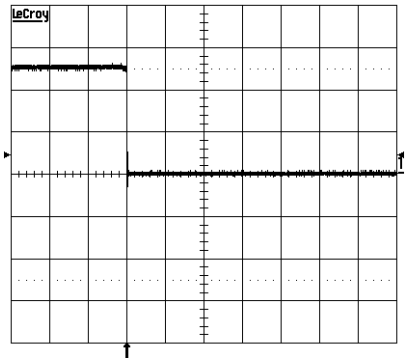
Dissipated power vs. load current and input voltage at T_C = +25 °C

Start-Up



Start-up at Io=60A resistive load at T_C = +25 °C, V_{in} = 53 V. Start enabled by connecting V_{in}.
Top trace: output voltage (2 V/div.).
Bottom trace: input voltage (20 V/div.).
Time scale: 20 ms/div.

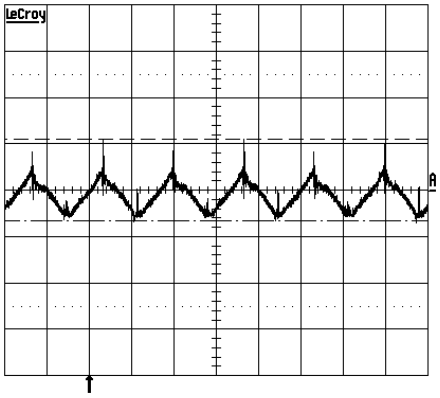
Turn-Off



Turn-off at I_O = 60 A resistive load at T_C = +25 °C, V_{in} = 53 V. Turn-off enabled by disconnecting V_{in}.
Trace: output voltage (2 V/div.).
Time scale: 5 ms/div.

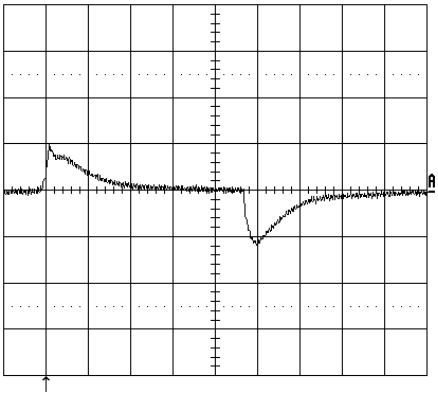
PKL 4311 PIT Typical Characteristics

Output Ripple



Output voltage ripple (50 mV/div.) at T_C = +25 °C
V_{in} = 53 V, I_O = 60 A resistive load.
Band width = 20 MHz.
Time scale: 2 µs / div.

Transient



Output voltage response to load current step-change (15-45-15 A) at T_C = +25 °C, V_{in} = 53 V.
Trace: output voltage (420 mV/div.).
dI/dt = 4 A/µs
Time scale: 50 µs/div.

Output Voltage Adjust

The resistor value for an adjusted output voltage is calculated by using the following equations:

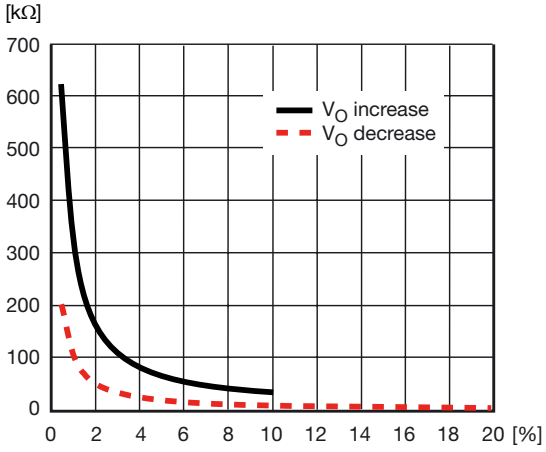
Output Voltage Adjust Upwards, Increase:
R_{adj}= [(V_O(100+Δ%)/(1.225Δ%))-(100+2Δ%)/Δ%] kOhm

Output Voltage Adjust Downwards, Decrease:
R_{adj}= [100/Δ%-2] kOhm

Ex. Increase 5% to: 5.25 V_{dc}
(5(100+5)/(1.225*5)-(100+2*5)/5 = 64 kOhm

Ex. Decrease 5% to: 4.75 V_{dc}
(100/5)-2= 18 kOhm

Output Voltage Adjust



Output voltage adjust resistor value vs. percentage change.

PKL 4213 PIT Output

T_C = —40…+100°C, V= 36 ...75V, sense pins connected to output pins unless otherwise specified.

Characteristics		Conditions	Output			Unit
			min	typ	max	
V_{Oi}	Output voltage initial setting and accuracy	T_C = +25 °C, V_I = 53 V, I_O = I_{Omax}	11.8	12	12.2	V
	Output adjust range	I_O = I_{Omax}	9.6		13.2	V
V_O	Output voltage tolerance band	I_O = 0.1...1 x I_{Omax}	11.64		12.36	V
	Idling voltage	I_O = 0	11.64		12.36	V
	Line regulation	I_O = I_{Omax}		12	20	mV
	Load regulation	V_I = 53 V, I_O = 0.01...1 x I_{Omax}		12	20	mV
V_{tr}	Load transient voltage deviation	I_O = 0.1...1 x I_{Omax} , V_I = 53 V Load step = 0.25 x I_{Omax} di/dt = 1A/µs		+/-200		mV
t_{tr}	Load transient recovery time	I_O = 0.1...1 x I_{Omax} , V_I = 53 loadstep = 0.25x I_{Omax}		200		µs
t_r	Ramp-up time	I_O = 0.1...0.9 x V_O		15		ms
t_s	Start-up time	From V_I connected to V_O = 0.9 x V_{OI}		20	30	ms
I_O	Output current		0		20	A
P_{Omax}	Max output power	At V_O = V_{Onom}	240			W
I_{lim}	Current limit threshold	T_C < T_{Cmax}		23.5	28	A
I_{sc}	Short circuit current	T_C = 25 °C		26	29	A
V_{Oac}	Output ripple & noise	I_O = I_{Omax} , f < 4-20 MHz		80	150	mV_{p-p}
SVR	Supply voltage rejection (ac)	f = 100 Hz sinewave , 1 Vp-p , V_I = 53 V	50			dB
OVP	Over voltage protection	V_I = 53 V		14.9		V

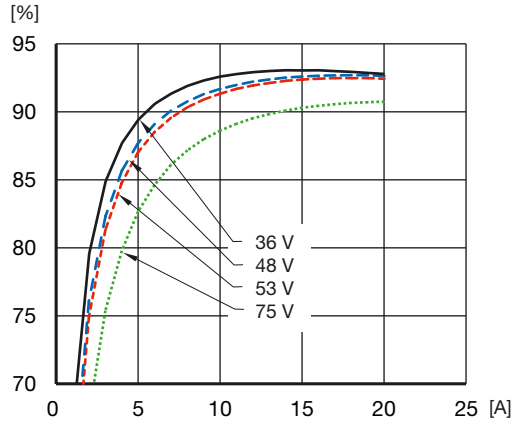
Miscellaneous

T_C = —40…+100°C, V= 36 ...75V, sense pins connected to output pins unless otherwise specified.

Characteristics		Conditions	min	typ	max	Unit
η	Efficiency - 50% load	T_C = +25 °C, V_I = 53 V, I_O = 0.5 x I_{Omax}		91.5		%
η	Efficiency - 100% load	T_C = +25 °C, V_I = 53 V, I_O = I_{Omax}		92.5		%
P_d	Power Dissipation	T_C = +25 °C, V_I = 53 V, I_O = I_{Omax}		19.9		W
f_s	Switching frequency	I_O = 0 ... 1.0 x I_{Omax}		200		kHz
I_{Imax}	Maximum input current	1.1 x V_{Oi} x I_{Omax} / η / V_{Imin}		7.9		A

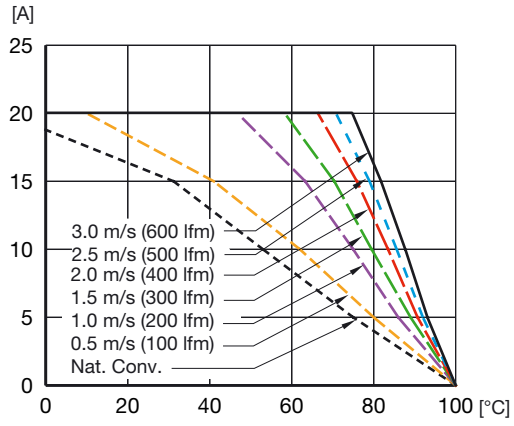
PKL 4213 PIT Typical Characteristics

Efficiency



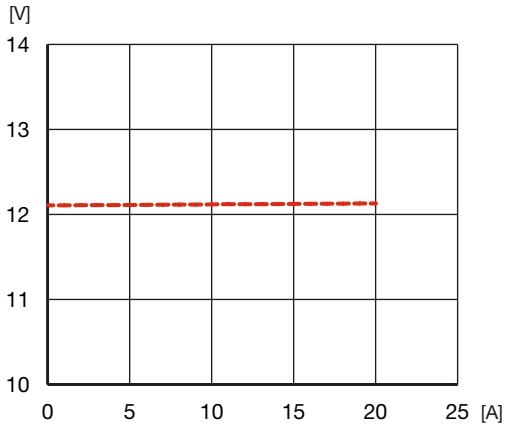
Efficiency vs. load current and input voltage at T_C = +25 °C

Output Current Derating



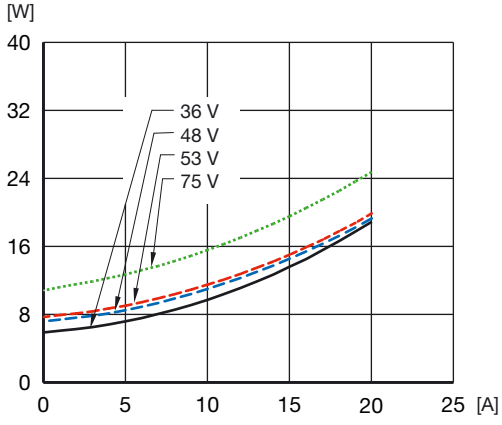
Available load current vs. ambient air temperature and airflow at V_{in} = 53 V.

Output Characteristic



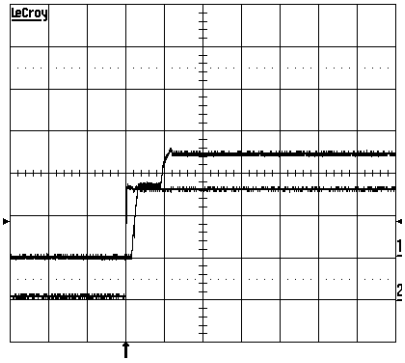
Output voltage vs. load current at T_C = +25 °C, V_{in} = 53 V.

Power Dissipation



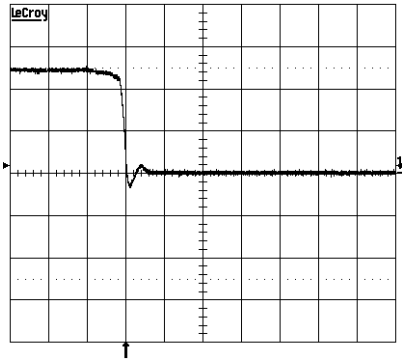
Dissipated power vs. load current and input voltage at T_C = +25 °C

Start-Up



Start-up at I_O = 20 A resistive load at T_C = +25 °C, V_{in} = 53 V. Start enabled by connecting V_{in}.
Top trace: output voltage (5 V/div.).
Bottom trace: input voltage (20 V/div.).
Time scale: 20 ms/div.

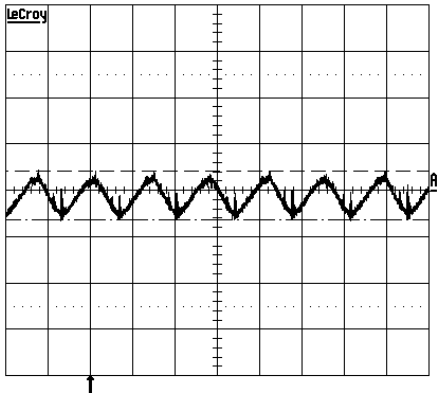
Turn-Off



Turn-off at I_O = 20 A resistive load at T_C = +25 °C, V_{in} = 53 V. Turn-off enabled by disconnecting V_{in}.
Trace: output voltage (5 V/div.).
Time scale: 0.2 ms/div.

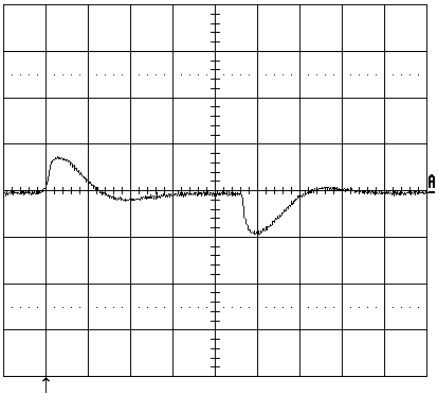
PKL 4213 PIT Typical Characteristics

Output Ripple



Output voltage ripple (50 mV/div.) at T_C = +25 °C
V_{in} = 53 V, I_O = 20 A resistive load.
Band width = 20 MHz.
Time scale: 2 µs/div.

Transient



Output voltage response to load current step-change (5-15-5 A) at T_C = +25 °C, V_{in} = 53 V.
Trace: output voltage (0.84 V/div.).
dI/dt = 4 A/µs
Time scale: 50 µs/div.

Output Voltage Adjust

The resistor value for an adjusted output voltage is calculated by using the following equations:

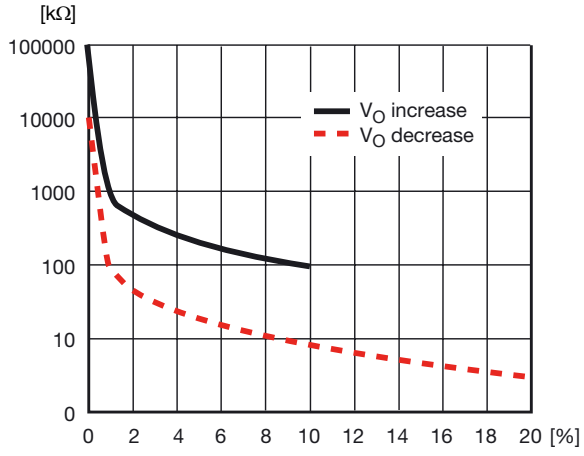
Output Voltage Adjust Upwards, Increase:
R_{adj}= [(V_O(100+Δ%)/(1.225Δ%))-(100+2Δ%)/Δ%] kOhm

Output Voltage Adjust Downwards, Decrease:
R_{adj}= [100/Δ%-2] kOhm

Ex. Increase 2% to: 12.24 V_{dc}
12(100+2)/(1.225*2)-(100+2*2)/2 = 447 kOhm

Ex. Decrease 2% to: 11.76 V_{dc}
(100/2)-2= 48 kOhm

Output Voltage Adjust



Output voltage adjust resistor value vs. percentage change.

PKL 4313 PIT Output

T_C = —40…+100°C, V= 36 ...75V, sense pins connected to output pins unless otherwise specified.

Characteristics		Conditions	Output			Unit
			min	typ	max	
V_{Oi}	Output voltage initial setting and accuracy	T_C = +25 °C, V_I = 53 V, I_O = I_{Omax}	11.8	12	12.2	V
	Output adjust range	I_O = I_{Omax}	9.6		13.2	V
V_O	Output voltage tolerance band	I_O = 0.1...1 x I_{Omax}	11.64		12.36	V
	Idling voltage	I_O = 0	11.64		12.36	V
	Line regulation	I_O = I_{Omax}		12	20	mV
	Load regulation	V_I = 53 V, I_O = 0.01...1 x I_{Omax}		12	20	mV
V_{tr}	Load transient voltage deviation	I_O = 0.1...1 x I_{Omax} , V_I = 53 V Load step = 0.25 x I_{Omax} di/dt = 1A/µs		+/-200		mV
t_{tr}	Load transient recovery time	I_O = 0.1...1 x I_{Omax} , V_I = 53 loadstep = 0.25x I_{Omax}		200		µs
t_r	Ramp-up time	I_O = 0.1...0.9 x V_O		15		ms
t_s	Start-up time	From V_I connected to V_O = 0.9 x V_{OI}		20	30	ms
I_O	Output current		0		25	A
P_{Omax}	Max output power	At V_O = V_{Onom}	300			W
I_{lim}	Current limit threshold	T_C < T_{Cmax}		27.5	32	A
I_{sc}	Short circuit current	T_C = 25 °C		30	42	A
V_{Oac}	Output ripple & noise	I_O = I_{Omax} , f < 4-20 MHz		80	150	mV_{p-p}
SVR	Supply voltage rejection (ac)	f = 100 Hz sinewave , 1 Vp-p , V_I = 53 V	50			dB
OVP	Over voltage protection	V_I = 53 V		14.9		V

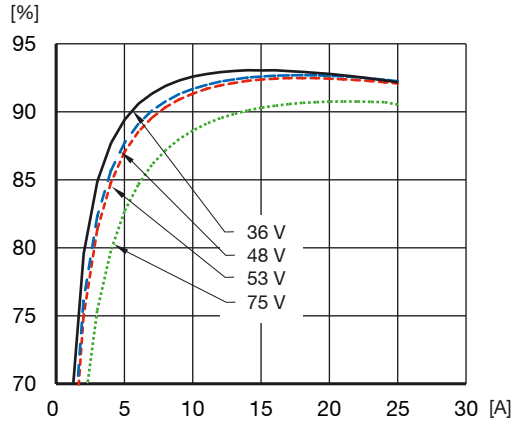
Miscellaneous

T_C = —40…+100°C, V= 36 ...75V, sense pins connected to output pins unless otherwise specified.

Characteristics		Conditions	min	typ	max	Unit
η	Efficiency - 50% load	T_C = +25 °C, V_I = 53 V, I_O = 0.5 x I_{Omax}		92		%
η	Efficiency - 100% load	T_C = +25 °C, V_I = 53 V, I_O = I_{Omax}		92		%
P_d	Power Dissipation	T_C = +25 °C, V_I = 53 V, I_O = I_{Omax}		26		W
f_s	Switching frequency	I_O = 0 ... 1.0 x I_{Omax}		200		kHz
I_{Imax}	Maximum input current	1.1 x V_{Oi} x I_{Omax} / η / V_{Imin}		9.9		A

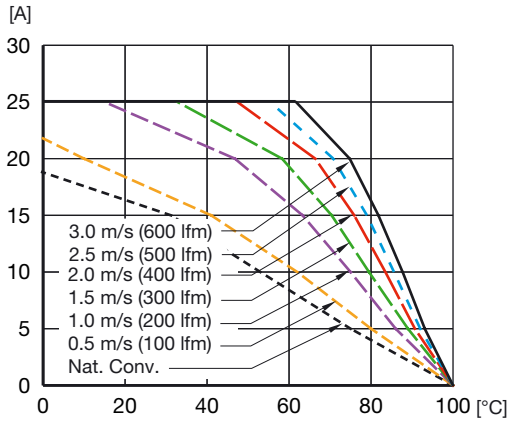
PKL 4313 PIT Typical Characteristics

Efficiency



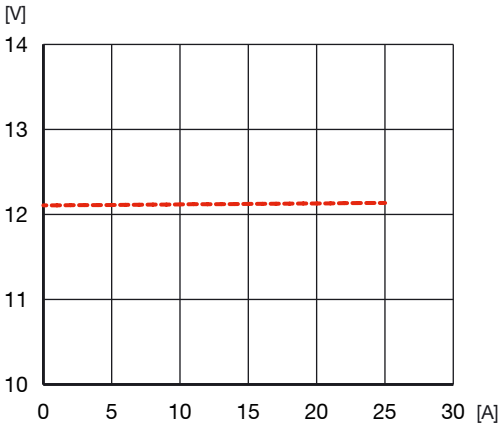
Efficiency vs. load current and input voltage at T_C = +25 °C

Output Current Derating



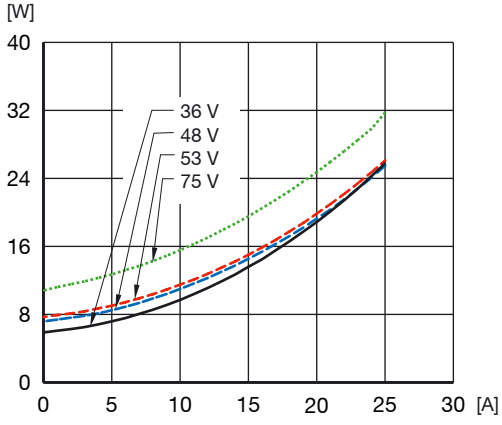
Available load current vs. ambient air temperature and airflow at V_{in} = 53 V.

Output Characteristic



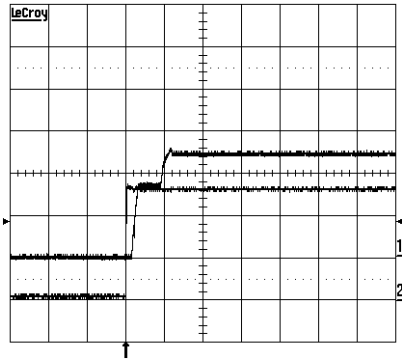
Output voltage vs. load current at T_C = +25 °C, V_{in} = 53 V.

Power Dissipation



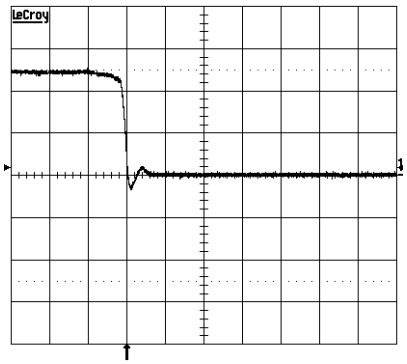
Dissipated power vs. load current and input voltage at T_C = +25 °C

Start-Up



Start-up at I_O = 25 A resistive load at T_C = +25 °C, V_{in} = 53 V. Start enabled by connecting V_{in}.
Top trace: output voltage (5 V/div.).
Bottom trace: input voltage (20 V/div.).
Time scale: 20 ms/div.

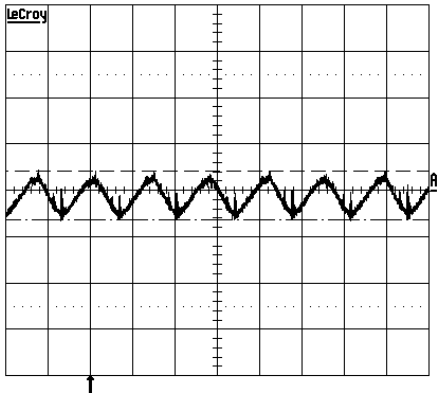
Turn-Off



Turn-off at I_O = 25 A resistive load at T_C = +25 °C, V_{in} = 53 V. Turn-off enabled by disconnecting V_{in}.
Trace: output voltage (5 V/div.).
Time scale: 0.2 ms/div.

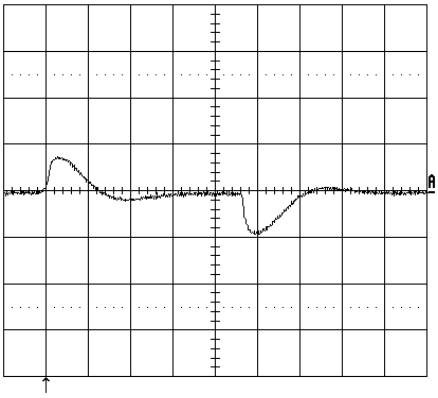
PKL 4313 PIT Typical Characteristics

Output Ripple



Output voltage ripple (50 mV/div.) at T_C = +25 °C
V_{in} = 53 V, I_O = 25 A resistive load.
Band width = 20 MHz.
Time scale: 2 µs/div.

Transient



Output voltage response to load current step-change (6.25-18.75-6.25 A) at T_C = +25 °C, V_{in} = 53 V.
Trace: output voltage (0.84 V/div.).
dI/dt = 4 A/µs
Time scale: 50 µs/div.

Output Voltage Adjust

The resistor value for an adjusted output voltage is calculated by using the following equations:

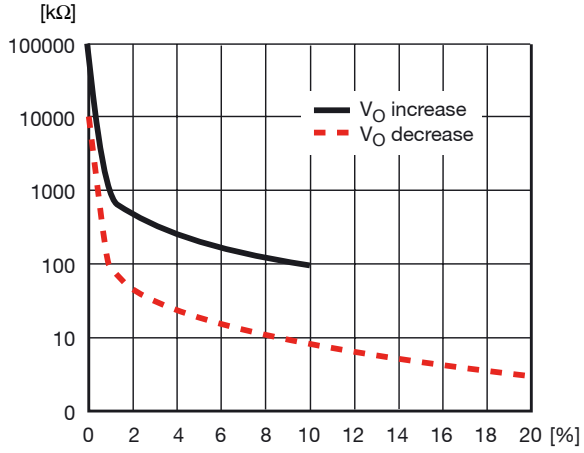
Output Voltage Adjust Upwards, Increase:
R_{adj}= [(V_O(100+Δ%)/(1.225Δ%))-(100+2Δ%)/Δ%] kOhm

Output Voltage Adjust Downwards, Decrease:
R_{adj}= [100/Δ%-2] kOhm

Ex. Increase 2% to: 12.24 V_{dc}
12(100+2)/(1.225*2)-(100+2*2)/2 = 447 kOhm

Ex. Decrease 2% to: 11.76 V_{dc}
(100/2)-2= 48 kOhm

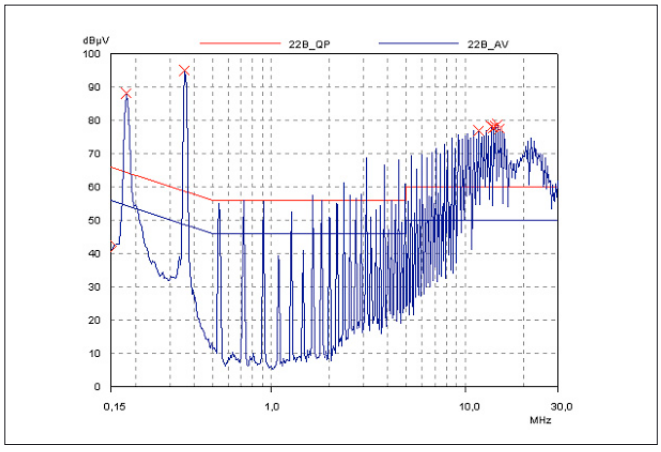
Output Voltage Adjust



Output voltage adjust resistor value vs. percentage change.

EMC Specification

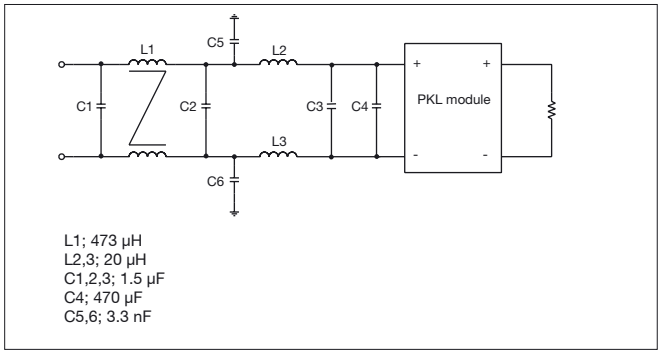
The conducted EMI measurement is performed using a module placed directly on the test bench.
The fundamental switching frequency is 150 kHz for PKL 4118B PIT @ V_I = 53V, I_O = (0.1...1.0) × I_{Omax}.



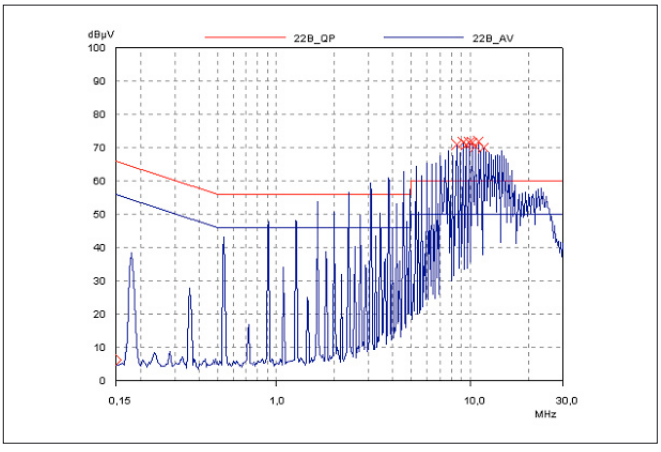
PKL 4118B PIT without filter.

External filter (class B)

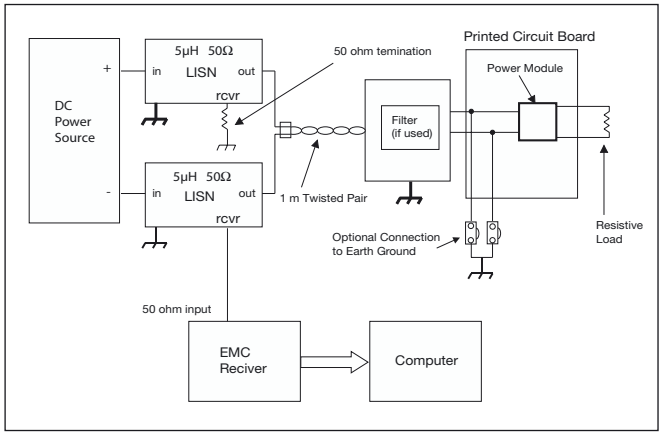
Recommended external input filter.



The capacitors are ceramic type. Low ESR is critical for acheiveing these results.



PKL 4118B PIT with filter.



Test set-up.

Layout Recommendation

The radiated EMI performance of the DC/DC converter will be optimised by including a ground plane in the PCB area under the DC/DC converter. This approach will return switching noise to ground as directly as possible, with improvements to both emissions and susceptibility. If one ground trace is used, it should be connected to the input return. Alternatively, two ground traces may be used, with the trace under the input side of the DC/DC converter connected to the input return and the trace under the output side of the DC/DC converter connected to the output return. Make sure to use appropriate safety isolation spacing between these two return traces. The use of two traces as described will provide the capability of routing the input noise and output noise back to their respective returns.

Operating Information

Input Voltage

The input voltage range 36…75Vdc meets the requirements of the European Telecom Standard ETS 300 132-2 for normal input voltage range in –48V and –60V DC systems, -40.5…-57.0V and –50.0…-72V respectively. At input voltages exceeding 75V, the power loss will be higher than at normal input voltage and T_C must be limited to absolute max +100 °C (PKL 4118B PIT max +110 °C). The absolute maximum continuous input voltage is 80 Vdc.

Turn-Off Input Voltage

The PKL 4000 Series DC/DC converters monitor the input voltage and will turn on and turn off at predetermined levels. The minimum hysteresis between turn on and turn off input voltage is 1V where the turn on input voltage is the highest.

Remote Control (RC)

The PKL 4000 Series DC/DC converters have remote control function referenced to the primary side (minus input), with negative and positive logic options available. The RC function is CMOS open drain compatible. Maximum sink current is 1mA. When the RC pin is left open, the voltage generated on the RC pin by the DC/DC converter is 3.5-6.0V. The maximum allowable leakage current of the switch is 50 µA.

The standard converter is provided with “negative logic” remote control and will be off until the RC pin is connected to the minus input. To turn on the converter the voltage between RC pin and minus input should be less than 1V. To turn off the converter the RC pin should be left open, or connected to a voltage higher than 4V referenced to minus input. In situations where it is desired to have the converter power up automatically without the need for control signals or a switch, the RC pin can be wired directly to the –Input circuit on the application board.

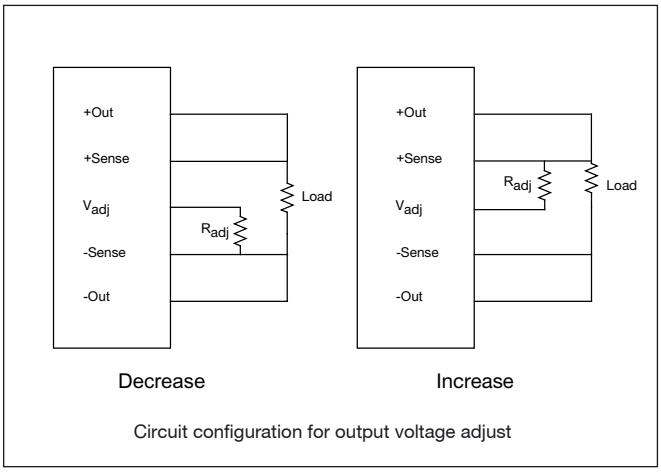
The second option is “positive logic” remote control, which can be ordered by adding the suffix “P” to the end of the part number. The converter will turn on if the input voltage is applied with the RC pin open. Turn off is achieved by connecting the RC pin to the minus input. To ensure safe turn off the voltage difference between minus input pin and the RC pin shall be less than 1V. The converter will restart when this connection is opened.

Remote Sense

All PKL 4000 Series DC/DC converters have remote sense that can be used to compensate for moderate amounts of resistance in the distribution system and allow for voltage regulation at the load or other selected point. The remote sense lines will carry very little current and do not need a large cross sectional area. However, the sense lines on the PCB should be located close to a ground trace or ground plane. In a discrete wiring situation, the use of twisted pair wires or other technique to reduce noise susceptibility is highly recommended. The remote sense circuitry will compensate for up to 10% voltage drop between the sense voltage and the voltage at the output pins. The output voltage and the remote sense voltage offset must be less than the minimum over voltage trip point. If the remote sense is not needed the –Sense should be connected to –Out and +Sense should be connected to +Out.

Output Voltage Adjust (V_{adj})

All PKL 4000 Series DC/DC converters have an Output Voltage adjust pin (Vadj). This pin can be used to adjust the output voltage above or below Output voltage initial setting. When increasing the output voltage, the voltage at the output pins (including any remote sense offset) must be kept below the overvoltage trip point, to prevent the converter from shut down. Also note that at increased output voltages the maximum power rating of the converter remains the same, and the output current capability will decrease correspondingly. To decrease the output voltage the resistor should be connected between Vadj pin and –Sense pin. To increase the voltage the resistor should be connected between Vadj pin and +Sense pin. The resistor value of the Output voltage adjust function is according to information given under the output section.



Circuit configuration for output voltage adjust

Current Limit Protection

The PKL 4000 Series DC/DC converters include current limiting circuitry that allows them to withstand continuous overloads or short circuit conditions on the output. The output voltage will decrease towards zero for output currents in excess of max output current (Iomax).
The converter will resume normal operation after removal of the overload. The load distribution system should be designed to carry the maximum output short circuit current specified.

Over Voltage Protection (OVP)

The PKL 4000 Series DC/DC converters have latching output overvoltage protection. In the event of an over-voltage condition, the converter will shut down immediately. The converter can be restarted by cycling the input voltage or using the remote control function.

Over Temperature Protection (OTP)

The PKL 4000 Series DC/DC converters are protected from thermal overload by an internal over temperature shutdown circuit. When the baseplate or case temperature exceeds 110 °C (PKL4118B 120 °C) the converter will shut down immediately (latching). The converter can be restarted by cycling the input voltage or using the remote control function.

Input And Output Impedance

The impedance of both the power source and the load will interact with the impedance of the DC/DC converter. It is most important to have a ratio between L and C as low as possible, i.e. a low characteristic impedance, both at the input and output, as the converters have a low energy storage capability. The PKL 4000 Series DC/DC converters have been designed to be completely stable without the need for external capacitors on the input or the output circuits. The performance in some applications can be enhanced by addition of external capacitance as described under maximum capacitive load. If the distribution of the input voltage source to the converter contains significant inductance, the addition of a 100 µF capacitor across the input of the converter will help insure stability. This capacitor is not required when powering the DC/DC converter from a low impedance source with short, low inductance, input power leads.

Maximum Capacitive Load

When powering loads with significant dynamic current requirements, the voltage regulation at the load can be improved by addition of decoupling capacitance at the load. The most affective technique is to locate low ESR ceramic capacitors as close to the load as possible, using several capacitors to lower the effective ESR. These ceramic capacitors will handle short duration high-frequency components of dynamic load changes. In addition, higher values of electrolytic capacitors should be used to handle the mid-frequency components. It is equally important to use good design practice when configuring the DC distribution system.
Low resistance and low inductance PCB (printed circuit board) layouts and cabling should be used. Remember that when using remote sensing, all resistance, inductance and capacitance of the distribution system is within the feedback loop of the converter. This can have affect on the converters compensation and the resulting stability and dynamic response performance. As a “rule of thumb”, 100 µF/A of output current can be used without any additional analysis. For example with a 25A converter, values of decoupling capacitance up to 2500 µF can be used without regard to stability. With larger values of capacitance, the load transient recovery time can exceed the specified value. As much of the capacitance as possible should be outside the remote sensing loop and close to the load. The absolute maximum value of output capacitance is 10 000 µF. For values larger than this, please contact your local Ericsson Power Modules representative.

Parallel Operation

The PKL 4000 Series DC/DC converters can be paralleled safely without any external components, however good matching between the initial voltage setting and the layout impedence/ resistance can change the performance. Please consult with your Ericsson representative should parallelling the PKL 4000 series for increased power be desired.

Thermal Consideration

General

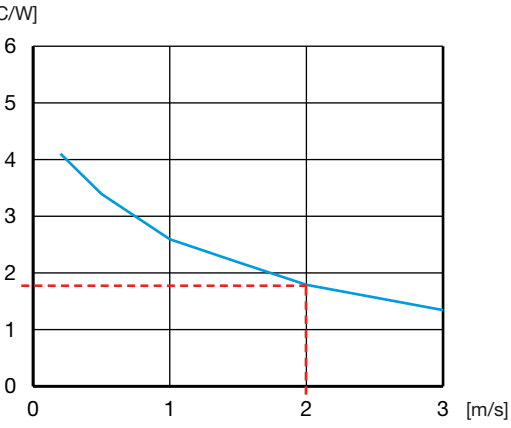
The PKL 4000 Series DC/DC converters are designed to operate in a variety of thermal environments, however sufficient cooling should be provided to help ensure reliable operation. Heat is removed by conduction, convection and radiation to the surrounding environment. Increased airflow enhances the heat transfer via convection. The available load current vs. ambient air temperature and airflow at Vin=53 V for each model is according to the information given under the output section. The test is done in a wind tunnel with a cross section of 305x305 mm, the DC/DC converter vertically mounted on a 16 layer PCB with a size of 254x254 mm. Proper cooling can be verified by measuring the temperature of selected devices.

Calculation of ambient temperature

By using the thermal resistance the maximum allowed ambient temperature can be calculated.

1. The powerloss is calculated by using the formula ((1/η) - 1) × output power = power losses.
   η = efficiency of converter. E.g 85 % = 0.85

2. Find the value of the thermal resistance in the diagram by using the airflow speed at the module. Take the thermal resistance x powerloss to get the temperature increase.



Thermal resistance vs. airspeed measured at the converter. Tested in windtunnel with a cross section of 305×305 mm mounted on a 16 layer PCB with a size of 254×254 mm.

3. Max allowed calculated ambient temperature is: Max T_C of DC/DC converter —temperature increase.

Example: PKL 4118B PIT
Conditions:
Input voltage 53 V
Max case temperature 110 °C
Output current 80 A
Efficiency 81.5%
Airflow 2 m/s

1. $((\frac{1}{0.815}) - 1) \times 144$ W = 32.6 W (powerloss)

2. 32.6W × 1.8 °C/W = 58.68 °C (temperature increase)

3. 110 °C - 58.7 °C = max ambient temperature is 51.3 °C

The real temperature will be dependent on several factors, like PCB size and type, direction of airflow, air turbulence, heatsinking etc. It is recommended to verify the temperature by testing.

Miscellaneous

Soldering Information

The PKL 4000 Series DC/DC converters are intended for through hole mounting on a PCB. When wave soldering is used max temperature on the pins are specified to 215°C for 10 seconds. Maximum preheat rate of 4°C/s is suggested. When hand soldering is used a thermocouple needs to be mounted on the DC/DC converter pins to verify that pin temperatures doe not exceed 215°C for longer than 10 seconds with the used soldering tools.

No-clean flux is recommended to avoid entrapment of cleaning fluids in cavities inside of the DC/DC power module. The residues may affect long time reliability and isolation voltage.

Delivery Package Information

PKL 4000 series standard delivery package is a 50 pcs box
One box contains 5 full trays.

Tray Specification

Material:	ESD PET
Max surface resistance:	$<10^{10}$ Ohm/sq
Color:	Clear
Capacity:	10 pcs/tray
Weight:	1100 g

Design for Environment (DfE)

The PKL 4000 Series DC/DC converters are designed to fulfill the wanted functionality with minimum environmental impact. The converters are presently assembled using low lead solder and electroless nickel plated brass pins. Lead free solder will be used in the coming year.
All packaging used for shipping is recyclable.

Quality

Reliability

The Mean Time Between Failure (MTBF) of the PKL 4000 series DC/DC converter family is calculated to be greater than (>) 3.7million hours at full output power and a baseplate or case temperature of 90°C using the Ericsson failure rate data system (TILDA/Preditool). The Ericsson failure rate data system is based on field failure rates and is continuously updated. The data corresponds to actual failure rates of components used in Information Technology and Telecom equipment in temperature controlled environments (T_A= -5...+65°C). The data is considered to have a confidence level of 90%. For more information please refer to Design Note 002.

Quality Statement

The PKL 4000 series DC/DC converters are designed and manufactured in an industrial environment where quality systems and methods like ISO 9000, 6σ (sigma), and SPC are intensively in use to boost the continuous improvements strategy. Infant mortality or early failures in the products are screened out and they are subjected to an ATE-based final test. Conservative design rules, design reviews and product qualifications, plus the high competence of an engaged work force, contribute to the high quality of our products.

Limitation of Liability

Ericsson Power Modules does not make any other warranties, expressed or implied including any warranty of merchantability or fitness for a particular purpose (including, but not limited to, use in life support applications, where malfunctions of product can cause injury to a person's health or life).

Product Program

V_I	V_O/I_O max Output 1	P_O max	Ordering No.	Page	Comment
48/60	1.8 V/60 A	108 W	PKL 4118 PIT	4-6	
48/60	1.8 V/80 A	144 W	PKL 4118B PIT	7-9	
48/60	2.5 V/50 A	125 W	PKL 4119 PIT	10-12	
48/60	2.5 V/60 A	150 W	PKL 4119A PIT	13-15	
48/60	2.5 V/80 A	200 W	PKL 4219A PIT	16-18	
48/60	3.3 V/50 A	165 W	PKL 4110 PIT	19-21	
48/60	3.3 V/60 A	198 W	PKL 4110A PIT	22-24	
48/60	5.0 V/50 A	250 W	PKL 4211 PIT	25-27	
48/60	5.0 V/60 A	300 W	PKL 4311 PIT	28-30	
48/60	12 V/20 A	240 W	PKL 4213 PIT	31-33	
48/60	12 V/25 A	300 W	PKL 4313 PIT	34-36	
48/60	28 V/11 A	310 W	PKL 4316 PIT		See PKL 4316 datasheet
48/60	28 V/13 A	366 W	PKL 4316A PIT		See PKL 4316 datasheet

The PKL series DC/DC converter may be ordered with different options listed in the Product Options Table.

For more information about the complete product program, please refer to our website: www.ericsson.com/powermodules

Product Options

Option	Suffix	Example
Negative Remote Control logic Industry standard Output Adjust	T	PKL 4118B PIT
Positive logic option	P	PKL 4219A PIPT
Standard half-brick pin configuration	SP	PKL 4110A PITSP
Non-threaded standoff with increased length 0.5 mm (0.02 in)	M	PKL 4118B PITM
Lead length 3.68 mm (0.145 in)	LA	PKL 4118B PITLA
Lead length 4.57 mm (0.180 in)	LB	PKL 4118B PITLB
Lead length 2.80 mm (0.11 in)	LC	PKL 4118B PITLC

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The latest and most complete information can be found on our website

Datasheet

EN/LZT 146 047 R4A