

PIC18F04/05/14/15Q41 Silicon Errata and Data Sheet Clarifications

The PIC18F04/05/14/15Q41 devices that you have received conform functionally to the current device data sheet (DS40002242D), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in the table below.

The errata described in this document will be addressed in future revisions of the PIC18F04/05/14/15Q41 silicon.

Note: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current.

Table 1. Silicon Device Identification

Part Number	Device ID	Revision ID		
		A4	A5	D1
PIC18F04Q41	0x7540	0xA004	0xA005	0xA0C1
PIC18F05Q41	0x7500	0xA004	0xA005	0xA0C1
PIC18F14Q41	0x7520	0xA004	0xA005	0xA0C1
PIC18F15Q41	0x75E0	0xA004	0xA005	0xA0C1



Important: Refer to the **Device/Revision ID** section in the current “**PIC18-Q41 Family Programming Specification**” (DS40002143) for more detailed information on Device Identification and Revision IDs for your specific device.

Table 2. Silicon Issue Summary

Module	Feature	Item No.	Issue Summary	Affected Revisions		
				A4	A5	D1
Analog-to-Digital Converter with Computation	ADCC	1.1.1.	ADC cannot operate in certain low-power conditions	X		
		1.1.2.	Double Sample Conversions	X	X	X
Electrical Specifications	ADC Offset Error	1.2.1.	ADC Offset Error specification lowered in ECH, ECM and ECL modes			X
Oscillator	XT mode	1.3.1.	Maximum clock frequency limited to 2 MHz for XT mode	X		
	Fail-Safe Clock Monitor	1.3.2.	Enabling the FOSC Fail-Safe Clock Monitor alongside the Primary or Secondary Oscillator Clock Monitor causes issues in Sleep	X		
	EC mode	1.3.3.	Maximum clock frequency for EC mode is 32 MHz for $V_{DD} < 2.0V$	X		
I ² C	I ² C	1.4.1.	I2CxADR0/1/2/3 registers have incorrect Reset value	X		
		1.4.2.	I ² C Start and/or Stop Flags May be Set When I ² C is Enabled	X	X	X
Operational Amplifier	OPA	1.5.1.	The Charge Pump On Control (CPON) bit is reserved	X		
	OPA	1.5.2.	Internal resistor ladder does not disconnect in Unity Gain mode	X		
Universal Asynchronous Receiver Transmitter	UART	1.6.1.	UART TXDE signal may go low before the STOP bit has been entirely transmitted.	X	X	X
		1.6.2.	Asynchronous 9-bit UART Address Mode Address Mismatch	X		
Signal Measurement Timer	SMT	1.7.1.	Reset Bit	X	X	X

Note: Only those issues indicated in the last column apply to the current silicon revision.

1. Silicon Errata Issues

CAUTION

Notice: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated by the bold font in the following tables apply to the current silicon revision.

1.1 Module: Analog-to-Digital Converter with Computation (ADCC)

1.1.1 ADC Cannot Operate in Certain Low-Power Conditions

The ADC will not function when all of the following conditions exist: When the MCU system clock is sourced from LFINTOSC or SOSC and when both the BOR and FVR features are disabled.

Work around

- Method 1: Use a system clock other than LFINTOSC or SOSC.
- Method 2: Enable the BOR feature.
- Method 3: Enable the FVR feature.

Affected Silicon Revisions

A4	A5	D1
X		

1.1.2 Double Sample Conversions

When enabling a Double Sample Conversion ($DSEN = 1$), with no Precharge time ($ADPRE = 0$) and no Acquisition time ($ADACQ = 0$), the maximum number of cycles of acquisition time is inserted prior to the second conversion. The first conversion will be performed as expected with no Precharge time and no Acquisition time. It is only between the first and second conversions where a maximum number of cycles of Acquisition time is performed unexpectedly.

Work around

- Method 1: Disable Double Sample Conversion ($DSEN = 0$) and perform two single conversions back to back.
- Method 2: If adding acquisition time is acceptable, then select no Precharge time, along with the desired Acquisition time.

Affected Silicon Revisions

A4	A5	D1
X	X	X

1.2 Module: Electrical Specifications

1.2.1 ADC Offset Error Specification Lowered in ECH, ECM and ECL Modes

When operating the device using an external clock source as the system clock in ECH, ECM or ECL mode, the ADC Offset Error (AD04: E_{OFF}) is updated to 12 Least Significant bits.

Work around

To meet the specified ADC Offset Error limit of 6 Least Significant bits, do not operate the device using the system clock in ECH, ECM or ECL mode when using the ADC.

Affected Silicon Revisions

A4	A5	D1
		X

1.3 Module: Oscillator**1.3.1 Maximum Clock Frequency Limited to 2 MHz for XT Mode**

The maximum clock frequency for the intermediate gain setting that supports quartz crystal and ceramic resonator operation (XT mode) is being reduced from 4 MHz to 2 MHz.

Work around

For crystal or resonator frequencies above 2 MHz, use HS mode.

Affected Silicon Revisions

A4	A5	D1
X		

1.3.2 Enabling the FOSC Fail-Safe Clock Monitor Alongside the Primary or Secondary Oscillator Clock Monitor Causes Issues with Sleep

When the FOSC Fail-Safe Clock Monitor is enabled (FCMEN Configuration bit = 1) and either the Primary or Secondary Fail-Safe Clock Monitor is also enabled (FCMENS and/or FCMENP = 1), putting the device to Sleep will cause a Fail-Safe condition to trigger. This has the effect of erroneously triggering Fail-Safe interrupts when there has not been a clock interruption. This can also cause the Watchdog Timer to not properly wake up the part from Sleep.

Work around

If proper functionality in Sleep is required, do not enable the Primary or Secondary Fail-Safe Clock Monitor while the FOSC Fail-Safe Clock Monitor is enabled. If Primary or Secondary Clock Monitoring in Sleep is desired, disable the FOSC Fail-Safe Clock Monitor before the device goes to Sleep.

Affected Silicon Revisions

A4	A5	D1
X		

1.3.3 Maximum Clock Frequency for EC Mode Is 32 MHz for $V_{DD} < 2.0V$

When configured in External Clock High-Power (ECH) mode and operating at $V_{DD} < 2.0V$, the maximum input clock frequency is 32 MHz.

Work around

To obtain a system clock frequency of 64 MHz in ECH mode at $V_{DD} < 2.0V$, use a 16 MHz external clock in conjunction with the 4x Phase-Locked Loop (PLL) circuit (i.e., either RSTOSC Configuration bits = 0b010 or OSCCON1bits.NOSC = 0b010).

Affected Silicon Revisions

A4	A5	D1
X		

1.4 Module: I²C**1.4.1 The I2CxADR0/1/2/3 Registers Have Incorrect Reset Value**

The I2CxADR0/2 registers reset to 0xFF when the I2CxMD is enabled instead of 0x00. The I2CxADR1/3 registers reset to 0xFE when the I2CxMD is enabled instead of 0x00.

Work around

None.

Affected Silicon Revisions

A4	A5	D1
X		

1.4.2 The I²C Start and/or Stop Flags May Be Set When I²C Is Enabled

When I²C is enabled, erroneous Start and/or Stop conditions may be detected. This can generate erroneous I²C interrupts if enabled.

Work around

Use the following procedure to correctly detect the Start and Stop conditions:

1. Disable the Start and Stop conditions interrupt functions.
2. Enable the I²C module.
3. Wait 250 ns + six instructions cycles ($F_{OSC}/4$).
4. Clear the Start and Stop conditions interrupt flags.
5. Enable the Start and Stop conditions interrupt functions if used.

```
I2CxPIEBits.SCIE = 0; // Disable Start conditoin interrupt
I2CxPIEBits.PCIE = 0; // Disable Stop condition interrupt
I2CxCON0bits.EN = 1; // Enable I2C
Delay(); // Wait for 250ns + 6 instruction cycles (FOSC/4)
I2CxPIRbits.SCIF = 0; // Clear the Start condition interrupt flags
I2CxPIRbits.PCIF = 0; // Clear the Stop condition interrupt flags
I2CxPIEBits.SCIE = 1; // Enable Start condition interrupt if used
I2CxPIEBits.PCIE = 1; // Enable Stop condition interrupt if used
```

Affected Silicon Revisions

A4	A5	D1
X	X	X

1.5 Module: Operational Amplifier**1.5.1 The Charge Pump On Control (CPON) Bit Is Reserved**

When not operating the OPA near the rails, the Charge Pump On Control (CPON) bit can be used to disable the charge pump in order to save on current consumption. This feature is currently not available, and the charge pump is always enabled whenever the OPA module is in operation.

Work around

None.

Affected Silicon Revisions

A4	A5	D1
X		

1.5.2 Internal Resistor Ladder Does Not Disconnect in Unity Gain Mode

When using the OPA module in a unity gain configuration, the internal resistor ladder will not automatically disconnect from the operational amplifier, which may adversely affect the gain of the circuit. This applies when the peripheral has been configured to operate in Unity Gain mode in software by setting the UG bit, or in hardware using the hardware controlled override feature.

Work around

Disconnect the internal resistor ladder from the operational amplifier by writing to the Inverting Input Channel Selection (NCH) bits. All signals can be disconnected from the operational amplifier by writing `0b000` to the NCH bits.

Affected Silicon Revisions

A4	A5	D1
X		

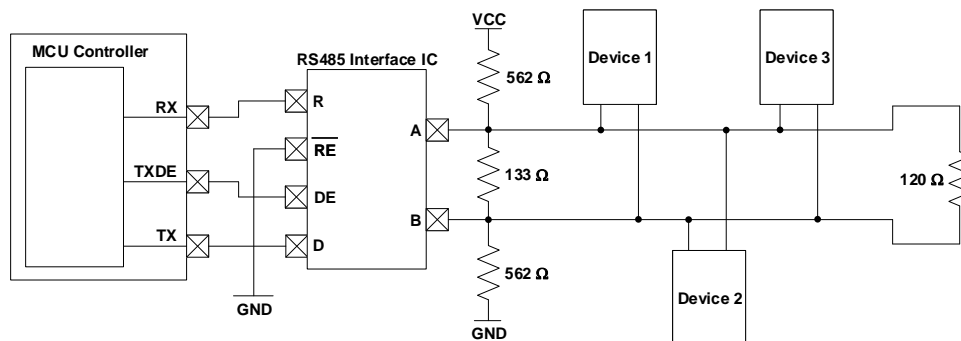
1.6 Module: Universal Asynchronous Receiver Transmitter

1.6.1 UART TXDE Signal May go Low Before The STOP Bit Has Been Entirely Transmitted.

The UART Transmit Drive Enable (TXDE) signal could potentially transition into a low state before the UART STOP bit has been entirely transmitted due to the effects of parasitic capacitance on the TX line. In some applications, this could result in communication being prematurely terminated due to the TXDE bit going low before the STOP bit has had enough time to settle.

Work around

In order to ensure that the STOP bit settles into its final logic state before the TXDE signal transitions low, a biasing circuit can be implemented. A biasing circuit allows the TX line to either be driven high or low, rather than being left in a floating tri-state mode where prolonged rise or fall times could lead to communication being disrupted. This bias circuit should only be implemented on one end of the serial bus, and a termination resistor should be used on the other end. The figure below show an example of a bias circuit that can be used to achieve this. Please note that the resistor values used in this circuit are recommendations, and that the actual resistor values required may vary based on the application.



Affected Silicon Revisions

A4	A5	D1
X	X	X

1.6.2 Asynchronous 9-bit UART Address Mode Address Mismatch

In Asynchronous 9-bit UART Address mode there is the possibility that a false address mismatch may occur even when the address of both devices match, or that a false address match may occur when there is an address mismatch between the devices.

Work around

None. Do not use the UART modules in Asynchronous 9-bit Address Mode

Affected Silicon Revisions

A4	A5	D1
X		

1.7 Module: SMT**1.7.1 Reset Bit**

If the SMT clock prescaler is set to any value other than '00', setting the RST bit will cause the module to stop working. The RST bit will remain at the value '1', the counter will not increment, and no interrupts will be generated. The problem is cleared by turning the module off and on, or by a device reset.

Work around

- Method 1: Do not set the RST bit; manual reset is usually not required for typical operation because the measurement logic will reset the counter automatically.
- Method 2: Write zero to the counter manually. The module enable or the clock should be disabled during this.
- Method 3: Use 1:1 prescaler (PS = 00).
- Method 4: Use the CLKREF subsystem to provide a prescaled clock and set PS = 00.

Affected Silicon Revisions

A4	A5	D1
X	X	X

2. Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS40002242D):

Note:

Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

2.1 Memory Programming Specifications

The flash memory cell endurance specification is reduced to 1K minimum. The corresponding parameter (E_p) will be updated in the next revision of datasheet (DS40002242E).

Table 2-1. Memory Programming

Standard Operating Conditions (unless otherwise stated)							
Param No.	Sym.	Device Characteristics	Min.	Typ†	Max.	Units	Conditions
Data EEPROM Memory Specifications							
MEM20	E_D	DataEE Byte Endurance	100k	—	—	E/W	$-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$
MEM21	T_{D_RET}	Characteristic Retention	—	40	—	Year	Provided no other specifications are violated
MEM22	N_{D_REF}	Total Erase/Write Cycles before Refresh	1M	4M	—	E/W	$-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$
MEM23	V_{D_RW}	V_{DD} for Read or Erase/Write operation	V_{DDMIN}	—	V_{DDMAX}	V	
MEM24	T_{D_BEW}	Byte Erase and Write Cycle Time	—	—	11	ms	
Program Flash Memory Specifications							
MEM30	E_p	Flash Memory Cell Endurance	10k	—	—	E/W	$-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ (Note 1)
MEM32	T_{P_RET}	Characteristic Retention	—	40	—	Year	Provided no other specifications are violated
MEM33	V_{P_RD}	V_{DD} for Read operation	V_{DDMIN}	—	V_{DDMAX}	V	
MEM34	V_{P_REW}	V_{DD} for Row Erase or Write operation	V_{DDMIN}	—	V_{DDMAX}	V	
MEM35	T_{P_REW}	Self-Timed Page Write	—	—	10	ms	
MEM36	T_{SE}	Self-Timed Page Erase	—	—	11	ms	
MEM37	T_{P_WRD}	Self-Timed Word Write	—	—	75	μs	
† Data in “Typ” column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.							
Note:							
1. Flash Memory Cell Endurance for the Flash memory is defined as: One Row Erase operation and one Self-Timed Write.							

2.2 UART Baud Rate Equation

The UART Baud Rate equation in the UxBRG register contains a typo and will provide the incorrect UART Baud Rate. The correct equation is shown below. The correction to this equation is shown in bold.

$$\text{UART Baud Rate} = [\text{Fosc} * (1 + (\text{BRGS} * 3))] / [(16 * (\text{BRG} + 1))]$$

2.3 Power-Down Current (I_{PD}) Specifications

The Power-Down current (I_{PD}) electrical specifications for FVR Buffer 2, I_{PD} Base when VREGPM = 01, and the Operational Amplifier have been modified. The corresponding parameters (I_{PD_FVR_BUF2}, I_{PD}, and I_{PD_OPA}) will be updated in the next revision of the datasheet (DS40002242E).

Table 2-2. Power-Down Current (I_{PD})^(1,2)

Standard Operating Conditions (unless otherwise stated)										
Param. No.	Sym.	Device Characteristics	Min.	Typ.†	Max. +85°C	Max. +125°C	Units	Conditions		
								V _{DD}	VREGPM	Note
D200	I_{PD}	I_{PD} Base	—	1.1	3.3	4.6	μA	3.0V	'b11	
			—	0.9	12.1	33.3	μA	3.0V	'b10	
			—	38.0	54.0	78.0	μA	3.0V	'b01	
			—	152	190	198.5	μA	3.0V	'b00	
D201	I _{PD_WDT}	Low-Frequency Internal Oscillator/WDT	—	1.5	3.8	5.1	μA	3.0V	'b11	
D202	I _{PD_SOSC}	Secondary Oscillator (S _O SC)	—	2.1	4.6	7.9	μA	3.0V	'b11	
D203	I _{PD_LPBOR}	Low-Power Brown-out Reset (LPBOR)	—	1.3	3.5	4.8	μA	3.0V	'b11	
D204	I _{PD_FVR_BUF1}	FVR Buffer 1 (ADC)	—	174.7	249.7	255.4	μA	3.0V	'b11	
D204A	I_{PD_FVR_BUF2}	FVR Buffer 2 (DAC/CMP)	—	60.0	85.0	101.0	μA	3.0V	'bx1 or 'b10	
D205	I _{PD_BOR}	Brown-out Reset (BOR)	—	16.6	20.4	20.8	μA	3.0V	'b11	
D206	I _{PD_HLVD}	High/Low Voltage Detect (HLVD)	—	16.9	20.8	22.5	μA	3.0V	'b11	
D207	I _{PD_ADCA}	ADC - Active	—	483	789	790	μA	3.0V	'bx1 or 'b10	ADC is converting (Note 4)
D208	I _{PD_CMP}	Comparator	—	52.5	84.2	105	μA	3.0V	'b11	

.....continued

Standard Operating Conditions (unless otherwise stated)

Param. No.	Sym.	Device Characteristics	Min.	Typ.†	Max. +85°C	Max. +125°C	Units	Conditions		
								V _{DD}	V _{REGPM}	Note
D209	I _{PD_OPA}	Operational Amplifier	—	1.10	1.67	1.73	mA	3.0V	'b01	Charge Pump On; V _{ICM} = V _{DD} /2
			—	800	1160	1220	µA	3.0V	'b01	Charge Pump Off; V _{ICM} = V _{DD} /2

* These parameters are characterized but not tested.

† Data in “Typ.” column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Notes:

1. The peripheral current is the sum of the base I_{DD} and the additional current consumed when this peripheral is enabled. The peripheral Δ current can be determined by subtracting the base I_{DD} or I_{PD} current from this limit. Max. values must be used when calculating total current consumption.
2. The power-down current in Sleep mode does not depend on the oscillator type. Power-down current is measured with the part in Sleep mode with all I/O pins in high-impedance state and tied to V_{SS}.
3. All peripheral currents listed are on a per-peripheral basis if more than one instance of a peripheral is available.
4. ADC clock source is ADCRC.

3. Appendix A: Revision History

Doc. Rev.	Date	Comments
D	02/2022	Adding silicon erratum items 1.1.2, 1.6.1 and 1.7.1.
C	02/2021	Adding ADC offset errata and updating mask revision for KV00P RTP. Adding silicon revision D1. Adding silicon erratum items 1.5 and 1.6. Minor editorial corrections.
B	11/2020	Adding silicon revision A5.
A	07/2020	Initial document release.

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ISBN: 978-1-5224-9762-2

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