A product Line of
Diodes Incorporated

PI6C39X020401

Low Skew 1 to 4 Clock Buffer

Features

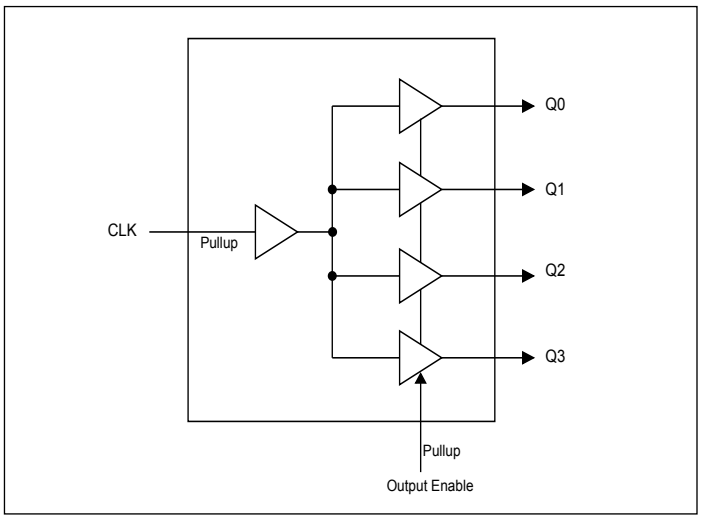
- Low skew outputs (50 ps)
- Low additive jitter RMS: 50fs
- Input/Output frequency up to 250MHz
- Operating Voltages of 1.5V to 3.3V
- Output Enable pin tri-states outputs
- 3.465V tolerant input clock
- Extended temp range: -40°C- 105°C
- Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)
- Halogen and Antimony Free. "Green" Device (Note 3)
- For automotive applications requiring specific change control (i.e. parts qualified to AEC-Q100/101/200, PPAP capable, and manufactured in IATF 16949 certified facilities), please contact us or your local Diodes representative.

  https://www.diodes.com/quality/product-definitions/
- Packaging (Pb-free & Green):
  - 8-pin, X1DFN (XEC)

Description

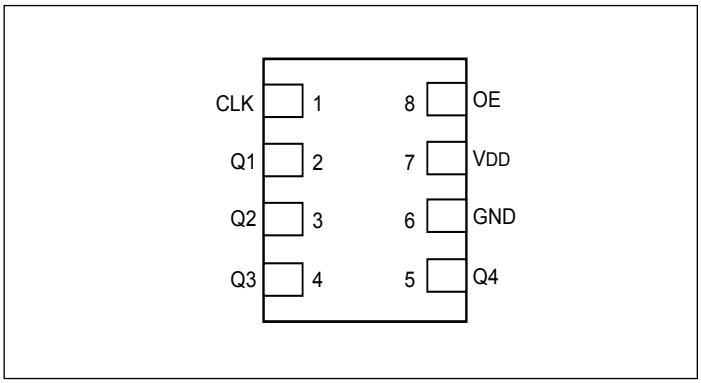
The PI6C39X020401 is a low skew, low additive jitter single input to four output clock buffer.

Block Diagram



Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

Pin Configuration



Pin Descriptions

Pin#	Pin Name	Type	Pin Description
1	CLK	Input	Clock Input. 3.3V tolerant input. Internal pull-up resistor.
2	Q1	Output	Clock Output 1.
3	Q2	Output	Clock Output 2.
4	Q3	Output	Clock Output 3.
5	Q4	Output	Clock Output 4.
6	GND	Power	Connect to ground.
7	VDD	Power	Connect to 1.5V, 1.8V, 2.5V or 3.3V.
8	OE	Input	Output Enable. Tri-states outputs when low. Internal pull-up resistor.

External Components

A minimum number of external components are required for proper operation. A decoupling capacitor of 0.01 µF should be connected between VDD on pin 7 and GND on pin 6, as close to the device as possible. A 33 Ω series terminating resistor may be used on each clock output if the trace is longer than 1 inch.

Maximum Ratings

Supply Voltage, VDD	4.6V
Output Enable and All Outputs	-0.5V to VDD+0.5V
CLK	-0.5V to 3.6V (VDD > 0V)
Storage Temperature	-65 to +150°C
Junction Temperature	125°C max
ESD Protection (HBM)	2000V

Note:

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended Operation Conditions

Parameter	Min.	Typ.	Max.	Units
Ambient Operating Temperature (Extended)	-40		+105	°C
Power Supply Voltage (measured in respect to GND)	+1.425		+3.465	V

DC Electrical Characteristics

VDD=1.5V ±5%, Ambient temperature -40 to +105°C, unless stated otherwise

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
VDD	Operating Voltage		1.425	1.5	1.575	V
V_{IH}	Input High Voltage(1)	CLK, OE	0.7xVDD		VDD	V
V_{IL}	Input Low Voltage(1)	CLK, OE			0.3xVDD	V
I_{IH}	Input High Current	CLK, OE	-1		1	µA
I_{IL}	Input Low Current	CLK, OE	-40			µA
V_{OH}	Output High Voltage	I_{OH} = -6mA	0.95			V
V_{OL}	Output Low Voltage	I_{OL} = 6mA			0.45	V
IDD	Operating Supply Current	No load, 133 MHz		10	18	mA
Z_O	Nominal Output Impedance			20		Ω
C_{IN}	Input Capacitance	CLK, OE pin		5		pF

Notes: 1. Nominal switching threshold is VDD/2

DC Electrical Characteristics Cont.

VDD=1.8 V ±5%, Ambient temperature -40 to +105°C, unless stated otherwise

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
VDD	Operating Voltage		1.7	1.8	1.89	V
V_{IH}	Input High Voltage(1)	CLK, OE	0.7xVDD		VDD	V
V_{IL}	Input Low Voltage(1)	CLK, OE			0.3xVDD	V
I_{IH}	Input High Current	CLK, OE	-1		1	µA
I_{IL}	Input Low Current	CLK, OE	-40			µA
V_{OH}	Output High Voltage	I_{OH} = -10mA	1.4			V
V_{OL}	Output Low Voltage	I_{OL} = 10mA			0.4	V
IDD	Operating Supply Current	No load, 133 MHz		13	21	mA
Z_O	Nominal Output Impedance			20		Ω
C_{IN}	Input Capacitance	CLK, OE pin		5		pF

Notes: 1. Nominal switching threshold is VDD/2

VDD=2.5V ±5%, Ambient temperature -40 to +105°C, unless stated otherwise

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
VDD	Operating Voltage		2.375	2.5	2.625	V
V_{IH}	Input High Voltage(1)	CLK, OE	0.7xVDD		VDD	V
V_{IL}	Input Low Voltage(1)	CLK, OE			0.3xVDD	V
I_{IH}	Input High Current	CLK, OE	-1		1	µA
I_{IL}	Input Low Current	CLK, OE	-60			µA
V_{OH}	Output High Voltage	I_{OH} = -16mA	1.8			V
V_{OL}	Output Low Voltage	I_{OL} = 16mA			0.4	V
IDD	Operating Supply Current	No load, 133 MHz		18	26	mA
Z_O	Nominal Output Impedance			20		Ω
C_{IN}	Input Capacitance	CLK, OE pin		5		pF

Notes: 1. Nominal switching threshold is VDD/2

DC Electrical Characteristics Cont.

VDD=3.3V ±5%, Ambient temperature -40 to +105°C, unless stated otherwise

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
VDD	Operating Voltage		3.135	3.3	3.465	V
V_{IH}	Input High Voltage(1)	CLK, OE	0.7xVDD		VDD	V
V_{IL}	Input Low Voltage(1)	CLK, OE			0.3xVDD	V
I_{IH}	Input High Current	CLK, OE	-1		1	µA
I_{IL}	Input Low Current	CLK, OE	-70			µA
V_{OH}	Output High Voltage	I_{OH} = -25mA	2.2			V
V_{OL}	Output Low Voltage	I_{OL} = 25mA			0.7	V
IDD	Operating Supply Current	No load, 133 MHz		22	35	mA
Z_O	Nominal Output Impedance			20		Ω
C_{IN}	Input Capacitance	CLK, OE pin		5		pF

Notes: 1. Nominal switching threshold is VDD/2

AC Electrical Characteristics

VDD=1.5V ±5%, Ambient temperature -40 to +105°C, unless stated otherwise

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
F_{OUT}	Output Frequency		0		200	MHz
tOR	Output Rise Time	0.3V to 1.2V		1	1.6	ns
tOF	Output Fall Time	1.2V to 0.3V		1	1.6	ns
T_{PD}	Propagation Delay(1)		2	3	5	ns
T_{SK}	Output to Output Skew(2)	Rising edges at VDD/2		50	65	ps
$t_{START-UP}$	Start-up Time	Part start-up time for valid outputs after VDD ramp-up			2	ms
t_{EN}	Output Enable Time	C_L < 5pF			3	cycles
t_{DIS}	Output Disable Time	C_L < 5pF			3	cycles

Notes:
1. With rail to rail input clock
2. Between any 2 outputs with equal loading.

AC Electrical Characteristics Cont.

VDD=1.8V ±5%, Ambient temperature -40 to +105°C, unless stated otherwise

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
F_{OUT}	Output Frequency		0		250	MHz
tOR	Output Rise Time	0.36V to 1.44V		0.6	1	ns
tOF	Output Fall Time	1.44V to 0.36V		0.6	1	ns
T_{PD}	Propagation Delay(1)		1.3	2	4	ns
T_{SK}	Output to Output Skew(2)	Rising edges at VDD/2		50	65	ps
J_{ADD}	Additive Jitter	@156.25MHz, 12k to 20MHz		0.03	0.05	ps
$t_{START-UP}$	Start-up Time	Part start-up time for valid outputs after VDD ramp-up			2	ms
t_{EN}	Output Enable Time	C_L < 5pF			3	cycles
t_{DIS}	Output Disable Time	C_L < 5pF			3	cycles

Notes:
1. With rail to rail input clock
2. Between any 2 outputs with equal loading.

VDD=2.5V ±5%, Ambient temperature -40 to +105°C, unless stated otherwise

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
F_{OUT}	Output Frequency		0		250	MHz
tOR	Output Rise Time	0.5V to 2V		0.6	1	ns
tOF	Output Fall Time	2V to 0.5V		0.6	1	ns
T_{PD}	Propagation Delay(1)		0.8	1.5	3	ns
T_{SK}	Output to Output Skew(1)	Rising edges at VDD/2		50	65	ps
J_{ADD}	Additive Jitter	@156.25MHz, 12k to 20MHz		0.035	0.05	ps
$t_{START-UP}$	Start-up Time	Part start-up time for valid outputs after VDD ramp-up			2	ms
t_{EN}	Output Enable Time	C_L < 5pF			3	cycles
t_{DIS}	Output Disable Time	C_L < 5pF			3	cycles

Notes:
1. With rail to rail input clock
2. Between any 2 outputs with equal loading.

AC Electrical Characteristics Cont.

VDD=3.3V ±10%, Ambient temperature -40 to +105°C, unless stated otherwise

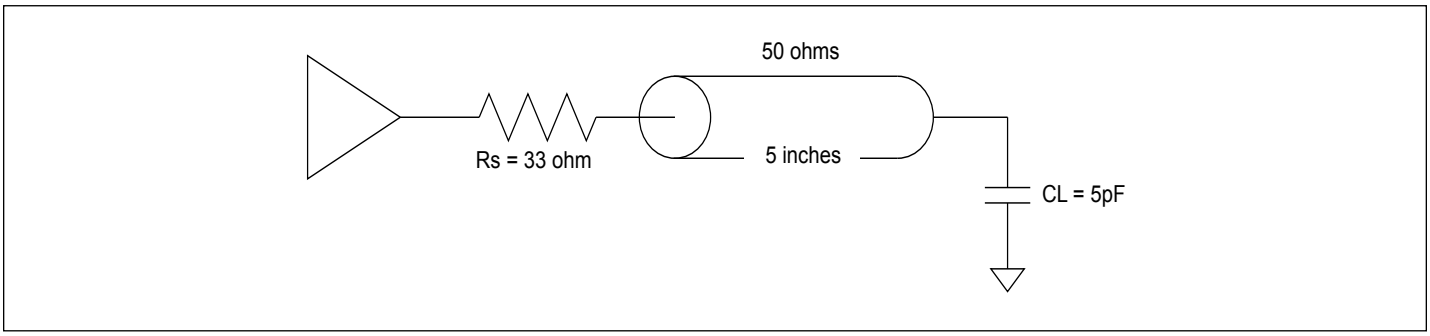
Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
F_{OUT}	Output Frequency		0		250	MHz
tOR	Output Rise Time	0.66V to 2.64V		0.6	1	ns
tOF	Output Fall Time	2.64V to 0.66V		0.6	1	ns
T_{PD}	Propagation Delay (1)		0.8	1.0	2.5	ns
T_{SK}	Output to Output Skew(2)	Rising edges at VDD/2		50	65	ps
J_{ADD}	Additive Jitter	@156.25MHz, 12k to 20MHz		0.037	0.05	ps
$t_{START-UP}$	Start-up Time	Part start-up time for valid outputs after VDD ramp-up			2	ms
t_{EN}	Output Enable Time	C_L < 5pF			3	cycles
t_{DIS}	Output Disable Time	C_L < 5pF			3	cycles

Notes:
1. With rail to rail input clock
2. Between any 2 outputs with equal loading.

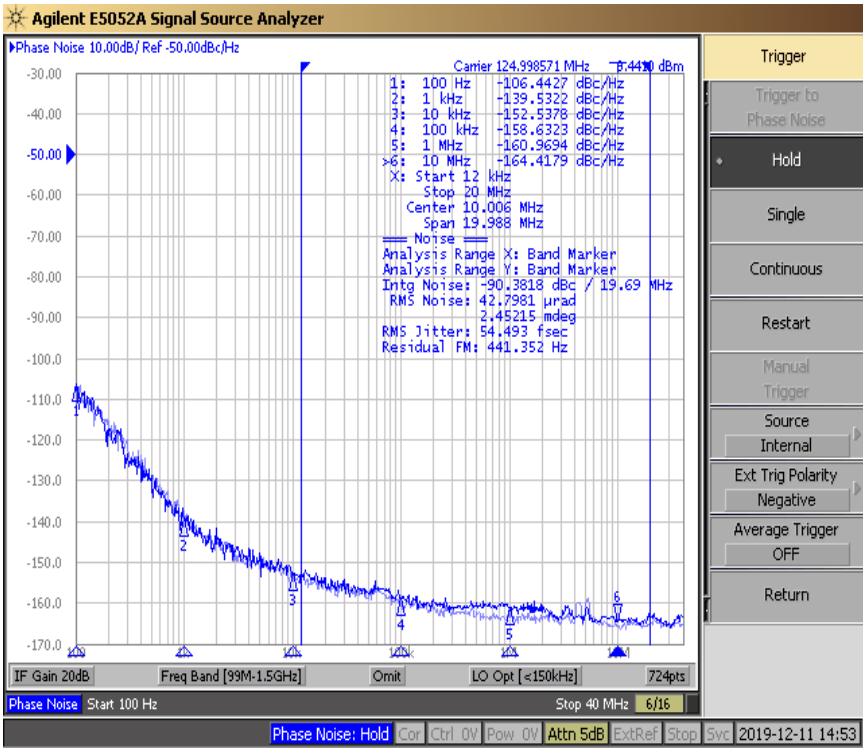
Thermal Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
θJA	Thermal Resistance Junction to Ambient	Still air		157		°C/W
θJC	Thermal Resistance Junction to Case			42		°C/W

Test Circuit



Additive Phase Noise Plot



Application Information

Suggest for Unused Inputs and Outputs

LVCMOS Input Control Pins

It is suggested to add pull-up=4.7k and pull-down=1k for LVCMOS pins even though they have internal pull-up/down but with much higher value (>=50k) for higher design reliability.

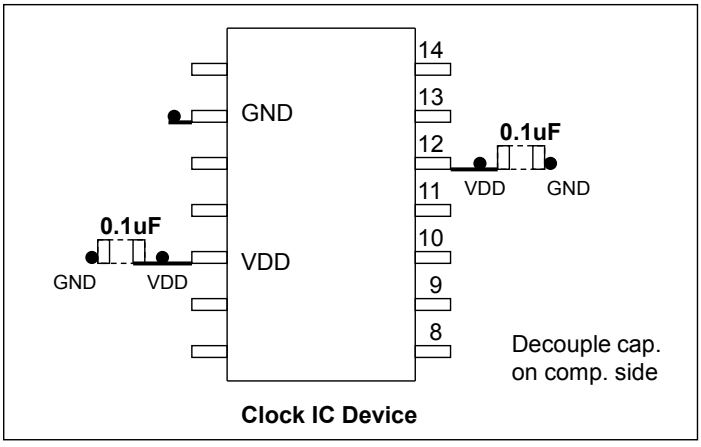
Outputs

All unused outputs are suggested to be left open and not connected to any trace. This can lower the IC power consumption.

Power Decoupling & Routing

VDD Pin Decoupling

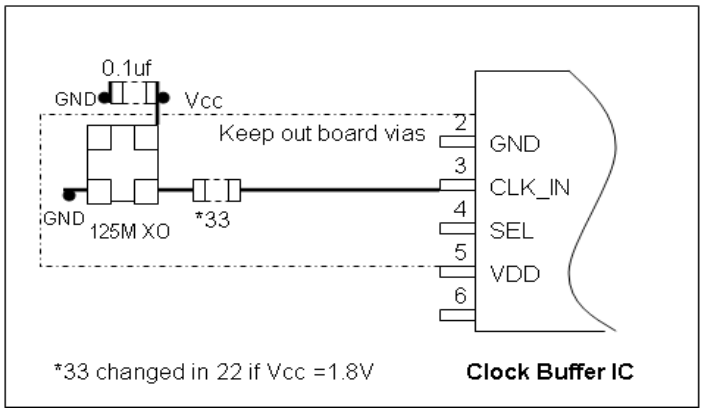
Each VDD pin must have a 0.1uF decoupling capacitor. For better decoupling, 1uF can be used. Locating the decoupling capacitor on the component side has better decoupling filter result as shown.



Placement of Decoupling Caps

CMOS Clock Trace Routing

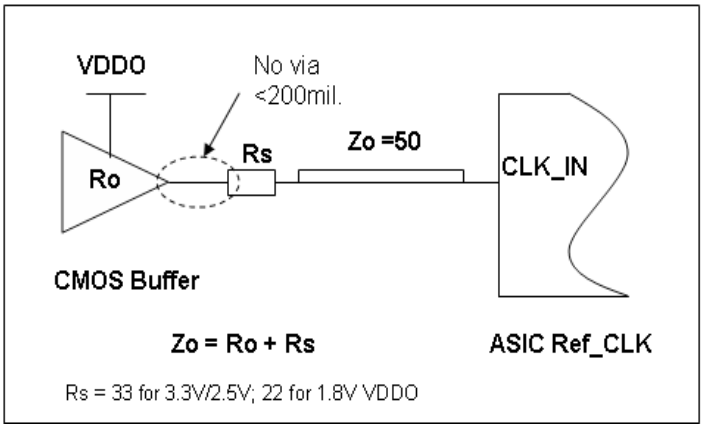
Please ensure that there is a sufficient keep-out area to the adjacent trace (>20mil.). In an example using a 125MHz XO driving a buffer IC, it is better to route the clock trace on the component side with a 33 ohm termination resistor.



CMOS Output Termination

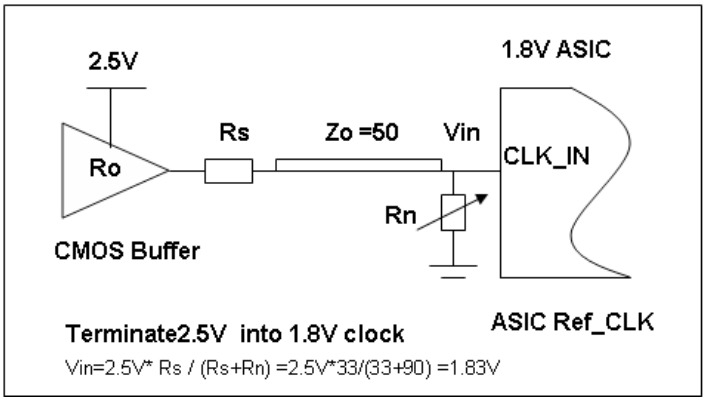
Popular CMOS Output Termination

The most popular CMOS termination is a serial resistor close to the output pin (<=200mil). It is simple and balances the drive strength. The resistor's value can be fine tuned for best performance during board bring-up based on VDDO voltage used.



Combining Serial and Parallel Termination

Designers can also use a parallel termination for CMOS outputs. For example, a 50 ohm pull-down resistor can be used at the Rx side to reduce signal reflection, but it reduces the signals V_swing in half. This pull-down can be combined with a serial resistor to form a smaller clock voltage difference. The following diagram shows how to transition a 2.5V clock into 1.8V clock.



Rs = 33 ohm with Rn = 100 ohm, to transition 3.3V CMOS to 2.5V

Rs = 43 ohm with Rn =70 ohm to transition 3.3V CMOS to 1.8V

Clock Jitter Definitions

Total Jitter = RJ + DJ

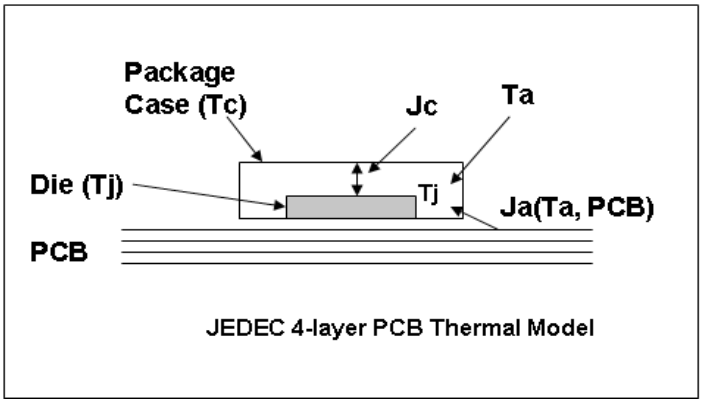
Random Jitter (RJ) is unpredictable and unbounded timing noise that can fit in a Gaussian math distribution in RMS. RJ test values are directly related with how long or how many test samples are available. Deterministic Jitter (DJ) is timing jitter that is predictable and periodic in fixed interference frequency. Total Jitter (TJ) is the combination of random jitter and deterministic jitter: , where is a factor based on total test sample count. JEDEC std. specifies digital clock TJ in 10k random samples.

Phase Jitter

Phase noise is short-term random noise attached on the clock carrier and it is a function of the clock offset from the carrier, for example dBc/Hz@10kHz which is phase noise power in 1-Hz normalized bandwidth vs. the carrier power @10kHz offset. Integration of phase noise in plot over a given frequency band yields RMS phase jitter, for example, to specify phase jitter <=1ps at 12k to 20MHz offset band as SONET standard specification.

Device Thermal Calculation

The JEDEC thermal model in a 4-layer PCB is shown below.



JEDEC 4-layer PCB Thermal Model

JEDEC IC Thermal Model

Important factors to influence device operating temperature are:

1) The power dissipation from the chip (P_chip) is after subtracting power dissipation from external loads. Generally it can be the no-load device Idd

2) Package type and PCB stack-up structure, for example, 1oz 4 layer board. PCB with more layers and are thicker has better heat dissipation

3) Chassis air flow and cooling mechanism. More air flow M/s and adding heat sink on device can reduce device final die junction temperature Tj

The individual device thermal calculation formula:

Tj = Ta + Pchip x Ja

Tc = Tj - Pchip x Jc

Ja ___ Package thermal resistance from die to the ambient air in C/W unit; This data is provided in JEDEC model simulation. An air flow of 1m/s will reduce Ja (still air) by 20~30%

Jc ___ Package thermal resistance from die to the package case in C/W unit

Tj ___ Die junction temperature in C (industry limit <125C max.)

Ta ___ Ambient air temperature in C

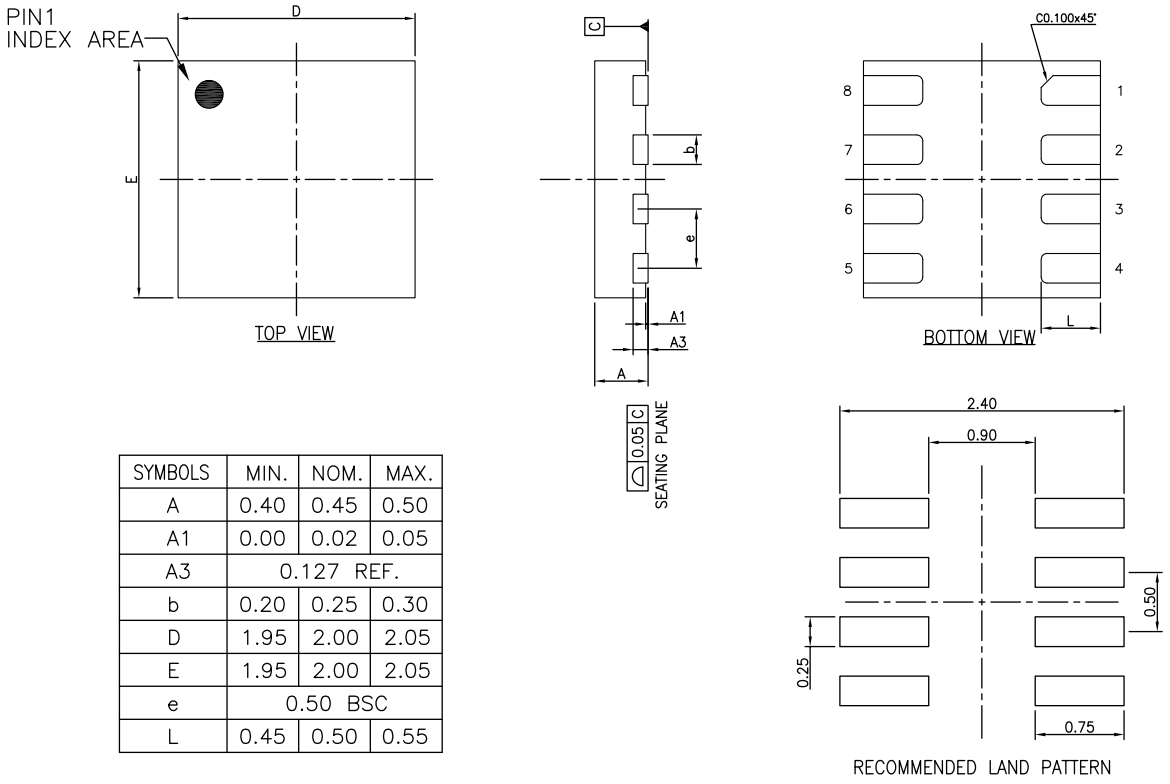
Tc ___ Package case temperature in C

Pchip___ IC actually consumes power through Iee/GND current

Part Marking

FZ: PI6C39X020401XECIE
Y: Year
W: Workweek
Line above first character denotes Lead-free and Green

Packaging Mechanical: 8-X1DFN (XEC)



SYMBOLS	MIN.	NOM.	MAX.
A	0.40	0.45	0.50
A1	0.00	0.02	0.05
A3		0.127 REF.	
b	0.20	0.25	0.30
D	1.95	2.00	2.05
E	1.95	2.00	2.05
e		0.50 BSC	
L	0.45	0.50	0.55

NOTE :
1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES.
2. Ref JEDEC MO-287
3. RECOMMENDED LAND PATTERN IS FOR REFERENCE ONLY.

DATE: 09/10/19

DESCRIPTION: 8-Contact, Extra Thin Dual Flat No-Lead (X1DFN)

PACKAGE CODE: XEC (XEC8)

DOCUMENT CONTROL #: PD-2242 **REVISION: --**

For latest package info.
please check: http://www.diodes.com/design/support/packaging/pericom-packaging/packaging-mechanicals-and-thermal-characteristics/

Ordering Information

Ordering Code	Package Code	Package Description
PI6C39X020401XECIEX	XEC	8-contact, Extra Thin Dual Flat No-Lead (X1DFN)

Notes:

1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
4. I = Industrial
5. E = Pb-free and Green
6. X suffix = Tape/Reel

IMPORTANT NOTICE

DIODES INCORPORATED MAKES NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARDS TO THIS DOCUMENT, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE (AND THEIR EQUIVALENTS UNDER THE LAWS OF ANY JURISDICTION).

Diodes Incorporated and its subsidiaries reserve the right to make modifications, enhancements, improvements, corrections or other changes without further notice to this document and any product described herein. Diodes Incorporated does not assume any liability arising out of the application or use of this document or any product described herein; neither does Diodes Incorporated convey any license under its patent or trademark rights, nor the rights of others. Any Customer or user of this document or products described herein in such applications shall assume all risks of such use and will agree to hold Diodes Incorporated and all the companies whose products are represented on Diodes Incorporated website, harmless against all damages.

Diodes Incorporated does not warrant or accept any liability whatsoever in respect of any products purchased through unauthorized sales channel.

Should Customers purchase or use Diodes Incorporated products for any unintended or unauthorized application, Customers shall indemnify and hold Diodes Incorporated and its representatives harmless against all claims, damages, expenses, and attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized application.

Products described herein may be covered by one or more United States, international or foreign patents pending. Product names and markings noted herein may also be covered by one or more United States, international or foreign trademarks.

This document is written in English but may be translated into multiple languages for reference. Only the English version of this document is the final and determinative format released by Diodes Incorporated.

LIFE SUPPORT

Diodes Incorporated products are specifically not authorized for use as critical components in life support devices or systems without the express written approval of the Chief Executive Officer of Diodes Incorporated. As used herein:

A. Life support devices or systems are devices or systems which:

1. are intended to implant into the body, or

2. support or sustain life and whose failure to perform when properly used in accordance with instructions for use provided in the labeling can be reasonably expected to result in significant injury to the user.

B. A critical component is any component in a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or to affect its safety or effectiveness.

Customers represent that they have all necessary expertise in the safety and regulatory ramifications of their life support devices or systems, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of Diodes Incorporated products in such safety-critical, life support devices or systems, notwithstanding any devices- or systems-related information or support that may be provided by Diodes Incorporated. Further, Customers must fully indemnify Diodes Incorporated and its representatives against any damages arising out of the use of Diodes Incorporated products in such safety-critical, life support devices or systems.

www.diodes.com